

# P-cell and N-cell based IGBT Module: Layout Design, Parasitic Extraction, and Experimental Verification

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**Abstract**— This paper proposes a novel packaging method for power electronics modules based on the concepts of P-cell and N-cell. It can reduce the stray inductance in the current commutation path in a phase-leg module and hence improve the switching behavior. Two IGBT phase-leg modules, specifically a P-cell and N-cell based module and a conventional module are designed. Using Ansoft Q3D Extractor, electromagnetic simulation is carried out to extract the stray inductance from the two modules. Switching behavior with different package parasitics is studied based on Saber simulation. Two prototype phase-leg modules based on two different designs are fabricated. The parasitics are measured using a precision impedance analyzer. The measurement results agree with the simulation very well.

**Key words** – IGBT, phase-leg module, P-cell, N-cell, commutation loop, stray inductance

## I. INTRODUCTION

Power electronic modules constitute one of the driving forces towards modularization and integration of power electronic systems [1]. It improves the system performance by greatly reducing the package parasitic impedances. During the past several years, power device and module packaging technology has evolved through multiple generations, each with incremental improvements in performance and reliability.

High reliability and long-term stability are always critical issues and especially essential in high power applications. For example, according to [2], a 30-year lifetime, 338,000 long-term cycles, and 12 million short-term temperature changes are required for traction applications. A scenario that is commonly used to explain the IGBT failure is the coefficient of the thermal expansion (CTE) mismatch between the silicon and copper base-plate in the thermal cycling. Actually, in practical application, many failures are caused by the parasitic effects. The parasitic inductance exists from the IGBT chip collector and emitter to their terminal connections, no matter what kind of

package technology is used. The parasitic inductance stores energy whenever the current flows through the interconnections inside the module. When it turns off, the energy is released directly as a voltage spike if there is no external snubber capacitor in the current loop. The spike is a function of inductance and  $di/dt$  rate. How to deal with the parasitics effect will ultimately affect the EMI, efficiency, and performance of a circuit [2]. In layout design of IGBT packages and power stages with both high switching speed and high power handling requirements, reducing parasitics is extremely important.

Generally, the package stray inductance can be classified into three categories, as follows [4]:

1. Inductance due to DBC substrate pattern;
2. Inductance due to bonding wires;
3. Inductance of electrode;

Table I lists the parasitics in a 300 A 1200 V commercial power module, which provides a rough idea of the scale and how the parasitics are distributed in a power module [3].

TABLE I. SUMMARY OF PARASITIC INDUCTANCE

	Bonding Wire	DBC Conductor Trace	Terminal Conductors
Parasitic Inductance	10-15 nH	4-7 nH	30-40 nH

There are several considerations and improvements in the structure of the package to reduce the parasitics of the module. They are reviewed in the following:

### A. Terminal Arrangement

A laminated structure has smaller self inductance [4]. Also, when paralleling the positive and negative terminals, it enables the coupling of the two inductors to the most extent as a result. The equivalent loop inductance equals the two self-inductances minus the mutual inductance. Therefore, the higher the mutual inductance is, the lower the loop inductance is.

### B. Bonding Wires Consideration

First, the interconnection bond wires should be as short as possible. Second, the direction of substrate current, which flows under the emitter bonding wires, is usually designed to be opposite to the direction of current flow in bonding wires.

### C. Utilization of the Substrate Area

Although the substrate has the smallest inductance, large substrate area can still make the inductance considerably large. This is especially true for high power modules because the paralleling of the power devices enlarges the substrate area. When doing the substrate layout, maximum utilization of the full substrate area should be done.

### D. "U-package" Technology

Mitsubishi made a major improvement on the bus bar structure in the sense of reduced stray inductance in 1996. The bus bars were molded into the sides of the case, aluminum wires were used to connect the substrate or die to the terminal. Paralleling the main electrodes and narrowing the space were made easy. The distance between both electrodes can be reduced to benefit from the eddy current effect. This also relieved "S" bends that were needed in the electrodes of conventional modules. Elimination of these "S" bends helped to further reduce the electrode inductance. Overall, as a result of these inductance reducing features, the new package has about one third the inductance of conventional modules [4].

To summarize, some general rules to reduce the parasitic inductance are listed in Table II [4].

TABLE II. GENERAL METHODS TO REDUCE INDUCTANCE

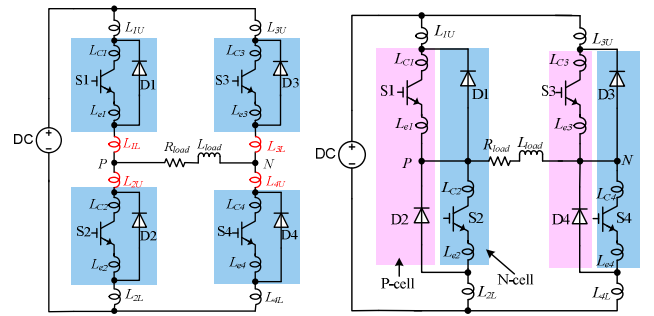
Classification	Inductance Reduction Methods
DBC Substrate Pattern	1. Widen the pattern width 2. Shorten the pattern length
Bonding Wires	1. Shorten the wire length 2. Increase the number of Al-wires 3. Increase the diameter of wires
Inductance of Electrode	1. Shorten the length 2. Increase the width 3. Parallel the main electrodes and reduce the space between the main electrodes 4. Use eddy current effect

Much work has been done to address the stray inductance reduction of power modules; however, one important issue has been neglected: the effective stray inductance while the module is operating. The stray inductance is everywhere in a module, the ones of most concern are those that are in the conduction path during switching on and switching off. Under inductive load

condition, current commutation is between upper IGBT and lower diode, or between lower IGBT and the upper diode. Therefore, in terms of natural current commutation path, it is more reasonable to construct a phase-leg by P-cell and N-cell [5][6]. During current commutation between active switch and diode, these inductances together with parasitic capacitance can cause voltage spikes and oscillations, which are the sources of electromagnetic interference and even cause damage to the devices under high  $di/dt$  condition [7][8]. Therefore modularization of P-cell and N-cell provides a new solution to reduce the stray inductance.

## II. IGBT MODULE PACKAGE MODELING AND PARASITICS EXTRACTION

As discussed in [9], P-cells and N-cells can form a phase-leg that has some benefits compared to the traditional anti-parallel phase-leg in inverters. Fig. 1 shows the diagrams of the two different inverter configurations. Under inductive load condition, current commutation is between  $S_1$  and  $D_2$  as shown in Fig. 1 (a) when current direction is from load terminal P to N, or between  $S_2$  and  $D_1$  when current is from N to P. Therefore, in terms of natural current commutation path, it is more reasonable to construct a phase-leg by P-cell and N-cell, as shown in Fig. 1 (b). Load current flows into the phase-leg through an N-cell and goes out of the phase-leg through a P-cell. Fig. 1 also shows the stray inductance within each phase-leg module. This stray inductance model is referred from [10].  $L_{1U}$  and  $L_{2L}$  are introduced by terminal leads;  $L_{1L}$ ,  $L_{2U}$  are the stray inductance of the internal bus connecting the upper and lower unit; the values of these four inductors are relatively large.  $L_{C1}$ ,  $L_{e1}$ ,  $L_{C2}$  and  $L_{e2}$ , are associated with the die and wire bond, which are relatively small. Since the physical distance between the two commuting devices is reduced, the inductance is also reduced. Comparing Fig. 1 (a) and (b), for the left phase-leg, inductances  $L_{1L}$ ,  $L_{2U}$  introduced by the internal bus are reduced in the cell structure.



(a) Conventional full bridge inverter (b) Proposed phase-leg inverter  
Fig. 1. Equivalent circuit with package parasitics.

Usually it is extremely expensive and time consuming to build power modules and verify the concept proposed in the last section. However, this process can be greatly simplified by the aid of software tool Ansoft Q3D Extractor. The software uses the method of moments (integral equations) and finite element methods to compute capacitance,

conductance, inductance, and resistance matrices. Providing the correct dimensions, material properties (resistivity of conductors and permittivity of insulators) and boundary conditions (the conductors and current paths), this software can extract the structural impedances of any arbitrary geometry. Thus, the module parasitics can be understood thoroughly before being practically built [11][12][13].

The conceptual phase-leg modules are built in Ansoft Q3D Extractor as shown in Fig. 2. For a better comparison purpose, the two modules are similar in terms of substrate size and lead frame position. The detailed dimensions are listed in Table III.

TABLE III. PHYSICAL SIZE OF THE TWO MODULES

	Conventional Layout	Proposed Layout
DBC Size (mm)	37.0×38.0	37.5×38.5
DBC Thickness (mil)	8(Cu), 25(Alumina)	8(Cu), 25(Alumina)
IGBT Size(mm)	5×5	5×5
Diode Size(mm)	5.85×5.85	5.85×5.85
Bond Wires	15 mils×2	15 mils×2

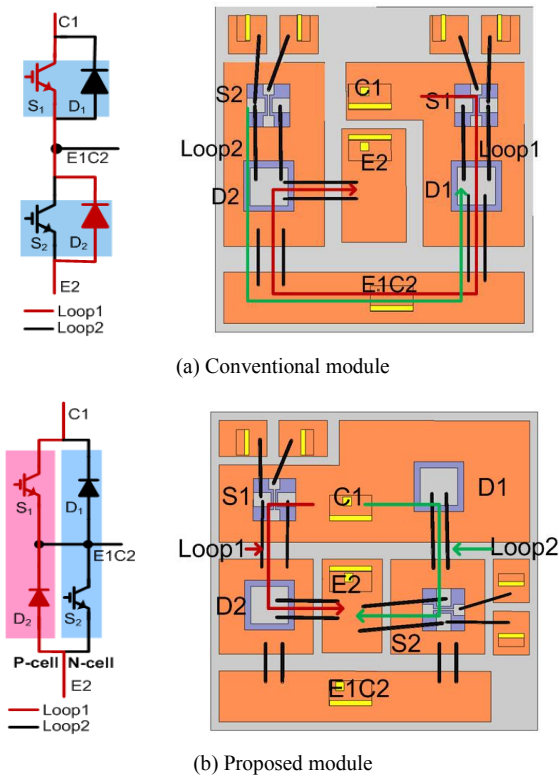


Fig. 2. Phase-leg module layout.

Fig. 2 shows the connection and physical layout of a conventional module and the proposed P-cell and N-cell structure module. Loop1 and Loop2 are two corresponding current commutation loops. In a conventional module (Fig. 2 (a)), the upper leg devices  $S_1$  and  $D_1$  are seated at one side,

while the lower leg, namely  $S_2$  and  $D_2$  are seated at the other side. The physical distance for Loop1 is shown as the red trace. In the proposed P-cell and N-cell modules, the two devices in the commutation loop are placed at the same side; thus, the physical length of the commutation loop is specifically reduced (Fig. 2 (b)). For example, Loop1 shown as the red trace starts from  $C_1$ , goes through only one group of wires, and then reaches  $D_2$ . This is much shorter than the same loop in a conventional module.

Also, other parasitic inductances associated with the module are studied thoroughly. The source and sink, which are the measuring points, are shown in Fig. 3 as the yellow area. The path from point A to point B is the commutation loop from the positive bus to the negative bus. There are two conduction paths: through  $S_1$ - $D_2$  which is loop1 shown in Fig. 2, and through  $S_2$ - $D_1$  which is loop2. The simulation is conducted this way: when calculating loop1, the materials of  $S_1$  and  $D_2$  are set to copper and  $S_2$   $D_1$  is set to silicon, so that only the  $S_1$ - $D_2$  path conducts; the other path is calculated the same way. The inductance of the bus bar is also calculated separately. The path from A to D is the positive bus bar, the path from B to E is the negative one, and the path from C to F is the AC output bus bar. They should have the same value since the same structure is used. In a commercial module, bus bars usually have larger dimensions and complex shape, however to simplify the fabrication process, the simulation uses a simpler copper bar. From H to G or from J to I is the gate drive loop.

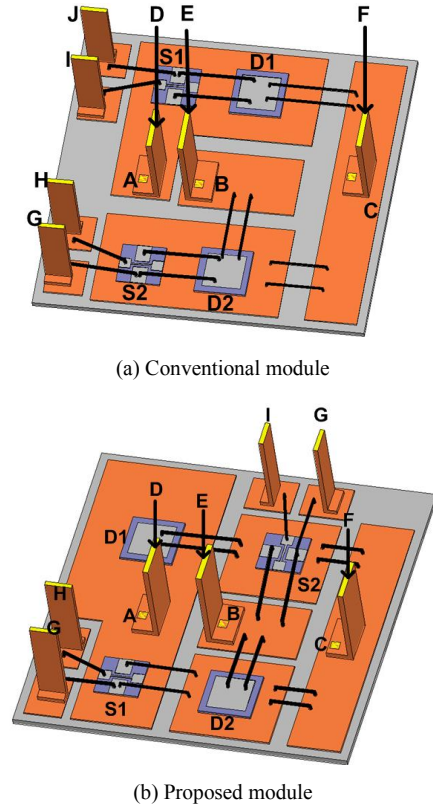


Fig. 3. Phase-leg modules with measuring points.

The simulation results are listed in Table IV. It can be seen that for AC values, in the conventional module, the inductances in traces A-B, which are the loop1 and loop2 in Fig. 2, are both around 20 nH, while in the proposed module they are less than 10 nH. As expected, the rearrangement of the dice layout has greatly reduced the inductance on the DBC trace, while the inductance values of the other components in two the modules are comparable. For DC values, there is also a substantial reduction in the loop inductance.

TABLE IV. PARASITIC RESISTANCE AND INDUCTANCE EXTRACTED FROM THE POWER MODULES

	Conventional Layout		Proposed Layout	
	DC Value (nH)	AC Value (nH)	DC Value (nH)	AC Value (nH)
A-B (Loop1)	38.3	20.5	11.7	7.2
A-B (Loop2)	38.3	20.3	14.4	8.6
A-D (also B-E or C-F)	4.2	3.5	4.2	3.5
G-H	16.6	13.5	16.6	13.5
I-J	16.6	13.5	16.6	13.5
E-C (via S2)	24.4	16.7	18.4	12.4
E-C (via D2)	21.4	14.6	15.8	11.3
C-D (via D1)	24.3	15.9	24.4	15.8
C-D (via S1)	27.1	20.8	20.9	14.7

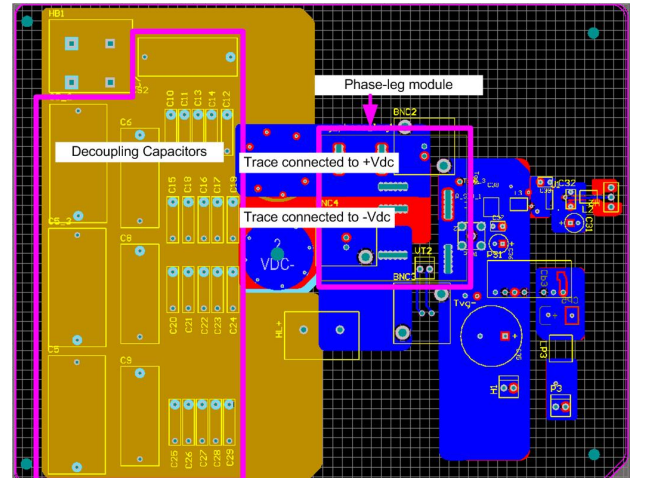
### III. EFFECTS OF PARASITIC PARAMETERS ON SWITCHING BEHAVIOR

After the extraction of the module parasitics, mainly the stray inductance, a circuit simulation is performed to characterize the switching behavior for the two different power module layout cases.

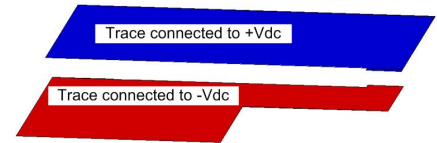
Typically, a double pulse tester is used to characterize the switching behavior under the influence of the module parasitics. However, not only the power module has parasitics, but the DC bus also introduces relatively large parasitics to the commutation loop, comparing with the module parasitics. The DC power comes from the supply and a large aluminum electrolytic capacitor, and then goes to the PCB. Several low ESR decoupling film capacitors are used to compensate the ESL of the cable. Therefore, only the inductance from the capacitor to the DC bus needs to be considered. The printed circuit board (PCB) is shown in Fig. 4 (a). The decoupling capacitors and the power module are shown in the figure. The traces (polygon) between these two are the ones that should be counted for the parasitics. To estimate the value, this part is analyzed using Q3D Extractor. Specifically, the top and bottom layers PCB design are exported to Q3D Extractor, the gate drive parts are deleted for simplification. Fig. 4 (b) shows the shapes of the two

traces after simplification. After the material is assigned and the space between different layers is set correctly, the parasitics can be extracted. For this specific design, the parasitic inductance is 28.4 nH.

Synopsys Saber is used to carry out the circuit simulation. The double pulse test circuit is shown in Fig. 5. Typically, only two pulses are applied to each IGBT, specifically the first pulse is used to obtain the desired current. The switch turns off at the desired current, current commutates to the diode, and turn-off behavior can be observed accordingly. After a short while, the switch is turned on at the second pulse. Due to the existence of the large inductive load, the current does not change much, and turn-on behavior under the desired current can be observed.



(a) PCB of the double pulse tester



(b) The DC link traces from which the parasitics are extracted

Fig. 4. Double pulse tester PCB design.

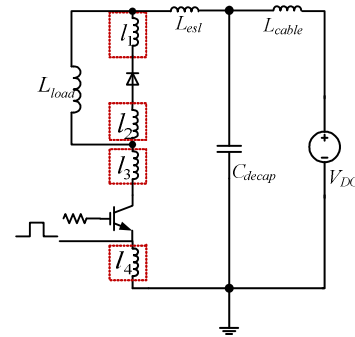


Fig. 5. Double pulse tester circuit.

The parameters used in the double pulse tester are shown in Table V.  $l_1$ ,  $l_2$ ,  $l_3$  and  $l_4$  are the point to point inductance,

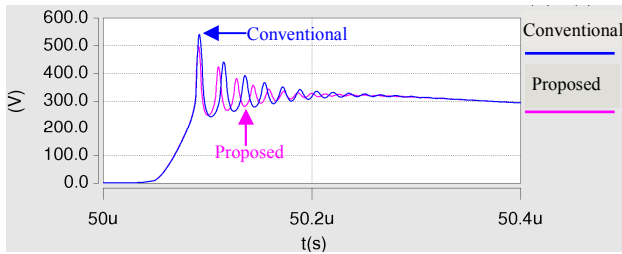


while the loop inductance in Table IV is the sum of these four inductances. The IGBT and diode are practical models from the Saber library. The Fairchild IGBT is rated 600 V/40 A; the IR diode is rated at 600 V/ 45 A. The simulation is conducted under 300 V/ 30 A.

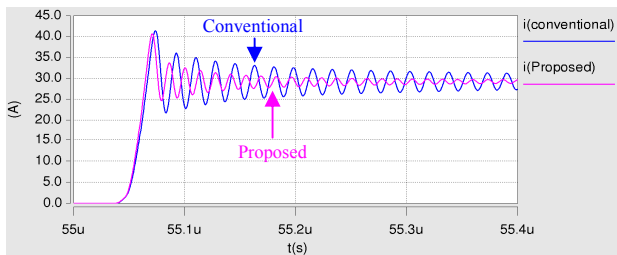
Simulation results from the double pulse tester show the superiority of the proposed module compared to the conventional one. The voltage across the IGBT during turn off is shown in Fig. 6 (a). After the voltage rises to the DC link voltage, there is an abrupt drop of the IGBT current, high  $di/dt$  causes a voltage drop across the stray inductance, which applies on the IGBT and causes voltage overshoot and oscillation. As can be seen, the voltage overshoot is 246 V in the conventional module, while that in the proposed module is 200 V. During turn-on, after the IGBT current reaches the load current, the diode reverse recovery begins, and the IGBT turn-on current has an overshoot. After that, this current rings between the parasitic inductance and the diode parasitic capacitance. This phenomenon is shown in Fig. 6 (b). The ringing damps fast in the proposed module as a result of the reduced inductance [9].

TABLE V. PARAMETERS IN DOUBLE PULSE TESTER

Parameters	Values
$L_{load}$	500 $\mu$ H
IGBT	HGTG40N60B3
Diode	HFA45HC60C
DC source voltage	300 V
$L_{esl}, C_{decap}$	28.4 nH, 3.38 $\mu$ F
$l_1, l_2, l_3, l_4$ in conventional module	8.6 nH, 5.1 nH, 5.1 nH, 8.6 nH
$l_1, l_2, l_3, l_4$ in proposed module	5.6 nH, 2.1 nH, 2.1 nH, 5.6 nH



(a) Voltage waveform across IGBT at turn-off.



(b) IGBT current waveform at turn-on.

Fig. 6. Switching behaviors under module parasitics.

#### IV. MEASUREMENT RESULTS

To verify the results of the parasitic extraction, the two phase-leg modules are fabricated and measured in the laboratory.

Since an IGBT is a normally off device, the commutation loop shown in Table IV is not conducting by nature. The inductance can be measured piece by piece; however, the inductance is too small to be accurate, and also, it does not take the coupling effect between the pieces into account. In the previous simulation, the devices are set to copper to get a conductive commutation loop. Actually, they have the same effect that the devices are set to conductor and the wires bond directly to DBC. Therefore, in the measurement, modules without devices are fabricated, in which the wires are bonded directly to DBC. Taking the conventional module loop2 in Fig. 2 for an example, to measure this loop inductance, S2 and D1 are conducting, so that the wires are bonded directly to the DBC where S2 and D1 seat as shown in Fig. 7. The conducting trace actually is from terminal C1 through DBC copper trace to D1, and through a group of bonding wires to the DBC where the output terminal seats, and then through another set of wires to S2 and through DBC to the negative terminal. The simulated result for this arrangement is very close to the values shown in Table IV.

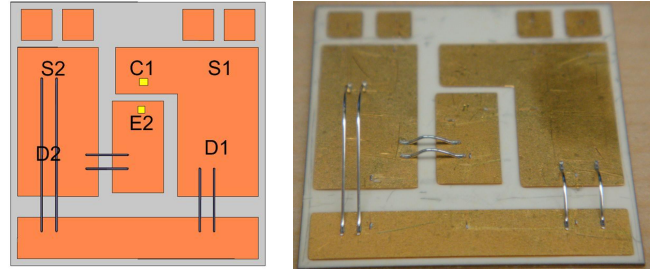


Fig. 7. Fabricated module for parasitic measurement (The left one is drawn in Q3D Extractor, the right one is the fabricated module).

Another concern is the measuring equipment. Since the inductance is very small, Agilent precision impedance analyzer 4294A is used as shown in Fig. 8. The frequency range is from 40 Hz to 110 MHz. High frequency is necessary for the small inductance to get a measurable impedance, so that when a current is applied to the inductance, a decent amount of voltage is ensured, therefore the accuracy of the measurement is guaranteed. Since the measurement uses alternative current, this result should compare to the AC simulation results listed in Table III. Meanwhile, using the correct probe fixture is also critical in this measurement. The commonly used alligator probe is not proper in this condition. The wires with the alligator probe introduce parasitics that are comparable to the one under test, and even larger. Here we use a pin probe; the shape of the probe is fixed. The parasitics with this probe is small and can be completely compensated through calibration.

Fig. 9 shows the measured results. The testing frequency range is from 1 MHz to 10 MHz, where the impedance of

the module is inductive. The level of the solid triangle in the left of the graph is the reference inductance value, which is shown at the top. The scale of the division is also shown at the top. With the reference and the scale, the value of the measurement line can be decided. For example, in Fig. 9 (a), the measured line is two to three divisions below the reference value, which is 28 nH, therefore the measured value is between 25 nH to 26 nH. The complete comparison of the measurement and simulation is listed in Table VI. The measurement value should compare with the AC simulation results, because in measurement, AC excitation is used.

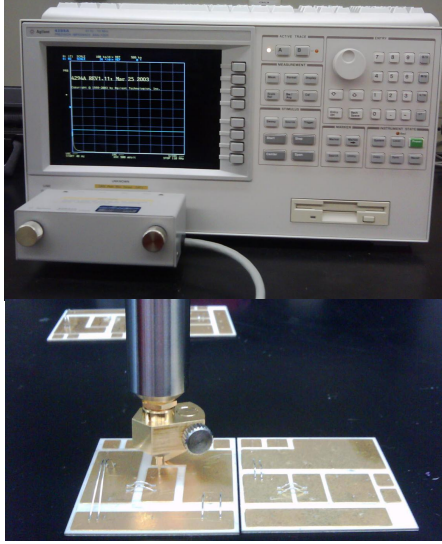


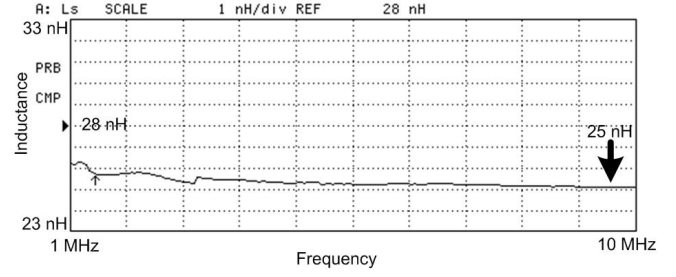
Fig. 8. Impedance analyzer and probe fixture in the experimental test.

TABLE VI. COMPARISON OF THE MEASUREMENT AND SIMULATION

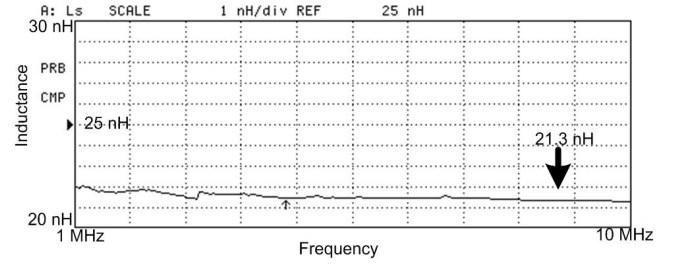
		Simulation Result (nH)	Measurement Result (nH)
Conventional Module	Loop 1	20.5	25
	Loop 2	20.3	21
Proposed Module	Loop 1	7.2	6.5
	Loop 2	8.6	6

## V. CONCLUSIONS

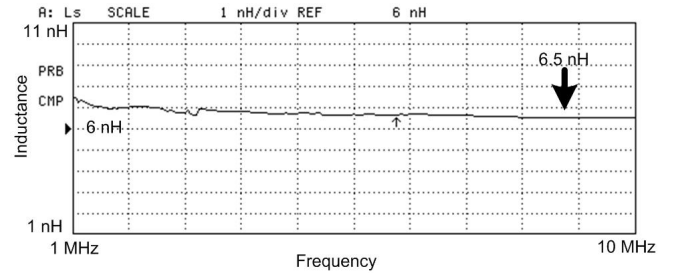
To reduce the stray inductance in an IGBT power module, a new layout design is proposed based on the P-cell and N-cell concept. The superiority of the proposed IGBT module compared to the conventional anti-parallel switching cell is presented in terms of layout design, parasitics extraction, circuit simulation and experimental test. The results show that the stray inductance of the proposed IGBT module is dramatically reduced due to the use of P-cell and N-cell. Also, due to the reduction of stray inductance, the overshoot voltage and ring current are also reduced during switching off and on, respectively. Thus, the proposed module will improve the system performance and reliability.



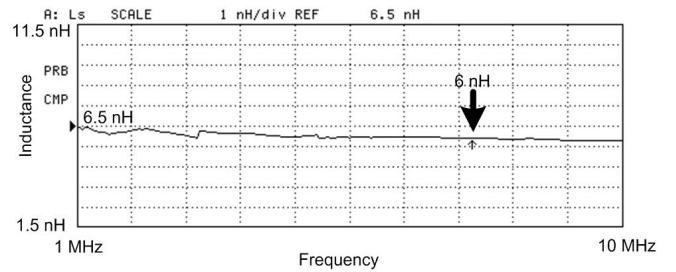
(a) Measured result of stray inductance for conventional module loop1.



(b) Measured result of stray inductance for conventional module loop2.



(c) Measured result of stray inductance for proposed module loop1.



(d) Measured result of stray inductance for proposed module loop2.

Fig. 9. Measured results.

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