Active Harmonic Elimination in Multilevel Converters Using FPGA Control

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***Abstract*—This paper presents an optimal total harmonic distortion (THD) control algorithm referred to as active harmonic elimination method for cascaded H-bridges multilevel converter control with unequal DC sources. First, the multilevel converter is decoupled into unipolar converters, the low order harmonics, such as the 5th, 7th, 11th and 13th are eliminated by using elimination theory, and the minimum THD combination of unipolar converters for multilevel converter control is found. Next, the magnitudes and phases of the residual higher harmonics are computed and subtracted from the original output voltage waveform to eliminate these higher harmonics. To validate the proposed algorithm, the method is simulated by Matlab first. After the simulation, an experimental 11-level H-bridge multilevel converter with a real-time controller based on Altera FLEX 10K field programmable gate array (FPGA) is used to implement the algorithm with 8 μs control resolution. The experimental results show that the method can effectively eliminate the specific harmonics as expected, and the output voltage waveforms have low THD.**

Keywords-*Multilevel converter; active harmonic elimination; FPGA control.*

I. INTRODUCTION

Multilevel converters continue to receive more and more attention because of their high voltage operation capability, low switching losses (high efficiency) and low output of electro-magnetic interference (EMI). The desired output of a multilevel converter is synthesized by several sources of DC voltages. With an increasing number of DC voltage sources, the converter voltage output waveform approaches a nearly sinusoidal waveform while using a low switching frequency scheme. This results in low switching losses, and because several DC sources are used to synthesize the total output voltage, each switch experiences a lower dV/dt compared to a single level converter. Consequently, the multilevel converter technology is a promising technology for high power electric devices such as utility applications [3]-[5].

The traditional PWM method, space vector PWM method, sub-harmonic PWM method (SH-PWM) [11] and switching frequency optimal PWM (SFO-PWM) [12] for multilevel converters require equal DC voltage sources. One control method for multilevel converters is the fundamental frequency switching method. Such a scheme is considered in [7] wherein the transcendental equations characterizing the harmonic content are converted into polynomial equations [7]. Elimination theory [1] [2] [9](using resultants) was then used (along with the special symmetry properties of the equations) to determine the switching angles to eliminate specific harmonics, namely the 5th, 7th, 11th, and 13th. However, as the number of DC sources increases, the degrees of the polynomials in these equations are large and one reaches the limitations of the capability of contemporary computer algebra software tools (e.g., Mathematic or Maple) to solve the system of polynomial equations using elimination theory [8].

The benefit of the fundamental frequency switching method is its low switching frequency compared to other control methods. Generally, the computational complexity of the method limits its use to multilevel converters with equal DC sources. If one wanted to apply the method to multilevel converters with changing (unequal) DC sources, the set of transcendental equations to be solved are no longer symmetric and require the solution of a set of high-degree equations, which is beyond the capability of contemporary computer algebra. In order to use the method, the constant DC source voltages must be maintained which increases the cost of the system [10].

To overcome the computational difficulty of the resultant method with unequal DC voltage sources, a new optimal PWM algorithm is proposed in this paper. We refer to it as an active harmonic elimination method. Consider a multilevel converter with unequal DC voltage sources. For each level, the set of transcendental equations characterizing the harmonics is developed. The low order harmonics for each DC voltage source (the 5th, 7th, 11th and 13th in the experiments reported here) are eliminated using a unipolar switching scheme in which the switch angles are determined using elimination theory [7][8]. Then the combination for desired fundamental output voltage with the lowest total harmonic distortion (THD) is searched. Specifically chosen higher order harmonics (the odd non triplen harmonics from the 17th to the 25th in the experiments) are eliminated by using an additional switching angle (one for each higher harmonic) to generate the negative of the harmonic in order to cancel it. Therefore, the output voltage waveform will have low THD.

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An experimental 11-level H-bridge multilevel converter is employed to validate the method. The experimental results show that the fundamental frequency switching method can effectively eliminate low order harmonics. The experimental results also show that the active harmonic generating elimination method can effectively cancel specifically chosen higher order harmonics.

II. Resultant Method for Unipolar Switching Scheme Converter

Based on harmonic elimination theory, the control of the sinusoidal wave generation is to choose a series of switching angles to synthesize a desired sinusoidal voltage waveform. A typical 5-angle unipolar switching output is shown in Fig. 1.

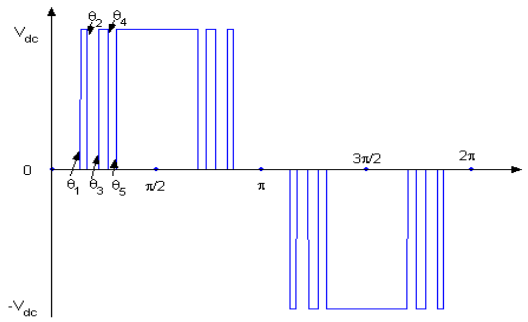

Fig. 1. 5-angle unipolar switching output

The Fourier series expansion of the output voltage waveform as shown in Fig. 1 is

$$V(t)=\sum_{n=1,3,5\ldots}^{\infty}\frac{4V_{dc}}{n\pi}[\cos(n\theta_1)-\cos(n\theta_2)+\cos(n\theta_3)-\cos(n\theta_4)+\cos(n\theta_5)]\sin(n\omega t) \tag{1}$$

Ideally, given a desired fundamental voltage V_1, one wants to determine the switching angles θ_1, θ_2, θ_3, θ_4 and θ_5 so that $V(\omega t)=V_1(\omega t)$, and specific higher harmonics of $V_n(\omega t)$ are equal to zero. For a three-phase application, the triplen harmonics in each phase need not be canceled as they automatically cancel in the line-to-line voltages. Here, the 5th, 7th, 11th, and 13th order harmonics are chosen to be removed.

That is, the switching angles must satisfy the following equations:

$$\begin{aligned}
&\cos(\theta_1)-\cos(\theta_2)+\cos(\theta_3)-\cos(\theta_4)+\cos(\theta_5)=m\\
&\cos(5\theta_1)-\cos(5\theta_2)+\cos(5\theta_3)-\cos(5\theta_4)+\cos(5\theta_5)=0\\
&\cos(7\theta_1)-\cos(7\theta_2)+\cos(7\theta_3)-\cos(7\theta_4)+\cos(7\theta_5)=0\\
&\cos(11\theta_1)-\cos(11\theta_2)+\cos(11\theta_3)-\cos(11\theta_4)+\cos(11\theta_5)=0\\
&\cos(13\theta_1)-\cos(13\theta_2)+\cos(13\theta_3)-\cos(13\theta_4)+\cos(13\theta_5)=0
\end{aligned} \tag{2}$$

Here, m is defined as modulation index:

$$m=\pi V_1/(4V_{dc}) \tag{3}$$

and the THD is computed as

$$THD=\frac{\sqrt{\sum_{i=5,7,11,13,\cdots}^{49}V_i^2}}{V_1} \tag{4}$$

The resultant method described in [8] is used here to find the solutions (when they exist). The switching angles θ_1, θ_2, θ_3, θ_4 and θ_5 solutions versus the modulation index are shown in Fig. 2. Fig. 3 shows the THD corresponding to the solutions.

From the switching angle solutions shown in Fig. 2, it can be derived that the solutions exist in a range of the modulation indices from 0 to 0.91. Some modulation indices have no solutions, and there are more than one solution sets for some modulation indices.

Fig. 3 shows that different solution sets have different THD values. Another feature is the THD is very high for the low modulation index range.

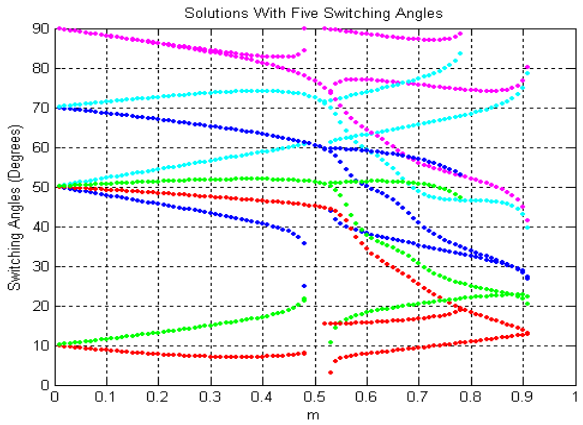

Fig. 2. Five-angle solutions vs. m

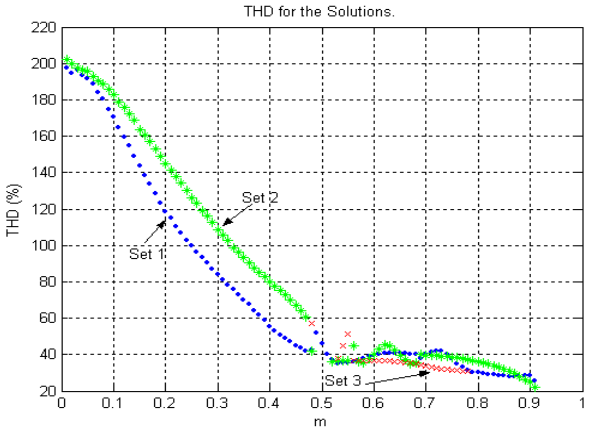

Fig. 3. THD vs. m

III. Proposed Multilevel Converter Control with Unequal DC Voltage Sources

A cascaded H-bridge multilevel converter can be viewed as several unipolar converters connected in series, and these unipolar converters can each be controlled independently. The control method inherently cannot generate low order harmonics since each unipolar converter does not generate low order harmonics even with unequal DC voltage sources.

Each unipolar converter for i=1, …, s (here s is the number of DC voltage sources) is required to satisfy the equations described in (2), that is

$$\begin{aligned}
&\cos(\theta_{i1})-\cos(\theta_{i2})+\cos(\theta_{i3})-\cos(\theta_{i4})+\cos(\theta_{i5})=m_i\\
&\cos(5\theta_{i1})-\cos(5\theta_{i2})+\cos(5\theta_{i3})-\cos(5\theta_{i4})+\cos(5\theta_{i5})=0\\
&\cos(7\theta_{i1})-\cos(7\theta_{i2})+\cos(7\theta_{i3})-\cos(7\theta_{i4})+\cos(7\theta_{i5})=0\\
&\cos(11\theta_{i1})-\cos(11\theta_{i2})+\cos(11\theta_{i3})-\cos(11\theta_{i4})+\cos(11\theta_{i5})=0\\
&\cos(13\theta_{i1})-\cos(13\theta_{i2})+\cos(13\theta_{i3})-\cos(13\theta_{i4})+\cos(13\theta_{i5})=0
\end{aligned} \tag{5}$$

The total modulation index $m=\Sigma_{i=1}^{s}c_i\left(V_{dci}/V_{dc}\right)m_i$, where V_{dc} is the nominal DC voltage, V_{dci} is the i^{th} DC voltage and c_i ($c_i\in\{-1,0,1\}$) is a "combination coefficient". For convenience, let $k_i=(V_{dci}\ /\ V_{dc})$ so that $m=\Sigma_{i=1}^{s}c_ik_im_i$. The problem here is: Given m and k_i for i=1,…, s compute c_i and m_i that minimizes the total harmonic distortion, i.e., $THD=\left(\sqrt{\Sigma_{i=5,7,11,13,\ldots}^{49}V_i^2}\right)/V_1$.

In other words, for each modulation index m, find the combination (c_i, m_i) for i=1,…, s of the DC sources that gives the lowest THD.

For example, for s=4, the goal is the lowest THD and the elimination of the 5th, 7th, 11th, 13th, 17th, 19th, 23rd and 25th harmonics. The optimal goal is to find a combination with s separate DC sources with lowest higher order harmonic distortion:

$$THD=\left(\sqrt{\Sigma_{i=29,31,35,37,\ldots}^{49}V_i^2}\right)/V_1 \tag{6}$$

Here, THD is only computed by higher order harmonics because the 5th, 7th, 11th, 13th harmonics are eliminated by unipolar switching scheme, and the 17th, 19th, 23rd, 25th will be eliminated by generating corresponding negative harmonics to cancel them. This will be introduced in the next section. A combination of the unipolar converters with the lowest THD will be given by (6). Therefore, there are no the 5th, 7th, 11th, 13th, 17th, 19th, 23rd, 25th harmonics, and the 29th, 31st, 35th, 37th, 41st, 43rd, 47th, 49th should be very low.

Consider a numerical example in which k_1=1.1617, k_2=1.0278, k_3=0.9722, k_4=0.9444. In this case, for each m one must solve $m=\Sigma_{i=1}^{s}c_ik_im_i$ for the (c_i, m_i) that minimize the THD. The minimum THD achieved by this method is shown in Fig. 4 and labeled Example 1. As another example, let k_1=1.0556, k_2=1.0278, k_3=1.0, k_4=0.9444 and again the minimum achievable THD is also plotted in Fig. 4 and labeled as Example 2. Although the THD for a single unipolar converter is high, these examples show that it can be low for a combination of several unipolar converters.

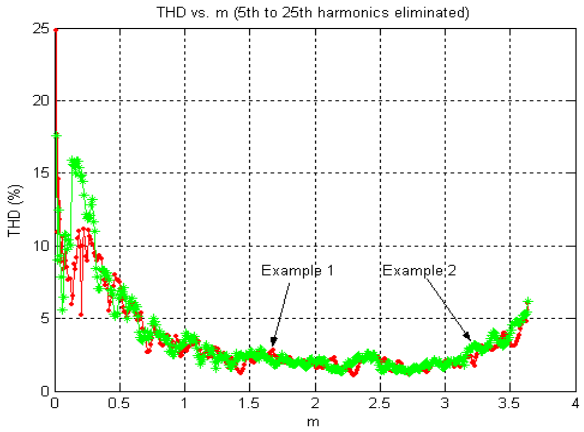

Fig. 4. Minimum THD with 5-25th harmonics eliminated

IV. Active Harmonic Generating Method to Eliminate High Order Harmonics

From equation (1), the voltage contents can be divided into four parts:

$$V(\omega t)=V_{p1}(t)+V_{p2}(t)+V_{p3}(t)+V_{p4}(t) \tag{7}$$

1. Fundamental frequency voltage:

$$V_{p1}(t)=\sum_{i}^{s}\frac{4c_ik_iV_{dc}}{\pi}[\cos(\theta_{i1})-\cos(\theta_{i2})+\cos(\theta_{i3})-\cos(\theta_{i4})+\cos(\theta_{i5})]\sin(\omega t) \tag{8}$$

2. Triplen harmonic voltages:

$$V_{p2}(t)=\sum_{i}^{s}\sum_{n=3,9,15,\cdots}\frac{4c_ik_iV_{dc}}{n\pi}[\cos(n\theta_{i1})-\cos(n\theta_{i2})+\cos(n\theta_{i3})-\cos(n\theta_{i4})+\cos(n\theta_{i5})]\sin(n\omega t) \tag{9}$$

3. Low order harmonic voltages that can be eliminated by applying resultant method.

$$V_{p3}(t)=\sum_{i}^{s}\sum_{n=5,7,11,13}\frac{4c_ik_iV_{dc}}{n\pi}[\cos(n\theta_{i1})-\cos(n\theta_{i2})+\cos(n\theta_{i3})-\cos(n\theta_{i4})+\cos(n\theta_{i5})]\sin(n\omega t) \tag{10}$$

4. High order harmonic voltages that have not been eliminated by the unipolar switching scheme.

$$V_{p4}(t)=\sum_{i}^{s}\sum_{n=17,19,23,\cdots}\frac{4c_ik_iV_{dc}}{n\pi}[\cos(n\theta_{i1})-\cos(n\theta_{i2})+\cos(n\theta_{i3})-\cos(n\theta_{i4})+\cos(n\theta_{i5})]\sin(n\omega t) \tag{11}$$

Assuming the application is a balanced three-phase system, the triplen harmonics (9) need not be eliminated. This then

leaves the higher order harmonics (11). To eliminate these harmonics, the active harmonic generating elimination method is used. A square wave is generated (one for each of these harmonics) whose fundamental is equal to the negative of the harmonic that is to be eliminated. For example, to eliminate the 17th harmonic, a square wave whose Fourier series expansion is

$$V(t) = -\sum_{i}^{s} \sum_{m=1,3,5\cdots} \frac{4c_i k_i V_{dc}}{m\pi} [\cos(mh\theta_{i1}) - \cos(mh\theta_{i2}) + \cos(mh\theta_{i3}) - \cos(mh\theta_{i4}) + \cos(mh\theta_{i5})] \sin(mh\omega t) \quad (12)$$

is generated. When h=17, the m=1 term of (12) cancels the n=17 term of (11) and the next harmonic of concern that is produced by (12) is at 5×17=85. This harmonic and higher ones (7×17, etc.) are easy to filter using a low-pass filter. Repeating the above procedure to the multilevel converter, the 19th, 23rd, etc. harmonics can all be eliminated. The net effect of this method is to remove the low order harmonics and to generate new higher order harmonics by increasing the switching frequency. The additional switching number in a cycle for the active harmonic elimination method is $N_{sw} \le \sum_{n=17,19,23,\cdots} n$. For example, if the harmonics are eliminated through 25th, the upper limit switching number is 84. Fig. 5 shows a simulation result with the harmonic elimination up to 25th.

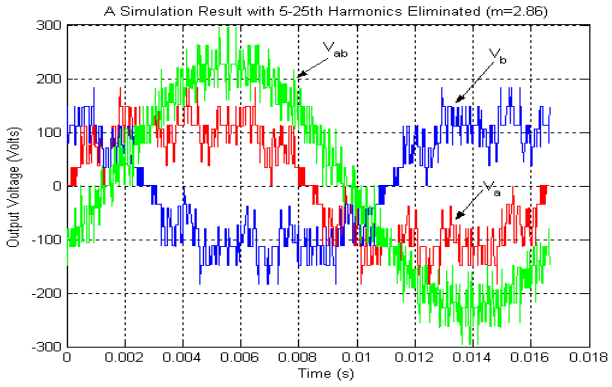

Fig. 5. Simulation voltage waveform with 5-25th harmonics eliminated (f=60Hz) (THD=1.79%)

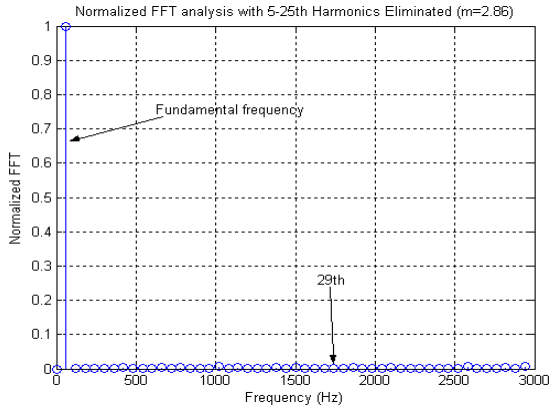

Fig. 6. Normalized FFT analysis of line-line voltage shown in Fig. 5 (f=60Hz)

The FFT analysis of the line-line voltage of Fig. 5 is shown in Fig. 6. The 5th, 7th, 11th, 13th, 17th, 19th, 23rd, 25th harmonics are zero, and the 29th, 31st, 35th, 37th, 41st, 43rd, 47th, 49th are very low, near zero.

V. HARDWARE IMPLEMENTATION

A real-time controller based on Altera FLEX 10K field programmable gate array (FPGA) is used to implement the algorithm. The block diagram of the controller is shown in Fig. 7.

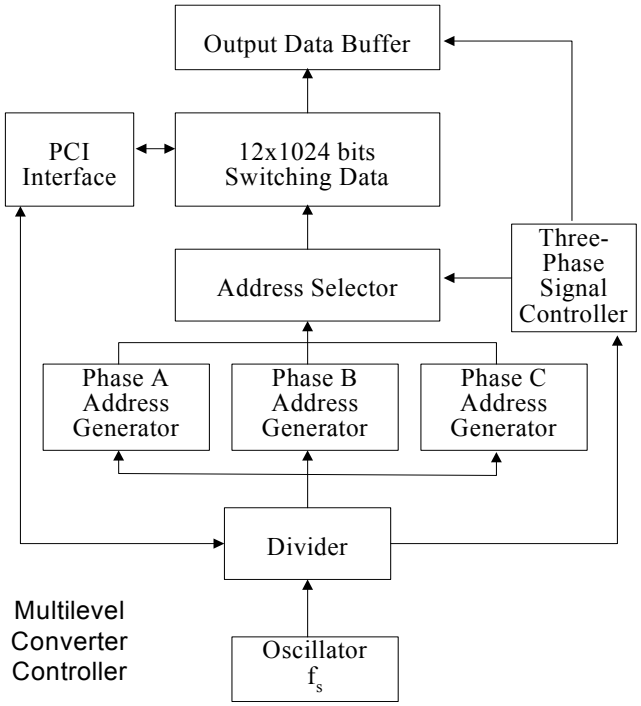

Fig. 7. Block diagram for the FPGA controller

The switching data are stored in a 12×1024 bits in-chip RAM. The RAM is used to store half cycle data up to a thirteen-level multilevel converter. An oscillator generates a fixed frequency clock signal, and a divider is used to generate the specified control clock signal corresponding to the multilevel converter output frequency. Three phase address generators share a public switching data RAM because they have the same switching data with different phase angle, and the switching data is only for one half cycle because the switching data is symmetric. For each step, the three-phase signal controller controls the address selector to fetch the corresponding switching data from the RAM to the output buffer. Assume the oscillator's frequency is f_s, the multilevel converter output frequency is f_0, and there are 2048 steps for each multilevel converter output cycle. The divider number N is:

$$N = f_s / f_0 / 2048 \quad (13)$$

The control resolution or the step size is:

$$T_s = 1 / f_0 / 2048 \quad (14)$$

If the output frequency f_0 is 60 Hz, the control resolution by (14) is 8.138 μs.

For convenience of operation, the FPGA controller was designed as a card to be plugged into a personal computer, which used a peripheral component interconnect (PCI) bus to communicate with the microcomputer. The whole system block is shown in Fig. 8.

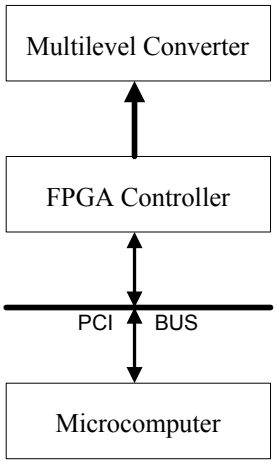

Fig. 8. System block

In Fig. 8, the microcomputer is used to interface with the user, compute the switching data and store the switching data into the RAM of the controller. The control signals are generated by FPGA hardware instead of software to guarantee real-time control performance of the system. The system structure also guarantees low computational load of the microcomputer because it just computes the switching data once for each modulation index m and its computational time cannot disturb the system's control performance.

VI. Experimental Results

The proposed multilevel converter control method has been implemented in an 11-level H-bridge multilevel converter, which is shown in Fig. 9, to eliminate the non-triplen harmonics up to the 25th where V_{dc}=36V, m=2.86 and k_1=1.1617, k_2=1.0278, k_3=0.9722, k_4=0.9444.

Fig. 9. 10 kW multilevel converter prototype

Fig. 10 shows the 60-Hz output line-line voltage waveform. Fig. 11 shows the FFT analysis of the line-line voltage. From the FFT plot in Fig. 11, it is seen that all harmonics up to the 25th have been eliminated. The THD based on theoretical computation, simulation, and experiment are 1.31%, 1.79%, and 2.28%, respectively. The THD for the experiment is a little higher than that of theoretical computation and simulation because the limitation of control resolution is 8 μs, and the switches are not ideal.

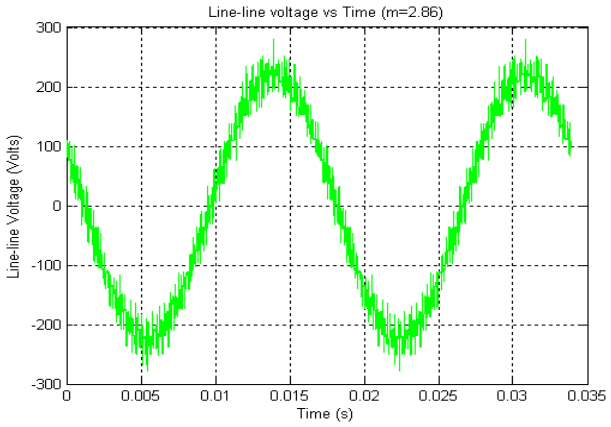

Fig. 10. Experimental line-line voltage with5-25th harmonics eliminated (f=60Hz) (THD=2.28%)

It can be seen from Fig. 10 that the line-line voltage waveform is very close to a sinusoidal waveform. Only very high frequency harmonics with low magnitudes exist in the line-line voltage.

The FFT analysis of the line-line voltage of Fig. 10 shown in Fig. 11 confirms the expectation that the 5th, 7th, 11th, 13th, 17th, 19th, 23rd, 25th harmonics are zero, and the 29th, 31st, 35th, 37th, 41st, 43rd, 47th, 49th are very low, near zero. This proves the theoretical computation and simulation.

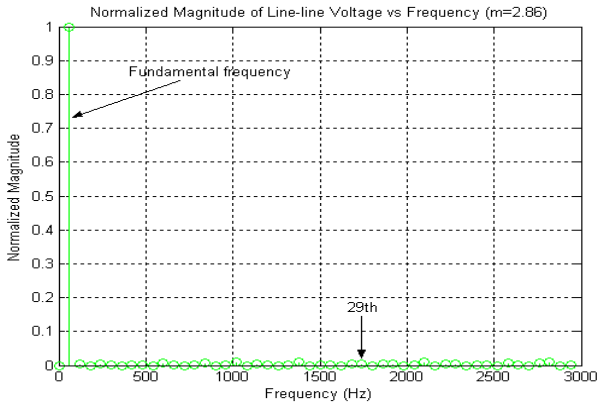

Fig. 11. Normalized FFT analysis of line-line voltage shown in Fig. 11

VII. CONCLUSION

This paper proposes and develops an active harmonic elimination control algorithm for multilevel converters with unequal DC voltage sources. The simulation results and experimental results show that the algorithm can be used to eliminate specific higher order harmonics effectively and result in a dramatic decrease in the output voltage THD.

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