Multilevel Cascade H-bridge Inverter DC Voltage Estimation Through Output Voltage Sensing

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***Abstract* — This work presents an approach to determine the input voltage value of each cell in a cascade H-bridge multilevel inverter using a sensor at the output of the inverter to eliminate all the dc voltage sensors measuring the individual source voltages. The input voltages can be equal or unequal. The MOSFET device datasheet, the ambient temperature, and the modulation strategy are utilized to estimate the switch voltage drop to compensate for the measurement. The output voltage is then processed by a DSP unit that uses the signals that command the switches to estimate the voltage at each cell. Simulation and experimental results are shown for a seven-level cascade multilevel inverter operating under a RLC load.**

I. INTRODUCTION

Multilevel converters make it possible to achieve medium voltage generation using low to medium voltage switches, preventing high dv/dt stress and need for series connection of switches while allowing higher converter power rating. Multilevel converters have less filter requirements, generate a staircase waveform, have better harmonic profile (lower total harmonic distortion), and have less switching losses. However, they need more components, driver isolation becomes complex since additional levels need isolated power supplies, and the cost is higher compared to conventional single-cell topologies [1-4].

Cascade H-bridge (CHB), diode-clamped and capacitor-clamped are among the most common topologies and are well documented in the literature [5-6]. In grid-connected or standalone applications, the DC source supplying each cell needs to be sensed and processed by the control system as the inverter power supply may vary. For example, interface of solar panels or fuel cell to the grid or for stand-alone systems requires voltage-sensing feedback to the control system [7]. Voltage sensors are also required in photovoltaic (PV) systems to accomplish maximum power point tracking (MPPT) and ensure power delivery maximization [8]. The CHB topology, with its multiple isolated power supplies, needs an individual sensor for each DC power supply. The number of sensors increases with an increasing number of levels. Additionally, the sensors on the upper levels require isolation due to the independent DC sources in the topology. The methodology proposed here calculates the individual input voltages using a single sensor at the output instead of a sensor for each H-bridge in the topology. This method will reduce the number of voltage sensors required in a multilevel topology by the number of H-bridges. One disadvantage comes from the fact that the sensor has to compensate the measured voltage with the effect of the on-state resistance, voltage drop, and stray inductance of the switches used. The approach to compensate the measured output voltage will be explained for a MOSFET-based seven-level CHB.

II. LEVEL VOLTAGE ESTIMATION

The 7-level cascade inverter topology is presented in Fig. 1(a). It has three full bridge series connected configuration with three isolated input DC supplies that may have different voltage levels. In order to determine the voltage level of each voltage input (V_{DCx}, where x is 1, 2 or 3), the voltage and current before the LC filter are sensed and processed to estimate the individual voltage levels. The same logic signals that are sent to the gate drivers are used by the DSP to determine the individual voltage levels. The internal DSP logic function takes into account the rise time, fall time, on-state resistance, and forward voltage drop. Level-shifted carriers v_{cr} are compared with the modulating signal v_m to generate the gate signals to the H-bridges. Those logic signals are taken to derive the measurement window where the output voltage is measured to determine the individual level. This is illustrated in Fig. 1(b).

The time available for voltage measurement of each level can be determined based on the modulation index and carrier frequency. In Fig. 1, a 540 Hz carrier frequency is illustrated with three cascade H-bridges (CHB) where switches Q_{1x} correspond to the lower HB and Q_{3x} the upper HB. Assuming that configuration, the total time available for each level to do a measurement is presented in Fig. 3 for 7, 9 and 11 level configurations. The height of the bar indicates the amount of time spent on that level. In Fig. 3(a) the blue bar (lower) indicates the time spent on HB1, the green bar (middle) indicates the time HB1 and HB2 are both

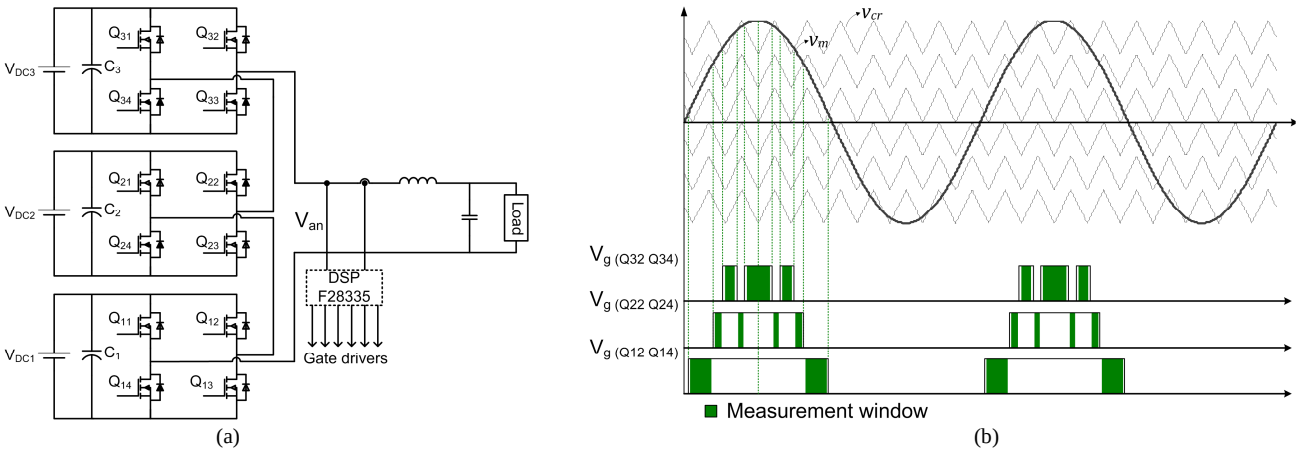


Figure 1. Seven-level cascade multilevel inverter (a) and level-shifted modulation at f_{cr} = 540 Hz (b).

on and the red bar (upper) the time all the levels are on. The total time adds up to less than 60Hz because of the level zero. In Fig. 3(a) for a 540Hz carrier frequency the smallest window available is approximately 2 ms for a modulation index greater than 0.8. This is equivalent to 100 measurements using a sample time of 20 us (50 kHz) during one cycle. The plots in Fig. 3 vary slightly depending on the way the carrier is generated. Additionally, a low modulation index may bypass the upper levels.

III. ON-STATE RESISTANCE

The switch on-state resistance will cause a voltage drop that needs to be compensated by the sensor. In the n-channel enhanced mode, the on-state resistance is proportional to the rate of change between the drain-to-source voltage v_{ds} and current i_{ds}.

$$R_{DS(ON)} = \left.\frac{\partial v_{ds}}{\partial i_{ds}}\right|_{V_{GS}=const.} \quad (1)$$

Then, the forward voltage drop at a given drain current I_D can be written as:

$$V_{drop} = I_D R_{DS(on)} \quad (2)$$

The inverter current is readily available at the output. However, the switch on-state resistance is dependent on the junction temperature that can be estimated if the ambient temperature and the thermal resistance over the thermal heat path can be determined. An equivalent thermal model is shown in Fig. 2 where the different thermal resistances are modeled as series resistors and the transients are modeled by the capacitors. Since steady state is being analyzed, the parallel capacitors will not be included in the model. The power loss (P_L) in the switch is modeled in the circuit of Fig. 2 as a current source, and the ambient (T_a) and junction (T_j) temperatures are represented as the node voltages. The thermal resistances are represented by resistors $R_{\theta jc}$, $R_{\theta ch}$, $R_{\theta ha}$.

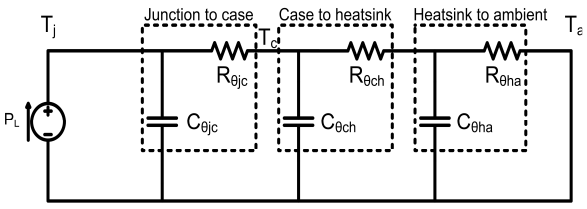


Figure 2. System equivalent thermal path model.

The junction temperature can be estimated in steady state for each switch by using (3),

$$T_j = T_a + P_L\left(R_{\theta jc} + R_{\theta ch} + R_{\theta ha}\right) \quad (3)$$

where,

$R_{\theta jc}$: Junction-to-case thermal resistance.

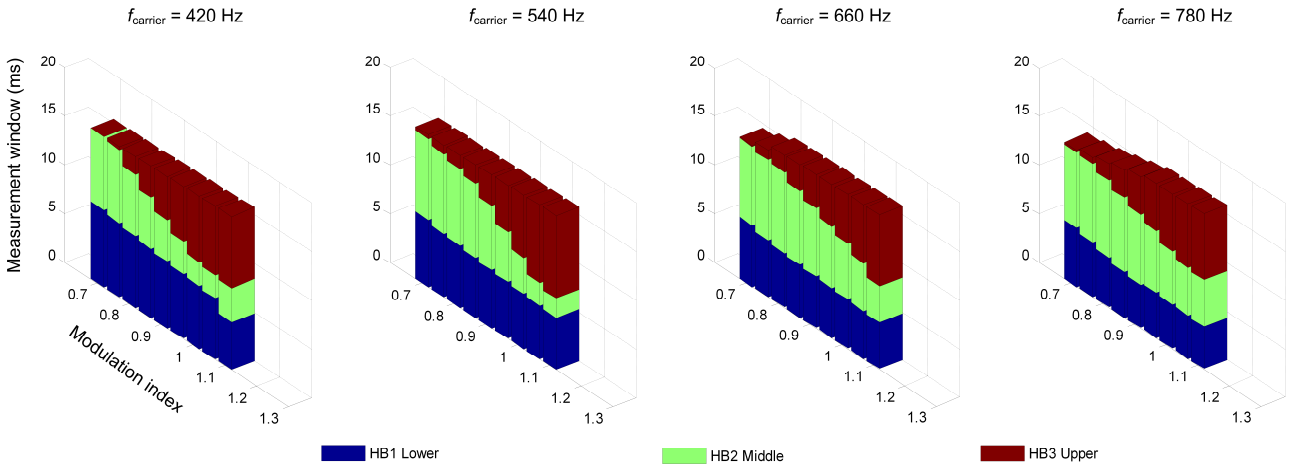
$R_{\theta ch}$: Case-to-heatsink thermal resistance.

$R_{\theta ha}$: Heatsink-to-ambient thermal resistance.

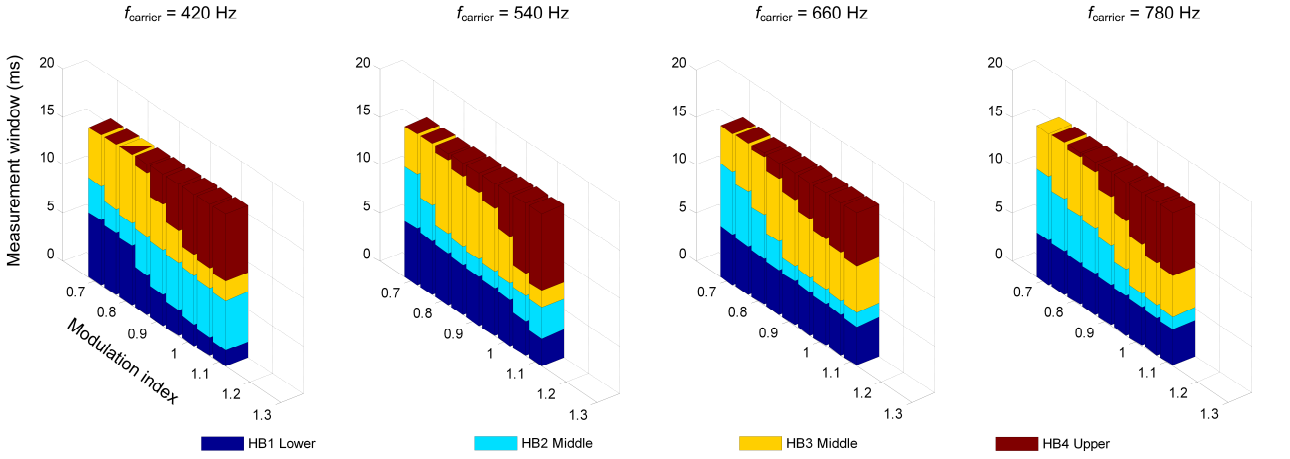
With the approximate junction temperature (T_j), the on-state resistance can be determined according to the datasheet curve. The main parameters of the power MOSFET switch used in this work are presented in Table 1.

TABLE I. IRFS4127 POWER MOSFET RELEVANT PARAMETERS.

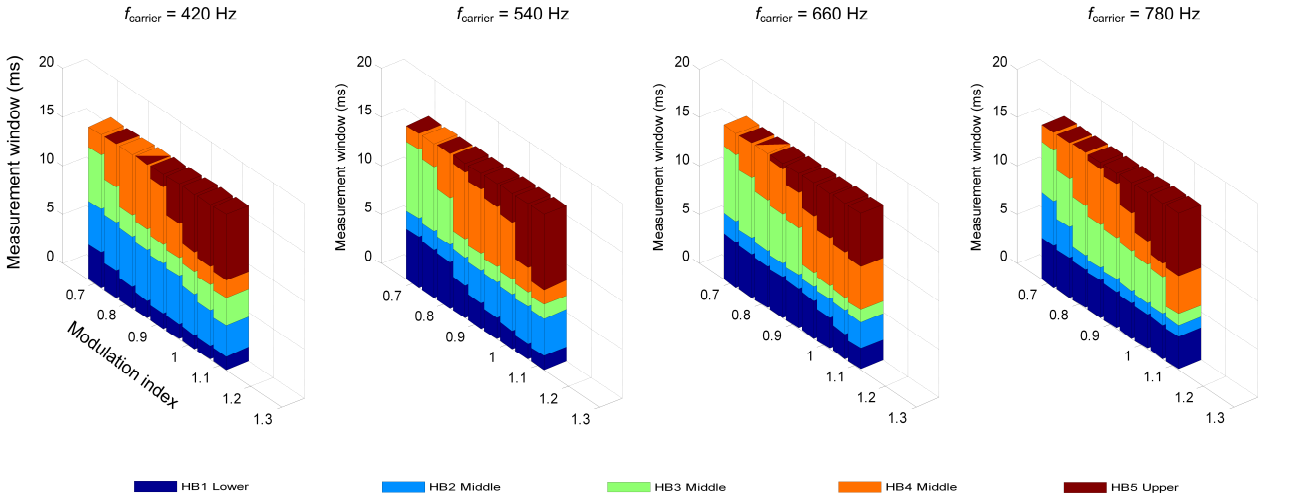
Parameter	***Value***
Break-down voltage (V_{dss})	200 V
Drain current (I_{ds})	72 A
On-state resistance (R_{ds})	18.2 Ω
Junction-to-Ambient thermal resistance ($R_{\theta JA}$)	40 ºC/W
Turn-off delay time ($t_{d(on)}$)	56 ns
Fall time (t_f)	22 ns



(a)



(b)



(c)

Figure 2. Measurement window for a full cycle using level-shifted modulation at different carrier frequencies in an (a) 7 level, (b) 9 level and (c) 11 level multilevel cascade inverter..

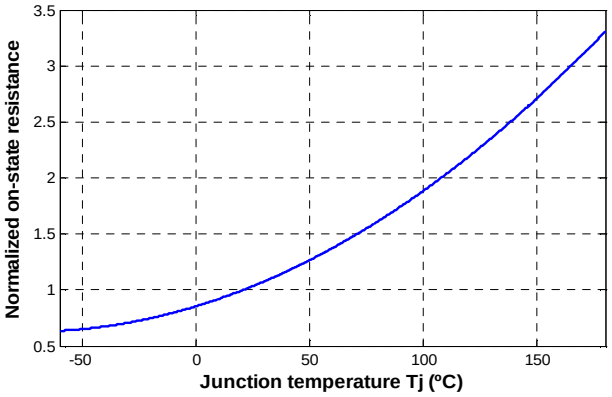


Figure 4. On-state resistance dependence on junction temperature.

The value of resistance shown in Table 1 is for 25°C at the junction. This semiconductor has the resistance dependence as depicted in Fig. 4 that can be used to estimate the on-state resistance. From ambient temperature (25ºC) to 100ºC, the on-state resistance almost doubles.

IV. Conduction Loss Estimation

When operating at low carrier switching frequencies the dominant losses will be due to conduction [9-12]. The average switching frequency of each device will be inversely proportional to the number of levels *m* [3] as defined in (4),

$$f_{sw,dev} = \frac{f_{cr}}{(m-1)} \tag{4}$$

Control of a CHB requires that at any time if the level is not on (in series), a current path must exist. At any time during inverter operation two switches will be on. If duty cycle swapping is used, then each switch will have an average power loss as shown in (5).

$$P_L = \frac{1}{12}\left(6R_{DS(on)}\right)I^2_{D(RMS)} \tag{5}$$

Note that the switch diode voltage drop is not included since during inverter normal operation condition it does not conduct current. At any time two switches must be on to provide the voltage level ($+V_{dc}$ or $-V_{dc}$) or a current path (zero level)

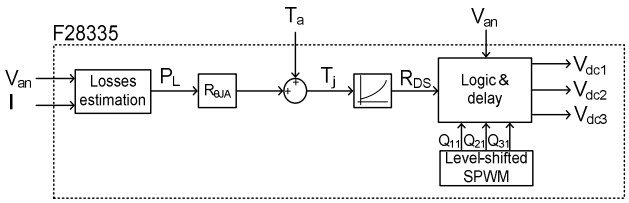


Figure 5. Control algorithm for voltage level estimation.

V. Control Algorithm

The control algorithm measures the output voltage before the LC filter over the first quarter of the output waveform using the gate driver signals as a reference. This is illustrated in Fig. 1(b). The measurement window shown is shorter than the signals that command the gate drivers to avoid influence of voltage transient on the switches. Such transients can be caused by stray inductances from *dv/dt* and/or *di/dt*. Over the measurement window shown in Fig. 1(b) the inverter output voltage is acquired, and the voltage of each individual H-bridge is calculated based on the control algorithm shown in Fig. 5. In order to determine the voltage level V_{dc1} based on the signals sent to Q_{11}, Q_{12}, Q_{21}, Q_{22}, Q_{31} and Q_{32}, the logic shown in (6) is evaluated.

$$V_{an} = V_{dc1} \xrightarrow{if} (Q_{11} XOR Q_{12}) \,\&\, (Q_{21} XNOR Q_{22}) \,\&\, (Q_{31} XNOR Q_{32}) \tag{6}$$

The upper levels can be determined indirectly as shown in (7) and (8).

$$(Q_{11} XOR\, Q_{12}) \,\&\, (Q_{21} XOR\, Q_{22}) \,\&\, (Q_{31} XNOR\, Q_{32}) \Rightarrow (V_{dc1} + V_{dc2}) \tag{7}$$

$$(Q_{11} XOR\, Q_{12}) \,\&\, (Q_{21} XOR\, Q_{22}) \,\&\, (Q_{31} XOR\, Q_{32}) \Rightarrow (V_{dc1} + V_{dc2} + V_{dc3}) \tag{8}$$

where,

& : Logic AND operator.

XOR : Logic exclusive OR operator.

XNOR : Logic inverse of exclusive OR operator.

The voltage and current values are measured to estimate the losses at each individual switch. The thermal resistance of the path can be determined by the physical characteristics and specification of the components used. A temperature sensor provides the ambient temperature so that the junction temperature can be estimated using (3) and (4). Next, the on-state resistance is obtained to correct the difference between

Figure 6. Single-phase 11-level cascade H-bridge multilevel inverter prototype.

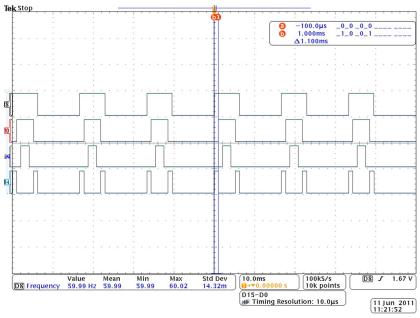


Figure 7. CHB switching signals for first half of fundamental and measurement window for lower level HB1.

the actual inverter output voltage and the switches' voltage drop. This corrected output voltage is the basis for determining the voltage of each individual level.

VI. Experimental

The 11-level cascade multilevel inverter is shown in Fig. 6. The three lower HBs are switched as in a 7-level multilevel while the upper two HBs are bypassed to avoid effect of their series switches. Results using the power MOSFET shown in Table 1 for a seven level inverter are shown in Fig. 7. In Fig. 7 the upper three waveforms are the gate signals for the first half of the fundamental frequency and the bottom waveform indicates the measurement window for calculating the voltage level for the lower HB. In Fig. 8 the output voltage and the conditioned voltage to be sent to the analog input of the DSP is shown. All three full bridges are operating with a 24V power supply. The measured voltages by the DSP were HB1=23.74 V, HB2=23.8 V and HB3=23.85 V averaged over the fundamental switching cycle.

VII. Conclusion

Voltage estimation using multilevel inverter output voltage sensing was shown in this work. This approach can reduce the number of sensors used in the CHB topology. Due to the nonlinearities involved in this approach, the voltage cannot be determined as precisely as if a sensor was at the input, but this method can achieve much cost savings for high level converters.

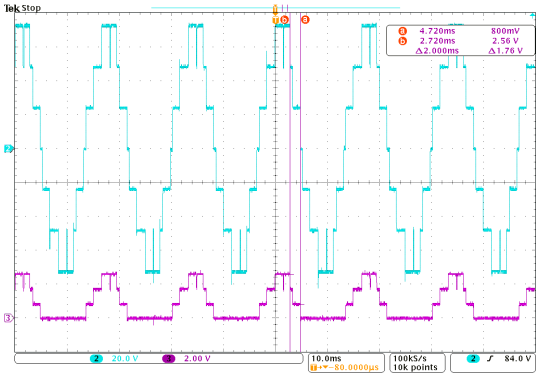


Figure 8. Output voltage waveform (blue) at 540Hz and signal processed by the DSP (purple).

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