Dynamic Performance and Control of a Multilevel Universal Power Conditioner

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***Abstract*¾ This paper presents the development of a control scheme for a multilevel diode-clamped converter connected in a series-parallel fashion to the electrical system such that it can compensate for deviations in utility voltage (sag, surge, and unbalance) and act as a harmonic and/or reactive current source for a load. New carrier-based multilevel pulse width modulation (PWM) techniques are identified to maximize switch utilization of the two back-to-back diode-clamped inverters that constitute the universal power conditioner. An experimental verification for a 6-level power conditioner is given.**

I. INTRODUCTION

Deregulation of the power industry will undoubtedly have a great impact on utilities' competition for customers. Industrial and commercial customers that cannot tolerate variations in their electrical supply likely will request "premium power." It is anticipated that they will want contracts detailing certain tolerances in a utility's voltage magnitude, distortion, and limits on the number of outages per year. Utilities, in turn, will probably put limitations on the power factor, current harmonic distortion, and peak power that the customer can impose on the utility. To meet the objectives detailed in these new premium power agreements, the implementation of advanced power electronic technologies that can simultaneously improve the power quality for both utilities and their customers will be in demand.

By connecting two active inverter-based filters with a common dc link, the combined back-to-back converter can be interfaced with the utility system in both a series and parallel manner. By having these *two* inverters connected to the electrical system, simultaneous control of the current demanded from the utility *and* the voltage delivered to the load can be accomplished. This series-parallel active power filter has been referred to as a universal power conditioner [1-3] when applied to electrical distribution systems, and as a universal power flow controller when applied at the transmission level [4-6].

Multilevel voltage source inverters' unique structure allows them to span high voltages and to reduce individual device switching frequency without the use of transformers. The diode-clamped inverter can synthesize a desired waveform from several levels of dc voltages, and all six phases of a back-to-back converter can share the same common dc link [7]. Consequently, the integration of a multilevel diode-clamped inverter into a universal power conditioner is an enticing prospect.

For a multilevel universal power conditioner (MUPC) that will perform sag compensation, the *majority of its operating mode will likely be in low modulation index operating regions* because sags are quite infrequent and for a minimal duration [8]. Because of this, how to maximize level usage in a diode-clamped inverter for low modulation indices has been previously explored. A novel carrier rotation technique has enabled active device usage to be balanced among a diode-clamped converter's constituent levels during low amplitude modulation index operating conditions [9]. The switching frequency could also be increased in conjunction with this method without exceeding the thermal limits of the active devices. This increased the frequency spectrum and hastened the dynamic response of the inverter, yet did not exceed the allowable switching loss of the active devices.

Because of the different compensation objectives of the series inverter and the parallel inverter, two distinct control techniques are adapted for their use. Simulation and experimental results verify that the algorithms developed will enable the back-to-back diode-clamped converter to quickly respond to deviations from established tolerances in the utility's voltage or the customer's current.

II. SERIES INVERTER CONTROL

Fig. 1 shows a block diagram of the two inverters (series and parallel) and the interconnection with the electrical system. For the analysis in this paper, the turns ratio for each

Prepared by the Oak Ridge National Laboratory, Oak Ridge, Tennessee 37831-8038, managed by Lockheed Martin Energy Research, Corp. for the U.S. Department of Energy under contract DE-AC05-96OR22464.

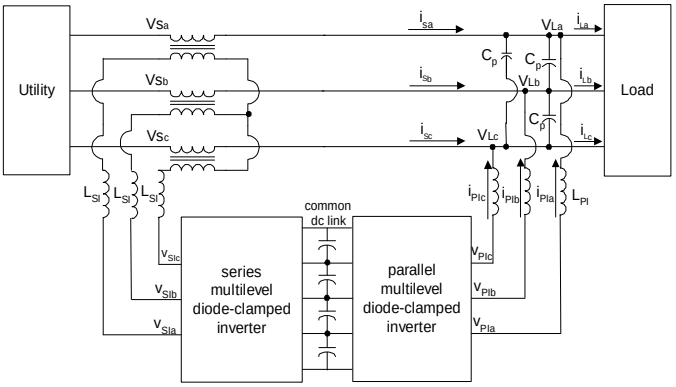


Fig. 1. Series-parallel connection to electrical system of back-to-back multilevel

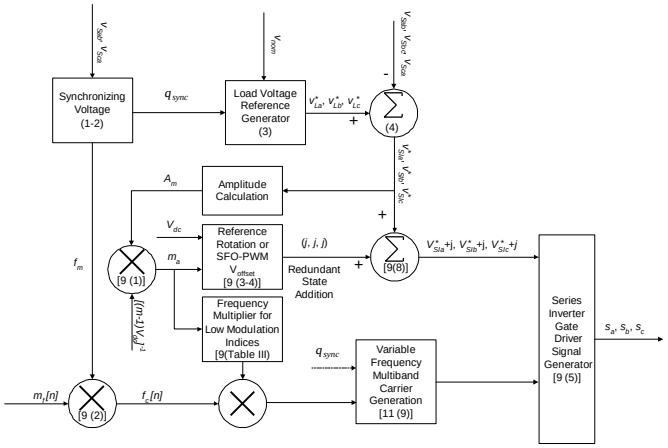


Fig. 2. Serial inverter control block diagram.

of the series transformers was chosen to be 1. The algorithm used to regulate the load voltage is the short time window sampling technique proposed by Joos and Moran [10]. The load reference voltage, which must be synchronized with the source phase voltages, is generated directly from the sample of two line-line source voltages over a short time frame. This technique requires that the source voltage be close to sinusoidal, which is the case for the majority of electrical installations at the interface between a large industrial customer and a utility.

To determine the phase angle for a sinusoidal synchronizing voltage, v_{sync}, one can make use of the following equations:

$$q_{sync} = \arctan\left[\frac{v_{sync_k} \cdot \sin(wT_s)}{v_{sync_k} \cdot \cos(wT_s) - v_{sync_{k-1}}}\right], \qquad (1)$$

$$\text{where } v_{sync} = \frac{v_{Sab} - v_{Sca}}{3}, \qquad (2)$$

and where v_{Sab} and v_{Sca} are source line-line instantaneous samples and T_s is the sampling period. For a system with 1024 samples per cycle, $wT_s = 2\pi/1024$ radians. By sampling these two line-line voltages, a synchronization signal can be obtained even if one or two of the phase voltages collapses to zero, as in the case of a single or double line to ground solid fault.

The three instantaneous load reference voltages can then be given by the following equations:

$$v_{La}^{*} = \frac{V_{nom}}{\sqrt{3}} \cdot \sin(q_{sync}),$$

$$v_{Lb}^{*} = \frac{V_{nom}}{\sqrt{3}} \cdot \sin\left(q_{sync} - \frac{2p}{3}\right), \qquad (3)$$

$$v_{Lc}^{*} = \frac{V_{nom}}{\sqrt{3}} \cdot \sin\left(q_{sync} + \frac{2p}{3}\right),$$

where V_{nom} is the nominal or desired line-line voltage for the load electrical system. The instantaneous reference signals for the series inverter to compensate for deviations in the source voltage are then equal to the difference between the instantaneous load reference voltages given in (3) and the actual source phase voltages derived from the line-line instantaneous samples:

$$v_{SIa}^{*} = v_{La}^{*} - \left(\frac{v_{Sab} - v_{Sca}}{3}\right),$$

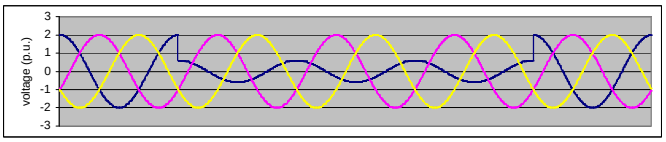
$$v_{SIb}^{*} = v_{Lb}^{*} - \left(\frac{v_{Sbc} - v_{Sab}}{3}\right), \qquad (4)$$

$$v_{SIc}^{*} = v_{Lc}^{*} - \left(\frac{v_{Sca} - v_{Sbc}}{3}\right).$$

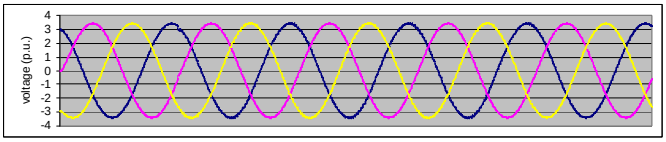
These three series inverter reference signals (4) are the modulation waveforms that are compared against a set of triangular carrier waves to determine the switching of the series inverter active devices.

A control structure is shown in block diagram form in Fig. 2. From the serial inverter reference voltages (4), the amplitude modulation index (m_a) is determined. For low modulation indices (m_a < 0.50 for all three phases), the carrier frequency can be increased, and the reference voltages are rotated among carrier bands as detailed in [9]. For high modulation indices (m_a > 1.00), SFO-PWM is implemented as discussed in [11].

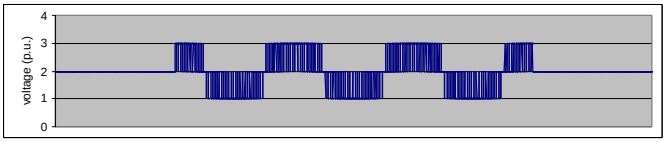
The modified reference signals, which may differ from the original reference signals by a triplen addition (SFO-PWM) or redundant state addition (reference rotation), are then



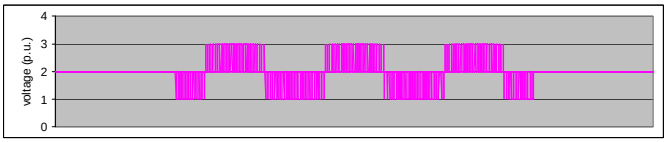
(a) source phase voltages, v_{Sa}, v_{Sb}, v_{Sc}



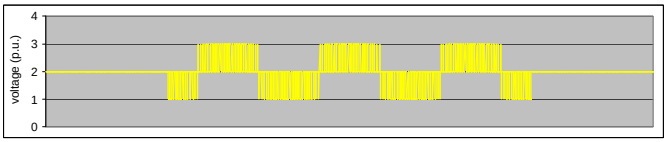
(b) load line-line voltages, v_{Lab}, v_{Lbc}, v_{Lca}



(c) series inverter phase voltage, v_{SIa}

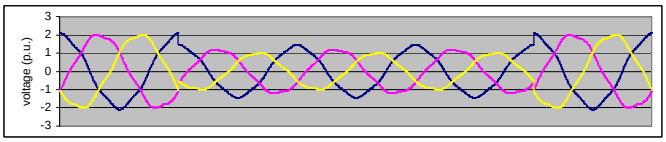


(d) series inverter phase voltage, v_{SIb}

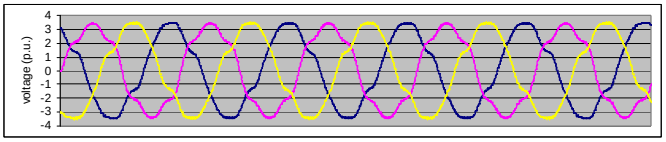


(e) series inverter phase voltage, v_{SIc}

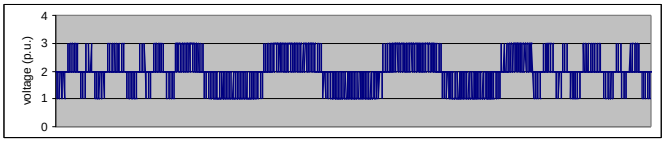
Fig. 3. System voltage waveforms for single-phase sag (v_{Sa}) to $0.3 \cdot V_{nom}$.



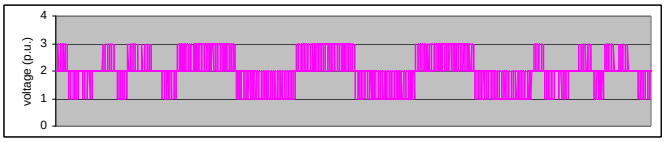
(a) source phase voltages, v_{Sa}, v_{Sb}, v_{Sc}



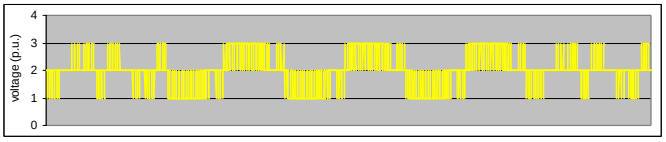
(b) load line-line voltages, v_{Lab}, v_{Lbc}, v_{Lca}



(c) series inverter phase voltage, v_{SIa}



(d) series inverter phase voltage, v_{SIb}



(e) series inverter phase voltage, v_{SIc}

Fig. 4. System voltage waveforms for three-phase unbalanced sag when source voltage has 5% 5th harmonic distortion.

compared against the multiband triangular carrier waveforms to calculate the switching signals that are the control signals for the active devices.

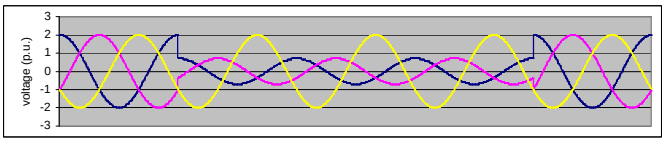
Computer simulations were used to evaluate the performance of the synchronizing and balancing algorithm under different sag or surge conditions. The amplitude magnitude of the load reference voltage V_{nom} was chosen to be equal to a 5-level diode-clamped MUPC's dc link voltage.

In order to reduce the ripple in the load voltage because of injection of voltage by the series inverter, the low pass filter formed by L_{SI} and C_p in Fig. 1 is necessary. For a 60 Hz electrical system, the optimum cutoff frequency of the filter was found to be 60 Hz. Higher cutoff frequencies of the filter resulted in high ripple content of the load voltage, and lower cutoff frequencies resulted in large phase shifts between the source voltage and load voltage and a reduction in the magnitude of the load voltage.

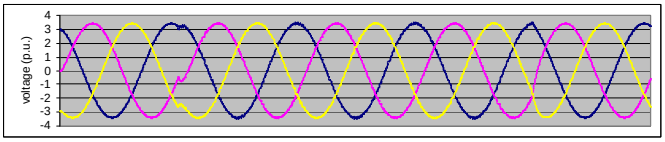
Fig. 3 shows series compensation for a single-phase fault on phase *a* that decreased its voltage to $0.3 \cdot V_{nom}$. The inverter compensates immediately and almost instantaneously for this fault such that the load voltage is well regulated and balanced. Even with this severe fault, the reference waveforms for the three phases of the inverter have an amplitude modulation index less than 0.5 (for a transformer turns ratio of 1), and hence only three of the five available levels in the diode-clamped inverter are needed. A single-phase fault that reduces the source voltage to less than $0.25 \cdot V_{nom}$ is necessary before use of all five levels in one phase of the diode-clamped inverter is required.

Jeon and Cho have shown that for voltage sags less than 50% of nominal the series inverter of a universal power conditioner would have to be rated to transfer more power than the rated load power, which in most applications would not be practical [2]. Likely, a power conditioner would only be designed to compensate for voltage sags that reduced the source voltage to no less than 50% of nominal. This is supported by the fact that industry surveys by EPRI have shown that voltage sags decreased the source voltage to less than 50% of nominal for only 22.5% of the occurrences [12].

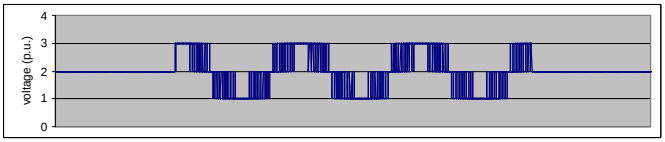
As shown in Fig. 3 (c), (d), and (e), the synchronization and voltage regulation algorithm makes use of all three inverter phases to compensate for a sag in just one of the three source



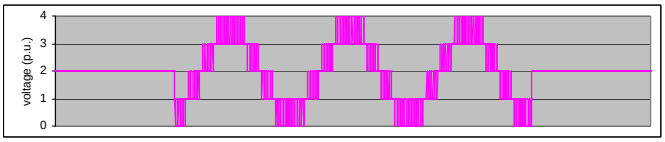
(a) source phase voltages, v_{Sa}, v_{Sb}, v_{Sc}



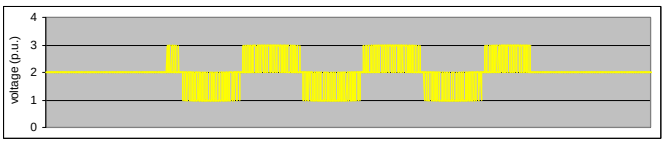
(b) load line-line voltages, v_{Lab}, v_{Lbc}, v_{Lca}



(c) series inverter phase voltage, v_{SIa}

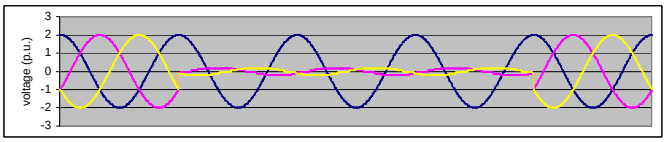


(d) series inverter phase voltage, v_{SIb}

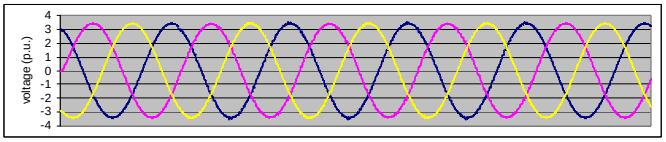


(e) series inverter phase voltage, v_{SIc}

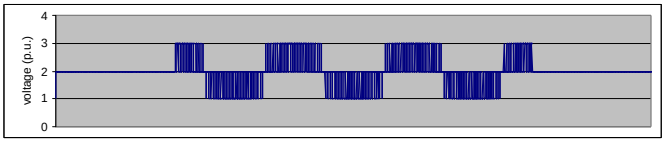
Fig. 5. System voltage waveforms for two-phase sag (v_{Sa},v_{Sb}) to $0.35 \cdot V_{nom}$.



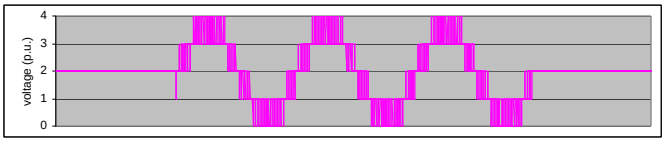
(a) source phase voltages, v_{Sa}, v_{Sb}, v_{Sc}



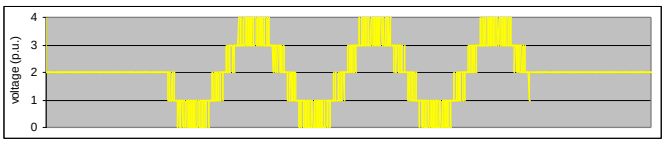
(b) load line-line voltages, v_{Lab}, v_{Lbc}, v_{Lca}



(c) series inverter phase voltage, v_{SIa}



(d) series inverter phase voltage, v_{SIb}



(e) series inverter phase voltage, v_{SIc}

Fig. 6. System voltage waveforms for two-phase sag (v_{Sb},v_{Sc}) to $0.10 \cdot V_{nom}$.

voltage phases. This illustrates that this algorithm is applicable only to three-phase, three-wire systems and not to three-phase, four-wire systems. For the example represented in Fig. 3, rotation of the reference waveform among different carrier band sets is possible as discussed in [9].

One drawback of the synchronizing and balancing algorithm is that it cannot compensate for voltage harmonics because it was derived for sinusoidal source voltages. The algorithm does function for small distortions in the source voltage (generally less than 5% total harmonic distortion), but the load voltage will have about the same harmonic content as the source voltage. Fig. 4 represents three source voltages that have a 5% 5^{th} harmonic sequence and experience a three-phase unbalanced sag for a three-cycle duration. The load voltage is balanced and well regulated, but it has about the same distortion as the source voltage.

For the algorithm defined by (1) and (2), a significant double-line fault that involves phase *a* results in a phase shift between the load voltage and source voltage at the initiation and conclusion of compensation by the series inverter. Fig. 5 represents the case where phases *a* and *b* have a double-line fault to ground that causes the source voltage to dip by 65% to $0.35 \cdot V_{nom}$. The phase shift in the load voltages can be seen at the beginning and end of the fault in Fig. 5(b). For this particular example, the phase shift introduced was 22.5°. The worst case would be when two phases are completely grounded, and the resultant phase shift is 60.8° in the phase voltage at the beginning and ending of voltage compensation.

Because phase *a* is the reference for the other two phases in the synchronization algorithm, simulations have shown that if phase *a* is not involved in the fault, however, no substantial phase shift is introduced in the load voltages. Fig. 6 shows the case where phases *b* and *c* of the source voltage have been reduced to $0.1 \cdot V_{nom}$ by a severe sag. As shown in Fig. 6, the load voltages are well regulated, even for this extreme case. This illustrates that a method which chose the unfaulted phase to be the reference during double-line faults would eliminate the phase shift displacement evident in the Fig. 5 example.

A double-line to ground fault that reduces the source voltage to less than $0.53 \cdot V_{nom}$ is necessary before all five

levels of the diode-clamped inverter are needed. A less severe fault will result in only three levels being used and reference rotation being possible [9].

III. Parallel Inverter Control

The parallel inverter is responsible for supplying the reactive and/or harmonic current demanded by the load. Generalized instantaneous power theory, as outlined by Peng in [13], is used for the control of the parallel inverter. This theory works well for balanced voltages, which should be the case for the load voltages because of the series compensation of the source voltage. For the case where unbalanced voltages are present, the instantaneous power theory where the currents are chosen to follow the voltage waveform is more appropriate [14].

Using instantaneous power theory (generalized *pq*-theory), the instantaneous reference current for the parallel compensation control is given by the following vector equation:

$$\vec{i}_{PI}^{\,*} = \frac{p_c^{\,*}\vec{v}_L}{\vec{v}_L \cdot \vec{v}_L} + \frac{\vec{q}_c^{\,*} \times \vec{v}_L}{\vec{v}_L \cdot \vec{v}_L} \tag{5}$$

where p_c* and $\vec{q}_c^{\,*}$ are extracted from the active and reactive power of the load, p_L and $\vec{q}_L$, which are given as follows:

$$p_L = \vec{v}_L \cdot \vec{i}_L = v_{La} \cdot i_{La} + v_{Lb} \cdot i_{Lb} + v_{Lc} \cdot i_{Lc}\,; \tag{6}$$

$$\vec{q}_L = \vec{v}_L \times \vec{i}_L\,, \tag{7}$$

$$\text{or } q_{La} = v_{Lb} \cdot i_{Lc} - v_{Lc} \cdot i_{Lb}\,,$$

$$q_{Lb} = v_{Lc} \cdot i_{La} - v_{La} \cdot i_{Lc}\,,$$

$$\text{and } q_{Lc} = v_{La} \cdot i_{Lb} - v_{Lb} \cdot i_{La}\,.$$

For the compensation objective of making the source current unity power factor (and sinusoidal for a source voltage with little distortion), $\vec{q}_c^{\,*}$ is set equal to $\vec{q}_L$ and p_c* is set equal to the load ripple active power $\tilde{p}_L$, where

$$\tilde{p}_L = p_L - \bar{p}_L\,, \tag{8}$$

and where $\bar{p}_L$ is the dc component of the load active power.

A low pass filter is necessary for extraction of the dc component from the load active power. A digital low pass filter was implemented as follows:

$$\bar{p}_{L_k} = \left(\frac{T_c}{T_s + T_c}\right) \cdot \bar{p}_{L_{k-1}} + \left(\frac{T_s}{T_s + T_c}\right) \cdot p_{L_k}\,, \tag{9}$$

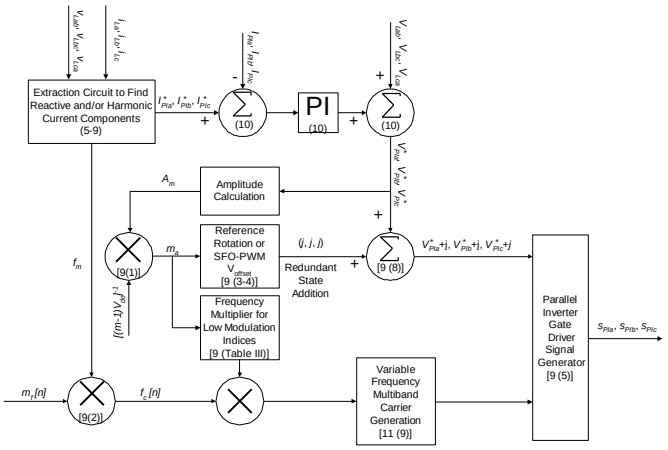


Fig. 7. Parallel inverter control block diagram.

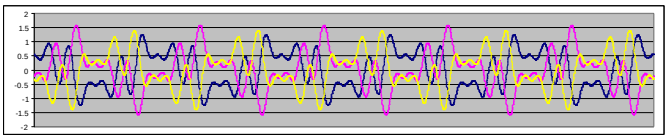
where T_c is the inverse of the filter's cutoff frequency f_c. For a sampling frequency of 1024 times per cycle and a 60 Hz electrical system, the optimum cutoff frequency of the low pass filter was found to be 5 Hz. Simulation results showed that with a lower cutoff frequency of the low pass filter, more of the active power ripple is filtered but at the expense of an extended response time to step changes in the load current. Higher cutoff frequencies resulted in better response times but at the expense of filtering less of the active power ripple. With the 5 Hz cutoff frequency, the response time to a step change was approximately 1.5 cycles and generally better than 90% of the active power ripple was filtered. A control structure is shown in block diagram form in Fig. 7.

The parallel inverter of the MUPC injects currents by impressing a voltage across the parallel inductors, L_{PI}, that is the difference between the load voltage V_L and output voltage V_{PI}. The parallel inverter has to provide a voltage V_{PI}* such that the inverter supplies a current that tracks the current reference computed in (5). This voltage is computed from the following vector equation:

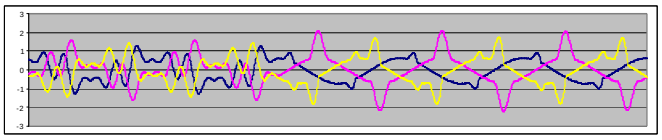
$$\vec{v}_{PI}^{\,*} = \vec{v}_L + \left(\vec{i}_{PI}^{\,*} - \vec{i}_{PI}\right) \cdot \frac{L_{PI}}{wT_s}\,. \tag{10}$$

Again from simulation, an impedance of the parallel inductance of $40 \cdot wT_s$ ohms yielded a current that tracked the reference current well. Smaller values resulted in compensation currents with a high ripple content; and for larger values, the tracking of the reference current was too slow to eliminate the distortion present in the load current.

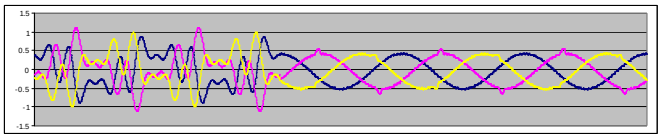
The parallel portion of the back-to-back converter must be able to inject sufficient voltage across the parallel inductance L_{PI} to compensate for harmonic and/or reactive load currents. Fig. 8 illustrates the effect that having a sufficient dc link



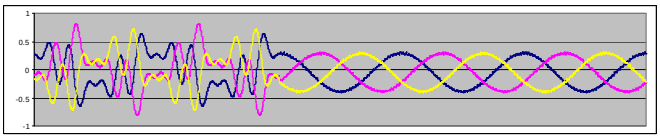
(a) load currents, i_{La}, i_{Lb}, i_{Lc}



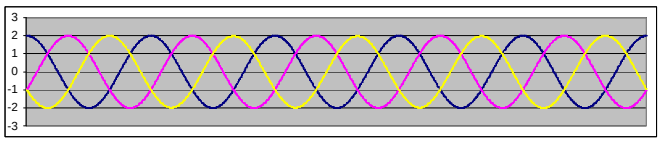
(b) source currents, i_{Sa}, i_{Sb}, i_{Sc} for amplitude(V_{nom}) = 100% dc link voltage



(c) source currents, i_{Sa}, i_{Sb}, i_{Sc} for amplitude(V_{nom}) = 70% dc link voltage

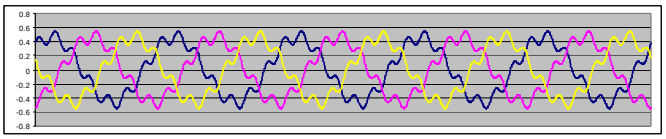


(d) source currents, i_{Sa}, i_{Sb}, i_{Sc} for amplitude(V_{nom}) = 50% dc link voltage

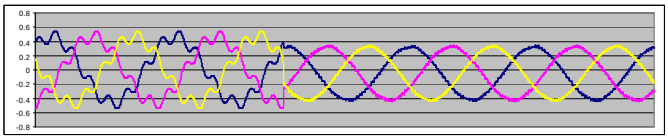


(e) source phase voltages, v_{sa}, v_{sb}, v_{sc}

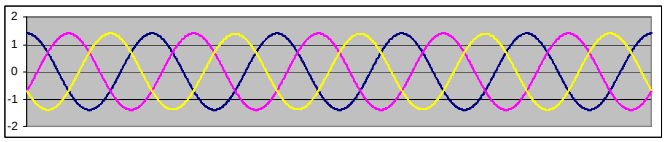
Fig. 8. System waveforms for current compensation for different parallel inverter amplitude modulation indices.



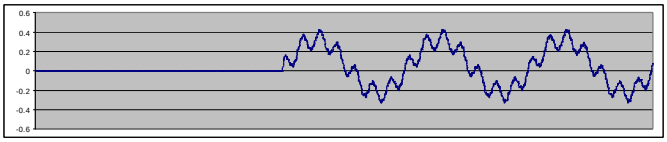
(a) load currents, i_{La}, i_{Lb}, i_{Lc}



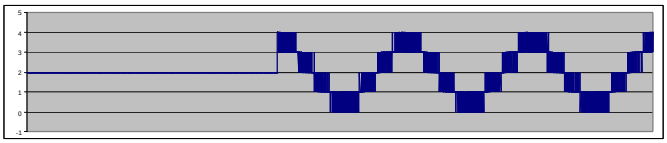
(b) source currents, i_{Sa}, i_{Sb}, i_{Sc}



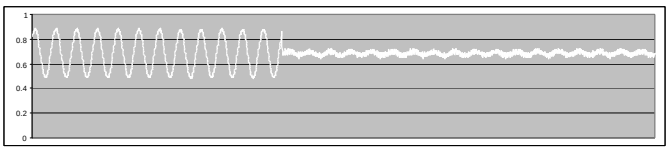
(c) source phase voltages, v_{Sa}, v_{Sb}, v_{Sc}



(d) parallel inverter current for phase a, i_{Pla}



(e) parallel inverter phase voltage, v_{Pla}



(f) load real power, p_L

Fig. 9. System waveforms for current compensation with load current that has 20% 7th harmonic component and a displacement power factor of 0.7.

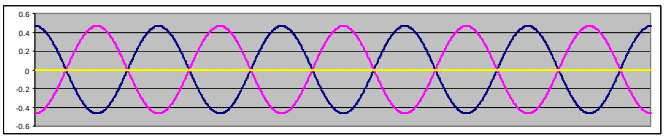
voltage has on the MUPC's ability to force the source current to be a sine wave at unity power factor. If the inverter has too low of a dc link voltage (equal to amplitude of V_{nom}), then it cannot inject enough voltage across the inductance to force the currents to fully compensate for the reactive and harmonic currents as shown in Fig 8(b). Fig 8(c) shows that the amplitude of the desired load voltage V_{nom} should not be more than 70% of the overall dc link voltage for the MUPC to be able to impress enough voltage across the parallel inductance to compensate for reactive currents when the load voltage is at its maximum or minimum amplitude. Without this margin, complete compensation of reactive currents may not be possible.

Fig. 9 shows waveforms for an electrical system with current compensation where the load current has a 20% 7th harmonic component and a 0.7 displacement power factor. The source current immediately becomes sinusoidal and in phase with the source phase voltages once compensation by the MUPC has begun. The parallel inverter supplies a substantial reactive current to compensate for the large reactive power drawn by the load.

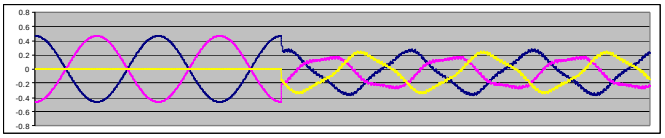
The filter described by (9) does not completely filter the ripple in the load real power for severely unbalanced conditions. Fig. 10 shows what the source voltage, load current, and source current look like for compensation of the load current under unbalanced current conditions (i_{Lb} = -i_{La}, i_{Lc} = 0). An ideal low-pass filter would completely eliminate the ripple in the transmitted real power such that the source currents were distortion-free sinusoids.

IV. Experimental Results

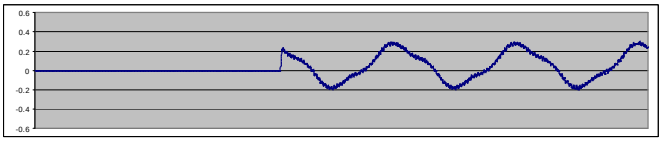
To validate the simulation results, a six-level three-phase back-to-back 10 kW diode-clamped converter [9] was fabricated and experimentally tested. The converter was



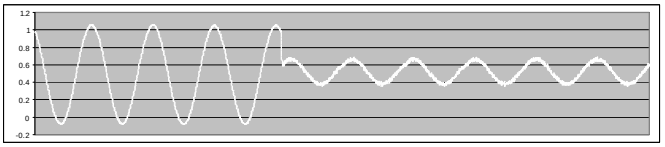
(a) load currents, i_{La}, i_{Lb}, i_{Lc}



(b) source currents, i_{Sa}, i_{Sb}, i_{Sc}



(c) parallel inverter current for phase *a*, i_{Pla}



(d) load real power, p_L

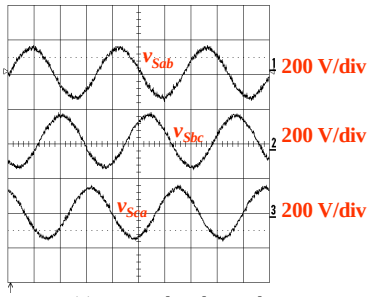
Fig. 10. System waveforms for current compensation under unbalanced current conditions (i_{Lb} = - i_{La}, i_{Lc} = 0) using the filter described by (9).

connected to an electrical system in a series-parallel manner and used as a universal power conditioner. The transformers used for injection of voltage by the series inverter were 0.75 kVA each and were wired such that the transformation ratio was 1 (240 V: 240 V). Each of the filter capacitors, *Cp*, was composed of four 6.8 µF capacitors wired in parallel. The parallel inductance L_{PI} was 18 mH in each phase.

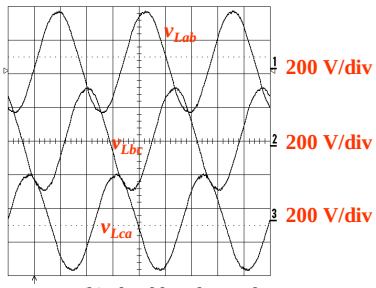
Compensation for a sag in the utility voltage to 45% of V_{nom} is shown for the MUPC in Fig. 11. The three line-line source voltages are shown in Fig. 11(a), and the three line-line load voltages are shown in Fig. 11(b). The MUPC injected a compensating voltage such that the load voltage was regulated to 205 Vrms. Fig. 11(c) shows the line-neutral voltage for phase *a* of the series inverter in addition to the line-line voltages of the source and load voltages.

The wye-connected secondary of the series injection transformers caused some triplen harmonic voltages to appear line-neutral across the inverter output phase voltages and resulted in some distortion of the phase voltage waveforms of the series inverter as shown in Fig. 11(c). However, because these were common-mode voltages, they did not show up in the line-line voltages as shown in Fig. 11(b).

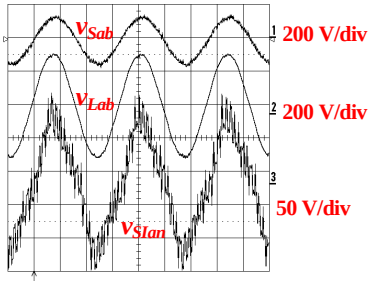
Fig 12 shows voltage and current waveforms for compensation by the MUPC of the reactive and harmonic portion of a load current that was mostly inductive (displacement power factor was 0.2). The parallel inverter



(a) source line-line voltages



(b) load line-line voltages



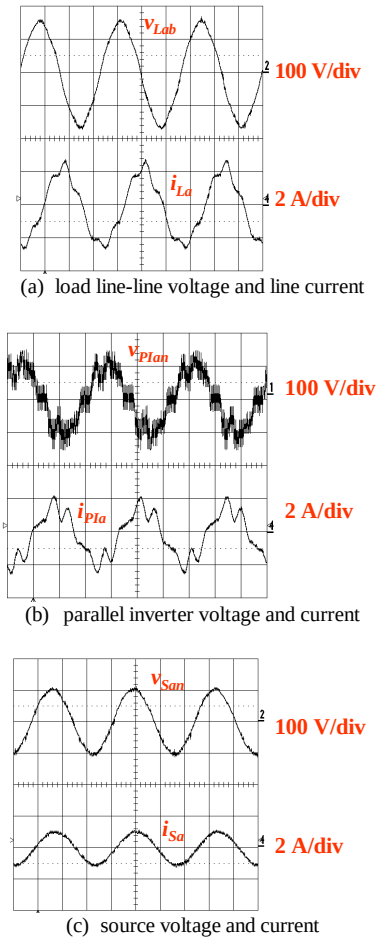
(c) series inverter voltage v_{Slan}, source voltage v_{Sab}, load voltage v_{Lab}

Fig. 11. Experimental voltage waveforms for MUPC compensation of source voltage sag on all three phases.

output the voltage shown in Fig. 12(b) such that the current shown in the same figure was injected into the electrical system. Fig. 12(c) shows the source current was controlled to be nearly sinusoidal (3% THD) and in phase with the source voltage such that the displacement power factor was near unity (p.f. = 0.95).

V. Conclusions

By connecting two diode-clamped inverters to a common dc link, the multilevel converter can be interfaced with an electrical distribution system in both a series and parallel manner. This universal power conditioner is capable of controlling both the current demanded from the utility and the voltage delivered to the customer at the same time. This integration of a multilevel inverter into the universal power conditioner enables the conditioner to be applied to higher voltage systems, and consequently higher power levels, without the use of bulky transformers. Additionally,



(a) load line-line voltage and line current

(b) parallel inverter voltage and current

(c) source voltage and current

Fig. 12. Experimental voltage and current waveforms for MUPC compen-sation of reactive and harmonic load current.

multilevel inverters offer extra degrees of freedom in the form of redundant voltage states, which when judiciously applied allow these inverters to operate proficiently over most of their operating regions.

In this paper, a control scheme was developed for a complete multilevel universal power conditioner system. Because of the different compensation objectives of the series inverter and parallel inverter, two distinct techniques were adapted for use by the two converters.

The short time window sampling technique employed for use with the series inverter enabled regulation of the load voltage under unbalanced fault conditions with the assumption that the source voltage is fairly sinusoidal. This technique enabled synchronism of the series inverter voltage injection with that of the source voltage even for extremely unbalanced source voltages such as when faults occur on the system.

Simulation results showed that only for a severe fault would all of the levels in a MUPC be required for compensation. For the majority of the sags experienced on an electrical system, only part of the voltage levels in a MUPC are used. Under these conditions, the rotation of level usage as described in [9] is an effective means of balancing level usage and in some cases increasing possible switching frequency without exceeding thermal limits of the active devices.

The generalized *pq*-method was used for load current compensation by the parallel inverter. This method minimized the currents drawn from the utility by eliminating all of the reactive power and the ripple in the real power transferred to the load.

Because the parallel inverter of the MUPC injects currents by impressing a voltage across an inductance with respect to the load voltage, in most cases all of the voltage levels in the parallel inverter are used. In addition, the amplitude of the desired load voltage V_{nom} should not be more than 70% of the dc link voltage, so that the MUPC can still impress the proper voltage across the parallel inductance when the load voltage is at its maximum or minimum amplitude.

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