A UNIVERSAL SOI-BASED HIGH TEMPERATURE GATE DRIVER INTEGRATED CIRCUIT FOR SIC POWER SWITCHES WITH ON-CHIP SHORT CIRCUIT PROTECTION

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Abstract- In recent years, increasing demand for hybrid electric vehicles (HEVs) has generated the need for reliable and low-cost high-temperature electronics which can operate at the high temperatures under the hood of these vehicles. A high-voltage and high temperature gate-driver integrated circuit for SiC FET switches with short circuit protection has been designed and implemented in a 0.8-micron silicon-on-insulator (SOI) high-voltage process. The prototype chip has been successfully tested up to 200 ℃ ambient temperature without any heat sink or cooling mechanism. This gate-driver chip can drive SiC power FETs of the DC-DC converters in a HEV, and future chip modifications will allow it to drive the SiC power FETs of the traction drive inverter. The converter modules along with the gate-driver chip will be placed very close to the engine where the temperature can reach up to 175 ℃. Successful operation of the chip at this temperature with or without minimal heat sink and without liquid cooling will help achieve greater power-to-volume as well as power-to-weight ratios for the power electronics module.

Keyword: SiC, BCD-on-SOI, high-voltage, gate-driver, short-circuit protection, high-temperature.

1. Introduction

World oil production has been speculated to reach its peak at 2015 or even earlier [1]. Failure to initiate mitigation of oil consumption will result in a significant impact on world economy. One effective method is to replace a large amount of fuel consuming vehicles because 99% of fuel used in transportation is provided by oil. Hybrid electric vehicles (HEVs) and plug-in HEVs (PHEVs), on the other hand, are potential substitutes due to their better fuel efficiency and high output power compared to conventional internal combustion engine vehicles (ICEVs).

A typical arrangement of a hybrid fuel cell vehicle is shown in Figure 1 [2]. Developments in hybrid automobile industry have generated an enormous need for different power electronic modules (such as DC/DC converters and DC/AC inverters) capable of working at elevated temperatures. Integration of power converters and smart power devices into the drive train requires semiconductor devices capable of working at 175˚C to 200˚C [3]. As of year 1977, the average cost of electronics per automobile has increased from $110 to $1510 at the end of 2003, despite the price reduction in semiconductor manufacturing [4, 5]. It is predicted that by 2013 each automotive will contain on average $2285 worth of electronics within its frame [5].

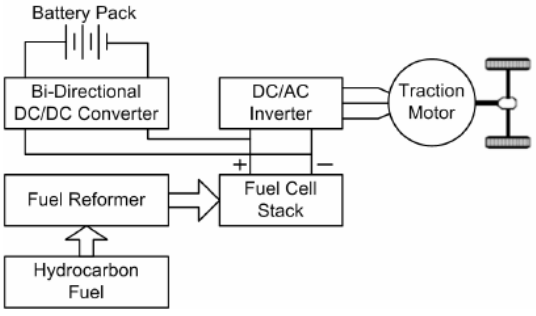

Fig. 1. Typical topological arrangement of a hybrid fuel cell vehicle drive train [2].

A summary of high-temperature automotive electronics requirements published by DaimlerChrysler, Eaton Corporation, and Auburn University is reproduced in Table I [6]. For most part of the cavity under the hood, the temperature can be more than 150˚C. Typically, the junction temperatures for integrated circuits are 10˚C to 15˚C higher than the ambient temperature. For power devices this can even reach 25˚C above the ambient temperature. Hence electronics used in automotives, especially those placed close to the engine, need to be able to work at temperatures above 175˚C.

TABLE I AUTOMOTIVE MAXIMUM TEMPERATURE RANGES [6]

On-Engine	150-200 ℃
In-Transmission	150-200 ℃
On Wheel-ABS sensors	150-250 ℃
Cylinder pressure	200-300 ℃
Exhaust sensing	Up to 850 ℃, ambient 300 ℃

In all power electronic circuits, a gate driver is an essential component for controlling "on" and "off" operations of the power switches. In HEVs or FCVs, power converter modules and their drivers and protection circuits are required to be placed near the engine to reduce the cabling length. Hence, the ambient temperature of the gate-driver IC will be more than 150 ℃. This work presents a silicon-on-insulator (SOI) based high-temperature, high-voltage integrated gate driver circuit targeted for automotive applications. The proposed gate driver circuit can work with either normally "ON" or normally "OFF" power switches with large drive current at elevated temperature. An on-chip short circuit protection circuitry is also employed in this work to ensure immediate detection and removal of any short circuit fault, which usually results from either wiring misconnections at the terminal or motor winding insulation failure [7]. Prototype driver circuits with short circuit protection have been successfully tested up to 200 ˚C ambient temperature while driving SiC switches (MOSFET and JFET) without any heat sink and thermal management. Simulation and test results for both circuits are presented in this paper.

2. High Temperature Semiconductor Devices and Process

Most commercially available Si-based power switches rate their maximum operating temperature of 125˚C for military and automotive applications. At higher temperature, the intrinsic carrier concentration of silicon becomes comparable to the intentional device doping, which creates undesired large leakage current, and leaves the conductivity of the semiconductor device out of control. Wide bandgap semiconductors (WBG), however, have much smaller intrinsic carrier concentration than their silicon counterparts. This property theoretically allows device operation at a junction temperature of more than 600˚C [8].

Among all the wide bandgap semiconductors, silicon carbide (SiC) based devices have been attracting continuous research in recent years [9]. The high breakdown field and high thermal conductivity of the SiC device provides extremely high power density and efficiency compared to silicon based devices. Unfortunately, SiC based power switches are not yet readily available in the commercial market. Only SiC Schottky diodes are commercially sold in the market.

On the other hand, for high temperature integrated circuits, conventional bulk CMOS processes will not only exhibit high leakage current due to the parasitic PN junction, but also suffer from device transconductance degradation at elevated temperature, which leads to the failure of overall circuit performance. The silicon-on-insulator (SOI) fabrication process offers a better solution because the buried insulation layer in its cross-sectional structure greatly inhibits the leakage path associated with the drain and the source PN junction diodes, which enables higher temperature operation. Moreover, the latch-up immunity and the reduced variation of the threshold voltage of the SOI process will further increase the reliability of the circuit operation at high temperatures. Typically, SOI-based circuits are capable of operating successfully in the 200 ℃-300 ℃ temperature range which is well above the range of conventional bulk silicon-based devices.

3. High-temperature, High-voltage Gate Driver Circuit with High Current Drive

In power converters, the flow of power from the source to the load is controlled by sequential turn ON and turn OFF operations of the power switches. The ability of their drivers to efficiently control the ON/OFF operations will have a great impact on the overall performance of the power electronic system. Several integrated gate driver circuit have been reported so far in the literature [10-14]. However, none of them are targeted for high temperature application. Companies like CISSOID have developed some commercially available gate driver circuits for -55˚C to +225˚C junction temperature operation [15], but the peak output drive current is much less than 1 A at elevated temperature. This paper presents the design of a high-temperature (≥ 200°C), high-voltage (10 V to 30 V) gate driver IC with high drive current (5 A) for wide bandgap power switches.

An earlier prototype of the proposed SOI-based high-temperature, high-voltage gate driver circuit was presented in [16, 17]. In the design presented in this paper, higher current drive capability and improved robustness of functional blocks across a wide temperature range have been achieved. Several protective features such as temperature sensor based thermal protection, under voltage lock out (UVLO), and short circuit protection have also been incorporated with the core gate driver circuit.

Block diagram level circuit topology of the proposed high-temperature SOI gate driver is illustrated in Figure 2. The circuit consists of seven building blocks, which are half-bridge high-voltage output stage (transistor pair M_H and M_L), low-side and high-side buffers, on-chip bootstrap capacitor based charge pump, constant current bias low-side to high-side level shifters, temperature independent dead-time controller, edge detection circuit, and input stage.

The input stage includes one Schmitt trigger to filter out any noise from the incoming logic signal and one logic gate to generate ENABLE signal from feedbacks received from three different protection circuits which are temperature sensor, under voltage lockout (UVLO), and short circuit protection. The high drive current is realized by the half bridge output stage, which consists of two high voltage and large aspect ratio n-type LDMOS transistors. The high-side and low-side buffers are utilized to drive the gates of the transistor pair in the output stage. The bootstrap capacitor (C_B) based charge pump generates a voltage above the highest output voltage for all the high-side devices and circuits. The level shifter circuit provides conversion of the incoming logic signal from the low-side voltage level (V_{DD} ~ V_{SS}) to the high-side voltage level (V_{OP_PLUS} ~ V_{DDH}). The temperature independent level shifter circuits have been designed to generate active low SET and RESET signals with temperature independent pulse magnitude for the SR latch. The dead-time controller circuit generates two non-overlapping copies of the input signal with temperature independent dead-time injected between them. The purpose of the edge detection circuit is to generate the narrow pulses (S and R) at the rising and the falling edges of the control signal generated by the dead-time controller circuit for control of the M_H transistor. The bootstrap capacitor based charge pump and the temperature independent dead-time controller circuit are discussed in section IV and V in detail, respectively.

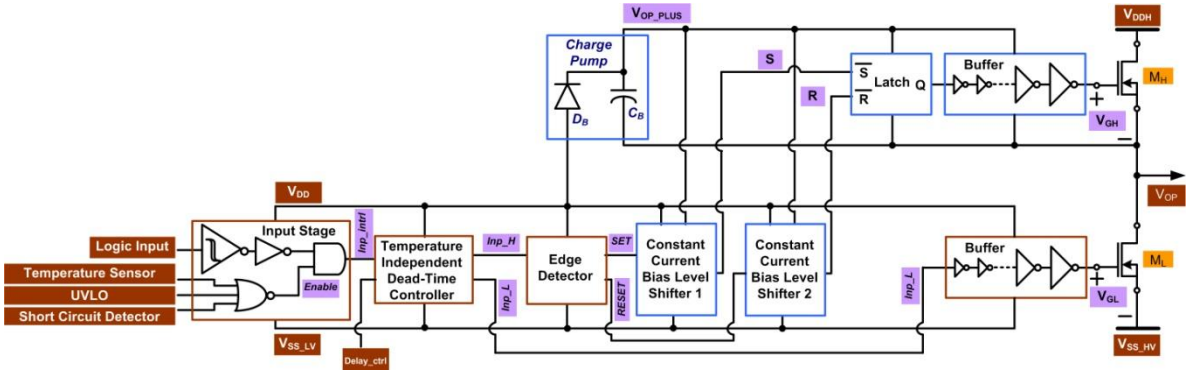

Fig. 2. Schematic of the high-temperature, high-voltage gate driver circuit with high output current.

4. Bootstrap Capacitor-based Charge Pump Circuit

The bootstrap circuit, consisting of a diode (D_B) and a bootstrap capacitor (C_B), supplies a voltage level higher than the most positive power supply available to the chip. Figure 3 depicts the circuit operation of the charge pump. When the output is low (M_L is ON and M_H is OFF) such that V_{OP} is tied to V_{SS}, the bootstrap capacitor is charged to V_B voltage which is given by,

$$V_B = V_{DD} - V_{DB} - V_{ML\_ON} \quad (1)$$

where V_{DB} is the forward voltage drop across D_B, V_{ML_ON} is the ON voltage of the low side NMOS transistor output stage, and V_{DD} is the voltage source charging the charge pump circuit. In the next phase (Figure 3(b)) when M_L is OFF and M_H is turned ON, the output V_{OP} starts to increase making the diode D_B reversed biased and the voltage across the capacitor starts working as a floating battery with V_{OP} working as the floating reference.

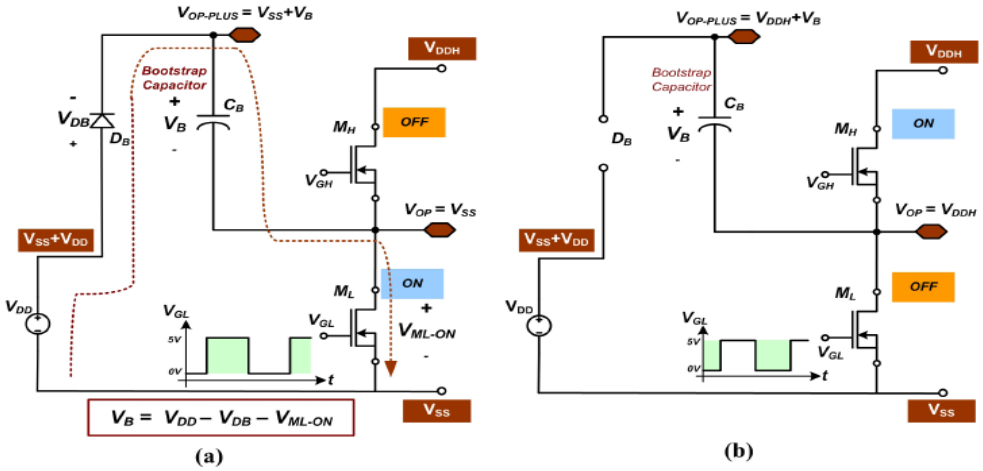

Fig. 3: Bootstrap capacitor based charge pump operation (a) charging the capacitor and (b) voltage across capacitor working as floating battery.

This voltage V_B sets the working voltage rail for the high-side buffer, SR latch, and level shifter. The charge stored on C_B will provide sufficient current to those circuits in order to generate the required gate signal (V_{GH}) for the high side output stage transistor. To make this bootstrap capacitor on-chip, the current consumption of the high-side circuit blocks were carefully designed to consume minimum possible current from the floating supply.

5. Temperature Independent Dead-Time Controller

To reduce the power consumption of the chip and to ensure the reliability of the circuit, it is very important to maintain non-overlapping ON and OFF signals of the high-voltage transistors in the output stage. Both transistors turning on at the same time will inevitably create a short circuit between the rail voltages (V_{DDH} and V_{SS}). The resulting large current flowing through the half bridge will increase the die temperature much higher than the ambient temperature thus degrading the lifetime of the gate driver. The dead-time controller block is designed to create two non-overlapping copies of the input signal.

Figure 4 shows the schematic of the dead-time controller circuit. The main building block of this circuit is the adjustable delay controller circuit that can inject a temperature independent phase lag to an incoming logic signal. A temperature-independent current bias circuit has been designed to provide constant current biasing to the adjustable delay controller circuit. Figure 5 shows the schematic of the temperature-independent current bias network developed using the zero-temperature coefficient (ZTC) [18] bias conditions of the NMOS and the PMOS transistors. Sizes of M_{P1} and M_{N1} transistors are determined such that their saturation drain-source current at ZTC bias voltage, I_{DS_ZTC} become equal i.e. $I_{bias1} = I_{bias2}$. Since the current through both the PMOS and NMOS current mirror branches are equal, the drain voltage of M_{N1} transistor tracks the V_{GS_ZTC} voltage of M_{N2} NMOS. Similarly,

the drain voltage of M_{P2} tracks V_{SG_ZTC} of M_{P1}. The resistance value required to keep these transistors operating in saturation with the ZTC bias voltages is calculated by:

$$R_{eq} = R_{11} + R_{12} = R_{21} + R_{22} = \frac{(V_{DD} - V_{SS}) - V_{SG\_ZTC} - V_{GS\_ZTC}}{I_{DS\_ZTC}} \quad (2)$$

Since both positive and negative temperature coefficient resistors are available in the SOI process, temperature independent resistor can be implemented, thus constant bias voltages V_P for the PMOS and V_N for the NMOS transistors are generated.

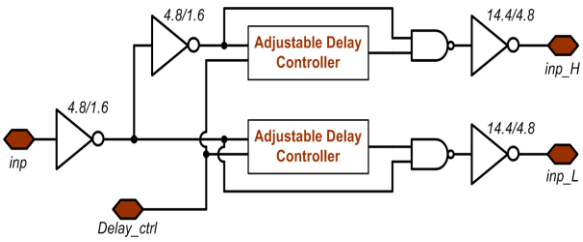

Fig. 4. Temperature independent dead-time controller circuit.

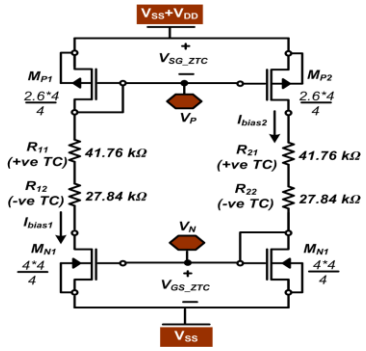

Fig. 5. Schematic of the temperature independent current bias network.

Figure 6 shows the schematic of the adjustable delay controller circuit with the temperature independent bias network. Constant bias voltage V_P is connected to the gates of all the PMOS transistors, which source constant pull-up currents to the inverters, and thus capacitors get charged by a constant current across the entire temperature range. Similarly, the constant bias voltage V_N is provided to all the NMOS transistors, which sink the constant pull down current from the inverters. This ensures the same rate of discharge of the capacitors over temperatures. Since the capacitors get charged and discharged by constant currents for the entire temperature range, the phase shift injected by this circuit remains virtually constant over temperature.

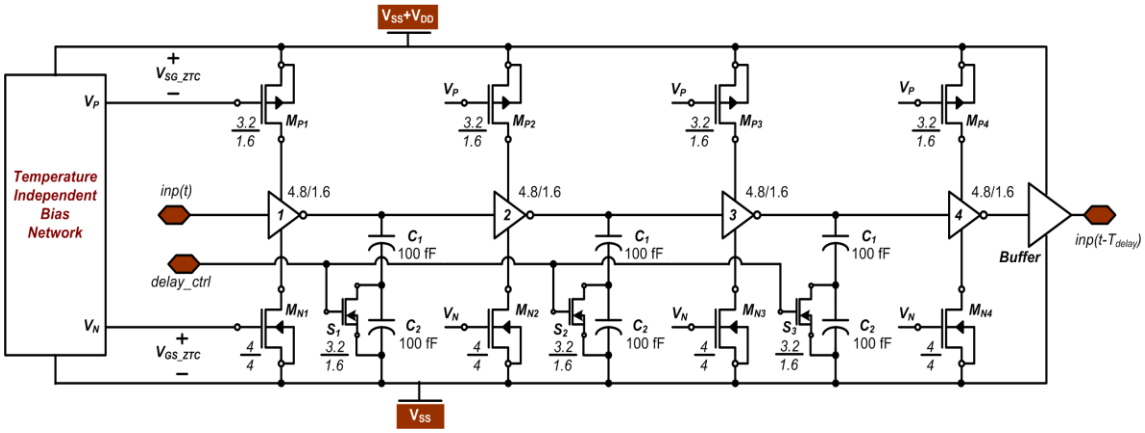

Fig. 6. Schematic of the temperature independent adjustable delay controller circuit.

6. On-Chip Short Circuit Protection Circuit

The maximum operating current in SiC power switches is restrained by its material quality deficiency. Overrated current density will place extreme electrical stress on the devices. Therefore, normally SiC power switches are only

operated at tens of amperes. A short circuit protection scheme is necessary to prevent the operating device from failure by exceeding its maximum current ratings. This work adopts the resistor sensing method to implement high temperature short circuit protection to take advantage of its flexibility with different power supply schemes for either SiC MOSFET or JFET power devices.

The block diagram shown in Figure 7 consists of a voltage reference, a rail-to-rail comparator, an output buffer, and an off-chip resistor. The off-chip resistor is connected in series with the source of the power switch and converts the fault current into voltage. It cannot be integrated on-chip since its value is selected based on the fault current level of one specific power switch and will withstand operating current of several amperes. A rail-to-rail comparator is employed to compare the short circuit sensing voltage input to the voltage reference which is generated by the voltage reference block. It is capable of discriminating mV-level signals, and designed with hysteresis for rejecting small nuisance input signals. The output buffer is powered by a 5 V digital supply, and used to output digital fault signals.

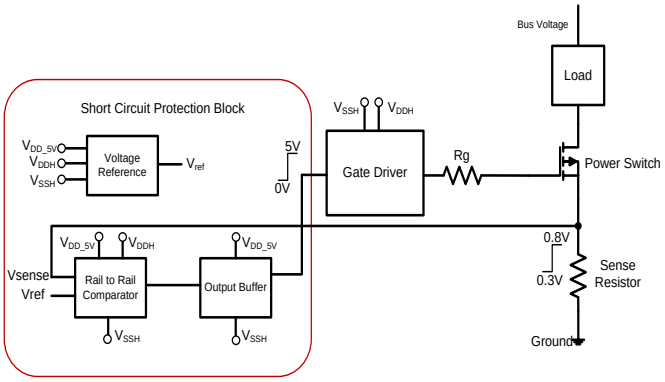

Fig. 7. Block diagram of the short circuit protection circuit.

The circuit monitors the current through the power switch via the voltage drop across the sense resistor to determine if it exceeds a certain fault level (i.e. 400 mV), and if so, the comparator will quickly detect a fault (i.e. in less than 10 ns) and then send a 5-V digital signal to the output buffer. The buffer is capable of distinguishing the fault signal from any nuisance current spike. Typically, for a current surge less than several microseconds, it will be filtered by the R-C delay in the buffer. If high current persists, the short circuit fault is identified by the output buffer; the fault signal is triggered and sent to the core gate driver circuit. This allows the gate driver to turn off the power switch completely in order to protect it from any further damage.

7. Measurement Results

The gate driver chip has been tested up to 200˚C without any heat sink and cooling. The test setup has been configured to drive a R-C load, a SiC MOSFET and a SiC JFET module respectively. Figure 8 shows the chip tested with on-chip current limiting resistor R_G of 4.3 Ω connected in series with an external 10 nF capacitive load at 200˚C. The 30 V peak-to-peak (-15 V to +15 V), 20 kHz gate pulse signal is generated by the chip. At 200˚C, the peak sourcing and the sinking currents were 2.5 A and 2.2 A, respectively. Figure 9 shows the change in the source and the sink current peaks with temperature variation for all three on-chip R_G values.

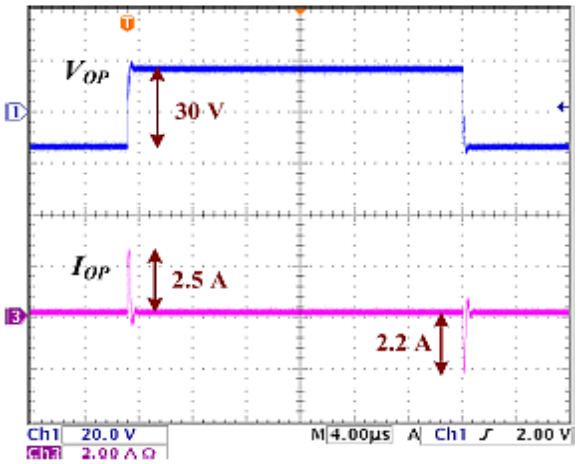

Fig. 8. R-C load test results at 200˚C with R_G = 4.3Ω and C_{Load} = 10 nF.

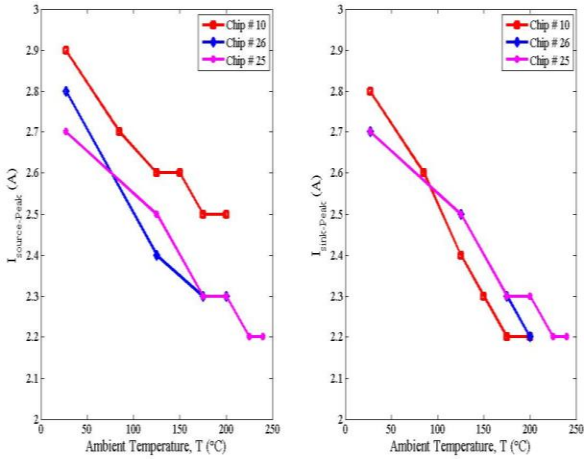

Fig. 9 R-C load measured peak drive current (sourcing and sinking) with three different on-chip resistances (R_G).

The measurements for gate driver circuit driving a SiC MOSFET and a SiC JFET module have also been conducted. Figure 10 shows the gate driver circuit provides 20 V peak-to-peak (+15 V to -5 V) drive signal to the gate terminal of the SiC MOSFET through the 3.4 Ω on-chip current limiting resistor at 200˚C. Rail voltage was set at 560 V, and a 7 A peak load current passed through the MOSFET.

Figure 11 depicts the gate driver circuit biased to generate an 8 V peak-to-peak (-5 V to 3 V) 1 kHz gate signal to control the JFET module which was connected to a 560 V rail voltage through an 80 Ω load resistor at 200˚C ambient temperature.

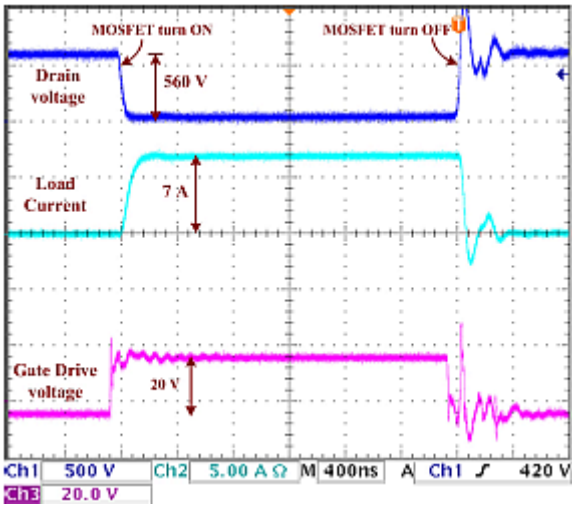

Fig. 10. Prototype circuit's test results at 200˚C when driving a 1200 V, 10 A SiC MOSFET.

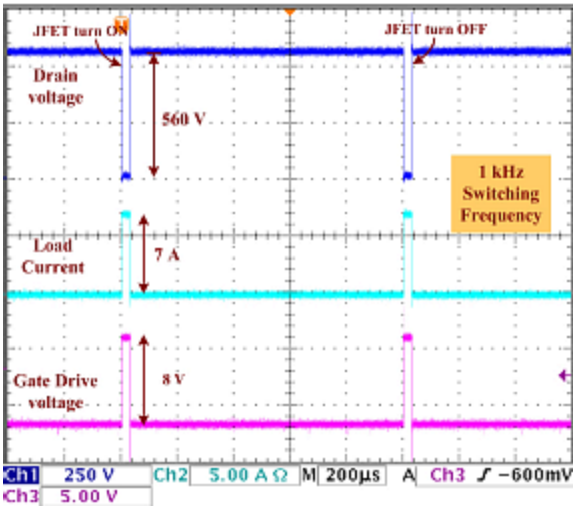

Fig. 11. SiC normally ON JFET module (1200 V, 50 A) test results at 200 ˚C and 1 kHz switching frequency.

The short circuit protection (SCP) circuit was also tested with a gate driver core circuit with gate resistor of 4.3 Ω and load capacitor of 10 nF. Figure 12 provides the transient response at 200˚C with the power supply voltage range of 30 V. The gate driver has been successfully turned "OFF" 8 µs after the fault current occurs. Other power supply schemes (V_{SSH} = −15 V, V_{DDH} = 5 V and V_{SSH} = −3 V, V_{DDH} = 7 V) have also been successfully tested to verify the protection function for either normally-ON and normally-OFF power devices.

Fig. 12. SCP tested with gate driver circuit and 10 nF load capacitor (200˚C).

8. Layout and chip implementation

This proposed high-temperature gate driver circuit has been designed and implemented in a 0.8-µm bipolar-CMOS-DMOS (BCD) on SOI process. The gate driver circuit and the on-chip short circuit protection have approximate areas of 10 mm^2 (4,050 µm × 2,600 µm) and 0.52 mm^2 (845 µm × 612 µm), respectively, including the bonding pads and the ESD protection circuits. Figsures 13 and 14 show the layout of the core gate driver circuit and the on-chip short circuit protection circuit, respectively. Figure 15 presents the photograph of the packaged chip in comparison with a dime. To improve the circuit reliability at high temperature, each individual circuit sub block is surrounded by trenches. The chip was packaged in a Kyocera 145-pin PGA ceramic package to facilitate testing numerous on-chip circuit blocks.

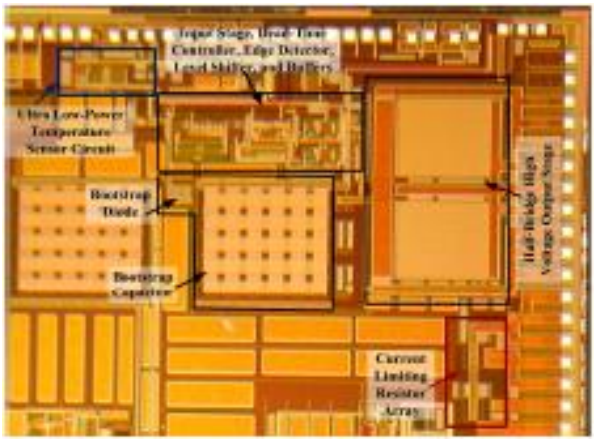

Fig.14. Microphotograph of the high-temperature gate driver circuit.

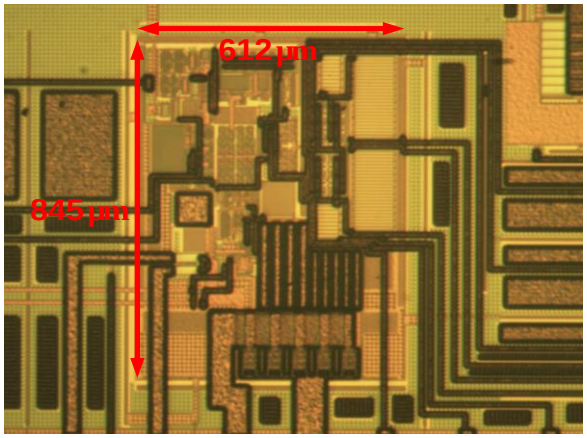

Fig. 15. Micrograph of the short circuit protection.

9. Conclusion

A universal SOI-based high temperature high voltage gate driver circuit with high drive current was proposed and fabricated. A short circuit protection circuit was also included on-chip to safeguard the power switch. The measured gate driver can supply 30V peak to peak output signal with 3A current drive at 200˚C, and is capable of driving several power switches in parallel. The next generation of the gate driver system with increased output current drive has also been designed. Protection circuits such as the gate current monitoring, de-saturation protection, and input isolation circuit have been realized.

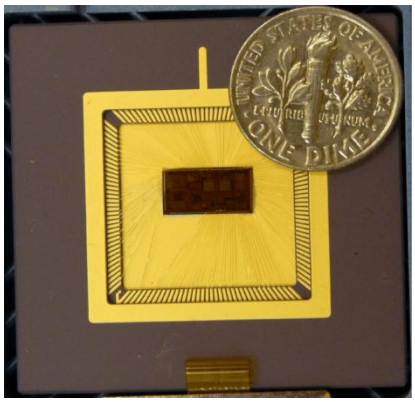

Fig.16. Packaged high-temperature gate driver IC.

10. Acknowledgment

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