Hybrid Cascaded Multilevel Inverter with PWM Control Method

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***Abstract*—A hybrid cascaded multilevel inverter with PWM method is presented in this paper. It consists of a standard 3-leg inverter (one leg for each phase) and H-bridge in series with each inverter leg. It can use only a single DC power source to supply a standard 3-leg inverter along with three full H-bridges supplied by capacitors. Multilevel carrier-based PWM method is used to produce a five-level phase voltage. The inverter can be used in hybrid electric vehicles (HEV) and electric vehicles (EV). A simulation model based on PSIM and MATLAB/SIMULINK is developed. An experimental 5 kW prototype inverter is built and tested. The results experimentally validate the proposed PWM hybrid cascaded multilevel inverter.**

I. Introduction

The multilevel inverter has gained much attention in recent years due to its advantages in high power with low harmonics applications. The general function of the multilevel inverter is to synthesize a desired high voltage from several levels of dc voltages that can be batteries, fuel cells, etc.

In this paper, the proposed hybrid cascaded multilevel inverter includes a standard 3-leg inverter (one leg for each phase) and H-bridge in series with each inverter leg. It can use only a single DC power source to supply a standard 3-leg inverter along with three full H-bridges supplied by capacitors. Traditionally, each H-bridge requires a DC power source [1-5]. Multilevel carrier-based PWM method is used to produce a five level phase voltage.

The inverter can be used in hybrid electric vehicles (HEV) and electric vehicles (EV). An HEV combines a conventional internal combustion engine, a battery pack, and an electric motor. An EV includes rechargeable batteries and an electric motor. The power inverter that drives the electric motor is a key device of a HEV and EV.

To develop the model of a hybrid multilevel inverter, a simulation is done based on PSIM and MATLAB/SIMULINK platforms. Their integration makes the design and analysis of a hybrid multilevel inverter more complete and detailed [6]. A 5 kW prototype has experimentally validated the proposed PWM hybrid cascaded multilevel inverter.

II. Operation Principle of the Hybrid Multilevel Inverter

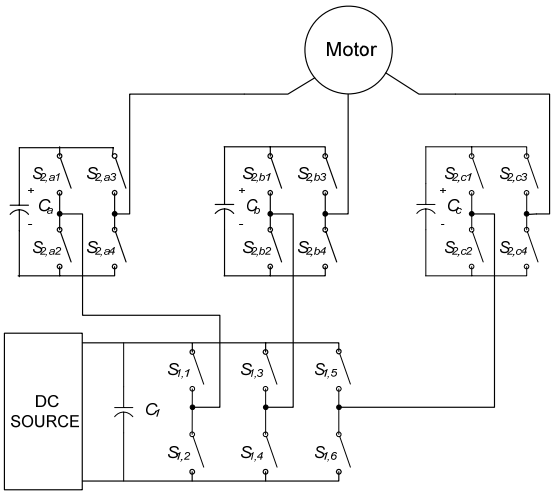

Fig. 1. Topology of the hybrid cascaded multilevel inverter.

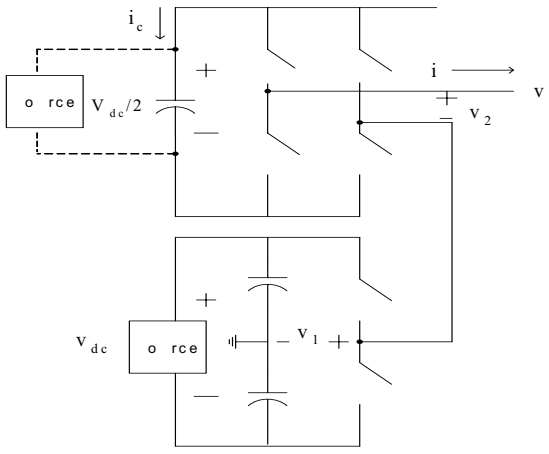

Fig. 2. Simplified single-phase topology of the hybrid cascaded multilevel inverter.

The topology of the proposed hybrid multilevel inverter is shown in Fig. 1. Fig. 2 shows a simplified single-phase topology. The bottom is one leg of a

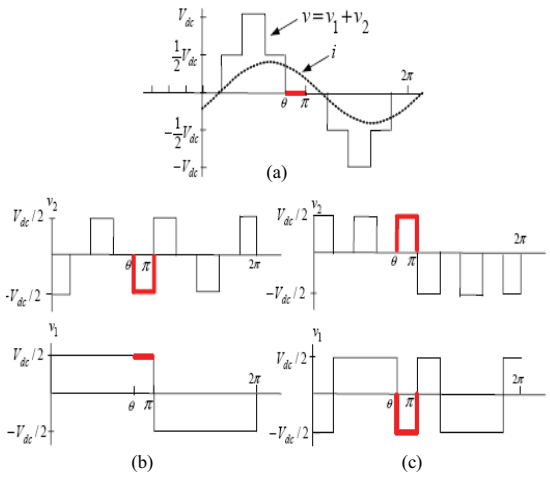

Fig. 3. Capacitor voltage regulation process.

standard 3-leg inverter with a DC power source. The top is an H-bridge in series with each standard inverter leg. The H-bridge can use a separate DC power source or a capacitor as the dc power source [7-11].

The output voltage v_1 of this leg (with respect to the ground) is either $+V_{dc}/2$ (S_5 closed) or $-V_{dc}/2$ (S_6 closed). This leg is connected in series with a full H-bridge that in turn is supplied by a capacitor voltage. If the capacitor is kept charged to $V_{dc}/2$, then the output voltage of the H-bridge can take on the values $+V_{dc}/2$ (S_1, S_4 closed), 0 (S_1, S_2 closed or S_3, S_4 closed), or $-V_{dc}/2$ (S_2, S_3 closed). An example output waveform that this topology can achieve is shown in Fig. 3 (a). When the output voltage $v = v_1 + v_2$ is required to be zero, one can either set $v_1 = +V_{dc}/2$ and $v_2 = -V_{dc}/2$ or $v_1 = -V_{dc}/2$ and $v_2 = +V_{dc}/2$. It is this flexibility in choosing how to make that output voltage zero that is exploited to regulate the capacitor voltage.

When only a dc power source is used in the inverter, that is, the H-bridge uses a capacitor as the dc power source, the capacitor's voltage regulation control details are illustrated in Fig. 3. During $\theta_1 \le \theta \le \pi$, the output voltage in Fig. 2 is zero and the current i > 0. If S_1, S_4 are closed (so that $v_2 = +V_{dc}/2$) along with S_6 closed (so that $v_1 = -V_{dc}/2$), then the capacitor is discharging ($i_c = -i < 0$ see Fig. 3 (b)) and $v = v_1 + v_2 = 0$. On the other hand, if S_2, S_3 are closed (so that $v_2 = -V_{dc}/2$) and S_5 is also closed (so that $v_1 = +V_{dc}/2$), then the capacitor is charging ($i_c = i > 0$ see Fig. 3 (c)) and $v = v_1 + v_2 = 0$. The case $i < 0$ is accomplished by simply reversing the switch positions of the $i > 0$ case for charge and discharge of the capacitor. Consequently, the method consists of monitoring the output current and the capacitor voltage so that during periods of zero voltage output, either the switches S_1, S_4, and S_6 are closed or the switches S_2, S_3, S_5 are closed depending on whether it is necessary to charge or discharge the capacitor.

As Fig. 3 illustrates, this method of regulating the capacitor voltage depends on the voltage and current not being in phase. That means one needs positive (or negative) current when the voltage is passing through zero in order to charge or discharge the capacitor. Consequently, the amount of capacitor voltage the scheme can regulate depends on the phase angle difference of output voltage and current. It is noted that the above capacitor voltage regulation method is described using a fundamental frequency modulation scheme because it is easier to illustrate [7]. The PWM scheme uses the same method as described in the next section.

III. PSIM AND SIMULINK CO-SIMULATION

The modulation control schemes for the multilevel inverter can be divided into two categories, fundamental switching frequency [1][4][8] and high switching

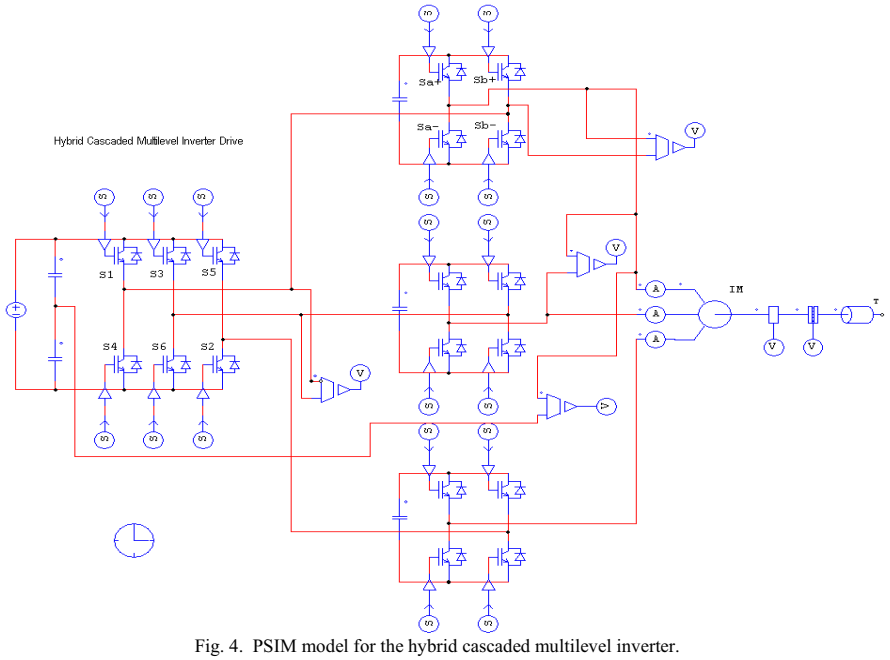

Fig. 4. PSIM model for the hybrid cascaded multilevel inverter.

frequency PWM [4][12-16] such as multilevel carrier-based PWM, selective harmonic elimination and multilevel space vector PWM. Both PWM and fundamental frequency switching methods can be used for the hybrid multilevel inverter. Multilevel carrier-based PWM strategies are the most popular methods because they are easily implemented. Three major carrier-based techniques that are used in a conventional inverter can be applied in a multilevel inverter: sinusoidal PWM (SPWM), third harmonic injection PWM (THPWM), and space vector PWM (SVM). SPWM is a popular method in industrial applications. It uses several triangle carrier signals, one carrier for each level and one reference, or modulation, signal per phase. In the proposed inverter, the top H-bridge inverter is operated under the SPWM mode and the bottom standard 3-leg inverter is operated under square-wave mode in order to reduce switching loss.

For an m-level inverter, the amplitude modulation index, m_a, is defined as

$$m_a = \frac{A_m}{(m-1)A_C}, \quad (1)$$

where, A_m is the peak-to-peak reference waveform amplitude, A_c is the peak-to-peak carrier waveform amplitude.

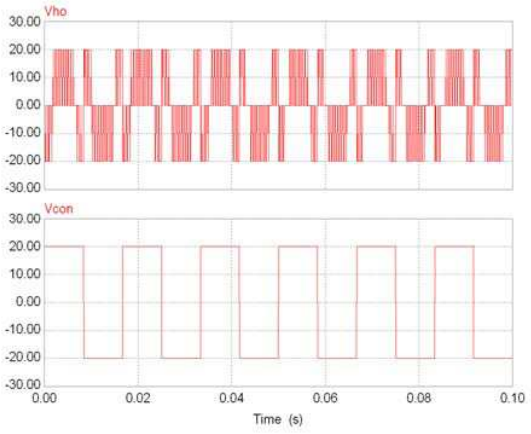

Fig. 5. H-bridge (top) and standard inverter (bottom) output voltage.

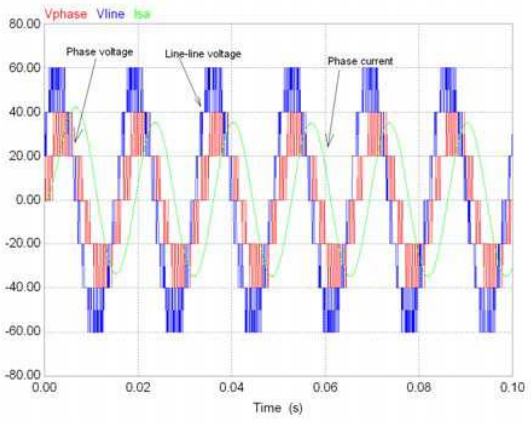

Fig. 6. Output line-line and phase voltage, phase current of the hybrid cascaded multilevel inverter (m_a=0.8).

In this paper, the simulation model is developed with PSIM and MATALB/SIMULINK. The PSIM model for the power circuit is shown in Fig. 4. Its control functions are completed in MATLAB/SIMULINK. One can therefore make full use of PSIM's capability in power simulation and MATLAB/SIMULINK's capability in control simulation in a complementary way.

A key issue to realize the control method is that the capacitors voltages (V_c) need to be kept regulated to one half of the DC voltage ($V_{dc}/2$). To regulate a capacitor's voltage, if $i > 0$ and $V_c < V_{dc}/2$, the inverter controls the bottom inverter to output $V_{dc}/2$ and the top H-bridge to output $-V_{dc}/2$ for inverter's 0 voltage output; if $i > 0$ and $V_c > V_{dc}/2$, the inverter controls the bottom inverter to output $-V_{dc}/2$ and the top H-bridge to output $V_{dc}/2$ for inverter's 0 voltage output. The $i < 0$ situation is similar to the $i > 0$ situation, the controller just needs to reverse its switching signals.

The top H-bridge and bottom standard 3-leg inverter output voltage waveform are shown in Fig. 5. Fig. 6 shows the simulation results, which include phase voltage, line-line voltage, and phase current. The output phase voltage is five-level and the output phase current is sinusoidal. Moreover, the PWM scheme makes the inverter output zero voltage for significant time intervals so that the capacitor can be charged or discharged during these periods.

IV. Experiment Verification

A 5 kW prototype using power MOSFETs (100V, 180A) as shown in Fig. 7 has been built in order to verify the proposed hybrid multilevel inverter. The load is a 15 hp three-phase induction motor, which is loaded less than 5 kW. An Altera FLEX 10K field programmable gate array (FPGA) controller is used to implement the control algorithm to drive the motor with the real-time variable output voltage and variable frequency.

The FPGA controller is designed as a card to be plugged into a personal computer, which uses a peripheral component interconnect (PCI) bus to communicate with the microcomputer in which a Visual Basic interface is used to input and adjust the control schemes and parameters.

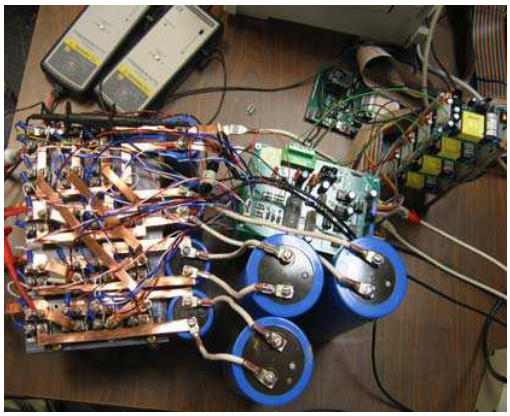

Fig. 7. 5 kW hybrid cascaded multilevel inverter prototype.

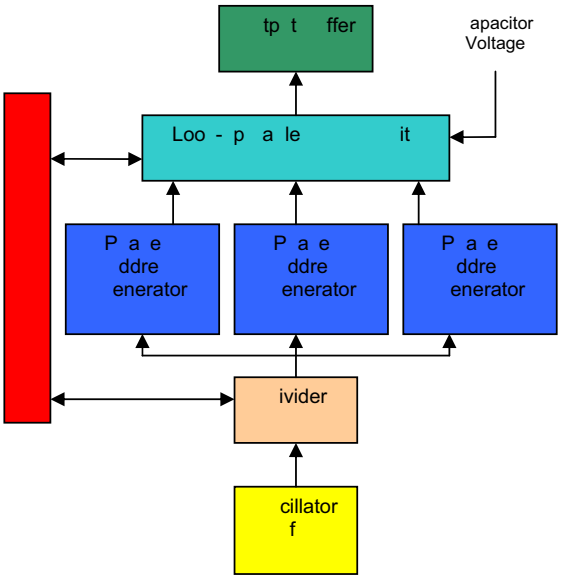

Fig. 8. FPGA controller block diagram.

The capacitor voltage is detected by a voltage sensor and fed into the FPGA controller to realize the capacitor voltage regulation. The block diagram of the FPGA controller is shown in Fig. 8.

Switching signal data are stored in a 12×1024 bits in-chip RAM. An oscillator generates a fixed frequency clock signal, and a divider is used to generate the specified control clock signal corresponding to the converter output frequency. Three phase address generators share a public switching data RAM because they have the same switching data with only a different phase angle. (The switching data is only for one half cycle because the switching data is symmetric.) For each step, the three-phase signal controller controls the address selector to fetch the corresponding switching data from the RAM to the output buffer according to the capacitor's voltage.

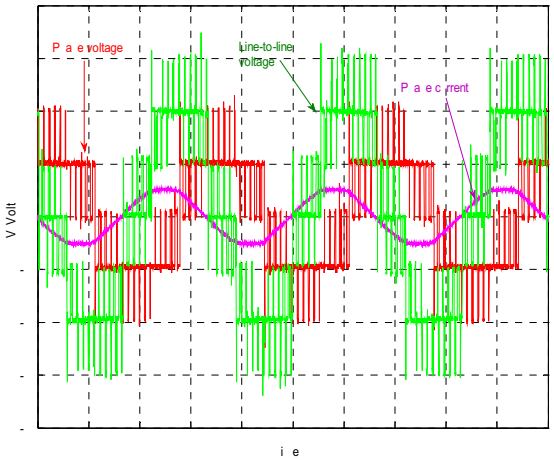

Fig. 9. Output line-line and phase voltage, phase current of the hybrid cascaded multilevel inverter (m_a=0.8).

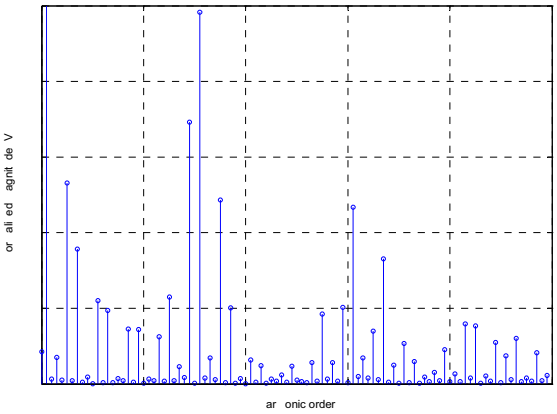

Fig. 10. Normalized FFT analysis of phase voltage.

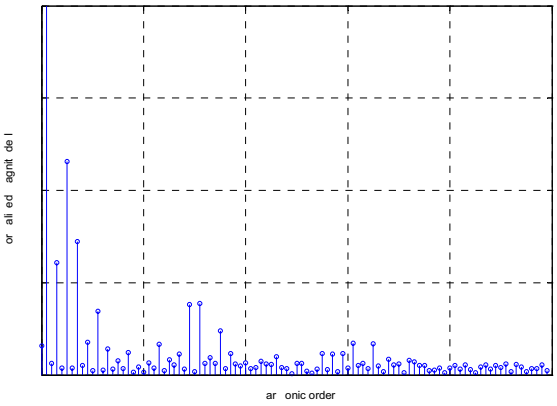

Fig. 11. Normalized FFT analysis of phase current.

The experimental results including phase voltage, line-line voltage, and phase current are shown in Fig. 9. DC bus voltage is 40V. The capacitor voltage is kept regulated to one half of the DC bus voltage. The output phase voltage is five-level. The phase current waveform is close to sinusoidal. Fig. 10 and Fig. 11 show the normalized FFT analysis results of phase voltage and phase current.

V. Conclusion

A simulation model for the hybrid multilevel inverter is developed in PSIM and SIMULINK co-simulation platform. The inverter output is a five level phase voltage. The paper presents the main circuit model in PSIM and simulation results in detail. The experiment and FFT analysis results verified the proposed hybrid cascaded multilevel inverter with a PWM control method.

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