Fundamental Frequency Switching Strategies of a Seven-Level Hybrid Cascaded H-Bridge Multilevel Inverter

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***Abstract*—This paper presents a cascaded H-bridge multilevel inverter that can be implemented using only a single dc power source and capacitors. Standard cascaded multilevel inverters require n dc sources for $2n + 1$ levels. Without requiring transformers, the scheme proposed here allows the use of a single dc power source (e.g., a battery or a fuel cell stack) with the remaining $n - 1$ dc sources being capacitors, which is referred to as hybrid cascaded H-bridge multilevel inverter (HCMLI) in this paper. It is shown that the inverter can simultaneously maintain the dc voltage level of the capacitors and choose a fundamental frequency switching pattern to produce a nearly sinusoidal output. HCMLI using only a single dc source for each phase is promising for high-power motor drive applications as it significantly decreases the number of required dc power supplies, provides high-quality output power due to its high number of output levels, and results in high conversion efficiency and low thermal stress as it uses a fundamental frequency switching scheme. This paper mainly discusses control of seven-level HCMLI with fundamental frequency switching control and how its modulation index range can be extended using triplen harmonic compensation.**

***Index Terms*—Fundamental frequency modulation control, hybrid cascaded H-bridge multilevel inverter (HCMLI), triplen harmonic compensation.**

I. Introduction

THE MULTILEVEL inverter is a promising power electronics topology for high-power applications because of its low electromagnetic interference (EMI) and high efficiency with low-switching-frequency control method [1]–[6].

Traditionally, each phase of a cascaded multilevel inverter requires n dc sources for $2n + 1$ levels. For many applications, obtaining so many separate dc sources may preclude the use of such an inverter. To reduce the number of dc sources required when the cascaded H-bridge multilevel inverter is applied to a motor drive, a scheme is proposed in this paper that allows the use of a single dc source (such as battery or fuel cell) as the first dc source with the remaining $n - 1$ dc sources being capacitors in the cascaded H-bridges multilevel inverter, which is referred to as the hybrid cascaded H-bridge multilevel inverter (HCMLI) [7]–[9]. Previous work has shown that pulsewidth modulation (PWM) control can be used on HCMLI [10]. Compared to the traditional cascaded H-bridge multilevel inverter, the proposed HCMLI has a low number of dc sources and retains the low-switching-frequency advantage.

The authors have been working on the multilevel inverter harmonic elimination control technologies based on harmonic elimination mathematics theory, and present several findings, such as complete switching angle solution technology and active harmonic elimination technology. The seven-level multilevel inverter fundamental frequency harmonic elimination method and triplen harmonic injection for modulation index extension method have been published in previous papers. All the technologies published in the previous papers can be applied to normal multilevel inverters to satisfy different application requirements.

However, the published technologies cannot be directly applied to HCMLI as the capacitors are not dc sources. The control goal of the HCMLI needs to maintain the balance of the dc voltage level of the capacitors while producing a nearly sinusoidal three-phase output voltage using a low-switching-frequency harmonic elimination method. This paper focuses on how to apply the seven-level fundamental frequency harmonic elimination method to HCMLI and extend its modulation index range, and presents new findings on HCLMI control other than normal cascaded H-bridge multilevel inverters.

II. Working Principle of HCLMI

To operate a cascaded multilevel inverter using a single dc source, capacitors are used as the dc sources for all but the first source. To explain, consider a cascaded multilevel inverter with two H-bridges as shown in Fig. 1. The dc source for the first H-bridge (H_1) is a battery or fuel cell with an output voltage of $V_{\rm dc}$, while the dc source for the second H-bridge (H_2) is a capacitor whose voltage is to be held at V_c. The output voltage of the first H-bridge is denoted by v_1 and the output of the second H-bridge is denoted by v_2 so that the output voltage of

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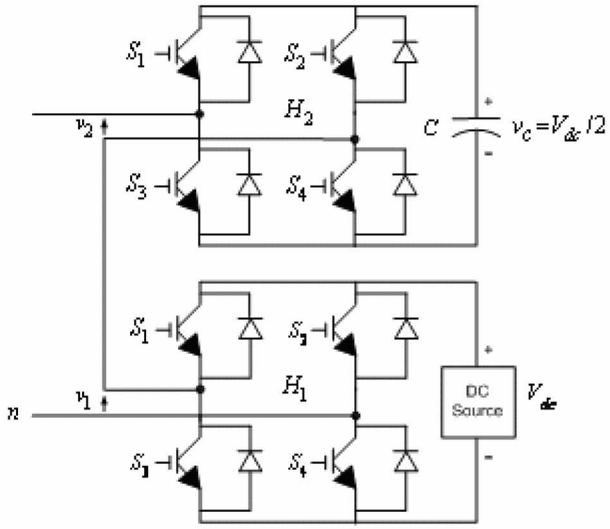
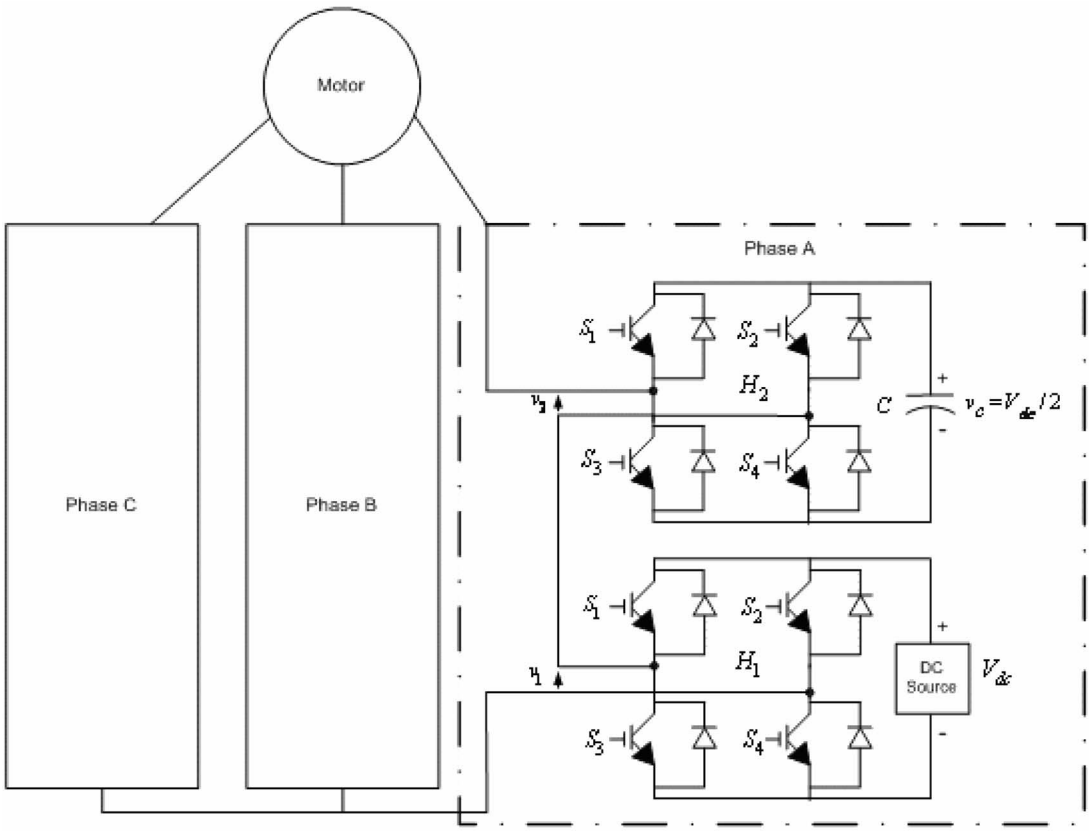


(a)



(b)

Fig. 1. Topology of the proposed multilevel inverter with a single dc source for first level and capacitors for other levels. (a) Single-phase topology. (b) Three-phase topology.

the cascaded multilevel inverter is

$$v(t) = v_1(t) + v_2(t). \tag{1}$$

By opening and closing the switches of H_1 appropriately, the output voltage v_1 can be made equal to $-V_{\rm dc}$, 0, or $V_{\rm dc}$, while similarly the output voltage of H_2 can be made equal to $-V_c$, 0, or V_c by opening and closing its switches appropriately. Therefore, the output voltage of the inverter can have the values $-(V_{\rm dc}+V_c)$, $-V_{\rm dc}$, $-(V_{\rm dc}-V_c)$, $-V_c$, 0, V_c, $(V_{\rm dc}-V_c)$, $V_{\rm dc}$, and $(V_{\rm dc}+V_c)$, which constitute nine possible output levels.

To balance the capacitor's voltage, not all the possible voltage levels must be used in a cycle. A simple seven-level output voltage case $-3V_{\rm dc}/2$, $-V_{\rm dc}$, $-V_{\rm dc}/2$, 0, $V_{\rm dc}/2$, $V_{\rm dc}$, $3V_{\rm dc}/2$ can be designed, as shown in Fig. 2, when the capacitor's voltage

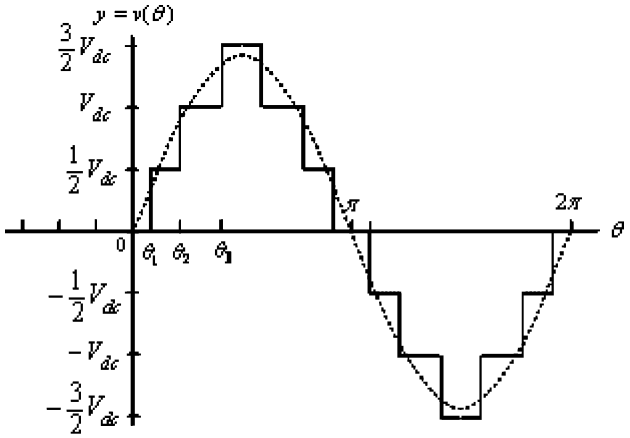


Fig. 2. Seven-level equal step output-voltage waveform.

TABLE I
OUTPUT VOLTAGES FOR A SEVEN-LEVEL INVERTER

θ	v_1	v_2	$v = v_1 + v_2$
$0 \le \theta < \theta_1$	0	0	0
$\theta_1 \le \theta < \theta_2$	0	$V_{dc}/2$	$V_{dc}/2$
$\theta_1 \le \theta < \theta_2$	V_{dc}	$-V_{dc}/2$	$V_{dc}/2$
$\theta_2 \le \theta < \theta_3$	V_{dc}	0	V_{dc}
$\theta_3 \le \theta < \pi/2$	V_{dc}	$V_{dc}/2$	$3V_{dc}/2$

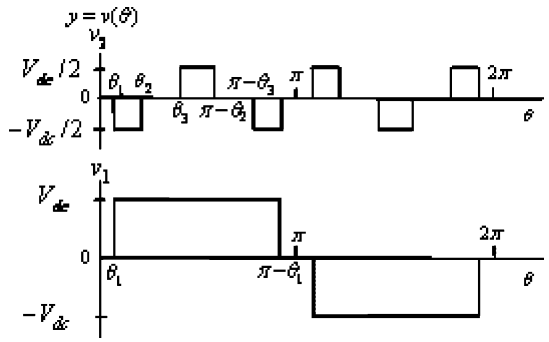


Fig. 3. H-bridge voltages v_1 and v_2 control for $\theta_1 \le \theta < \theta_2$, $v_1 = V_{\rm dc}$ and $v_2 = -V_{\rm dc}/2$.

V_c is chosen as $V_{\rm dc}/2$. Table I shows how a waveform can be generated using the topology of Fig. 1.

Fig. 3 shows how the waveform of Fig. 2 is generated if for $\theta_1 \le \theta < \theta_2, v_1 = V_{\rm dc}$ and $v_2 = -V_{\rm dc}/2$ are chosen. Similarly, Fig. 4 shows how the waveform of Fig. 2 is generated if for $\theta_1 \le \theta < \theta_2, v_1 = 0$ and $v_2 = V_{\rm dc}/2$ is chosen. The fact that the output-voltage level $V_{\rm dc}/2$ can be achieved in two different ways is exploited to keep the capacitor voltage regulated. Specifically, one measures the capacitor voltage v_c and the inverter current i. Then, if $v_c < V_{\rm dc}/2$ and $i > 0$, one sets $v_1 = V_{\rm dc}$ and $v_2 = -V_{\rm dc}/2$, and the capacitor is being charged. Table II summarizes this case along with the discharge case $v_c > V_{\rm dc}/2$.

By choosing the nominal value of the capacitor voltage to be one-half that of the dc source, the values of the levels are equal; however, this is not strictly required. The criteria for this capacitor balancing scheme is that: 1) the capacitance value is

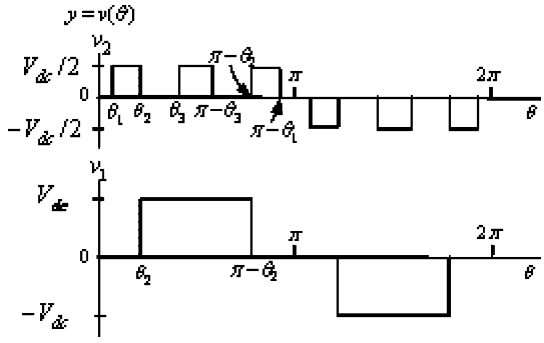


Fig. 4. H-bridge voltages v_1 and v_2 control for $\theta_1 \le \theta < \theta_2$, $v_1 = 0$ and $v_2 = V_{\rm dc}/2$.

TABLE II
CONTROLLER FOR CAPACITOR VOLTAGE LEVEL

System State	v_1	v_2	$v = v_1 + v_2$	Capacitor State
$v_c < V_{dc}/2, i > 0$	V_{dc}	$-V_{dc}/2$	$V_{dc}/2$	Charging
$v_c < V_{dc}/2, i < 0$	0	$V_{dc}/2$	$V_{dc}/2$	Charging
$v_c > V_{dc}/2, i > 0$	0	$V_{dc}/2$	$V_{dc}/2$	Discharging
$v_c > V_{dc}/2, i < 0$	V_{dc}	$-V_{dc}/2$	$V_{dc}/2$	Discharging

chosen large enough so that the variation of its voltage around its nominal value is small (generally speaking, one can choose the capacitor–load time constant to be ten times than that of the fundamental period); and 2) the capacitor charging energy is greater than or equal to the capacitor discharge energy in a cycle.

III. MODULATION CONTROL

Generally, traditional PWM control methods and space vector PWM methods are applied to multilevel-inverter modulation control [15]–[27]. These methods will cause extra losses due to high switching frequencies. For this reason, low-switching-frequency control methods, such as selective harmonic elimination method [11]–[14], [28]–[34], fundamental frequency switching method [11], [14], or active harmonic elimination method, can be used for the HCMLI control [13]. Here, fundamental frequency method is used.

The Fourier series expansion of the seven-level equal step output voltage waveform shown in Fig. 2 is

$$V(\omega t) = \sum_{n=1,3,5\ldots}^{\infty} \frac{2V_{\rm dc}}{n\pi}(\cos(n\theta_1) + \cos(n\theta_2) + \cos(n\theta_3))\sin(n\omega t) \quad (2)$$

where n is the harmonic number of the output voltage of the multilevel inverter. Ideally, given a desired fundamental voltage V_1, one wants to determine the switching angles θ_1, θ_2, and θ_3 so that $V(\omega t) = V_1 \sin(\omega t)$, and specific higher harmonics of $V(n\omega t)$ are eliminated. For three-phase inverter applications, the triplen harmonics in each phase need not be canceled as they automatically cancel in the line-to-line voltages. In this paper, the goal is to achieve the fundamental and eliminate the fifth and seventh harmonics. Using (2), this can be formulated

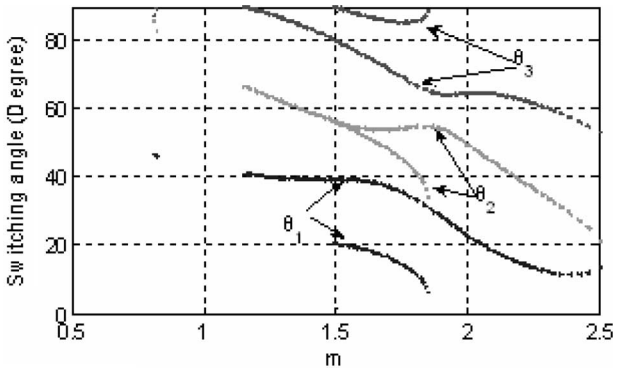


Fig. 5. Solution of switching angles for seven-level multilevel converter.

as the solution to the following equations:

$$\begin{aligned}&\cos(\theta_1)+\cos(\theta_2)+\cos(\theta_3)=m\\&\cos(5\theta_1)+\cos(5\theta_2)+\cos(5\theta_3)=0\\&\cos(7\theta_1)+\cos(7\theta_2)+\cos(7\theta_3)=0.\end{aligned}\tag{3}$$

This is a system of three transcendental equations in the three unknowns θ_1, θ_2, and θ_3. There are many ways one can solve for the angles. Here, the resultant method [31], [32] is used to find all the switching angles that are shown in Fig. 5 [31], and the modulation index m is defined in this paper as

$$m=\frac{V_1}{(4/\pi_1)(V_{\rm dc}/2)}.\tag{4}$$

IV. Conditions of Capacitor Voltage Balance Control

We now show the ability to balance the capacitor voltage, which is related to the modulation index and the load power factor angle. To explain, Fig. 6 shows the voltage waveform and three current waveforms corresponding power factor angles $-\pi/6$, 0, and $\pi/6$.

To analyze the voltage balance situation due to capacitor charging and discharging in detail, a power factor angle φ shown in Fig. 6(b) is used. Here, charging amount is defined as

$$Q_{\rm charging}=\int_0^{2\pi} I_{\rm charging}\,d\theta\tag{5}$$

and discharging amount is defined as

$$Q_{\rm discharging}=\int_0^{2\pi} I_{\rm discharging}\,d\theta.\tag{6}$$

Then, in a whole cycle, the net accumulation charge amount is

$$Q_{\rm accumulation}=Q_{\rm charging}-Q_{\rm discharging}.\tag{7}$$

Therefore, to achieve capacitor voltage regulation, the net accumulation amount must be greater than zero in a whole cycle. As the capacitor charging is restricted by the switching angles and time periods of the output voltage waveform, the key control issue is to charge the capacitor as much as possible.

Applying fundamental frequency switching angles to (5)–(7), and assuming the power factor angle is φ, as shown in Fig. 6(b), and the load current is

$$i_{\rm load}=I\sin(\theta-\varphi).\tag{8}$$

The capacitors' voltage balance condition is

$$\begin{aligned}Q_{\rm accumulation}=&\int_{\theta_1}^{\theta_2}|I\sin(\theta-\varphi)|d\theta+\int_{\pi-\theta_2}^{\pi-\theta_1}|I\sin(\theta-\varphi)|d\theta\\&-\int_{\theta_3}^{\pi-\theta_3}|I\sin(\theta-\varphi)|\,d\theta\geq 0.\end{aligned}\tag{9}$$

To implement (9), a current sensor is needed to detect the current direction and use it for the switching control. For practical applications, a current sensor is not desired. Therefore, the capacitors' voltage balance condition becomes

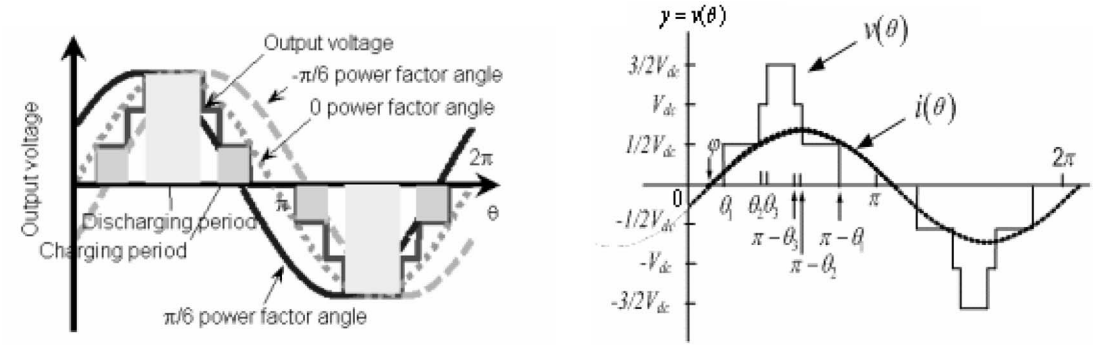
$$\begin{aligned}Q_{\rm accumulation}=&\int_{\theta_1}^{\theta_2}I\sin(\theta-\varphi)d\theta+\int_{\pi-\theta_2}^{\pi-\theta_1}I\sin(\theta-\varphi)d\theta\\&-\int_{\theta_3}^{\pi-\theta_3}I\sin(\theta-\varphi)d\theta\geq 0.\end{aligned}\tag{10}$$

Based on the aforementioned analysis, numerical computation was performed by using switching angles shown in Fig. 5. The net accumulation amounts of power factor angles 0 and $\pm\pi/6$ are calculated for the seven-level output voltage case, and the accumulation curves with and without current direction control are shown in Fig. 7(a) and (b). From (9) and (10), it can be expected that the amount of accumulation is proportional to the load current, but the accumulation curve shape is unique for any load current. For this reason, Fig. 7 shows the curve shape for all the load current (y-axis does not mark any value). For both cases, the highest modulation index that can balance the capacitor's voltage is around 1.54. It means that for high modulation indexes above 1.54, the discharging amount is greater than the charging amount, which results in the inability to regulate the capacitor's voltage. For practical applications, this modulation index range is somewhat narrow. An improved method is needed to extend the modulation index range.

Fig. 7(a) and (b) shows cases for power factor angle cases $-\pi/6$, 0, and $\pi/6$. All of their balance points are $m=1.54$, and $\pm\pi/6$ curves are overlapped. If the absolute value of the power factor angle is between 0 and $\pi/6$, the curve lies between 0 and $\pm\pi/6$ curves. It can also be seen that there are some spikes in the curves. This is because the switching angles shown in Fig. 5 are not continuous for these points. The accumulation amount is decreasing when the modulation index is increasing; this is because the charging period is decreasing and discharging period is increasing.

V. Modulation Index Extension Control by Injecting Triplen Harmonics

The key point of the capacitor voltage balance control at high modulation index is to increase the charging time and decrease the discharging time. To do this, triplen harmonic voltage injection method is proposed. The triplen harmonic voltage is a



(a) (b)

Fig. 6. (a) Capacitor charging and discharging time with different power factor angles. (b) Load current with power factor φ.

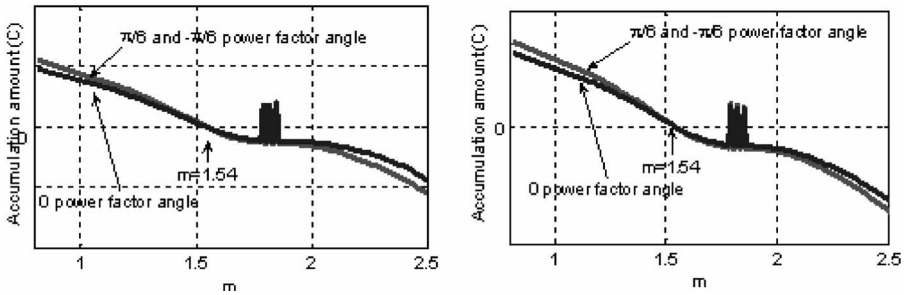


Fig. 7. Accumulation curve without triplen harmonic voltage compensation. (a) With current direction detection. (b) Without current direction detection.

square wave with a frequency equal to three times the fundamental frequency with amplitude of $V_{\rm dc}/2$. The triplen harmonic shown in Fig. 8(b) can be represented by

$$V_{\rm tri}(\omega t) = \sum_{n=1,3,5\ldots}^{\infty} \frac{2V_{\rm dc}}{n\pi}\cos(n\theta_3)\sin(3n\omega t) \qquad (11)$$

and is injected into the original seven-level output voltage shown in Fig. 8(a) to obtain an output voltage waveform shown in Fig. 8(c). The triplen harmonic voltages will automatically cancel in the line–line voltages of three-phase systems, and will not change the fundamental frequency contents [9]. The only effect is to change the charging period and discharging period. The charging and discharging times with triplen harmonic injection are shown in Fig. 9. From Fig. 9, it can be seen that the original long discharging period has been changed into two short discharging periods.

The capacitor's voltage balance conditions with and without current direction detection are now (12) and (13), respectively

$$\begin{aligned} Q_{\rm accumulation} = &\int_{\frac{\pi}{6}-\frac{\theta_3}{2}}^{\theta_1} |I\ \sin(\theta-\varphi)|\,d\theta \\ &+ \int_{\pi-\theta_1}^{\frac{5\pi}{6}+\frac{\theta_3}{2}} |I\sin(\theta-\varphi)|\,d\theta \\ &- \int_{\theta_2}^{\theta_3} |I\sin(\theta-\varphi)|\,d\theta \\ &- \int_{\pi-\theta_3}^{\pi-\theta_2} |I\sin(\theta-\varphi)|\,d\theta \geq 0 \qquad (12) \end{aligned}$$

$$\begin{aligned} Q_{\rm accumulation} = &\int_{\frac{\pi}{6}-\frac{\theta_3}{2}}^{\theta_1} I\sin(\theta-\varphi)d\theta \\ &+ \int_{\pi-\theta_1}^{\frac{5\pi}{6}+\frac{\theta_3}{2}} I\sin(\theta-\varphi)d\theta \\ &- \int_{\theta_2}^{\theta_3} I\sin(\theta-\varphi)d\theta \\ &- \int_{\pi-\theta_3}^{\pi-\theta_2} I\sin(\theta-\varphi)d\theta \geq 0. \qquad (13) \end{aligned}$$

If triplen harmonic voltage compensation method is used, the accumulation curve, using switching angles shown in Fig. 5 based on (12) and (13), is shown in Fig. 10. If current direction control is used, the highest possible modulation index while still balancing the capacitor's voltage is 1.98 for a power factor angle 0 and 2.08 for power factor angles $\pm\pi/6$, which are shown in Fig. 10(a). If current direction detection is not used, the highest possible modulation index while still balancing the capacitor's voltage is 1.98 for power factor angles 0 and $\pm\pi/6$, which are shown in Fig. 10(b). If the absolute value of the power factor angle is between 0 and $\pi/6$, the curve will lie between the two curves of 0 and $\pm\pi/6$.

Similar to the seven-level without triplen harmonic case, from (12) and (13), it can be expected that the amount of accumulation is proportional to the load current, but the accumulation curve shape is unique for any load current. For this reason, Fig. 10 shows the curve shape for all the load current (y-axis does not mark any value). Comparing the accumulation curves of

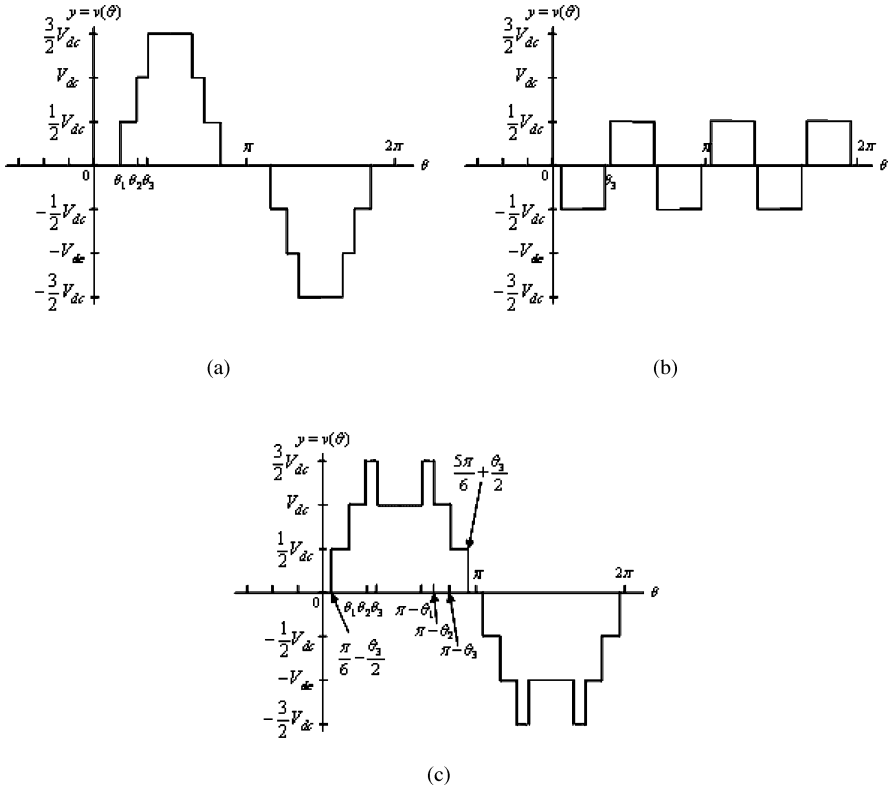


Fig. 8. Output voltage waveform with triplen harmonic compensation. (a) Original seven-level output waveform. (b) Injected triplen square wave. (c) Final output waveform.

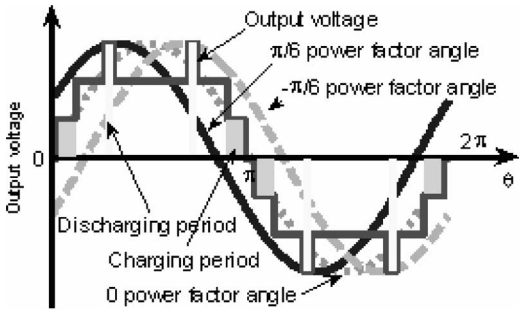


Fig. 9. Capacitor charging and discharging time with different power factor angles with triplen harmonic voltage compensation.

Fig. 10(a) and (b), it is observed that the current direction control does not affect the modulation index range too much.

Comparing Fig. 10 to Fig. 7, it is observed that a modulation index of at least 1.98 can be achieved using triplen harmonic compensation while also keeping the capacitor regulated. Compared to 1.54 without triplen harmonic compensation, this is a 33% extension.

VI. Experimental Results

To experimentally validate the proposed HCMLI with seven-level equal-step output-voltage-modulation control scheme, a prototype three-phase-cascaded H-bridge multilevel inverter has been built using MOSFETs as the switching devices. Three dc power supplies (one for each phase) feed the inverter. A real-time variable output voltage, variable-frequency three-phase inverter controller based on Altera FLEX 10K field-programmable gate array (FPGA) is used to implement the control algorithm.

To maintain the capacitor's voltage balance, a comparator using an operational amplifier is used to detect the capacitor's voltage and feed the voltage signal into the FPGA controller. A 1-hp induction motor is connected to the motor drive as its load. In the experimental implementation, the capacitors' voltages are regulated to $V_{\rm dc}/2 = 24$ V. As discussed previously, the current direction control will not affect the modulation index range too much. Current direction signal is not used for the capacitor's voltage balance control in the experiments.

A. Fundamental Frequency Modulation Control Without Triplen Harmonic Compensation

For voltage balance control without triplen harmonic compensation method, the modulation index $m = 1.32$ and stator frequency $f = 60$ Hz are chosen for the experiment. Fig. 11 shows the output phase voltage waveform, and Fig. 12 shows the corresponding normalized fast Fourier transform (FFT) spectrum of the line–line voltage. The phase current waveform is shown in Fig. 13, and Fig. 14 shows the corresponding normalized FFT spectrum of the phase current. The current harmonics are less than the corresponding voltage harmonics as the stator inductance of the induction motor acts as a low-pass filter.

From the voltage spectrum distribution in Fig. 12, it is seen that the fifth and seventh harmonic voltages are nearly zero, and the triplen harmonic voltages (such as the third, ninth, etc.) are

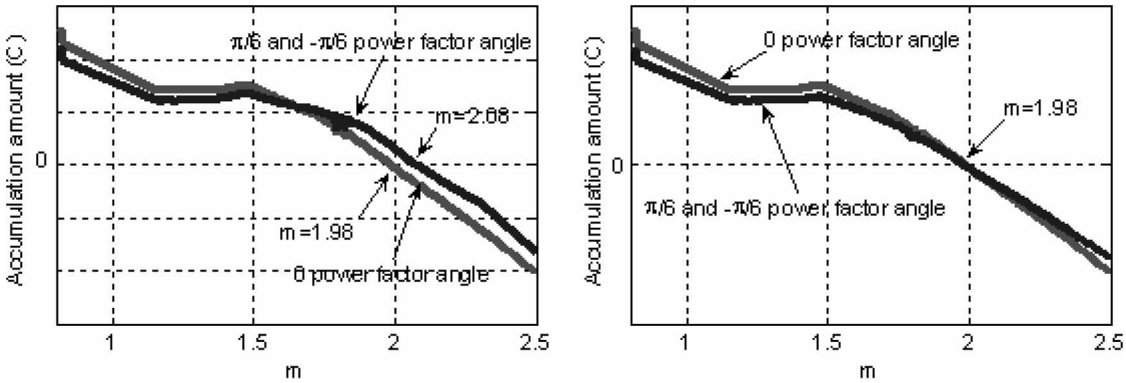


Fig. 10. Accumulation curve with triplen harmonic voltage compensation. (a) With current direction control. (b) Without current direction control.

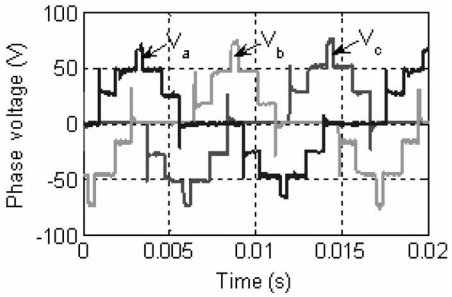


Fig. 11. Output phase voltage waveform for $m = 1.32$, $f = 60$ Hz.

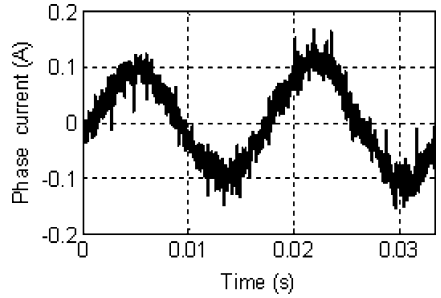


Fig. 13. Output current waveform for $m = 1.32$, $f = 60$ Hz.

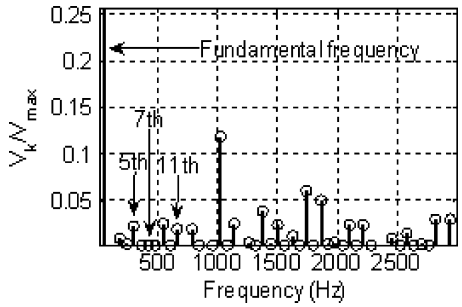


Fig. 12. Normalized FFT analysis of line–line voltage for $m = 1.32$, $f = 60$ Hz.

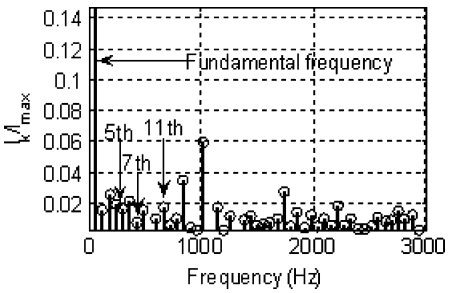


Fig. 14. Normalized FFT analysis of phase current for $m = 1.32$, $f = 60$ Hz.

also very low. From the current spectrum distribution shown in Fig. 14, it is seen that it has very low fifth or seventh current harmonics, and very low triplen current harmonics. Also, the simulation shows that the 11th harmonic is 1.68%, and the experimental 11th harmonic shown in Fig. 12 is 2%. The simulation result matches the experimental result very well.

B. Fundamental Frequency Modulation Control With Triplen Harmonic Compensation

For voltage balance control using the triplen harmonic compensation method, the modulation index $m = 1.97$ and stator frequency $f = 45$ Hz are chosen for the experiment. Fig. 15 shows the output phase voltage waveform, while Fig. 16 shows the corresponding normalized FFT spectrum of the line–line voltage. The phase current waveform is shown in Fig. 17, and

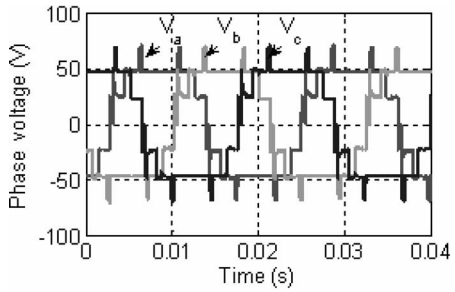


Fig. 15. Output phase voltage waveform for $m = 1.97$, $f = 45$ Hz.

Fig. 18 shows the corresponding normalized FFT spectrum of the phase current.

It can be observed that the capacitor's voltage is regulated at 24 V, which is half of the dc source voltage.

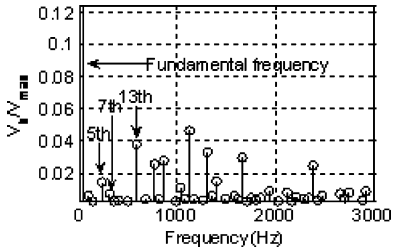


Fig. 16. Normalized FFT analysis of line–line voltage for $m = 1.97$, $f = 45$ Hz.

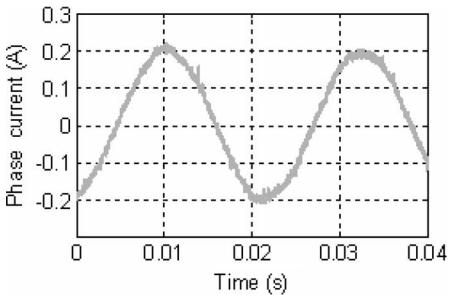


Fig. 17. Output current waveform for $m = 1.97$, $f = 45$ Hz.

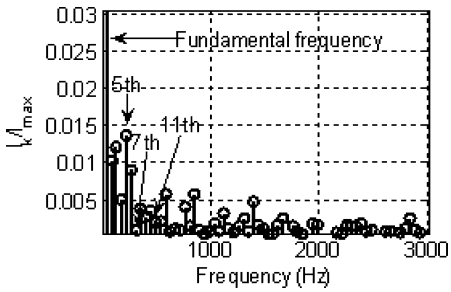


Fig. 18. Normalized FFT analysis of phase current for $m = 1.97$, $f = 45$ Hz.

From the voltage spectrum distribution in Fig. 16, it is seen that the fifth and seventh harmonic voltages are nearly zero, and the triplen harmonic voltages (such as the third, ninth, etc.) are also very low. From the current spectrum distribution shown in Fig. 18, it is seen that it has low fifth or seventh current harmonics, as well as low triplen current harmonics. Again the current harmonics are less than the corresponding voltage harmonics as the stator inductance of the induction motor acts as a low-pass filter. Also, the simulation shows that the 13th harmonic is 3.4%, and the experimental 13th harmonic shown in Fig. 16 is 3.8%. The simulation result matches the experimental result very well.

It is also observed that for modulation index in the range 1.54–1.97, the seven-level output voltage waveform with triplen harmonic compensation can balance the capacitors' voltages. However, the seven-level output voltage waveform without triplen harmonic compensation is unable to balance the capacitors' voltages.

In theory, the capacitor voltage balance can reach modulation index $m = 1.98$. However, in the actual experiments, due to the switching loss, conduction loss of the switching devices, and the wire copper loss of the circuit, the modulation index for capacitor's voltage balance is seen to be slightly less than 1.98. This is observed through experiments that the capacitor's voltage is maintained at a lower voltage than the desired $V_{\rm dc}/2$ if the modulation index is 1.98.

VII. Conclusion

This paper proposed an HCMLI that uses only one power source for each phase while producing desired multilevel voltage waveforms. A fundamental frequency switching control algorithm was developed, and a triplen harmonic compensation method was also developed to extend the modulation index range for which the capacitor voltage can be regulated. Simulation and experiments were performed to show the proposed method work in practice.

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