Lecture 10: Isolated Converters II & DCM Introduction

ECE 481: Power Electronics
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Announcements

• Midterm exam due Thursday, start of class
• Hw #3 returned today
• Missing HW assignments
3. [30 pts] Design of a Boost Converter

The boost converter in Fig. 3 connects a lead-acid battery to a 48 V DC bus. The converter input is the battery voltage, which has characteristics:
- Maximum \( V_{in} \): 15 V
- Minimum \( V_{in} \): 10 V

The maximum output power is 100 W, and the switching frequency is 100 kHz. The inductance \( L \) is chosen to be 10 \( \mu \)H, and the capacitance may be assumed to be very large for parts (a)-(c).

![Booster Converter Diagram]

Figure 3: Booster Converter

a) [10 pts] A number of parts are available for both the MOSFET and diode. Important characteristics of each device are shown in Tables 1 and II. The rated maximum currents and voltages are the maximum instantaneous values which the devices can handle.

**Table I: MOSFET Devices**

<table>
<thead>
<tr>
<th>Device</th>
<th>Rated max ( I_{D} )</th>
<th>Rated max ( V_{G} )</th>
<th>( R_{D} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>40 V</td>
<td>30 A</td>
<td>5 m( \Omega )</td>
</tr>
<tr>
<td>II</td>
<td>100 V</td>
<td>15 A</td>
<td>15 m( \Omega )</td>
</tr>
<tr>
<td>III</td>
<td>100 V</td>
<td>20 A</td>
<td>50 m( \Omega )</td>
</tr>
<tr>
<td>IV</td>
<td>150 V</td>
<td>15 A</td>
<td>30 m( \Omega )</td>
</tr>
<tr>
<td>V</td>
<td>150 V</td>
<td>20 A</td>
<td>75 m( \Omega )</td>
</tr>
</tbody>
</table>

**Table II: Diode Devices**

<table>
<thead>
<tr>
<th>Device</th>
<th>Rated max ( V_{D} )</th>
<th>Rated max ( I_{D} )</th>
<th>( V_{F} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>VI</td>
<td>40 V</td>
<td>20 A</td>
<td>0.5 V</td>
</tr>
<tr>
<td>VII</td>
<td>100 V</td>
<td>15 A</td>
<td>1.0 V</td>
</tr>
<tr>
<td>VIII</td>
<td>150 V</td>
<td>5 A</td>
<td>0.7 V</td>
</tr>
<tr>
<td>IX</td>
<td>200 V</td>
<td>20 A</td>
<td>1.5 V</td>
</tr>
</tbody>
</table>

Select one MOSFET and one diode which will work best in this converter. Explain why you.

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6.3.1. Full-bridge and half-bridge isolated buck converters

**Full-bridge isolated buck converter**

![Full-bridge isolated buck converter diagram]
Full Bridge Switch Structure

- During first switching period: transistors \( Q_1 \) and \( Q_2 \) conduct for time \( DT_t \), applying volt-seconds \( V \times DT_t \) to primary winding
- During next switching period: transistors \( Q_3 \) and \( Q_4 \) conduct for time \( DT_t \), applying volt-seconds \( -V \times DT_t \) to primary winding
- Transformer volt-second balance is obtained over two switching periods
- Effect of nonidealities?
Effect of nonidealities on transformer volt-second balance

Volt-seconds applied to primary winding during first switching period:

\[ (V_{f1} - (O_1 + O_2 \text{ forward voltage drops})) \times O_1 \text{ conduction time} \]

Volt-seconds applied to primary winding during next switching period:

\[ -(V_{f2} - (O_2 + O_3 \text{ forward voltage drops})) \times O_2 \text{ conduction time} \]

These volt-seconds never add to exactly zero.

Net volt-seconds are applied to primary winding

Magnetizing current slowly increases in magnitude

Saturation can be prevented by placing a capacitor in series with primary, or by use of current programmed mode (Chapter 12)

Operation of secondary-side diodes

- During second \((T/2)\) subinterval, both secondary-side diodes conduct
- Output filter inductor current divides approximately equally between diodes
- Secondary amp-turns add to approximately zero
- Essentially no net magnetization of transformer core by secondary winding currents
Volt-second balance on output filter inductor

\[ V = \{v_i\} \quad \Rightarrow \quad \langle v_i \rangle = \forall \text{ conducting devices:} \]

\[ V = nDV_{g} \]

\[ M(D) \leq nD \quad \text{buck converter with turns ratio} \]

Half-bridge isolated buck converter

- Replace transistors \( Q_3 \) and \( Q_4 \) with large capacitors
- Voltage at capacitor centerpoint is \( 0.5V_g \)
- \( v_i(t) \) is reduced by a factor of two
- \( M = 0.5nD \)

\[ \langle v_i \rangle = \frac{D(V_g - V_{b})}{2} + \frac{D(D - V_{b})}{2} \]
6.3.3. Push-pull isolated buck converter

\[ V = nDV \]

0 ≤ D ≤ 1

Waveforms: push-pull

- Used with low-voltage inputs
- Secondary-side circuit identical to full bridge
- As in full bridge, transformer volt-second balance is obtained over two switching periods
- Effect of nonidealities on transformer volt-second balance?
- Current programmed control can be used to mitigate transformer saturation problems. Duty cycle control not recommended.
6.3.2. Forward converter

- Buck-derived transformer-isolated converter
- Single-transistor and two-transistor versions
- Maximum duty cycle is limited
- Transformer is reset while transistor is off

Forward converter
with transformer equivalent circuit
Forward converter: waveforms

- Magnetizing current, in conjunction with diode $D_1$, operates in discontinuous conduction mode.
- Output filter inductor, in conjunction with diode $D_2$, may operate in either CCM or DCM.

Subinterval 1: transistor conducts

- $D_{on}$
- $D_{off}$
- $i_1 = \frac{v_{in}}{R}$
- $i_2 = \frac{v_{out}}{R}$
- $i_3 = \frac{v_{out}}{R}$
- $i_4 = \frac{v_{out}}{R}$

- $D < 0.5$ for transformer reset.
Subinterval 2: transformer reset

\[ V_g \]

\[ n_1 : n_2 : n_3 \]

\[ i_M \]

\[ v_{R1} = v_2 \]

\[ L \]

\[ D_1 \text{ off} \]

\[ D_2 \text{ off} \]

\[ i_L = \frac{i_M}{i_1} \]

\[ v_3 = v_2 - v_g \]

\[ n_1 = n_2 \]

\[ D_3 \text{ on} \]

\[ v_{R3} \]

\[ C \]

\[ R \]

\[ V \]

Subinterval 3

\[ V_g \]

\[ L \]

\[ Q_1 \text{ off} \]

\[ D_1 \text{ off} \]

\[ n_1 : n_2 : n_3 \]
Magnetizing inductance volt-second balance

\[ \langle v_t \rangle = D\{V_s\} + D_3(-V_n/n_2) + D_4(0) = 0 \]

Transformer reset

From magnetizing current volt-second balance:

\[ \langle i_M \rangle = D\{V_s\} + D_3(-V_n/n_2) + D_4(0) = 0 \]

Solve for \( D_3 \):

\[ D_3 = \frac{n_2}{n_1} \cdot D \]

\( D_3 \) cannot be negative. But \( D_3 = 1 - D - D_2 \). Hence

\[ D_3 = 1 - D - D_2 \geq 0 \]

\[ D_3 = 1 - D \left(1 + \frac{n_2}{n_1}\right) \geq 0 \]

Solve for \( D \):

\[ D \leq \frac{1 - \frac{n_2}{n_1}}{1 + \frac{n_2}{n_1}} \quad \text{for} \quad n_1 = n_2; \quad D \leq \frac{1}{2} \]
What happens when $D > 0.5$

magnetizing current waveforms, for $n_1 = n_2$

Conversion ratio $M(D)$

$\langle v_{D3} \rangle = V = \frac{n_3}{n_1} DV_s$
Maximum duty cycle vs. transistor voltage stress

Maximum duty cycle limited to

\[ D \leq \frac{1}{1 + \frac{n_2}{n_1}} \]

which can be increased by increasing the turns ratio \( n_1 \) / \( n_2 \). But this increases the peak transistor voltage:

\[ \max(v_{qi}) = V_s \left( 1 + \frac{n_1}{n_2} \right) \]

For \( n_1 = n_2 \):

\[ D \leq \frac{1}{2} \quad \text{and} \quad \max(v_{qi}) = 2V_s \]

The two-transistor forward converter

\[ V = nDV_s \quad D \leq \frac{1}{2} \quad \max(v_{qi}) = \max(v_{q2}) = V_s \]
Chapter 5. The Discontinuous Conduction Mode

5.1. Origin of the discontinuous conduction mode, and mode boundary
5.2. Analysis of the conversion ratio $M(D, K)$
5.3. Boost converter example
5.4. Summary of results and key points

Introduction to Discontinuous Conduction Mode (DCM)

- Occurs because switching ripple in inductor current or capacitor voltage causes polarity of applied switch current or voltage to reverse, such that the current- or voltage-unidirectional assumptions made in realizing the switch are violated.
- Commonly occurs in dc-dc converters and rectifiers, having single-quadrant switches. May also occur in converters having two-quadrant switches.
- Typical example: dc-dc converter operating at light load (small load current). Sometimes, dc-dc converters and rectifiers are purposely designed to operate in DCM at all loads.
- Properties of converters change radically when DCM is entered:
  - $M$ becomes load-dependent
  - Output impedance is increased
  - Dynamics are altered
  - Control of output voltage may be lost when load is removed
5.1. Origin of the discontinuous conduction mode, and mode boundary

Buck converter example, with single-quadrant switches

Minimum diode current is \( (I - \Delta I_d) \)
Dc component \( I = V/R \)
Current ripple is \( \Delta I_d = \frac{(V_s - V)}{2L} DT = \frac{V_s DDT}{2L} \)
Note that \( I \) depends on load, but \( \Delta I_d \) does not.

Reduction of load current

Increase \( R \), until \( I = \Delta I_d \)
Minimum diode current is \( (I - \Delta I_d) \)
Dc component \( I = V/R \)
Current ripple is \( \Delta I_d = \frac{(V_s - V)}{2L} DT = \frac{V_s DDT}{2L} \)
Note that \( I \) depends on load, but \( \Delta I_d \) does not.
Further reduce load current

Increase $R$ some more, such that $I < \Delta I_i$.

Dc component $I = \frac{V}{R}$

Current ripple is $\Delta I_i = \frac{(V_i - V)}{2L} D T_i = \frac{V_i D T_i}{2L}$

Note that $I$ depends on load, but $\Delta I_i$ does not.

The load current continues to be positive and non-zero.

Mode boundary

Boundary

@ $I = 0$

- $I > \Delta I_i$ for CCM
- $I < \Delta I_i$ for DCM

Insert buck converter expressions for $I$ and $\Delta I_i$:

\[ \frac{DV_i}{R} \leq \frac{DDT_i V_i}{2L} \leq \Delta I_i \]

Simplify:

\[ \frac{2L}{R} \leq D \]

This expression is of the form

\[
\begin{cases}
  K < K_{op}(D) & \text{for DCM} \\
  K = \frac{2L}{R} \quad \text{and} \quad K_{op}(D) = D' 
\end{cases}
\]

where $K$ is unallowed parameter

as $L \downarrow \frac{1}{R}$

$D$ closer to DCM

as $\frac{1}{L} \downarrow \frac{R}{D}$

$D$ further from DCM

as $R \downarrow \frac{1}{R}$
**Critical load resistance** \( R_{\text{crit}} \)

Solve \( K_{\text{crit}} \) equation for load resistance \( R \):

\[
R \begin{cases} < R_{\text{crit}}(D) & \text{for CCM} \\ > R_{\text{crit}}(D) & \text{for DCM} \end{cases}
\]

where

\[
R_{\text{crit}}(D) = \frac{2L}{DT_e}
\]
Summary: mode boundary

\[ K > K_{m1}(D) \quad \text{or} \quad R < R_{m1}(D) \quad \text{for CCM} \]
\[ K < K_{m2}(D) \quad \text{or} \quad R > R_{m2}(D) \quad \text{for DCM} \]

<table>
<thead>
<tr>
<th>Converter</th>
<th>( K_{m1}(D) )</th>
<th>( \max_{D \in [0,1]} (K_{m1}) )</th>
<th>( R_{m1}(D) )</th>
<th>( \min_{R \in \mathbb{R}^+} (R_{m1}) )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Buck</td>
<td>((1 - D))</td>
<td>(1)</td>
<td>((1 - D)T)</td>
<td>(\frac{2L}{I})</td>
</tr>
<tr>
<td>Boost</td>
<td>(D(1 - D)^2)</td>
<td>(\frac{4}{27})</td>
<td>(D(1 - D)^2T)</td>
<td>(\frac{22}{7} \frac{L}{I})</td>
</tr>
<tr>
<td>Back-boost</td>
<td>((1 - D)^2)</td>
<td>(1)</td>
<td>(\frac{2L}{(1 - D)^2T})</td>
<td>(\frac{2L}{I})</td>
</tr>
</tbody>
</table>

5.2. Analysis of the conversion ratio \(M(D,K)\)

Analysis techniques for the discontinuous conduction mode:

- Inductor volt-second balance:
  \[ \langle v_i \rangle = \frac{1}{T} \int_0^T v_i(t) \, dt = 0 \]

- Capacitor charge balance:
  \[ \langle i_C \rangle = \frac{1}{C} \int_0^C i_C(t) \, dt = 0 \]

Small ripple approximation sometimes applies:

- \(v(t) = V\) because \(\Delta v \ll V\)
- \(i(t) = I\) is a poor approximation when \(\Delta i > I\)

Converter steady-state equations obtained via charge balance on each capacitor and volt-second balance on each inductor. Use care in applying small ripple approximation.
Example: Analysis of DCM buck converter $M(D,K)$