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Office Phone: 865-974-5442
Class: Tu, Th 2:10-3:25 in Min Kao 405
Office Hours: Tuesday 10:00-11:00 am 
and by appointment

**Recommended Textbook**

Addison-Wesley, March 11, 2010

**Prerequisites**

Familiarity with digital VLSI design and Cadence IC design tools comparable to that obtained in ECE 433/533. If you feel that your background knowledge may be insufficient, please see the instructor. In many cases it will be possible to acquire sufficient familiarity with the tools by working through some additional tutorial material.

**Homework**

Homework will be assigned and graded. The primary purpose of the homework assignments is to help you master the concepts and practice applying them. In this class, homework will be distinguished from the project by the criteria of having a known solution. Homework assignments will vary in scale from fairly simple problems from the textbook (e.g. drawing a schematic of a particular adder topology) to a larger design problem (e.g. designing an SRAM). In this sense, the “Homeworks” may at times seem similar to “Projects” from other classes.

Discussion of the homework problems is allowed and encouraged, but copying of homework is cheating. The work you turn in must be your own.

**Final Project**

Projects will be performed using the CAD tools available on department servers. Reports must be typed or word-processed. Correct spelling and grammar, clear descriptions, and readable figures are expected.

**CAD Presentations**

A large component of the class is learning CAD techniques to increase productivity in IC design and automate certain tasks. Many of these techniques will be covered in a student-led arrangement. Each topic will be assigned to a student or team of students, who will then investigate the topic and develop materials to demonstrate the method to the rest of the class through both an in-class presentation and a tutorial in document or video form to be posted to the class wiki. The “CAD Presentations” component of the course grade listed below includes the content delivered, the thoroughness with
which the topic is addressed, and the quality and clarity of the in-class presentation and web-based documentation.

**Grading**

<table>
<thead>
<tr>
<th>Component</th>
<th>Percentage</th>
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<tbody>
<tr>
<td>Project 1</td>
<td>15%</td>
</tr>
<tr>
<td>Project 2</td>
<td>25%</td>
</tr>
<tr>
<td>CAD Presentations</td>
<td>30%</td>
</tr>
<tr>
<td>Homework</td>
<td>15%</td>
</tr>
<tr>
<td>Journal Paper Report</td>
<td>5%</td>
</tr>
<tr>
<td>Participation</td>
<td>10%</td>
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<tr>
<td><strong>Total</strong></td>
<td><strong>100%</strong></td>
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</tbody>
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Grading scale: A(≥90%), B+(86 to 89%), B(80 to 85%), C+(76 to 79%), C(70 to 75%), D(60 to 69%), F(<60%).

**Late Assignments**

Homework assignments and project reports are due at the beginning of class. Late assignments will be penalized 10% per day or fraction thereof. Project reports and homework assignments will not be accepted more than three days late. If unavoidable circumstances require you to turn an assignment in late, contact the instructor as early as possible.

**Notes on the Calendar**

There will be no class October 15th (Fall Break), or November 26th (Thanksgiving). The last day to withdraw with a grade of “W” is November 10th, 2015. The dates given here for topics and exams are tentative. Changes in key dates will be announced in class and by email.

**Academic Integrity**

The EECS Department takes very seriously its obligation to the University and the engineering profession to produce graduates that are trustworthy, ethical, and competent in their field. Therefore, no academic dishonesty of any kind will be tolerated in this class. The typical penalty for cheating will be a failing grade in the class. Egregious cases will be reported to the dean with a recommended penalty of expulsion from the university. See the “Hilltopics” Student Handbook (http://dos.utk.edu/hilltopics) for more information on this matter.

**Students with Disabilities**

Inform the instructor as soon as possible of any special needs that you may have. Please bring in a letter from the Office of Disability Services (http://ods.utk.edu/) to help us find the appropriate accommodations.

**Topics**

Material covered in this class can be roughly divided into two categories: advanced digital VLSI concepts and advanced CAD techniques. The items below constitute a tentative list of the topics within each of those two categories. Based on time and interest we will likely omit some of these topics and we may add others.

**VLSI Concepts**

- Memories (SRAM, DRAM, Flash)
- High-performance data path components (adders, multipliers, others)
• Clock Trees, Synchronization issues
• I/O and Intra-chip communication
• Reliability
• Power distribution
• Low-voltage/subthreshold logic
• Cell library design
• Alternative Logic Families (dynamic, Domino, current-mode, etc.)
• Asynchronous digital Systems
• Design of programmable logic

CAD Techniques

• Basic Synthesis w/ place and route
• Advanced synthesis topics, e.g. optimizing performance, area, power.
• Verilog/VHDL - coding for synthesis
• Mixed-Signal, System-level simulations
• Estimating power
• Semi-automated routing
• Scripting/automating analog layout
• Writing P-Cells
• Scripting simulation
• Automatic logic cell generation
• Automatically characterizing cells/libraries