In the CMOS process of your choice, design the schematic for a 2-input NAND or NOR gate. Create a logical symbol for the gate. Lay out your cell. Follow the guidelines posted on the class web page and use only metal 1 and below for routing within the cell. After the cell is DRC and LVS clean, create a 3-high by 2-wide array of cells tiled together to show that they abut correctly on the top, bottom, and sides. Overlay a grid of M2 and M3 wires on the routing grid that you have chosen; this layout should pass DRC, but no LVS is needed. Then build a schematic and layout for a circuit using three gates to calculate the function $Y = AB + CD$ or $Y = (A + B)(C + D)$. Turn in both schematic and layout for the gate, the array, and the three-gate circuit, and the results from a transient simulation of the three-gate circuit demonstrating correct functionality. Include a table showing the following information: horizontal grid pitch, vertical grid pitch, cell width, cell height.

- Problem 11.2 from W&H.
- Problem 11.7 from W&H.