Due Tuesday October 20, 2015. To be done individually.

1. Continuing with the design of your 128 word \( \times \) 4-bit SRAM, build an HDL model of the SRAM. For this and the next problem only, you may use code scoured from the internet, but do cite anything that you use (including code you modify).

2. Build a test bench for your SRAM. Demonstrate it by testing your model. We will later use this same test bench to verify your SRAM design.

3. Use the Place & Route flow to take the synthesized multiplier design from HW3 and generate a layout. Import the layout back into Cadence and run LVS and DRC. Resolve any errors. Turn in a printout of the layout and the DRC/LVS pass indicators.