ECE692

**Design of a DAB Converter**

In this problem, you will design a 200-to-12V, 120 W dual active bridge converter for power supply applications. The goal is to produce the highest efficiency through selection of the modulation, transistor sizes, and details of the magnetics.

![DAB Converter Diagram](image)

<table>
<thead>
<tr>
<th>Table I: Implementation technology and specification</th>
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<tbody>
<tr>
<td>$r_{on} C_{ds}$</td>
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<td>5 mΩ·nF</td>
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All of the transistors are implemented in a fixed technology node, which exhibits a constant figure of merit $r_{on} C_{ds}$, e.g. doubling the transistor resistance will result in the $C_{ds}$ capacitance reducing by half. The leakage inductance has constant $L/R_L$, e.g. doubling inductance doubles resistance. Core loss of the leakage inductance may be neglected. The transformer has negligible resistance, but exhibits core loss which can be modeled by the Steinmetz Equation,

$$P_{core} = K_{fe} f_s \alpha (\Delta B)^\beta$$

$P_{core}$ is in units of [mW/cm³] for the parameters in Table I and with $f_s$ and $\Delta B$ in units of Hz and T, respectively. The transformer core has effective area $A_c$ and volume $V_e$. The secondary of the transformer always has a single turn. The high efficiency approximation can be used when calculating core loss; all other loss mechanisms should be calculated without approximation.

The output voltage should be 12 V in steady-state. DC error and ripple less than 100 mV may be neglected.

All waveforms in the converter must be consistent with the physical limitations of the topology and devices.

In your design, attempt to achieve the highest efficiency possible. Formal optimization is not required, though you will be assessed on correctness of your analysis and the efficiency it achieves. In addition to your modeled efficiency, select and report

i. The on-resistance of each device
ii. The leakage inductance
iii. The number of primary turns $n_p$ of the transformer
iv. Dead time, phase shift, duty cycle, and any other details of the gate drive waveforms for all devices

Additionally, turn in plot(s) of $v_p(t)$, $v_s(t)$, $i_L(t)$, and $v_{out}(t)$, and details of how you arrived at your design.