Final Project

- Select a dc-dc converter and application, design a closed-loop digital controller
- **Detail**
  - Converter Design (brief, may leverage midterm)
  - Target performance (both large and small-signal)
    - should be aggressive
  - Design and final implementation
- **Design must include**
  - Realistic ADC/PWM models (sampling, delay, quantization)
  - At least two additional nonlinearities (Nonlinear controller, GSS, etc.)
  - At least one technique from an IEEE publication not directly discussed in class
- **Validation must include**
  - Direct comparison between small-signal prediction and large-signal performance
  - Testing over conditions motivating valid operation in a realistic use case
- **Apply techniques from class**
- **Should result in prototype-ready paper design**
- Validate through simulation (PLECs/Simulink)
- **Report Due December 9th**
  - Narrative of analysis and results
  - Clear but minimally “wordy”
  - IEEE format (though incomplete content w.r.t. review and explanation)

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**Frequency Response**

CT: \( G_T(s \rightarrow \omega) = \frac{\omega_0}{\omega s} = -\frac{j \omega_0}{\omega} \)

DT: \( G_T(z \rightarrow e^{j\omega T_z}) = \frac{\omega_0 T_z}{2} \frac{1 + e^{-j\omega T_z}}{1 - e^{-j\omega T_z}} = -\frac{j \omega_0 T_z}{2} \frac{\cos \left( \frac{\omega T_z}{2} \right)}{\sin \left( \frac{\omega T_z}{2} \right)} \)

\( G_T(z \rightarrow e^{j\omega T_z}) = \left( -\frac{j \omega_0 T_z}{2} \frac{1}{\tan \left( \frac{\omega T_z}{2} \right)} \right) \)

for \( \frac{\omega T_z}{2} \ll 1 \)

\( G_T \approx -\frac{j \omega_0 T_z}{2} \frac{1}{\omega^2} = -\frac{j \omega_0}{\omega} \)

Here \( T_z \) is the sampling period.
Mapping Between Domains

Compensator Design Approach

- Find $T_u(z)$ (uncompensated loop gain)
- Map $T_u(z) \rightarrow T_u'(p)$ using $\textcircled{1}$
- Prewarp any frequency specifications using $\textcircled{2}$
- Design $G_c'(p)$ using traditional s-domain tools/analysis
- Map $G_c'(p) \rightarrow G_c(z)$ using $\textcircled{3}$

Pick a $G_c(z)$

Map into template $G_c'(p)$
**Example Design**

![Diagram of Example Design]

\[ \text{DAB (Hw6)} \]

\[
200 \cdot h \cdot 12V \quad 10A \quad \text{In+}
\]

\[
C_0 = 20 \mu F
\]

\[
f = 1 \text{MHz}
\]

\[
L_f = 35 \text{mH}
\]

\[
r_{\text{m, p}} = 50 \text{m} \Omega
\]

\[
r_{\text{m, s}} = 1 \text{m} \Omega
\]

\[
N_p : N_s = 1 : \frac{V_b}{V}
\]

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**Plant Model**

DAB = half-cycle symmetry applies

\[
\Phi = \left( \frac{1}{\pi} e^{A_t \cdot \frac{j}{2}} \right) \Gamma_{HC}
\]

\[
\Gamma = e^{A_u \cdot t} \left( A_s - A_o \right) X_p
\]

\[
\Phi = \begin{bmatrix} 0 & 0 & 0 & 1 \end{bmatrix}
\]

Note: Generalized state space for two dead times, device conduction

\[
0 \geq \sigma(x, u, t, \omega)
\]

\[
\omega = \begin{bmatrix} t \end{bmatrix}
\]

\[
\begin{bmatrix} 0 \end{bmatrix} = \begin{bmatrix} V_p - (-V_b) \\ V_s - (-V_{m, s}) \end{bmatrix}
\]
ADC and PWM Model

ADC: 10-bit \( V_{FS} = 3.3V \) \( t_{CONV} \leq t_1 \)

\[ k_{ADC} = \frac{2^{10}}{3.3} \]

PWM: \( f_{CH} = 200\text{MHz} \)

\[ N_r = \frac{f_{FULL}}{f_0} = 200 \]

\[ K_{PWM} = \frac{T_s}{N_r} \]

Sensing Gain \( H = \frac{1}{10} \) \rightarrow \text{Vout} \rightarrow \text{ADC}

Note: In this case, include filter in plant model.

Loop Gain

\[ T_u(z) = G_{VP}(z) H K_{ADC} K_{PWM} \]