Limit Cycling

\[ V_{out} = \frac{1}{N_{\text{dac}}} \left( \frac{1}{4} \right) \frac{V_{in}}{2} \Rightarrow \frac{1}{4} = \frac{32 \text{mV}}{16} \quad \text{@ 10-bit ADC} \]

\[ V_{out} = \frac{1}{l} \left( \frac{\partial m(t)}{\partial t} \right) \frac{V_{in}}{2} \Rightarrow \text{solve DAC steady-state @ ty} \]

\[ \Rightarrow \frac{3.07V}{64} \]

for new limit cycling we want

\[ 8_{\text{in}} \text{ must be } \leq 8_{\text{out}} \]

\[ \text{Need 100x change in} \]

Assume use of Hybrid DRAM w/ 64 delay elements

\[ N_{t} = 200 \cdot 64 \]

\[ \text{& Drop ADC to 9-bits, } N_{\text{adc}} = 9 \]

\[ V_{out} = 64 \text{mV} \Rightarrow V_{\text{out}} = \frac{3.07}{64} = 48 \text{mV} \]

New Compensator

GLD

Bode Diagram

Magnitude (dB)

Phase (deg)

Frequency (Hz)

Bode Diagram

Magnitude (dB)

Phase (deg)

Frequency (Hz)

\[ N_{\text{adc}} = 9 \quad N_{t} = 128 \cdot 64 \]

New

\[ k_2 = 22 \]

\[ k_2 = 435.5 \]
High Res Modulator

integral Gain

No limit cycling condition: $P_{error} \& k_i \leq 1$

$\Rightarrow \text{set } k_i > 1$
New Compensator

Low Ki
Low Ki

Anti-Windup (Not actually a problem in previous show)