Switching Loss Estimation in a Buck-Boost Converter

The noninverting buck-boost converter of Fig. 1 is switched using the given logic-level signals, $s_1$ and $s_2$. The topology is used to design a power converter with the following characteristics:

- Input voltage $V_g = 400$ V
- Output voltage $V = 200$ V
- Output resistance $R = 40$
- Switching frequency $f_s = 500$ kHz

All devices, $M_1$-$M_4$, are implemented with a silicon MOSFET. Its parasitics are summarized in the attached datasheet. Note that, as with all datasheets, not all of the information contained is explicitly necessary for the calculations here. Consider a “slow” gate driver with $V_{GS} = 10$ V and $I_g = 1$ A. Both $L$ and $C_{out}$ are large. The dead times are longer than any switching transient dynamics, but you may assume that $t_{d1} + t_{d2} \ll T_s$.

a) Neglecting all nonidealities and losses, solve for the converter duty cycle $D$, which is the portion of each switching period in which $s_1$ is high.

b) Solve for the conduction loss due to devices’ on-resistance.

c) Sketch the drain-to-source voltage, gate-to-source voltage, and drain current of the following MOSFETs during the specified transition. Label all salient features

   i) $M_1$ turn on
   ii) $M_3$ turn on

d) Solve for the total switching loss due to (if applicable)

   i) device output capacitance $C_{oss}$
   ii) $v-i$ overlap due to the gate drive
   iii) gate switching
   iv) reverse recovery of the devices’ body diodes

e) Solve for the total power dissipation of each individual device, $M_1$-$M_4$

f) Estimate the power required from a 10 V auxiliary supply for this circuit.