Overlap Time

9 Typ. gate charge

\[ V_{GS} = f(Q_{gate}); I_D = 5.2 \text{ A pulsed} \]

parameter: \( V_{DD} \)

<table>
<thead>
<tr>
<th>Gate threshold voltage</th>
<th>( V_{GS(th)} )</th>
<th>( V_{DS(th)} V_{GS(th)}, I_D = 0.34 \text{ mA} )</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>2.5</td>
<td>3</td>
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<td>3</td>
<td>3.5</td>
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</table>

<table>
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<tr>
<th>Gate resistance ( R_C )</th>
<th>( f = 1 \text{ MHz, open drain} )</th>
<th>-</th>
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</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>1.6</td>
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<td>( \Omega )</td>
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</tbody>
</table>

- Graph showing \( V_{GS} \) vs. \( Q_{gate} \)
- Circuit diagram with \( V_{DC} \) and \( I_L \)
FET Turn-On
Device Transconductance
Example Simulation

.ic V(g) = 0
.tran 0 50n 0 1p

I=IF(V(g)<10,1,0)

.model myD D(n=.01)
.model testFET VDMOS(Rg=.1 Rd=0 Rs=0 Vto=3 Kp=9 Cgdmax=0p + Cgdm=0p Cgs=0p Cjo=1.5f Is=26p Rb=0m Vds=600 Ron=385m Qg=0n)
Simulation Waveforms – Turn On

- V(g)
- V(sw)
- Id(Mn1)+I(Cgd)
- I(Cgs)
- -I(Cgd)
Turn-Off Transition
Turn-off

The graph shows the voltage and current changes over time during the turn-off process. The graph includes:

- Voltage (V(g)) with a range from 10V to 0V.
- Switch voltage (V(sw)) with a range from 360V to 0V.
- Drain current (I_d(Mn1) + I(Cgd)) with a range from 1.1A to 0.1A.
- Source current (-I(Cgs)) with a range from 1.0A to 0.0A.
- Gate current (I(Cgd)) with a range from 1.0A to 0.0A.

The time axis ranges from 0ns to 20ns.
Turn-Off (Drain Dominated)
Gate- vs. Drain-Limited Switching
Simulation Results: $C_{ds}$ Sweep
Limitations on Switching Speed