Simulation Modeling

Circuit Simulation

• LTSpice
  – Other tools accepted, but not supported
• Choose model type (switching, averaged, dynamic)
• Supplement analytical work rather than repeating it
• Show results which clearly demonstrate what matches and what does not with respect to experiments (i.e. ringing, slopes, etc.)
LTSpice Modeling Examples

- Example files added to course materials page
  - Custom model
  - VDMOS model
  - Manufacturer Model

Custom Transistor Model

```plaintext
.model myD D(n=.001)
.model mySw SW(Ron=10m Roff=1G Von=1 Voff = .5 )
```

![Custom Transistor Model Diagram]
VDMOS Model

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
<th>Units</th>
<th>Default</th>
<th>Example</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vto</td>
<td>Threshold voltage</td>
<td>V</td>
<td>0</td>
<td>1.0</td>
</tr>
<tr>
<td>Kp</td>
<td>Transconductance parameter</td>
<td>A/V²</td>
<td>1.</td>
<td>.5</td>
</tr>
<tr>
<td>phi</td>
<td>Surface inversion potential</td>
<td>V</td>
<td>0.6</td>
<td>0.65</td>
</tr>
<tr>
<td>Lambda</td>
<td>Channel-length modulation</td>
<td>1/V</td>
<td>0.</td>
<td>0.02</td>
</tr>
<tr>
<td>mtriode</td>
<td>Conductance multiplier in triode region(allow independent fit of triode and saturation regions)</td>
<td></td>
<td>1.</td>
<td>2.</td>
</tr>
<tr>
<td>subthres</td>
<td>Current(pert volt) Vds) to switch from square law to exponential subthreshold conduction</td>
<td>A/V</td>
<td>0.</td>
<td>1n</td>
</tr>
<tr>
<td>BV</td>
<td>Vds breakdown voltage</td>
<td>V</td>
<td>Infin.</td>
<td>40</td>
</tr>
<tr>
<td>IBV</td>
<td>Current at Vds=BV</td>
<td>A</td>
<td>100µA</td>
<td>1µ</td>
</tr>
<tr>
<td>HUV</td>
<td>Vds breakdown emission coefficient</td>
<td></td>
<td>1.</td>
<td>10</td>
</tr>
<tr>
<td>Rd</td>
<td>Drain ohmic resistance</td>
<td>Ω</td>
<td>0.</td>
<td>1.</td>
</tr>
<tr>
<td>Rs</td>
<td>Source ohmic resistance</td>
<td>Ω</td>
<td>0.</td>
<td>1.</td>
</tr>
<tr>
<td>Rg</td>
<td>Gate ohmic resistance</td>
<td>Ω</td>
<td>0.</td>
<td>2.</td>
</tr>
<tr>
<td>Rs2</td>
<td>Drain-source shunt resistance</td>
<td>Ω</td>
<td>Infin.</td>
<td>10MΩ</td>
</tr>
<tr>
<td>Rb</td>
<td>Body diode ohmic resistance</td>
<td>Ω</td>
<td>0.</td>
<td>.5</td>
</tr>
<tr>
<td>Cio</td>
<td>Zero-bias body diode</td>
<td>F</td>
<td>0.</td>
<td>1n</td>
</tr>
</tbody>
</table>

Note: any other parameters ignored
- E.g. ron = 3m Qg = 1n mfg = Infineon

Manufacturer Device Model

- Text-only netlist model of device including additional parasitics and temperature effects
- May slow or stop simulation if timestep and accuracy are not adjusted appropriately
Full Switching Simulation

```
.model myMOS VDMOS(Rg=1 Vto=4.5 Rd=14m Rs=10m Rb=17m Kp=30 Cgdmax=.5p Cgdmn=.05n Cgs=.2n Cjo=.03n Is=88p)
.lib switch.lib
.tran 1
.ic V(out)=0
.ic I(L1)=0
```

```
R7 10  
M2 myMOS
L1 L
V1  
U1  
R8 10
M1 myMOS
C1 C
R2 R
```

Component Attribute Editor

- **Prefix**: X
- **InstName**: U1
- **SpaceModel**: GateDrive_GDLphse
- **Value**:  
- **Value2**: 
  - **SpaceLine**: Vbh=5 Tau1=10 Tau2=10 T1=1000 pW=1
  - **SpaceLine2**:  

This is the fourth attribute to appear on the notlist line.
Full Switching Model

- Gives valuable insight into circuit operation
  - Understand expected waveforms
  - Identify discrepancies between predicted and experimental operation
- Slow to simulate; significant high frequency content
- Cannot perform AC analysis
Averaged Switch Modeling: Motivation

• A large-signal, nonlinear model of converter is difficult for hand analysis, but well suited to simulation across a wide range of operating points
• Want an averaged model to speed up simulation speed
• Also allows linearization (AC analysis) for control design

Nonlinear, Averaged Circuit

\[
L \frac{d\langle i_L \rangle}{dt} = \langle v_{bat} \rangle - (1 - d)\langle v_{bus} \rangle
\]

\[
C \frac{d\langle v_{bus} \rangle}{dt} = (1 - d)\langle i_L \rangle - \langle i_{bus} \rangle
\]

for simulation: no need to linearize.
Implementation in LTSpice

Averaged Switch Model
What known error(s) will be present in loss predictions with this model?
Experiment 4: Closed-Loop Boost

Experiment 3: Open Loop

Experiment 4: Closed Loop

Current Control

Current Controller:
Regulate $i_L(t) =$ control input

Two control loops:
1) Fast (inner) current loop control
   - Not Averaged
2) Slow (outer) voltage loop control
   - Averaged

Effective low-pass filter averaged models can be used when $f \ll f_S$
Averaged vs CPM

Voltage-Mode

Averaged Current-Mode

Current Programmed Mode

Current Programmed Control (CPM)

$P_f$ → current-to-voltage gain of the sensing circuit

$i_{up,k} = i_{f}(0) = i_{ref}$ every period
**Current Programmed Control**

- Covered in Ch. 12 of *Fundamentals of Power Electronics*

- Advantages of current programmed control:
  - Simpler dynamics — inductor pole is moved to high frequency
  - Simple robust output voltage control, with large phase margin, can be obtained without use of compensator lead networks
  - Transistor failures due to excessive current can be prevented simply by limiting \( i_c(t) \)
  - It is always necessary to sense the transistor current, to protect against overcurrent failures
  - Transformer saturation problems in bridge or push-pull converters can be mitigated

- A disadvantage: susceptibility to noise
A Simple First-Order Model

The First-Order Approximation

\[ \langle i_L(t) \rangle_{T_s} = i_c(t) \]

- Neglects switching ripple
- Yields physical insight and simple first-order model
- Accurate when converter operates well into CCM (so that switching ripple is small)
- Accurate when artificial ramp (discussed later) is small
- Resulting small-signal relation:
  \[ i_L(s) \approx i_c(s) \]
Averaged Modeling

Large-Signal Nonlinear Model
Implementation in LTSpice

Averaged, Small-Signal Model

\[
L \frac{d\hat{i}_c}{dt} = \langle V_g \rangle - \hat{d}(t) \langle V \rangle \\
- \text{Replace } i_c = \hat{i}_c \\
- \text{Linearize in Laplace domain}
\]

\[
C \frac{d\hat{v}_s}{dt} = \hat{d}(t)\langle i_e \rangle - \frac{\langle V \rangle}{R}
\]

\[
sL\hat{i}_c = \hat{v}_g + \hat{v}_a - \hat{d}\hat{v}
\]

- \( \hat{d} \) is no longer controlled → eliminate

\[
\hat{d} = \frac{1}{V} (sL\hat{i}_c - \hat{v}_g + \hat{d}\hat{v})
\]
Boost CCM CPM Small-Signal Model

\[ sC\hat{u} = D\frac{\hat{i}_c}{c} - \frac{\hat{u}}{R} - \frac{E_l}{V} \left( sL\hat{i}_c - \hat{V}_y - D\hat{v} \right) \]

\[ sC\hat{u} = \hat{i}_c \left( D' - \frac{E_l}{V} sL \right) + \hat{V}_y \frac{I_c}{V} - \frac{\hat{u}}{R} - \frac{E_l}{V} \frac{\hat{v}}{R} \]

\[ \tau_{\omega t} = D\hat{I}_c \rightarrow \frac{\hat{I}_c}{V} = \frac{\hat{I}_{out}}{D'V} - \frac{\hat{v}}{R} \]

\[ sC\hat{u} = \hat{i}_c \left( D' - \frac{E_l}{V} \frac{sL}{R_0} \right) + \hat{V}_y \frac{1}{DR_0} - \frac{\hat{u}}{R} - \frac{\hat{v}}{R} \]

For Pwm control:
\[ G_{vi} = \frac{\hat{u}_c}{\hat{i}_c} \]

DC Optimal gain:
\[ G_{vi} = D' \left( 1 - \frac{sL}{D'R} \right) \cdot \left( R + \frac{\frac{1}{2}}{R} + \frac{1}{2} \right) \]

Gain:
\[ G_{vi} = \frac{D'R}{2} \cdot \frac{1 - \frac{1}{2}}{1 + \frac{2}{1}} \]

Same RHP zeros as in Gva

Single pole!!
CPM Transfer Functions

Fig. 12.28 Comparison of CPM control with duty-cycle control, for the control-to-output frequency response of the buck converter example.

Voltage Control

* Reminder: this neglects $\text{le}$.
CPM Oscillations for $D > 0.5$

- The current programmed controller is inherently unstable for $D > 0.5$, regardless of the converter topology.
- Controller can be stabilized by addition of an artificial ramp.

Inductor Current Waveform in CCM

Inductor current slopes $m_1$ and $-m_2$:

- Buck converter:
  \[ m_1 = \frac{v_g - v}{L}, \quad -m_2 = -\frac{v}{L} \]
- Boost converter:
  \[ m_1 = \frac{v_g}{L}, \quad -m_2 = \frac{v_g - v}{L} \]
- Buck-boost converter:
  \[ m_1 = \frac{v_g}{L}, \quad -m_2 = \frac{v}{L} \]
Introducing a Perturbation

Change in Inductor Current Over $T_s$

$$\hat{i}_c(t) = m_1 \hat{d}T_s$$
$$\hat{i}_c(T_s) = \hat{i}_c(0) \frac{-m_2}{m_1}$$
$$\hat{i}_c(2T_s) = \hat{i}_c(T_s) \left( \frac{-m_2}{m_1} \right) = \hat{i}_c(0) \left( \frac{-m_2}{m_1} \right)^2$$
$$\hat{i}_c(\eta T_s) = \hat{i}_c(0) \left( \frac{-m_2}{m_1} \right)^\eta$$

$$\lambda = \frac{-m_2}{m_1} = \frac{D}{\bar{D}}$$

need $|\lambda| < 1$ for stability
Example: Unstable operation for $D=0.6$

$$\alpha = -\frac{D}{D'} = \left( -\frac{0.6}{0.4} \right) = -1.5$$

Example: Stable operation for $D=1/3$

$$\alpha = -\frac{D}{D'} = \left( -\frac{1/3}{2/3} \right) = -0.5$$
Stabilization Through Artificial Ramp

Now, transistor switches off when
\[ i_a(dT_s) + i_L(dT_s) = i_c \]
or,
\[ i_L(dT_s) = i_c - i_a(dT_s) \]

if \( i_a > i_c \) \( \rightarrow \) PWM control
if \( i_a < i_c \) \( \rightarrow \) CPM

Final Value of Inductor Current

First subinterval:
\[ \hat{i}_L(0) = -\hat{d}T_s \left( m_1 - m_a \right) \]

Second subinterval:
\[ \hat{i}_L(T_s) = -\hat{d}T_s \left( m_2 - m_2 \right) \]

Net change over one switching period:
\[ \hat{i}_L(T_s) = \hat{i}_L(0) \left( -\frac{m_2 - m_a}{m_1 + m_a} \right) \]

After \( n \) switching periods:
\[ \hat{i}_L(nT_s) = \hat{i}_L((n-1)T_s) \left( -\frac{m_2 - m_a}{m_1 + m_a} \right) = \hat{i}_L(0) \left( -\frac{m_2 - m_a}{m_1 + m_a} \right)^n = \hat{i}_L(0) \alpha^n \]

Characteristic value:
\[ \alpha = -\frac{m_2 - m_a}{m_1 + m_a} \]

\[ |\hat{i}_L(nT_s)| \rightarrow \begin{cases} 0 & \text{when } |\alpha| < 1 \\ \infty & \text{when } |\alpha| > 1 \end{cases} \]
Artificial Ramp: Additional Notes

- For stability, require $|\alpha| < 1$
  \[ \alpha = -\frac{1 - \frac{m_a}{m_2}}{D' + \frac{m_a}{m_2}} \]
- Common choices:
  - $m_a = 0.5 \ m_2$ (stable for all duty cycles)
  - $m_a = m_2$ (deadbeat)
- Artificial ramp decreases sensitivity to noise

More Accurate Models

- The simple models of the previous section yield insight into the low-frequency behavior of CPM converters
- Unfortunately, they do not always predict everything that we need to know:
  - Line-to-output transfer function of the buck converter
  - Dynamics at frequencies approaching $f_s$
- More accurate model accounts for nonideal operation of current mode controller built-in feedback loop
- Converter duty-cycle-controlled model, plus block diagram that accurately models equations of current mode controller
- See Section 12.3 for additional info
More Accurate Model

- Simple model assumes $i_L = i_C$ always
- Accounting for ripple, and artificial ramp weakens this approximation
- Using sampled data modeling

$$\hat{i}_L = \hat{i}_C = \frac{1}{1 + \frac{1}{Q_s} \left(\frac{s}{2\pi f_s/2}\right) + \left(\frac{s}{2\pi f_s/2}\right)^2}$$

Where

$$Q_s = \frac{2}{\pi \left(\frac{2}{1 - \alpha} - 1\right)}$$


Note: Comparison toDatasheet

![Application Information](image)

**Figure 30.** Effect of Initial Perturbation when $dl/di < -1$

$$\alpha = |1 - \frac{1}{K}|$$

The relationship between $dl/di$ and K factor is illustrated in the graphic below.

![Graph](image)

**Figure 31.** $dl/di$ vs K Factor

The absolute minimum value of K is 0.5. When K<0.5, the amplitude of $dl_i$ is greater than the amplitude of $dl_d$ and any initial perturbation results in sub-harmonic oscillation. If K=1, any initial perturbation will be removed in one switching cycle. This is known as one-cycle damping. When $-1 < dl_i/dl_d < 0$, any initial perturbation will be under-damped. Any perturbation will be over-damped when $0 < dl_i/dl_d < 1$. 

The University of Tennessee, Knoxville
Application to Experiment 4

- Complex switching controller
- Read the datasheet first

Startup: Switching
Startup: No Switching

Short-Circuit: Switching
Short-Circuit: No Switching

LM5121: Functionality
Internal Functional Model in LTSpice

- Accuracy/functionality not guaranteed
- Used for insight only

In-Circuit Simulation

```
.model mysw sw(Von=3 Voff=2 Ron=.1 Roff = 1Meg)
.model myMOS VDMOS(Rg=1 Vto=4.5 Rd=14m Rs=10m Rb=17m Kp=30 Cgdmax =.5p Cgdmmin =.05n Cgs=.2n Cjo=.03p Is=88p)
.tran 1 uic
.ic V(out)=0
.ic I(I1)=0
.ic V(ss) =0
```

```plaintext
R9 90k
R10 10k
C1 1mf
R1 10k
R3 10
R4 10
C3 500µf
M1 myMOS
C2 0.005µf
M2 myMOS
D1 100µ
D2 100µ
V3 PULSE(0 5 250m 1p 0 1)
R8 1
R5 97.6k
R6 2.4k
```
Sim Results

A Tip: Debug Internal of Subcircuit
Experiment 4: Gate Driver Selection

Experiment 4: Closing the Loop

• Closed-loop operation in steps
  1. Open-loop operation with LM5121 modulator
     - Requires “tricking” LM5121
  2. Closed-loop current regulation
  3. Closed-loop voltage and current regulation
Open-Loop Operation

Setting the Electronic Load

Low-frequency model

1. Open Loop:
   \[ V = \frac{V_o}{D} \]
   \[ P_{out} = \frac{(V_o/D) \cdot I}{R} \]

2. Current Loop Only
   \[ R = \frac{V_o}{I} \]
   \[ P_{out} = I \cdot V_o \]

3. Voltage \& Current Loop
   \[ V = \text{voltage} \]
   \[ P_{out} = \frac{V_o^2}{R} \]

Be careful with how you set electronic load

Safest: ① & ③ current or resistance

② voltage

Select the highest value for current or voltage.