Nano-power tunable bump circuit using wide-input-range pseudo-differential transconductor

Junjie Lu, Tan Yang, M.S. Jahan and J. Holleman

An ultra-low-power tunable bump circuit is presented. It incorporates a novel wide-input-range tunable pseudo-differential transconductor linearised using the drain resistances of saturated transistors. Measurement results show that the transconductor has a 5 V differential input range with <20% of linearity error. The bump circuit demonstrates tunability of the centre, width and height, consuming 18.9 nW power from a 3 V supply, occupying 988 μm² in a 0.13 μm CMOS process.

Introduction: Circuits with bell-shaped transfer functions are widely used to provide similarity measures in analogue signal processing systems such as pattern classifiers [1, 2], support vector machines [3] and deep learning engines [4]. Such nonlinear radial basis functions can be realised with the classic bump circuit [5]. However, the original implementation lacks the ability to change the width of its transfer function. Variable width can be obtained by pre-scaling the input voltage before connecting to the bump generator. The pre-scaling circuit using multi-input floating gate transistors [1] or a digital-to-analogue converter [3] consumes area and increase the power overhead. In [2, 6], the widths of bump-like circuits are varied by switching binary-sized transistors, but the number of possible widths is limited. A Gaussian function can be directly synthesised by exponentiating the Euclidean distance [7], but this approach can lead to a complex circuit and large area.

In this Letter, we propose implementing a bump circuit by preceding the current correlator [5] with a tunable transconductor to achieve variable width and height. The design of linear transconductors in subthreshold CMOS is challenging as the linear range of a conventional differential pair diminishes with the gate overdrive, and reaches its old CMOS is challenging as the linear range of a conventional transconductor...
The transconductor outputs $I_1$ and $I_2$ are mirrored off chip by two additional PMOSs at nodes $a$ and $b$, omitted in Fig. 1. The differential output currents with different $I_{W}$ are plotted in Fig. 3a with $I_{W} = 2$ nA and balanced input voltage with $V_{cm} = 1.5$ V. The normalised $g_m$ when $I_{W} = 0$ is plotted in Fig. 3b, showing an input range of 5 V with $g_m$ error below 20%, covering almost the entire input common mode range.

The transconductor with $<20\%$ linearity error and bump transfer functions are plotted in Fig. 3, showing variable centre, width and height of $V_{out}$ when $I_{W} = 0$ is plotted in Fig. 3. The offset $V_{o}$ is $1.5$ V, $I_{W} = 4$ nA, respectively. Fig. 4 also demonstrates that parameters are individually tunable.

Fig. 4 Measured bump transfer functions showing variable centre, width, and height

(a) Variable centre
(b) Variable width
(c) Variable height

The nonlinearity can be attributed to the second term in (2), as well as the second-order effects such as the dependence of $g_m$ on $V_{DS}$. It is tolerable in bump generator applications as the bump output itself is an approximation of a highly nonlinear function [1–3, 5, 6]. The offset of about 100 mV is due to the device mismatch and can be calibrated out by utilising floating gate techniques such as that in [12].

The transfer functions of the bump circuit with regard to one input $V_{in2}$ are plotted in Fig. 4, showing variable centre, width and height by varying $V_{in}$, $I_{W}$ and $I_{LB}$, respectively. Fig. 4 also demonstrates that the circuit works properly with unbalanced input.

The one-dimensional (1D) bump output can be extended to higher dimensions to represent multivariate probability distribution by cascading multiple bump circuits, i.e. connecting $I_{LB}$ of one circuit to the $I_{W}$ input of the next circuit. The measured 2D bump output is plotted in Fig. 5. Just as in the 1D case, each dimension’s parameters are individually tunable. To evaluate the computational throughput of the circuit, the step response time is measured. With $I_{W} = I_{LB} = 1$ nA, the output current 95% settling time is 45 μs when the differential input steps from 0 to 1 V.

Table 1 summarises the measured performance of the proposed bump circuit. Compared with other recently reported works, the proposed circuit occupies smaller area and consumes significantly lower power.

| Table 1: Performance summary and comparison |
|---|---|---|---|---|
| This work | [1] | [6] | [?] |
| Technology (μm) | 0.13 | 0.5 | 0.13 | 0.18 |
| Supply voltage (V) | 3 | 3.3 | 1.2 | 0.7 |
| Power | 18.9 mW | 90 μW | 10.5 μW | 485 nW |
| Area (μm²) | 988 | 3444 | 1050 | — |
| Response time (μs) | 45 | 10 | — | 9.6 |

*Simulation results

Conclusion: We present an ultra-low-power tunable bump circuit to provide similarity measures in analogue signal processing. It incorporates a novel transconductor linearised using drain resistances of saturated transistors. We show in the analysis that the proposed transconductor can achieve tunable $g_m$ with a wide-input range. Measurement results demonstrate a 5 V differential input range of the transconductor with $<20\%$ linearity error and bump transfer functions with tunable centre, width and height. We also demonstrate 2D bump outputs by cascading two bump circuits on the same chip.

Acknowledgments: This work was supported by the NSF (grant CCF-1218492) and DARPA (grant HR0011-13-2-016).

© The Institution of Engineering and Technology 2014
20 March 2014
doi: 10.1049/el.2014.0920
One or more of the Figures in this Letter are available in colour online.

Junjie Lu, Tan Yang, M.S. Jahan and J. Holleman (Department of Electrical Engineering and Computer Science, The University of Tennessee, 1520 Middle Drive, Knoxville, TN 37996, USA)
E-mail: jlu9@utk.edu

References


ELECTRONICS LETTERS 19th June 2014 Vol. 50 No. 13 pp. 921–923