An Introduction to the EKV Model and a Comparison of EKV to BSIM

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Overview

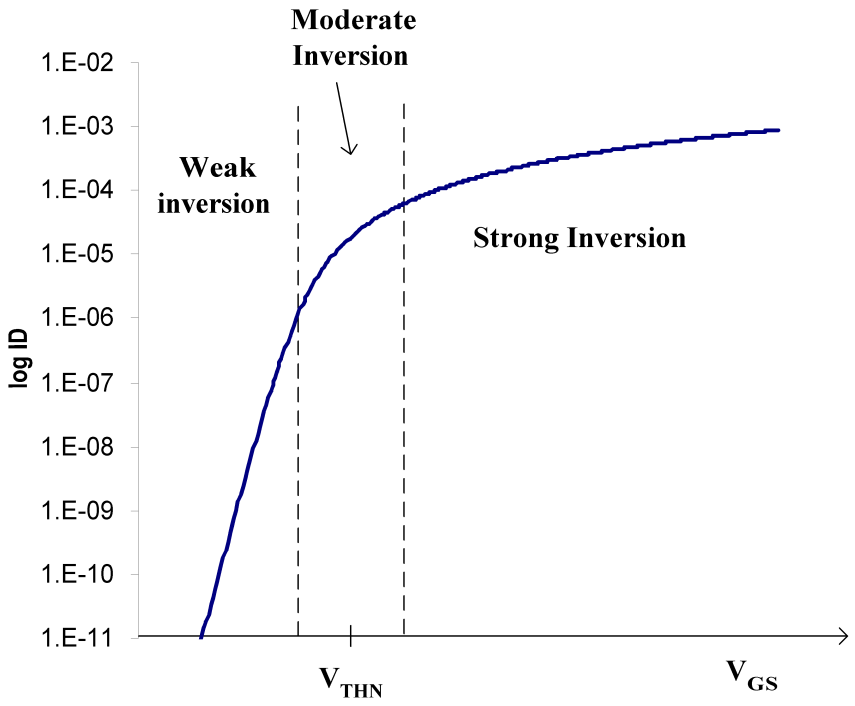
- Characterizing MOSFET operating regions
- EKV model fundamentals
- Sizing MOSFETs using the EKV model
- Comparison of analog performance of BSIM and EKV models

MOSFET Operating Regions

- In analog design, it is critical to understand the different operating regions of the MOS transistor (unless stated otherwise, saturation operation is assumed throughout this discussion)
- The MOS transistor has three distinct operating regions which are defined by the gate–source voltage
  - Weak inversion: $V_{GS} - V_{TH} < -50$ mV
  - Moderate inversion: -50 mV $< V_{GS} - V_{TH} <$ 250 mV
  - Strong Inversion: $V_{GS} - V_{TH} > 250$ mV

MOSFET Operating Regions

- The following plot presents the log I_D–V_{GS} characteristics of a standard MOSFET



MOSFET Operating Regions

- MOSFET characteristics in each operating region (assumes fixed bias current)

Parameter	Weak Inv.	Moderate Inv.	Strong Inv.
g_m	High	Mod.	Low
Area	Large	Mod.	Small
$V_{DS(Sat)}$	Min.(~100 mV)	130 mV – 250 mV	> 250 mV
f_T	Low	Mod.	High
e_n	Low	Mod.	High

MOSFET Operating Regions

- Designers often consider operating regions separately, using different design equations for weak and strong inversion; traditionally no design equations have been available for moderate inversion

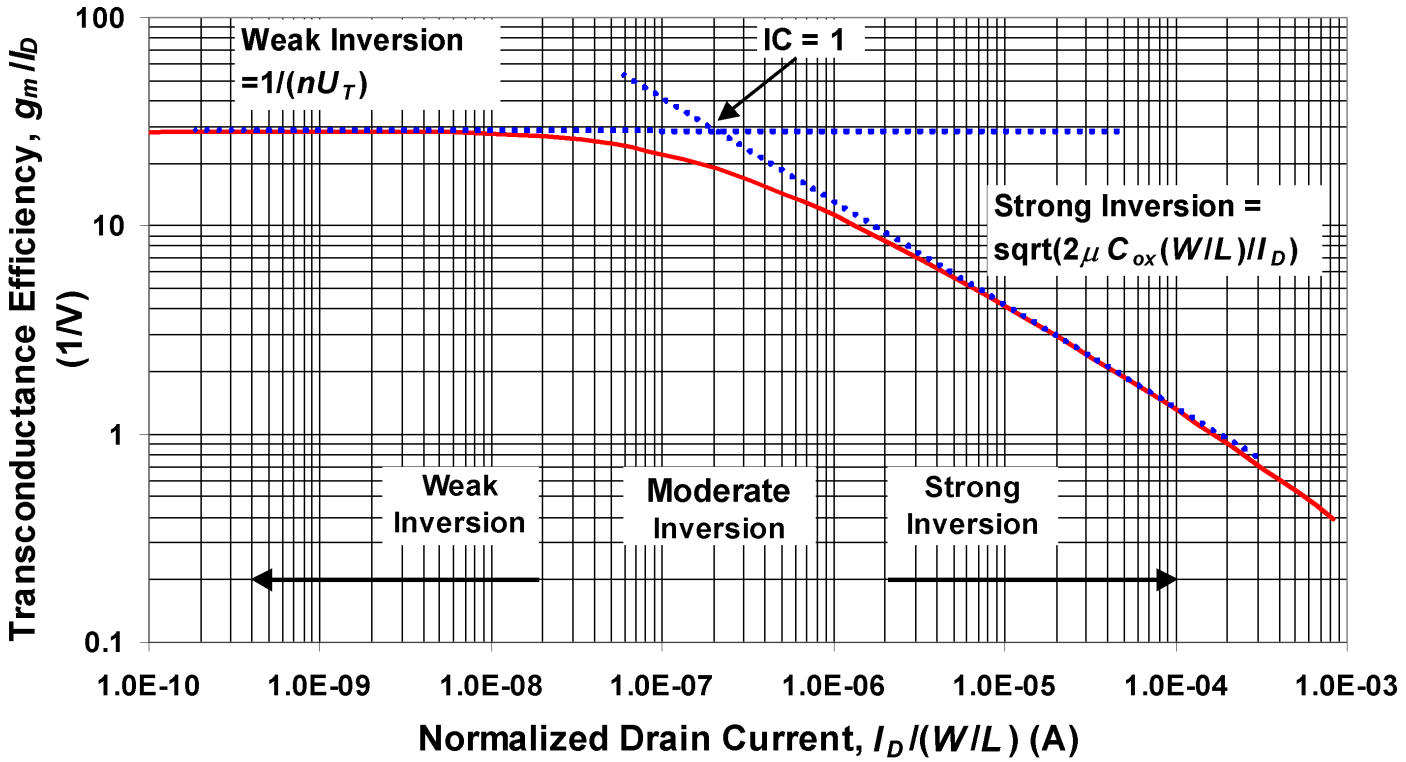
	I_D (assumes V_{BS}=0)	g_m
Weak Inversion	$I_D = 2nmC_{ox}\left(W/L\right)U_T^2 \exp\left(\frac{V_{GS}-V_{TO}}{nU_T}\right)$	$g_m = \frac{I_D}{nU_T}$
Strong Inversion	$I_D = \frac{mC_{ox}}{2}\frac{W}{L}\left(V_{GS}-V_{TO}\right)^2$	$g_m = \sqrt{2mC_{ox}\left(W/L\right)I_D}$

MOSFET Operating Regions

- Transonductance efficiency and inversion coefficient are important concepts for analog CMOS because they
  - Allow the designer to consider MOSFET operation over a continuum of inversion levels
  - Give simple rules for MOSFET sizing in all operating regions: for any combination of W, L, and I_D
  - Allow the designer to explicitly choose an operating region, which is extremely helpful since each operating region has distinct characteristics that may or may not be advantageous for a given application

MOSFET Operating Regions

- g_m-Efficiency vs. Normalized Drain Current



MOSFET Operating Regions

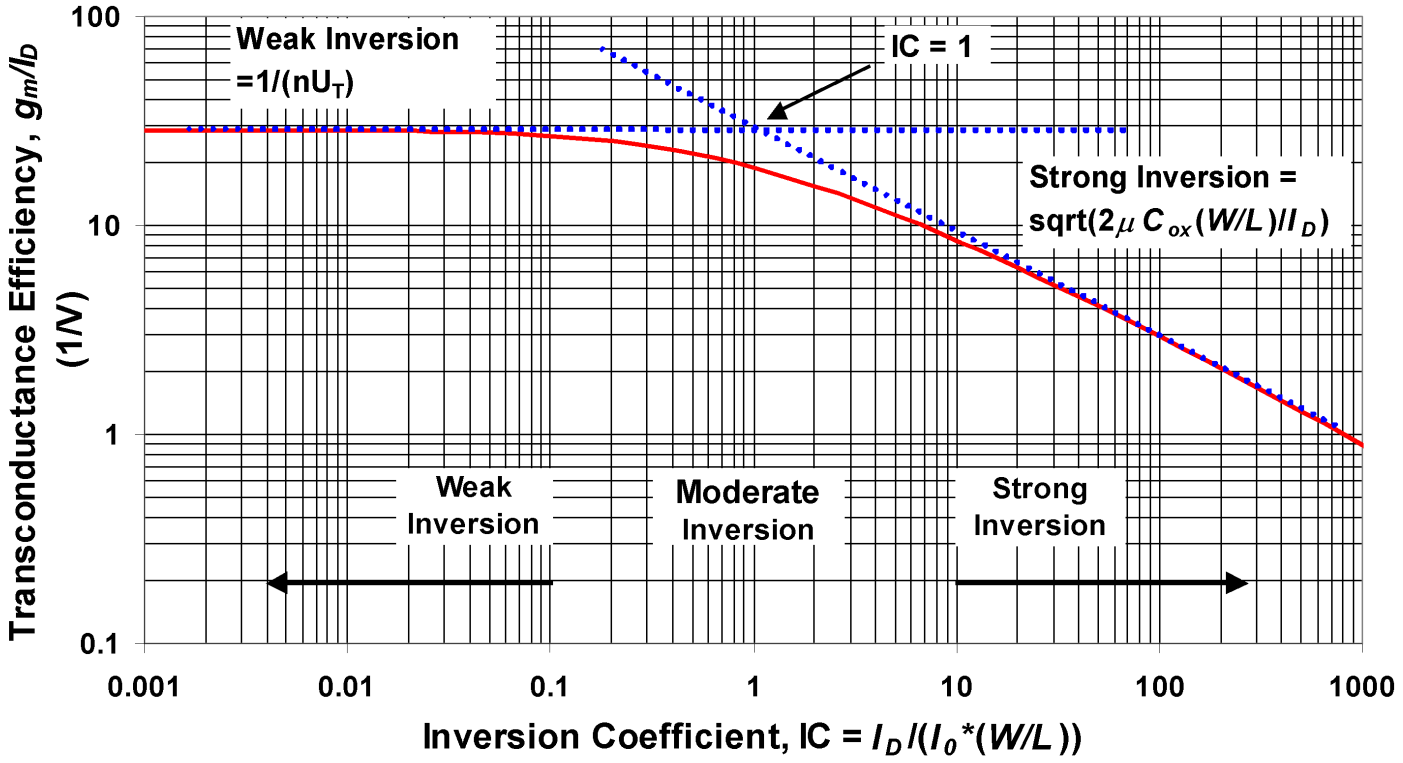
- Mathematically inversion coefficient is defined as

$$IC = \frac{I_d}{I_0\left(W/L\right)} = \frac{I_d}{2mnC_{ox}U_T^2\left(W/L\right)}$$

  - Where I_0 referred to as the technology current and is equal to roughly 250 nA for NMOS devices in a 0.35-µm technology and 100 nA for PMOS devices in a 0.35-µm technology (for another feature size the technology current can be scaled by the ratio $L_{MIN}/0.35$)
- The operating region of the transistor can be found from the inversion coefficient by noting that: IC < 0.1 → W.I., 0.1 < IC < 10 →M.I., IC > 10 → S.I.

MOSFET Operating Regions

- g_m-Efficiency vs. Inversion Coefficient

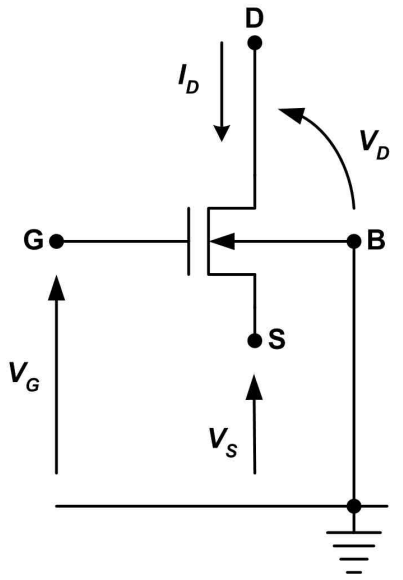


EKV Model Fundamentals

- The Enz Krummenacher Vittoz (EKV) model was introduced in the mid-90's to meet the needs of analog circuit designers
- Currently EKV 2.6 is the most widely used version, and it is supported by most Spice simulators
- EKV is a physics based model that requires only 18 DC parameters
- Major drawback of EKV 2.6: oversimplified formulation of short channel effects (e.g. DIBL)

EKV Model Fundamentals

- The EKV model is unique for several reasons:
  - First, all terminal voltages are referred to the local substrate, thus the inherent device symmetry is maintained.



MOSFET model used in EKV

- Second, EKV defines the drain current as the combination of a forward current controlled by the source, and a reverse current controlled by the drain

$$I_D = I_F - I_R$$

EKV Model Fundamentals

- The drain current is normalized by the so-called specific current

$$i_d = \frac{I_D}{I_S} = i_f - i_r$$

where

$$I_S = 2mnC_{OX}\left(W/L\right)U_T^2$$

is similar to the “technology current” defined by Binkley

- Note that i_f alone is identical to the “inversion coefficient” defined by Vittoz and very similar to the “fixed inversion coefficient” defined by Binkley. Thus, by definition, the inversion coefficient based design technique assumes saturation operation (i.e. $i_r = 0$).

EKV Model Fundamentals

- Finally the normalized MOSFET current is defined over any inversion level using an interpolation function

$$i_f = \left[\ln\left(1 + \exp\left(\frac{v_p - v_s}{2} \right) \right) \right]^2$$

$$i_r = \left[\ln\left(1 + \exp\left(\frac{v_p - v_d}{2} \right) \right) \right]^2$$

where

$$V_P \cong \frac{V_G - V_{TO}}{n}, \quad v_i = \frac{V_I}{U_T}$$

EKV Model Fundamentals

- Several expressions which are useful for circuit design, and which are defined over all operating regions, can be developed using the EKV model

$$v_p - v_s = 2\ln\left(\exp\left(\sqrt{i_f}\right)-1\right)^{*}$$

$$\frac{g_m}{I_F} = \left(\frac{1}{nU_T}\right)\left(\frac{1-\exp\left(-\sqrt{i_f}\right)}{\sqrt{i_f}}\right)^{*}$$

$$V_{DS(Sat)} = 2U_T \ln\left(\frac{\exp\left(\sqrt{i_f}\right)-1}{\exp\left(\sqrt{i_f/a}\right)-1}\right)^{**}, \quad a \cong 25$$

$$f_T \cong \frac{mU_T}{pL^2}\left(\sqrt{1+4i_f}-1\right)^{***}$$

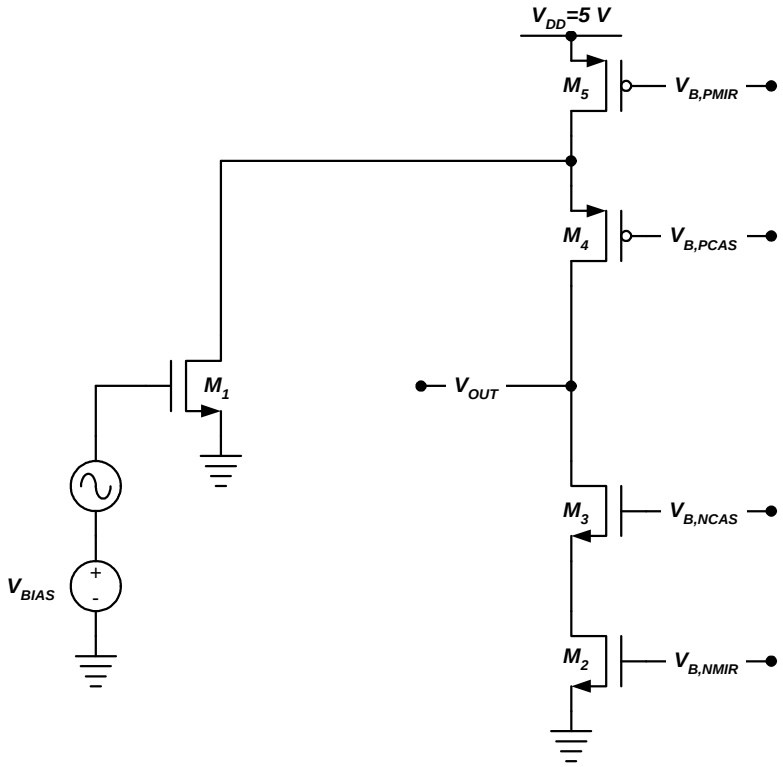
*Enz, Krummenacher, and Vittoz, Analog Integrated Circuits and Signal Processing, 1995.

**Minch, ISCAS, 2002.

***Cunha et al, JSSC, 1998.

Sizing MOSFETs

- One of the most important applications of inversion coefficient is in sizing MOSFETs
- Consider the single-ended amplifier shown below



Sizing MOSFETs

- Design Example: Size the MOSFETs in the previous circuit so that each device is biased in the center of moderate inversion with a current of 20 μA (except M_5 which will have a current of 40 μA)

$$NMOS: IC = 1 = \frac{20\ mA}{(250\ nA)(W/L)} \rightarrow (W/L) = \underline{80}$$

$$PMOS: (W/L) = 2.5(80) = \underline{200}$$

Sizing MOSFETs

- Referring to the previously presented single-ended amplifier, consider the trade-offs in biasing devices in different operating regions
- Assumptions: All devices have a channel length of 1 μm; all devices are biased at the same current, except for M_5 which is biased at twice the nominal current

Sizing MOSFETs

IC	I_{BIAS} (μA)	g_m (μmho)	Output Swing (V)	Total Gate Area $(\mu m)^2$	Non-dominant pole (MHz)
0.01	20	600	4.5	84,000	4
0.1	20	580	4.5	8400	39
1.0	20	380	4.3	840	258
10	20	160	4	84	1085
100	20	60	2.5	8.4	4070

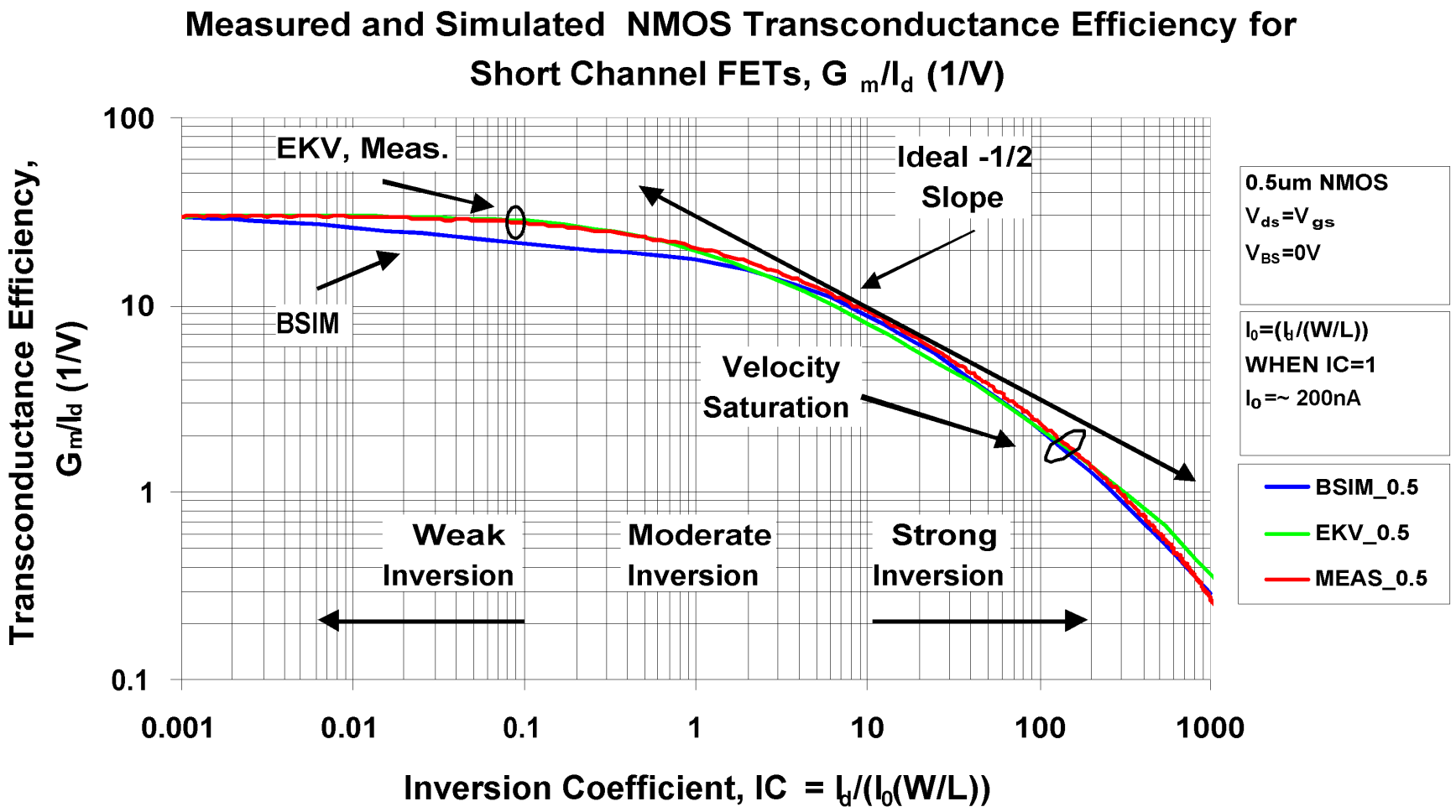
BSIM3V3 Model

- The Berkeley Short-Channel IGFET Model (BSIM) family of models was introduced as a compact model for short channel FETs
- BSIM3V3, currently the most popular version, is generally well suited for analog circuit design
  - BSIM3V3 boasts a very detailed model of output conductance that includes CLM and DIBL
- Major drawback: its highly empirical nature
  - DC model requires nearly 100 parameters

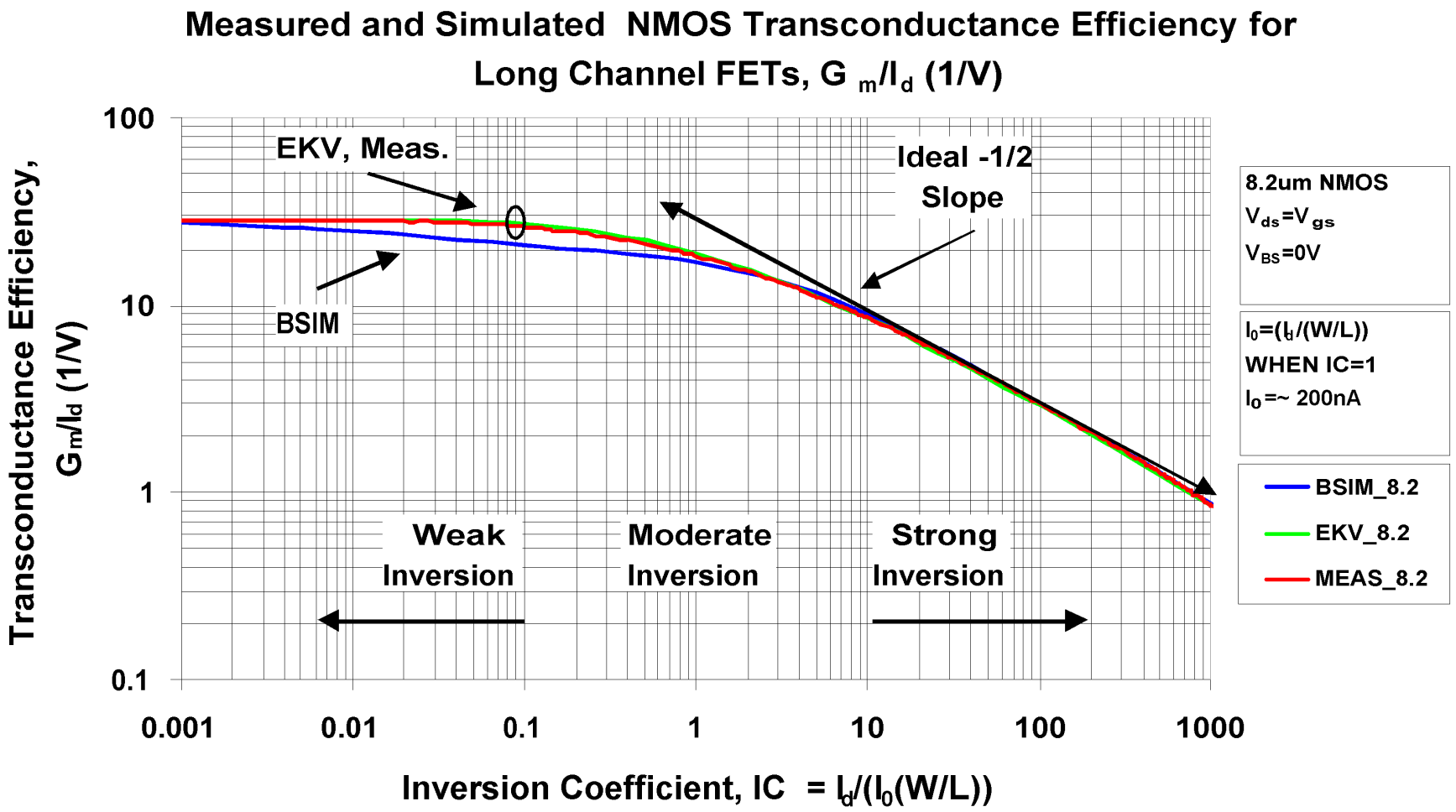
Comparison of BSIM3V3 and EKV2.6

- Transconductance and output conductance were simulated and measured for devices with a wide range of channel lengths (0.5 μm to 33 μm)
- These parameters were chosen because they have a first order effect on several important op-amp characteristics, and because they represent a difficult benchmark for a MOS model
- Measurement and simulation results are shown as a function of inversion coefficient

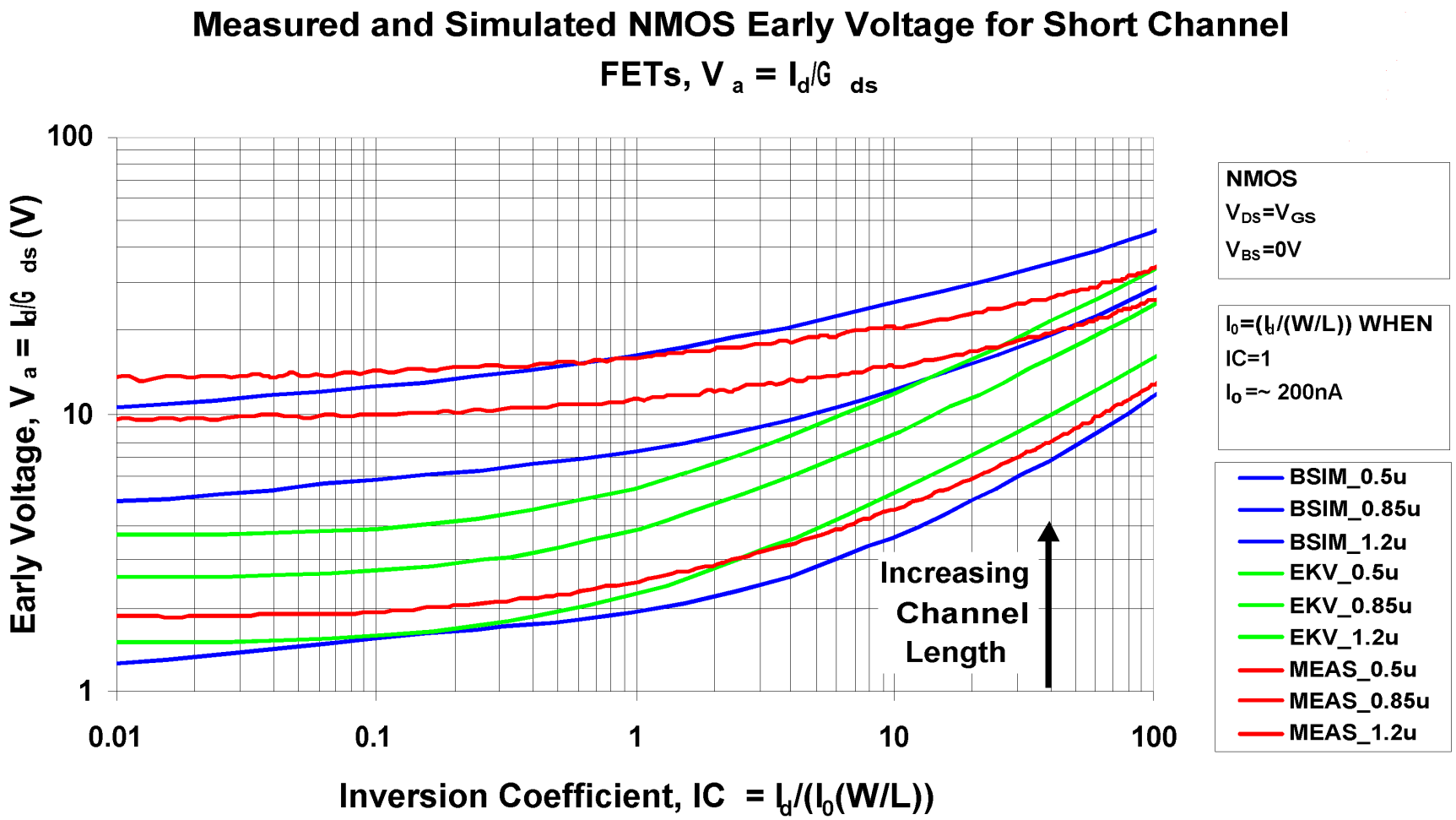
Simulation & Measurement Results



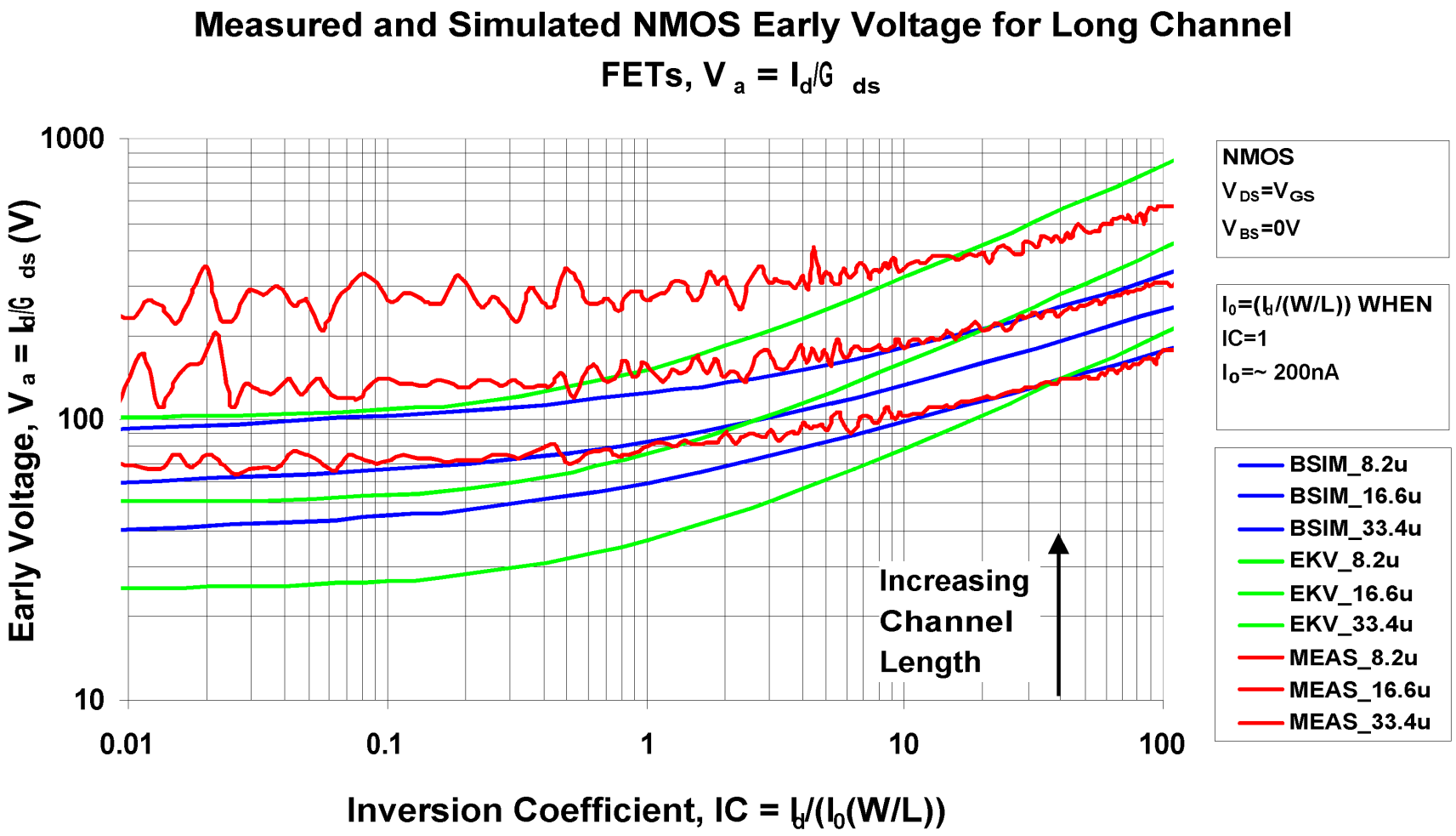
Simulation & Measurement Results



Simulation & Measurement Results



Simulation & Measurement Results



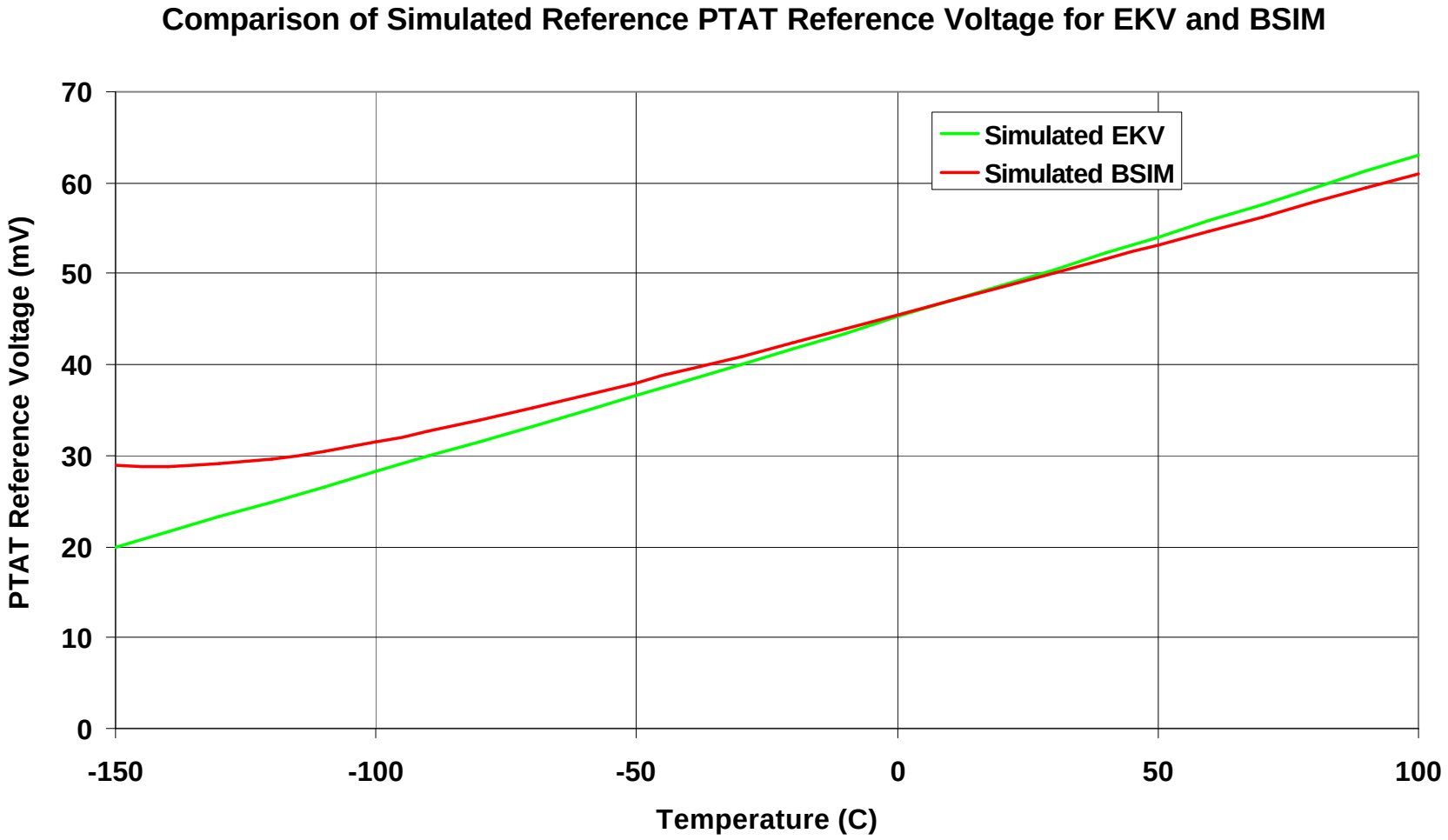
Which model is better?

- This is a loaded question, and you will get different answers based on who's asking.
- One issue that someone will bring up if they don't like the modeling results is that the model is good, but the extraction is bad.
  - This is essentially the nature vs. nurture argument as applied to device modeling, and it is difficult to find an objective answer.
- Also, this is a somewhat academic argument, since you are typically given only one model from the vendor, and you must use this.

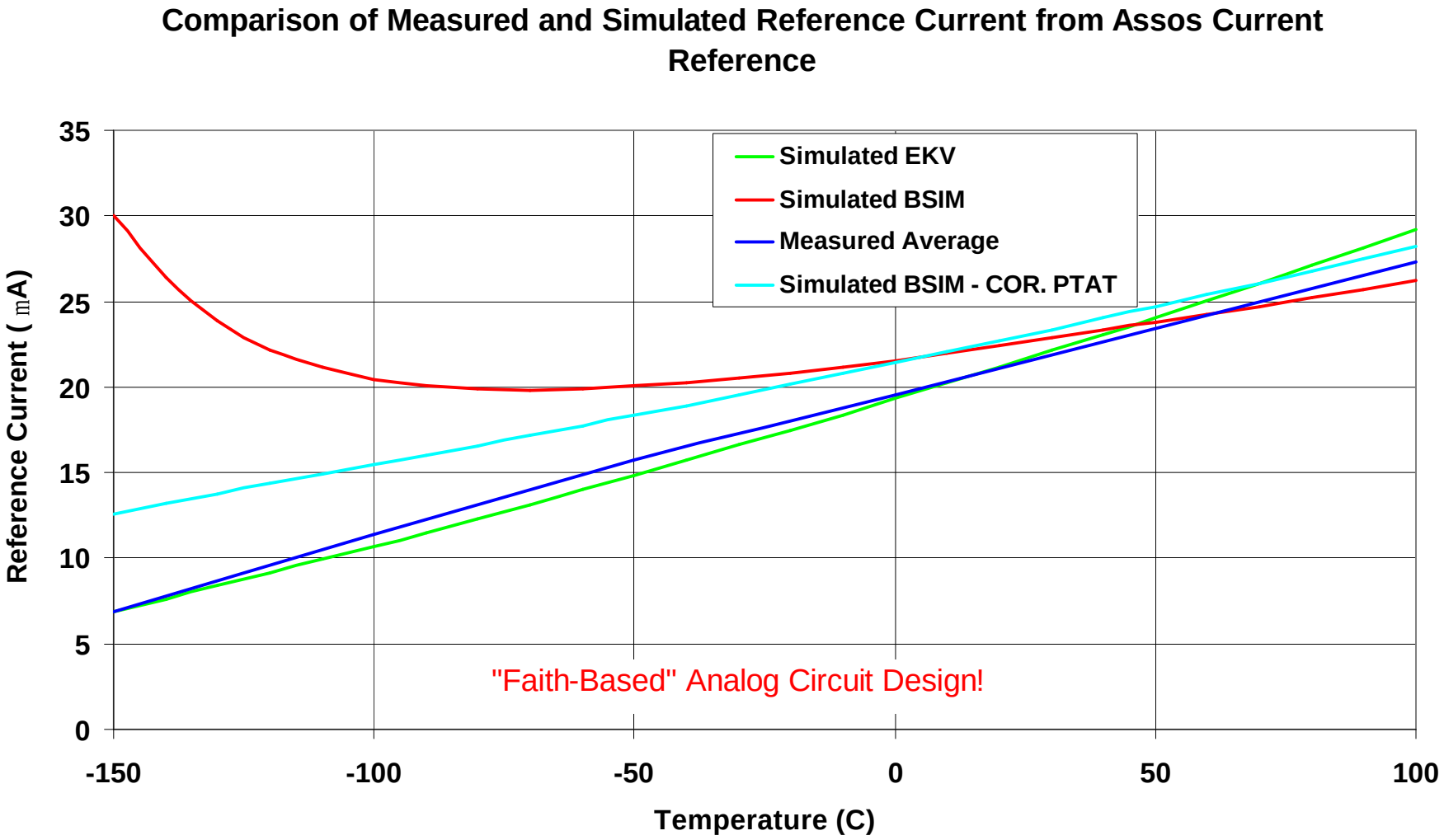
Which Model is Better?

- Generally speaking, we can say this:
  - BSIM is an accurate MOS model, which has been developed over a number years with a great amount of effort. We can know it's accurate because it is so widely used, with successful results. However, it is absolutely true that there are several aspects of BSIM related to analog design which are incorrect.
  - For long-channel MOSFETs EKV2.6 is a very good model. It is especially good at modeling weak and moderate inversion operation. However, its simplicity comes at a cost, and in many cases it is not adequate for modeling short-channel effects.
- Two examples where EKV is superior to BSIM that I have personally experienced are the modeling of PTAT voltage references at low temperatures, and the modeling of body-effect when V_{BS} is greater than zero.

BSIM & EKV


Comparison of Simulated Reference PTAT Reference Voltage for EKV and BSIM
PTAT Reference Voltage (mV)
70
60
50
40
30
20
10
0
-150
-100
-50
0
50
100
Temperature (C)
Simulated EKV
Simulated BSIM

BSIM & EKV


Comparison of Measured and Simulated Reference Current from Assos Current Reference
Simulated EKV
Simulated BSIM
Measured Average
Simulated BSIM - COR. PTAT
Reference Current (mA)
35
30
25
20
15
10
5
0
-150
-100
-50
0
50
100
Temperature (C)
"Faith-Based" Analog Circuit Design!