Background Review

Fabrication:

![Diagram of dice fabrication](image)

Figure 1.2 CMOS integrated circuits are fabricated on and in a silicon wafer.

Basic IC structure:

![Diagram of IC structure](image)

Figure 2.1 Illustration of the top and side view of a die.
Patterning in IC technology:

(a) Unprocessed wafer

(b) Cross-sectional view of (a)

(c) Grow oxide (glass or SiO₂) on wafer.

(d) Deposit photoresist

(e) Mask made resulting from LASH layout.

(f) Placement of the mask over the wafer.

(g) Exposing photoresist.

(h) Developing exposed photoresist.

(i) Etching oxide to expose wafer.

(j) Removal of photoresist.

**Figure 2.3** Sequence of events used in patterning.
Silicon-dioxide (SiO$_2$) growth:

$$t_{Si} = 0.45 \cdot t_{ox}$$

Wells in IC bulk-CMOS technology:
More detailed view of an \( n \)-well:

Beware of parasitics!

\[ I_D = I_S \left( \frac{qV_d}{e^{nkT}} - 1 \right) \]

\( I_D \) diode current
Determining resistance of IC structures:

\[ R = \frac{D}{t} \cdot \frac{L}{W} \]

\[ R = R_{\text{square}} \cdot \frac{L}{W} \]

**Figure 2.8** Calculation of the resistance of a rectangular block of material.

**Figure 2.9** (a) Figure for the calculation of the resistance of a corner section and (b) layout to avoid corners.
Fundamentals of \textit{pn} junctions:

\begin{align*}
    C_j &= \frac{C_{j0}}{m} \left[ 1 - \left( \frac{V_d}{\varphi_0} \right) \right]^{m} \quad \text{depletion capacitance} \\
    \varphi_0 &= \frac{kT}{q} \ln \left( \frac{N_A N_D}{n_i^2} \right) \quad \text{built-in potential} \\
    C_j &= \frac{C_{j0b}}{m_1} \left[ 1 - \left( \frac{V_d}{\varphi_0} \right) \right]^{m_1} + \frac{C_{j0s}}{m_2} \left[ 1 - \left( \frac{V_d}{\varphi_0} \right) \right]^{m_2}
\end{align*}

\textbf{Figure 2.11} Simple illustration of depletion region formation in a \textit{pn} junction.

\textbf{Figure 2.12} A \textit{pn} junction on the bottom and sides of the junction.
Depletion capacitance voltage dependence:

\[ C_{\phi}, \text{ zero-bias depletion capacitance} \]

\[ V_{d}, \text{ diode voltage} \]

\[ C_p, \text{ diode depletion capacitance} \]

\[ 1.12 \text{ pF} \]

**Figure 2.13** Sketch of diode depletion capacitance against diode reverse voltage.

**Figure 2.14** Charge distribution in a forward-biased diode.

\[ C_s = \frac{I_D}{n} \cdot \frac{1}{kT/q} \cdot \tau_T \]

\( p/n \) junction storage capacitance
RC delay through an $n$-well:

\[ t_d = 0.35 r c l^2 \]  

delay through distributed RC network

Other important background review topics (see text):
- metal electromigration
- ground bounce
- crosstalk

ESD protection:
The MOSFET

![MOSFET Diagram](image)

Figure 4.8 Layout of a MOSFET, cross-sectional and angled view.
• MOSFET fabrication:

![Diagram of MOSFET fabrication process]

- (a) Wafer with n-well defined
- (b) Cross-sectional view of (a)
- (c) Define n⁺ and n-well areas and grow thin/stress relief oxide
- (d) Deposit nitride over stress relief oxide
- (e) Implant of p⁺ in field region
- (f) Growth of the field oxide
- (g) Remove nitride and stress relief oxide
- (h) Deposit gate oxide and poly
- (i) Implant n⁺ source and drain regions
- (j) Implant p⁺ source and drain regions

**Figure 4.10** Sequence of events used in MOSFET formation.
• Oxide encroachment:

![Diagram showing oxide encroachment](image)

**Figure 4.11** Layout used to illustrate oxide encroachment.

Effective gate width calculation:

\[ W_{\text{eff}} = W_{\text{drawn}} - DW \]
• Lateral diffusion of source and drain:

![Diagram showing lateral diffusion](image)

**Figure 4.12** Layout used to illustrate lateral diffusion.

Effective gate length calculation:

\[ L_{\text{eff}} = L_{\text{drawn}} - 2 \cdot LD = L_{\text{drawn}} - DL \]

• MOSFET drain or source \( pn \) junction depletion capacitance:

![Diagram showing depletion capacitance](image)

**Figure 4.14** Depletion capacitances of \( n^+ \) to \( p \)-substrate.

Depletion capacitance:

\[ C_{j\text{dep}} = \frac{c_j \cdot A_D}{(1 + \frac{V_{DB}}{p_b})^m_{j}} + \frac{c_{jsw} \cdot P_D}{(1 + \frac{V_{DB}}{p_{bsw}})^{m_{jsw}}} \]