CREATING, ACQUIRING AND INTEGRATING REUSABLE IP

Prof. Don Bouldin, Ph.D.
Electrical & Computer Engineering
University of Tennessee
Knoxville, TN 37996-2100
dbouldin@tennessee.edu

IEEE Boston
14 November 2007
http://vlsi1.engr.utk.edu/~bouldin/boston

OUTLINE OF THIS PRESENTATION

- Design Productivity
- Intellectual Property Blocks
- Reuse Requirements
- The Changing Design Environment
- Acquiring IP Blocks
- Quality IP Metrics
- Collaborative Design
ELECTRONIC PRODUCTS ARE PERVERSIVE AND ALWAYS IMPROVING

Moore's Law: Every 18 months integrated circuit manufacturing can produce 2X performance for the same price or the same performance for half the price.

A DESIGN PRODUCTIVITY CRISIS WAS PREDICTED A DECADE AGO

The Impending Design Productivity Crisis

Logic Transistors per Chip

58%/Yr. Compounded Complexity growth rate

21%/Yr. Compounded Productivity growth rate

Source: SEMATECH

Maya Rubeiz  USAF Wright Labs  maya.rubeiz@sn.wpafb.af.mil  http://rassp.scra.org  1997
DESIGN PRODUCTIVITY HAS PROGRESSED RECENTLY

- 1947
  - 3 Nobel Laureates
  - 1 Transistor

- 2007
  - 3 ECE Students
  - 4M Transistors

Progress has been enabled by raising the level of abstraction and reusing previous sub-systems or blocks.

Design Example

Nokia 9000 wireless phone/PDA

- Personal digital assistant (PDA) and GSM cellular phone
- Embedded block imported into a CBA foundation
- “Required 2 Mask Designers instead of 20”
WE BUILD SKYSCRAPERS USING STANDARDIZED BLOCKS

So, let’s use standardized blocks to build systems:

Sears Tower, Chicago

www.lego.com

INTELLECTUAL PROPERTY BLOCKS

Design #1 without Planned Reuse

Design #2 without Planned Reuse

Design #3 without Planned Reuse

Design #1 For Reuse

Design #2 WITH IP

Design #3 WITH IP

IP blocks should have well-defined interfaces

Often, IP are more like patches that must be stitched together like a quilt
IP is created using a Hardware Description Language or HDL

```vhdl
CASE y IS
  WHEN A =>
    IF w = '0' THEN  y <= A ;
    ELSE  y <= B ;
    END IF ;
  WHEN B =>
    IF w = '0' THEN  y <= A ;
    ELSE  y <= C ;
    END IF ;
  WHEN C =>
    IF w = '0' THEN  y <= A ;
    ELSE  y <= C ;
    END IF ;
END CASE ;
```

An HDL design can be targeted to multiple layouts.
REQUIREMENTS FOR REUSABLE IP

• BASICS:
  - HDL Models
  - Functional Description
  - Application Intent
  - Interface Specifications
  - Authors and Owners
  - Size, Delay, Power Estimates
  - Packaging Info

• ALSO NEED:
  - Test Bench (Input Stimuli/Output Responses)
  - Tools and Versions Used/Needed
  - Foundry Used For Fab
  - Size, Delay, Power Measurements
  - Testability Features (BIST, JTAG, SCAN)

THE DESIGN METHOD HAS CHANGED

CUSTOMER Requirements
UNCHANGED
DESIGNER Specifications

OLD METHOD
1. Select ICs
2. Design/Fab PCB
3. Design blocks for new IC
4. Integrate blocks
5. System Integration

NEW METHOD
1. Select PCB with ICs
2. Select blocks for new IC
3. Design missing blocks
4. Integrate blocks
5. System Integration

UNCHANGED
IP CAN ATTRACT BUSINESS AND REDUCE RISK AND TIME-TO-MARKET

CUSTOMER

IP

Design Center

IP

Foundry

ASIC/FPGA

AN OPEN COMPETITIVE MARKET EXISTS

CUSTOMER

PORTABLE IP
(Multiple Suppliers)

REPOSITORY
www.design-reuse.com

Standards:
www.vsia.org
www.ieee.org

Foundry

Foundry

Foundry

ASIC/FPGA
FREE OPEN-SOURCE CORES

- LEON is an open-source 32-bit SPARC V8 CPU that was developed by the European Space Agency and is available for free at www.gaisler.com

- Other cores at www.opencores.org
  - USB 2.0
  - Ethernet MAC
  - DES/AES Encryption
  - FIR/IIR Filters
  - Floating Point Unit

QUALITY INTELLECTUAL PROPERTY

- The VSI (Virtual Socket Interface) Alliance (VSIA) is an open, international organization that includes representatives from all segments of the SoC industry: System houses, Semiconductor vendors, Electronic Design Automation (EDA) companies, and Intellectual Property (IP) providers. VSIA's mission is to dramatically enhance the productivity of the SoC design community.

- Quality Intellectual Property (QIP) Metric v3.0 is available for free from the VSIA website: www.vsia.org
QIP METRICS

DEVELOPING QUALITY IP

- Requirements should be mapped into an executable specification which produces the desired golden reference responses.
- HDL and FPGA responses must match the golden responses identically.
THE TESTBENCH CONTAINS THE STIMULI, RESPONSES AND UUT

- Functional stimuli are developed by the designer to mimic the system environment.
- The tester is written in HDL but is not synthesized into the FPGA.

Testbench (Tester + HDL Source Code)

RAPID VERIFICATION SAVES TIME

- Minimizing time-to-market encourages designers to develop only a few tests for simulation and then proceed to testing the design inside the FPGA in its real-world environment. The FPGA executes tests 500x faster than the simulator and the real-world system environment produces the tests automatically.
CONTROLLABILITY AND OBSERVABILITY AID DEBUGGING

- When errors are encountered on the FPGA board where tests are limited to the primary inputs and primary outputs, the designer can return to simulation where complete controllability and observability of all of the internal nodes are available for debugging.

POLISHING FOR REUSE

- Once the HDL source code has been verified in the FPGA, the design can be polished for reuse.

- This involves documenting the HDL and providing test access mechanisms for reuse as an embedded core per IEEE 1500: http://grouper.ieee.org/groups/1500

- Also, the tester code should be enhanced with assertion-based tests to achieve the desired HDL code coverage.

- Constrained, random-generated tests can be produced automatically for large HDL cores.
The simulator can produce coverage reports and identify missed statements in the code.

```
wait_clock(16);
IF (left_seg = X"6")
  -- check second state of 7-segment display
  THEN
  ASSERT false
  REPORT "Output signals set correctly (7-segment second state)"
  SEVERITY note;
  ELSE
  ASSERT false
  REPORT "Output not set correctly (7-segment second state)"
  SEVERITY warning;
END IF;
```

"Failure" stops simulation while "warning" does not. "Note" is used to document a correct response.
BUILT-IN SELF-TEST CODE

- The HDL source code can be augmented with Built-In Self-Test (BIST) code.
- BIST code can verify that the I/O and other likely failure modes are working properly or not.
- BIST code can also include functional test cases to assure proper operation before execution or during “idle” times.

GRAPHICAL TOOLS CAN REUSE AND CREATE IP BLOCKS

- Library cells (basic IP blocks) are integrated into a larger block that itself can be reused.
**ACQUIRING IP**

- **STAR IP:** Blocks requiring 100+ staff years to design (like ARM, MIPS) have become bestsellers and come with lots of support.

- **Small IP:** Blocks requiring 1-2 staff years to design are priced at 1/3 of the development cost. Buyers are skeptical about the value and often prefer to do these in-house.

- **Medium IP:** Blocks requiring 5-10 staff years are profitable for both seller and buyer. However, some suppliers have been bought by foundries to add to the foundries’ captive portfolios.

---

**ONCE UPON A TIME**

Pastor  Snowy Road  Church

County Road Dept.
THE GLOBAL ECONOMY

The Earth is NOT Flat
Boston or Bangalore or Knoxville
Actually, we live on a small planet.

COLLABORATIVE DESIGN

Collaborative Design of a System-on-Chip
http://www.cs.wright.edu/~tkprasad/courses/soc.html
DESIGN-FOR-REUSE and DESIGN-WITH-REUSE

SUMMARY AND CONCLUSIONS

- Design Productivity
- Intellectual Property Blocks
- Reuse Requirements
- The Changing Design Environment
- Acquiring IP Blocks
- Quality IP Metrics
- Collaborative Design