Donald W. Bouldin

POSITION: Professor Emeritus
Electrical Engineering & Computer Science
University of Tennessee

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EDUCATION: B. E. (Electrical Engineering), Vanderbilt University (1967)
M. S. (Electrical Engineering), Georgia Institute of Technology (1968)
Ph. D. (Electrical Engineering), Vanderbilt University (1975)

PERSONAL: U. S. Citizen born in Tennessee
Salutatorian, McKenzie High School, McKenzie, TN (1963)
Married: Karen D. Bouldin
Spouse's Education:
- B. S. (Education), University of Tennessee (1968)
- M. A. (Early Childhood Education), Peabody College/Vanderbilt (1974)

Spouse's Occupation: Wife, Mother and Homemaker
One son: Andrew J. Bouldin
Cedar Springs Presbyterian Church:
- Sunday School Superintendent (1984-1987)
- Deacon (1984-1988); Elder (1989-1991; 1994-1996)
- Sunday School Teacher (1991-92; 1993-94; 1996-97)

Christ Presbyterian Church: Member (1998–present)

Donald W. Bouldin

ABSTRACT:

Dr. Don Bouldin is Professor Emeritus of Electrical Engineering & Computer Science at the University of Tennessee, Knoxville. He received the B.E. (Electrical Engineering) from Vanderbilt University in 1967, the M.S. (Electrical Engineering) from Georgia Institute of Technology in 1968, and the Ph.D. (Electrical Engineering) from Vanderbilt University in 1975 when he joined the faculty at the University of Tennessee. During 1968-1972, he served as Electronics Officer in the U.S. Navy.

Prof. Bouldin served two years as Chairman of the Technical Committee on VLSI for the IEEE Computer Society. He received the TAB Pioneer Award from the IEEE for his participation in CompuSat-88, a tutorial videoconference that was broadcast to over 6000 engineers in North America. He has received other awards over the years for outstanding teaching at the university and meritorious service to the IEEE. In addition to teaching VLSI systems design classes at the University of Tennessee, he has served as an instructor for eight faculty enhancement short courses on VLSI and FPGAs sponsored by the National Science Foundation (NSF). These have been held at the University of Tennessee, the Massachusetts Microelectronics Center, Boston University and the California State University, Sacramento. He has also taught short courses on VLSI design at five IEEE Nuclear Science Symposia and has organized a summer VLSI course for the Instituto Tecnologico y de Estudios Superiores in Monterrey, Mexico. He has also presented several tutorials and seminars in Argentina, Belgium, Brazil, Canada, France, Germany, Hong Kong, India, Japan, Mexico, Netherlands, Norway, Thailand, South Korea, Switzerland, the United Kingdom and the United Arab Emirates.

He served as Guest Co-Editor for a series of four special issues on Microelectronic Systems that were published in the *IEEE Journal of Solid-State Circuits*. He was instrumental in gaining IEEE approval for the launching of the *IEEE Transactions on VLSI Systems* and served as its Editor-in-Chief during 1995-1996. He has also served as the chair of its Steering Committee.

For almost twenty years, Dr. Bouldin served as special Section Editor of the "VLSI Designer's Interface" column for *IEEE Circuits & Devices Magazine* and Editor of the Microelectronic Systems Newsletter that is posted on the web with notices broadcast electronically to over 3000 VLSI designers. He was the Technical Program Chairman for the 1996 International Symposium on Circuits and Systems and managed the review of 1400 papers.

Dr. Bouldin has authored over 250 publications and been the Principal Investigator for over nine million dollars of sponsored research, primarily with DARPA (Defense Advanced Research Projects Agency), the Office of Naval Research, NSF and the Oak Ridge National Laboratory. In 1997 Dr. Bouldin received the University of Tennessee Chancellor's Award for Research and Creative Achievement. Also in 1997, Dr. Bouldin was recognized as a Fellow of the IEEE for contributions to the design of special-purpose architectures using VLSI processors. In 2003 he received the Allen and Hoshall Award from the College of Engineering at the University of Tennessee for excellence in teaching and research and was also recognized as a 2003 Engineering Research Fellow. In 2006 he received the Charles E. Ferris Award sponsored by the Technical Society of Knoxville. He has been the major advisor for 14 Ph.D. and 98 M.S. students.

Dr. Bouldin retired in 2011 after 36 years with the University of Tennessee and is a consultant with the Oak Ridge National Laboratory.

RESEARCH SPONSORS:

[Sponsor-1] Collaborative Research and Development with the Health & Safety Research Division. (1976-1984, $ 600,000, Oak Ridge National Laboratory).

[Sponsor-2] Scene content analysis. (1977-1979, $ 250,000, Defense Advanced Research Projects Agency and the Space & Missile Systems Organization).

[Sponsor-3] Collaborative Research and Development with the Measurement & Controls Section of the Instrumentation & Controls Division. (1978-1988, $ 128,000, Oak Ridge National Laboratory).

[Sponsor-4] MOSIS Fabrication of Integrated Circuits for Education. (1984-2011, $ 150,000, National Science Foundation).

[Sponsor-5] Collaborative Research and Development with the Research Instruments Section of the Instrumentation & Controls Division. (1986-2007, $ 3,000,000, Oak Ridge National Laboratory).

[Sponsor-6] VLSI Design of a Telerobotic Controller for a Dual-Axis Manipulator Element. (1987-1988, $ 44,000, Telerobotics International).

[Sponsor-7] Field-Programmable Gate Array Equipment Grant. (1990, $ 15,000, National Science Foundation).

[Sponsor-8] Support for Workshop on Microelectronic Systems Education in the 1990's. (1990-1991, $ 12,500, National Science Foundation).

[Sponsor-9] Faculty Enhancement Short Course Entitled Designing Microelectronic Systems Using FPGAs. (1993, $ 75,059, National Science Foundation).

[Sponsor-10] Support for 1993 Workshop on Rapid Prototyping of Microelectronic Systems for Universities. (1993, $ 33,006, National Science Foundation).

[Sponsor-11] Faculty Enhancement Short Course Entitled Designing Microelectronic Systems Using FPGAs. (1994, $ 75,000, National Science Foundation).

[Sponsor-12] Group Travel Support to VLSI Design '94 in India (1994, $ 11,000, National Science Foundation)

[Sponsor-13] Design for Packageability: Early Consideration of Packaging from a Microelectronic System Designer's Viewpoint. (1994-1997, $ 1,444,444, Defense Advanced Research Projects Agency).

[Sponsor-14] Highly Integrated Signal Processors and Packaging. (1996-1997, $ 80,000, Maxwell Laboratories for AFRL Albuquerque).

RESEARCH SPONSORS (continued):

[Sponsor-15] CHAMPION: A Software Design Environment for Adaptive Computing Systems. (1997-2001, $ 1,226,607, Defense Advanced Research Projects Agency).

[Sponsor-16] Scalable Intracampus Research Grid Computing (with Prof. Jack Dongarra of Computer Science for hardware infrastructure). (2000-2004, $ 2,000,000, National Science Foundation).

[Sponsor-17] Towards an Automated Development Environment for Parallel Computing with Reconfigurable Processing Elements (with Prof. Mike Langston of Computer Science). (2000-2003, $ 375,000, NSF).

[Sponsor-18] Design of an Integrated Circuit for Multi-Chip Module Fault Tolerance. (2001-2004, $ 93,648, SAIC for AFRL Albuquerque).

[Sponsor-19] Datapath-driven Integrated Circuit Design for Mission-Specific Processing (with Prof. Wayne Dai of Univ. of California, Santa Cruz). (2001-2003, $ 1,195,822, Defense Advanced Research Projects Agency).

[Sponsor-20] Heterogeneous, High-Performance Reconfigurable Computers (with Prof. Greg Peterson). (2003-2005, $ 102,400 NSF).

[Sponsor-21] Hardware Acceleration for Information Security. (2003-2005, $ 472,000, Office of Naval Research).

RESEARCH EXPERIENCE:

[Research-1] Biomedical instrumentation. (1972-1975, Vanderbilt University, Electrical & Biomedical Engineering Department).

Minicomputer-based instrumentation was developed to generate dynamic random dot stereograms for eliciting visual evoked cortical potentials.

[Research-2] Controllers for studying gaseous and liquid dielectrics. (1976-1984, Oak Ridge National Laboratory, Health & Safety Research Division).

Several controllers were developed for experimental apparatus which permitted the study of the behavior of insulating media.

[Research-3] Scene content analysis. (1977-1979, University of Tennessee, Electrical & Computer Engineering Department).

A dimensionless measure of the structural entropy of a digitized image was developed to characterize the structural content of natural scenes containing man-made buildings.

[Research-4] High-speed data acquisition system. (1979-1980, Oak Ridge National Laboratory, Instrumentation & Controls Division).

An efficient algorithm was developed to generate channel addresses automatically for nuclear reactor experiments which required the acquisition of l00,000 data words per second from l000 individual channels of a dozen frequencies.

RESEARCH EXPERIENCE (continued):

[Research-5] Parallel processing for artificial intelligence applications. (1985-1988, Oak Ridge National Laboratory, Instrumentation & Controls Division).

A 64-node parallel machine was designed, built and tested for the purpose of accelerating the execution of rule-based programs used in artificial intelligence applications.

[Research-6] Development of integrated circuits for portable instruments. (1986-present, Oak Ridge National Laboratory, Instrumentation & Controls Division).

A solar-powered, infrared injection laser microminiature transmitting system to permit the tracking of killer bees. This work has been publicized in *Scientific American*, *Time Magazine (11 July 1988)* and more than 50 other publications with a photograph of an integrated circuit attached to the back of a bee. Also, integrated circuits have been developed for the next generation RADIAC for the U. S. Navy. These circuits include a RISC-based processor that has been optimized for low-power applications yet made source-code compatible with the Intel 80C51. Integrated circuit prototypes are synthesized and then fabricated via MOSIS.

[Research-7] Integrated circuit design for robotic applications. (1987-1988, Telerobotics International).

Integrated circuits were designed for a telerobotic controller for a dual-axis manuipulator element. These were fabricated and installed in a working system.

[Research-8] Integration and enhancement of computer-aided design VLSI tools. (1988-1989, Oak Ridge National Laboratory, Instrumentation & Controls Division).

Collaborative work with and the National Institute of Standards and Technology for the development of integrated circuits to monitor the performance of parallel processors. Sponsored by the Defense Advanced Research Projects Agency.

[Research-9] Design for Packageability: Early Consideration of Packaging from a Microelectronic System Designer's Viewpoint. (1994-1997, $1,444,444, Defense Advanced Research Projects Agency)

Global optimization of the entire microelectronic system may be achieved by incorporating critical packaging factors into the integrated circuit design flow. Multi-chip modules which illustrated the gain in system performance were designed, fabricated and measured. An area array pad router was developed.

[Research-10] Highly Integrated Signal Processors and Packaging. (1996-1997, $ 80,000, Maxwell Laboratories)

An experimental study of the speed-power tradeoffs for the sizing of drivers for inter-die communication in a multi-chip module (MCM) package was conducted along with an evaluation of candidate architectures for a proposed malleable signal processor.

RESEARCH EXPERIENCE (continued):

[Research-11] CHAMPION: A Software Design Environment for Adaptive Computing Systems. (1997-2001, $ 1,226,607, Defense Advanced Research Projects Agency)

The goal of this project was to automate the mapping of Khoros-based applications onto adaptive computing systems to improve designer productivity by 100x.

[Research-12] Scalable Intracampus Research Grid Computing (with Prof. Jack Dongarra of Computer Science for hardware infrastructure). (2000-2005, $ 2,000,000, National Science Foundation).

Clusters of workstations interconnected via the campus gigabit network are utilized to solve parallel applications. Our heterogenous cluster consists of twelve dual-node SUN Enterprise workstations plus eight Pentium PCs, each with a Virtex million-gate reconfigurable processor serving as an accelerator. We have also added ten VirtexII-Pro boards and two additional SUN Enterprise servers.

[Research-13] Towards an Automated Development Environment for Parallel Computing with Reconfigurable Processing Elements (with Prof. Mike Langston of Computer Science). (2000-2003, $ 375,000, NSF).

[Research-14] Datapath-driven Integrated Circuit Design for Mission-Specific Processing (with Prof. Wayne Dai of Univ. of California, Santa Cruz). (2001-2003, $ 1,195,822, Defense Advanced Research Projects Agency).

[Research-15] Design of a IC for Self-Organizing a Memory Stack (2001-2004, $ 93,000, SAIC for AFRL Albuquerque).

[Research-16] Hardware Acceleration for Information Security-Part I. (2003, $ 75,000, Tech-Soft for Office of Naval Research).

[Research-17] Hardware Acceleration for Information Security-Part II. (2003-5, $ 456,750, Univ. of Illinois for Office of Naval Research).

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TEACHING EXPERIENCE:

[Course-1] Engineering Computations, BE 1410 (Freshman). Structured problem solving of engineering applications were programmed using the BASIC computer language. Taught Spr 77, Spr 80 and Sum 80 (University of Tennessee).

[Course-2] Circuit Theory, EE 201 (Sophomore). Introductory course in electrical circuits for electrical engineers. Taught Sum 75 (Vanderbilt University).

[Course-3] Network Analysis, EE 202 (Sophomore). Introductory course in networks for electrical engineers. Taught Sum 75 (Vanderbilt University).

[Course-4] Fundamentals of Logic Design, EE 3180 (Junior). Number systems and codes; switching algebra; logic design of combinatoral circuits; minimization methods. Taught Fall 75 and Sum 76 (University of Tennessee).

[Course-5] Analog-to-Digital and Digital-to-Analog Conversion Techniques, EE 46l0 (Senior). Conversion of analog signals into digital codes and vice-versa; Analog computers and simulation; CSMP modeling of control systems. Taught Spr 76 and Win 77 (University of Tennessee).

[Course-6] Design of Sequential Circuits, EE 4620 (Senior). Analysis/synthesis of synchronous and asynchronous circuits; state assignment; incompletely-specified circuits; fault diagnosis. Taught Win 76 and Win 85 (University of Tennessee).

[Course-7] Digital Computer Design & Organization, EE 4630 (Senior). Organization of digital computers; memory and arithmetic elements; control units; microprogramming. Taught Fall 75, Sum 76, Spr 77 and Spr 85 (University of Tennessee).

[Course-8] Bioelectric Instrumentation, EE 4660 (Senior). Nature and origin of bioelectric potentials; transducers; amplifier requirements; ECG/EEG/EMG systems; medical imaging systems; safety. Taught Spr 76, Win 77, Fall 77, Spr 78, Win 79, Fall 79, Sum 80, Win 82, Spr 83, Win 84 and Spr 85 (University of Tennessee).

[Course-9] Microcomputer Interfacing, EE 4800 (Senior). Input and output considerations of microcomputers (TI 9900/Motorola 6800); Project-oriented course illustrating hardware and software tradeoffs. Taught Spr 80, Spr 81, Fall 81, Spr 82, Fall 83, Win 84, Spr 84 and Fall 84 (University of Tennessee).

[Course-10] Small Computer Systems, EE 4850 (Senior). Basic structure of small computer systems; input-output techniques; interrupt structures and operating systems; employs assembly language programming on LSI-ll. Taught Win 76 (University of Tennessee).

TEACHING EXPERIENCE (continued):

[Course-11] Digital Signal Processing–Hardware Considerations, EE 5040 (Graduate). Sampling theorem; analog-digital and digital-analog techniques; Fast Fourier transform; project implementing digital signal processing in hardware. Taught Fall 82 (University of Tennessee).

[Course-12] Logic Design & Automata Theory I, EE 5610 (Graduate). Review of design considreations for combinational and sequential circuits; fault diagnosis; designing maintainable systems Taught Fall 77, Fall 78, Fall 80, Fall 81, Fall 85 and Fall 86 (University of Tennessee).

[Course-13] Logic Design & Automata Theory II, EE 5620 (Graduate). State identification and structure realizations of sequential machines. Taught Win 78, Win 79, Win 81, Win 82, Win 86 and Win 87 (University of Tennessee).

[Course-14] Digital System Architecture, EE 5630 (Graduate). System organization; hardware; structures; I/0 considerations; signature analysis; interface and bus techniques; networking. Taught Spr 78, Spr 79, Spr 82, Spr 83, Spr 86 and Spr 87 (University of Tennessee).

[Course-15] Advanced Small Computer Systems, EE 5940 (Graduate). Real-time applications; peripheral devices; project-oriented to show hardware and software tradeoffs of microcomputers. Taught Fall 79 and Win 81 (University of Tennessee).

[Course-16] Microprogramming Concepts, EE 5950 (Graduate). Structured design of digital systems using microprogramming techniques on bit-slice devices. Taught Win 80 (University of Tennessee).

[Course-17]
Designing Application-Specific Integrated Circuits, EE 494/559 (Senior/Graduate). Logic synthesis and automatic layout generators are used to produce standard cell integrated circuits that are fabricated via MOSIS. Taught Spr 87, Spr 88, Spr 89, Spr 90 and Spr 91 (University of Tennessee).

[Course-18] Designing Field-Programmable Gate Arrays, ECE 552 (Graduate). Schematics are used to capture digital logic designs that are mapped into FPGAs (Actel, Altera and Xilinx). Taught Spr 92 (University of Tennessee).

[Course-19] Microcomputer Interfacing, ECE 451 (Senior). Input and output considerations of microcomputers (Motorola 68HC11); Project-oriented course illustrating hardware and software tradeoffs. Taught Fall 98 (University of Tennessee).

TEACHING EXPERIENCE (continued):

[Course-20] Designing Application-Specific Integrated Circuits, ECE 551 (Graduate). This project-oriented course presents an overview of the design of field-programmable gate arrays (FPGAs) and application-specific integrated circuits (ASICs). Each pair of students captures a design using a hardware description language (VHDL) and then uses synthesis and automatic placement and routing software to implement the design using multiple technologies (Altera and Xilinx). Taught Fall 92 thru Fall 11 (University of Tennessee).

[Course-21] Designing Microelectronic Systems, ECE 552 (Graduate). System-level designs are performed by teams of students using VHDL and prototyped using reconfigurable computers. The designs are also retargeted to testable ASICs and documented for re-use. Taught Spr 93 thru Spr 07 (University of Tennessee).

[Course-22] Computer-aided Design of VLSI Systems I, ECE 651 (Graduate). Layout of the mask layers of digital CMOS leaf cells is performed following standard cell and datapath formats for fabrication via MOSIS. Taught Fall 83, Fall 85 thru Fall 11. (University of Tennessee).

[Course-23] Computer-aided Design of VLSI Systems II, ECE 652 (Graduate). Teams of graduate students create and modify system-on-chip designs with re-usable intellectual property cores. Tradeoffs are explored at the architectural level and during logic synthesis and physical layout. Taught Spr 84, Spr 86 thru Spr07 (University of Tennessee).

UNIVERSITY SERVICE:

[Service-1] Faculty Coordinator for Electrical Engineering, National Engineers' Week Activites (1976-1978).

[Service-2] Student Chapter Advisior of the IEEE Computer Society Branch (1979-1991).

[Service-3] College of Engineering Representative to the University Faculty Senate (1979-1982).

[Service-4] Chairman of the Electrical Engineering Undergraduate Committee (1981-1984).

[Service-5] Chairman of the Electrical Engineering Semester Transition Committee (1985-1986).

[Service-6] Member, Electrical Engineering Department Head Search Committee (1983, 1993 and 1997).

[Service-7] Member, Electrical Engineering Faculty Search Committee (1995, 1997, 1999, 2000, 2001, 2002, 2003, 2004 and 2005).

[Service-8] Chairman, IT Administrator Search Committee (2002-2003).

[Service-9] Chairman, Cummulative Review Committees (2003).

CONSULTING EXPERIENCE:

[Consulting-1] Professional Engineer, Registered in Tennessee, Certificate # 9234 (1973-present).

[Consulting-2] Instructor of the Engineering Science Review and Professional Electrical Engineering Review Courses, University of Tennessee (1976-1997).

[Consulting-3] Development of Instrumentation and ASICs for Oak Ridge National Laboratory (1976-1993).

[Consulting-4] Instructor of Short Courses on Digital Test Systems for ITT Telecommunications, Milan, TN (1976-1978).

[Consulting-5] Instructor of Short Courses on Microprocessor Interfacing, DSP, ASICs and FPGAs for the University of Tennessee's Tennessee Industries Week (1978-1994).

[Consulting-6] Instructor of Short Courses on Microprocessor Interfacing for Texas Instruments, Johnson City, TN (1981-1982).

[Consulting-7] Presentor of the VLSI section of IEEE Computer Society's CompuSat-88 Satellite Videoconference (October 1988).

[Consulting-8] Development of digital and analog integrated circuits for positron emission tomographic scanners for CTI PET Systems, Inc. (1987-1993).

CONSULTING EXPERIENCE (continued):

[Consulting-9] Instructor of Short Courses on VLSI Systems Design at the IEEE Nuclear Science Symposia (1988, 1989, 1991, 1992, 1993 and 1994).

[Consulting-10] Instructor of NSF-sponsored Faculty Enhancement Course on VLSI Design held at the Massachusetts Microelectronics Center (1990-1992).

[Consulting-11] Instructor of NSF-sponsored Faculty Enhancement Course on FPGA Design held at the Boston University (1993), California State University, Sacramento (1993 and 1994) and the University of Tennessee (1993 and 1994).

[Consulting-12] Instructor of Designing Microelectronic Systems Using FPGAs for the Frontiers in Education Conference (1992).

[Consulting-13] Instructor of a summer VLSI course for the Instituto Tecnologico y de Estudios Superiores in Monterrey, Mexico (1993).

[Consulting-14] Instructor of Tutorial on FPGAs presented at VLSI Design-94 in Calcutta, India, IIT in Bangalore, India, Cadence Design Systems in New Delhi, India, ISCAS-95 in Seattle, WA and VLSI Eductor's Conference in Bangkok, Thailand, and VLSI-97 in Gramado, Brazil. (1994-1997).

[Consulting-15] Instructor of Tutorial on Designing Digital ASICs for Honeywell Kansas City Dept. of Energy Plant (2000).

[Consulting-16] Consultant on Intellectual Property Blocks for System-on-Chip Applications, Concorde Microsystems, Knoxville, TN (2001).

[Consulting-17] Expert Witness on Physical Design Automation, O'Melvin and Myers Attorneys, (1998-2001).

[Consulting-18] Consultant on Electronic Implementations for Touch Screens, Elo-Touch Systems, Menlo Park, CA (2000-2007).

[Consulting-19] Expert Witness on Microcontroller-Based Instrumentation, Brittian and Pitts Attorneys, (2005-2007).

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PATENTS:

[Patent-1] "Touch screen based topological mapping with resistance framing design",
United States Patent 6,650,319 issued November 18, 2003
Inventors: Sam Hurst, Rufus Ritchie, Don Bouldin and Bruce Warmack
Assignee: Elo Touchsystems, Inc. (Freemont, CA).

[Patent-2] "Touch sensor with non-uniform resistive band",
United States Patent 7,265,686 issued September 4, 2007
Inventors: Sam Hurst, Rufus Ritchie, Bruce Warmack, Don Bouldin and Joel Kent
Assignee: Tyco Electronics (Middletown, PA).

[Patent-3] "Touch sensor with relatively conductive grid",
United States Patent 7,800,589 issued September 21, 2010
Inventors: Sam Hurst, Rufus Ritchie, Don Bouldin and Bruce Warmack
Assignee: Tyco Electronics (Berwyn, PA).

[Patent-4] "Multiple-touch sensor",
United States Patent 7,952,564 issued May 31, 2011
Inventors: Sam Hurst, Bruce Warmack, Rufus Ritchie, Don Bouldin and David Ritchie
Assignee: TopoTec (Knoxville, TN).

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DONATIONS:

[Donation-1] Microcomputer-based development equipment. (1981-1982). Texas Instruments was solicited to donate to the University of Tennessee $ l50,000 of computing equipment to be used for developing advanced digital systems. This equipment consisted of a minicomputer, a T.I. 990/l2 model 20, and a microprocessor emulator. Also, twenty microcomputer interface systems were included to permit students to test their designs and programs.

[Donation-2] Integrated circuits for a hardware accelerator. (1981-1982). Hewlett Packard was solicited to donate to the University of Tennessee $ 80,000 of integrated circuits capable of performing 32-bit floating-point operations in less than a microsecond. These devices were incorporated into a hardware accelerator for a computational fluid dynamics laboratory.

[Donation-3] Public-domain software packages for computer-aided design of integrated circuits. (1983-2011). Numerous public-domain packages have been obtained over the years including: MAGIC, OCT, SIS, SPICE, LAGER and HYPER from the University of California, Berkeley, OLYMPUS and IRSIM from Stanford University, COSMOS from Carnegie-Mellon University, CAZM and SIGVIEW from the Microelectronics Center of North Carolina and RELAX from M.I.T.

[Donation-4] Engineering workstation for design of integrated circuits. (1984). Hewlett Packard was solicited to donate to the University of Tennessee $ 138,000 an HP-9000 32-bit minicomputer system and associated peripherals.

[Donation-5] Field-programmable gate array development system. (1991). Altera Corporation has donated a $ 15,000 system for educational use in an advanced logic design course.

[Donation-6] Field-programmable gate array development system. (1991). Actel Corporation has donated a $ 30,000 system for educational use in an advanced logic design course.

[Donation-7] Field-programmable gate array development system. (1992). Xilinx Corporation has donated a $ 43,000 system for educational use in an advanced logic design course.

[Donation-8] Computer-aided design software for VLSI circuits. (1992). Viewlogic Systems has made a donation valued at $ 1,354,600 which consits of 12 copies of *all* of their software products to permit the design and synthesis of integrated circuits using SPARCstations.

[Donation-9] Engineering workstations for design of microelectronic systems. (1993). Zellweger-Uster (formerly Spin Lab) of Knoxville has donated six SUN Sparcstations for educational use in advanced design courses.

DONATIONS (continued):

[Donation-10] Engineering workstations for logic emulation. (1994). IBM of Boca Raton, FL has donated eight Quickturn logic emulation workstations. Each consists of a Sparc-2 with 64 MBytes of internal RAM, 500 MBytes of disk and a 19-inch color screen. Faciltiies to emulate 40,000-gate logic designs are provided in each workstation.

[Donation-11] Computer-aided design software for designing multi-chip modules. (1995). Mentor Graphics donated $4.8 million of software.

[Donation-12] Computer-aided design software for physical IC layout. (1995). Cascade Design Automation donated their EPOCH package.

[Donation-13] Computer-aided design software for synthesis of ICs and FPGAs. (1995). Synopsys donated $6.2 million of software to permit designs to be captured, evaluated and synthesized automatically into application-specific integrated circuits or field-programmable gate arrays.

[Donation-14] Computer-aided design software for IC synthesis and physical layout. (2001). Cadence Design Systems donated $47.7 million of IC design software.

[Donation-15] Million-gate Virtex FPGAs for rapid prototyping. (2002). Xilinx donated an evaluation board and 480 XCV1000 devices valued at $244K.

[Donation-16] Computer-aided design software for automated physical layout of standard cells. (2002). Prolific donated their ProGenesis package valued at $375K.

[Donation-17] Computer-aided design software for automated characterization of standard cells. (2002). CircuitSemantics donated their DynaCell package valued at $75K.

[Donation-18] Programmable System-on-Chip Devices and development software for rapid prototyping. (2003). Xilinx donated ten VirtexII-Pro chips plus its EDK software valued at $22K.

[Donation-19] Computer-aided design software for IC synthesis and physical layout. (2004). Synopsys increased its 1995 donation to $24 million of software.

[Donation-20] Computer-aided design software for IC synthesis and physical layout. (2004). Synplicity.

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PROFESSIONAL ACTIVITIES:

[Professional-1] IEEE East Tennessee Section, Assistant Secretary-Treasurer (1978-1979).

[Professional-2] IEEE East Tennessee Section, Secretary-Treasurer (1979-1980).

[Professional-3] IEEE East Tennessee Section, Vice Chairman (1980-1981).

[Professional-4] IEEE East Tennessee Section, Chairman (1981-1982).

[Professional-5] IEEE East Tennessee Section, Past Chairman (1982-1983).

[Professional-6] IEEE East Tennessee Section, Director (1983-1985).

[Professional-7] IEEE Systems, Man and Cybernetics, AdCom (1984-1988).

[Professional-8] IEEE Computer Society Chapter of the East Tennessee Section, Co-Founder (1985).

[Professional-9] IEEE Computer Society Technical Committee on VLSI, Vice Chairman (1986-1987).

[Professional-10] IEEE Computer Society Technical Committee on VLSI, Chairman (1988-1989).

[Professional-11] IEEE Solid-State Circuits Council, Computer Society Representative (1992-1994).

[Professional-12] IEEE Trans. on VLSI Systems, Steering Committee Chairman (1997-1998).

[Professional-13] IEEE Trans. on VLSI Systems, EIC Search Committee Chairman (2002).

[Professional-14] IEEE Trans. on VLSI Systems, Steering Committee Member (2003-2007)

[Professional-15] IEEE Computer Society Fellows Selection Committee, Member (2003-2004).

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REFEREE & EDITORIAL SERVICE:

[Referee-1] *IEEE Transactions on Systems, Man and Cybernetics*, 1983-1987, 1991

[Referee-2] *International Journal of Parallel Programming*, 1987-1994

[Referee-3] *National Science Foundation*, 1987-2007

[Referee-4] *IEEE Circuits & Devices Magazine*, 1988-2007

[Referee-5] *McGraw-Hill*, 1989, 1991 and 1992

[Referee-6] *IEEE Computer*, 1990-1994

[Referee-7] *IEEE Journal of Solid-State Circuits*, 1990-1992

[Referee-8] *Prentice-Hall*, 1990-2007

[Referee-9] *Addison-Wesley*, 1990-2007

[Referee-10] *John Wiley & Sons*, 1991-2007

[Referee-11] *Gordon & Breach*, 1992

[Referee-12] *IEEE Transactions on VLSI Systems*, Associate Editor (1993-1994)

[Referee-13] *IEEE Transactions on VLSI Systems*, Editor-in-Chief (1995-1996)

[Referee-14] *International Journal on VLSI Design*, (1992-1998)

[Referee-15] *IEEE Transactions on VLSI Systems*, Steering Committee (2003 - 2007)

Donald W. Bouldin

TECHNICAL CONFERENCE COMMITTEE SERVICE:

[Conference-1] 1978 International Symposium on Gaseous Dielectrics, Knoxville, TN

[Conference-2] 1980 International Symposium on Gaseous Dielectrics, Knoxville, TN

[Conference-3] 1980 IEEE SoutheastCon-80, Nashville, TN

[Conference-4] 1982 International Symposium on Gaseous Dielectrics, Knoxville, TN

[Conference-5] 1984 International Symposium on Gaseous Dielectrics, Knoxville, TN

[Conference-6] 1987 IEEE Computer Society Workshop on VLSI, Clearwater, FL

[Conference-7] 1987 International Symposium on Gaseous Dielectrics, Knoxville, TN

[Conference-8] 1988 IEEE Computer Society Workshop on VLSI, Clearwater, FL

[Conference-9] 1988 IEEE SoutheastCon-88, Knoxville, TN

[Conference-10] 1988 VLSI Education Conference, Santa Clara, CA

[Conference-11] 1989 IEEE Computer Society Workshop on VLSI, Clearwater, FL

[Conference-12] 1989 VLSI Education Conference, Santa Clara, CA

[Conference-13] 1990 IEEE Computer Society Workshop on VLSI, Tampa, FL

[Conference-14] 1990 IEEE Southeastern Symposium on System Theory, Cookeville, TN

[Conference-15] 1990 Workshop on Microelectronic Systems Education in the 1990's, Washington, DC

[Conference-16] 1991 IEEE MultiChip Module Workshop, Santa Cruz, CA

[Conference-17] 1991 IEEE Computer Society Workshop on VLSI, Orlando, FL

[Conference-18] 1991 Great Lakes Symposium on VLSI, Kalamazoo, MI

[Conference-19] 1991 Advanced Research in VLSI Conference, Santa Cruz, CA

[Conference-20] 1991 Microelectronic System Education Conference, San Jose, CA

[Conference-21] 1991 International Test Conference, Nashville, TN

[Conference-22] 1992 IEEE Computer Society Workshop on VLSI, Clearwater, FL

[Conference-23] 1992 Great Lakes Symposium on VLSI, Kalamazoo, MI

[Conference-24] 1992 IEEE MultiChip Module Workshop, Santa Cruz, CA

TECHNICAL CONFERENCE COMMITTEE SERVICE (continued):

[Conference-25] 1993 IEEE MultiChip Module Workshop, Santa Cruz, CA

[Conference-26] 1994 IEEE MultiChip Module Workshop, Santa Cruz, CA

[Conference-27] 1995 IEEE MultiChip Module Workshop, Santa Cruz, CA

[Conference-28] 1995 VLSI Design Conference, Bangalore, INDIA

[Conference-29] 1996 IEEE MultiChip Module Workshop, Santa Cruz, CA

[Conference-30] 1996 VLSI Design Conference, Bangalore, INDIA

[Conference-31] 1996 IEEE Symposium on Custom Computing Machines (FCCM), Napa Valley, CA

[Conference-32] 1996 IEEE Computer Society Workshop on VLSI, Clearwater, FL

[Conference-33] 1997 IEEE MultiChip Module Workshop, Santa Cruz, CA

[Conference-34] 1997 VLSI Design Conference, Hyderabad, INDIA

[Conference-35] 1997 IEEE VLSI Test Symposium, Monterey, CA

[Conference-36] 1997 IEEE Symposium on Custom Computing Machines (FCCM), Napa Valley, CA

[Conference-37] 1997 International Intersociety Electronic Packaging Conference, Mauna Lani, HI

[Conference-38] 1997 IEEE Computer Society International Conference on Microelectronic Systems Education, Arlington, VA

[Conference-39] 1997 Advanced Research in VLSI Conference, Ann Arbor, MI

[Conference-40] 1997 IFIP International Conference on VLSI, Gramado, BRAZIL

[Conference-41] 1998 IEEE MultiChip Module Workshop, Santa Cruz, CA

[Conference-42] 1998 IEEE Symposium on Custom Computing Machines (FCCM), Napa Valley, CA

[Conference-43] 1998 Advanced Research in VLSI Conference, Atlanta, GA

[Conference-44] 1998 European Workshop on Microelectronics Education, Noordwijkerhout, NETHERLANDS

[Conference-45] 1999 IEEE Symposium on Custom Computing Machines (FCCM), Napa Valley, CA

TECHNICAL CONFERENCE COMMITTEE SERVICE (continued):

[Conference-46] 1999 IEEE Computer Society International Conference on Microelectronic Systems Education, Arlington, VA

[Conference-47] 1999 Symposium on Integrated Circuits and Systems Design, Rio, BRAZIL

[Conference-48] 2000 IEEE Symposium on Custom Computing Machines (FCCM), Napa Valley, CA

[Conference-49] 2000 IEEE International Conference on Electronics, Circuits and Systems, Kaslik, LEBANON

[Conference-50] 2000 Symposium on Integrated Circuits and Systems Design, Manaus, BRAZIL

[Conference-51] 2000 European Workshop on Microelectronics Education, Aix-en-Provence, FRANCE

[Conference-52] 2001 IEEE Symposium on Custom Computing Machines, Rohert Park, CA

[Conference-53] 2001 IEEE Computer Society International Conference on Microelectronic Systems Education, Las Vegas, NV

[Conference-54] 2001 Symposium on Integrated Circuits and Systems Design, Rio, BRAZIL

[Conference-55] 2002 International Workshop on Electronic Design Test and Applications, Christchurch, NEW ZEALAND

[Conference-56] 2002 IEEE Computer Society Symposium on VLSI, Pittsburgh, PA

[Conference-57] 2002 IEEE Symposium on Custom Computing Machines (FCCM), Napa Valley, CA

[Conference-58] 2002 European Workshop on Microelectronics Education, Vigo, SPAIN

[Conference-59] 2002 IEEE Symposium on Custom Computing Machines (FCCM), Napa Valley, CA

[Conference-60] 2002 IEEE International Conference on Field-Programmable Technology, Hong Kong, CHINA

[Conference-61] 2003 IEEE Computer Society Symposium on VLSI, Clearwater, FL

[Conference-62] 2003 IEEE Symposium on Custom Computing Machines (FCCM), Napa Valley, CA

[Conference-63] 2003 Northeast Workshop on Circuits and Systems, Montreal, CANADA

TECHNICAL CONFERENCE COMMITTEE SERVICE (continued):

[Conference-64] 2003 IEEE Computer Society International Conference on Microelectronic Systems Education, Anaheim, CA

[Conference-65] 2003 IEEE International Conference on Field-Programmable Technology, Tokyo, JAPAN

[Conference-66] 2004 International Workshop on Electronic Design Test and Applications, Perth, AUSTRALIA

[Conference-67] 2004 IEEE Computer Society Symposium on VLSI, Lafayette, LA

[Conference-68] 2004 Design Automation and Test in Europe, Paris, FRANCE

[Conference-69] 2004 IEEE Symposium on Custom Computing Machines (FCCM), Napa Valley, CA

[Conference-70] 2004 European Workshop on Microelectronics Education, Lausanne, SWITZERLAND

[Conference-71] 2004 Reconfigurable Architectures Workshop, Santa Fe, NM

[Conference-72] 2004 IEEE International Conference on Field-Programmable Technology, Brisbane, AUSTRALIA

[Conference-73] 2004 Northeast Workshop on Circuits and Systems, Montreal, CANADA

[Conference-74] 2005 Reconfigurable Architectures Workshop, Denver, CO

[Conference-75] 2005 IEEE Symposium on Custom Computing Machines (FCCM), Napa Valley, CA

[Conference-76] 2005 IEEE Computer Society Symposium on VLSI, Clearwater Beach, FL

[Conference-77] 2005 IEEE Computer Society International Conference on Microelectronic Systems Education, Anaheim, CA

[Conference-78] 2005 Engineering of Reconfigurable Systems and Algorithms Conference, Las Vegas, NV

[Conference-79] 2005 Northeast Workshop on Circuits and Systems, Quebec City, CANADA

[Conference-80] 2005 Midwest Symp. on Circuits and Systems, Cincinnati, OH

[Conference-81] 2005 IFIP VLSI-System-on-Chip Conference, Perth, AUSTRALIA

[Conference-82] 2005 EduTech Conference, Perth, AUSTRALIA

[Conference-83] 2005 Combined Exhibition of Advanced Technologies (CEATEC), Tokyo, JAPAN

TECHNICAL CONFERENCE COMMITTEE SERVICE (continued):

[Conference-84] 2006 Mobile Computing Hardware Architectures, Kauai, HI

[Conference-85] 2006 IEEE Computer Society Symposium on VLSI, Karlsruhe, Germany

[Conference-86] 2006 Reconfigurable Computing Education, Karlsruhe, Germany

[Conference-87] 2006 International Workshop on Electronic Design Test and Applications, Kuala Lumpur, MALAYSIA

[Conference-88] 2006 IEEE Conf. on Application-specific Systems, Architectures and Processors, Steamboat Springs, CO

[Conference-89] 2006 European Workshop on Microelectronics Education, Stockholm, SWEDEN

[Conference-90] 2006 Northeast Workshop on Circuits and Systems, Gatineau, CANADA

[Conference-91] 2006 IFIP VLSI-System-on-Chip Conference, Nice, FRANCE

[Conference-92] 2006 IEEE Symposium on Custom Computing Machines (FCCM), Napa Valley, CA

[Conference-93] 2006 Engineering of Reconfigurable Systems and Algorithms Conference, Las Vegas, NV

[Conference-94] 2007 IEEE Conf. on Application-specific Systems, Architectures and Processors, Montreal, CANADA

[Conference-95] 2007 IEEE Computer Society Symposium on VLSI, Porto Allegre, Brazil

[Conference-96] 2007 Reconfigurable Computing Education, Porto Allegre, Brazil

[Conference-97] 2007 Midwest Symp. on Circuits and Systems, Montreal, CANADA

[Conference-98] 2007 IEEE Computer Society International Conference on Microelectronic Systems Education, San Diego, CA

[Conference-99] 2007 Engineering of Reconfigurable Systems and Algorithms Conference, Las Vegas, NV

[Conference-100] 2008 International Workshop on Electronic Design Test and Applications, Hong Kong, CHINA

[Conference-101] 2008 Midwest Symp. on Circuits and Systems, Knoxville, TN

TECHNICAL CONFERENCE COMMITTEE SERVICE (continued):

[Conference-102] 2009 IEEE Computer Society International Conference on Microelectronic Systems Education, San Francisco, CA

[Conference-103] 2011 IEEE Computer Society International Conference on Microelectronic Systems Education, San Diego, CA

[Conference-104] 2012 European Workshop on Microelectroncs Education, Grenoble, France

HONORS:

[Honor-1] Naval R.O.T.C. Scholarship (1967-1967).

[Honor-2] Georgia Tech Tuition Scholarship (1967-1968).

[Honor-3] Vanderbilt University Graduate Teaching Fellowship (1972-1975).

[Honor-4] NIH Eye Institute Travel Fellowship (1975-1975).

[Honor-5] U.S. Navy Achievement Medal (1972).

[Honor-6] Sigma Xi, National Research Honor Society (1974-present).

[Honor-7] Tau Beta Pi, National Engineering Honor Society (1974-present).

[Honor-8] Outstanding Young Teacher Award, A. S. E. E. , University of Tennessee Chapter (1980-1981).

[Honor-9] I. B. M. Professorship at the University of Tennessee (1983-1987).

[Honor-10] Outstanding Service Award, IEEE East Tennessee Section (1985).

[Honor-11] Technical Activities Board Pioneer Award, IEEE Computer Society (1988).

[Honor-12] Meritorius Service Award, IEEE Computer Society (1989).

[Honor-13] Chancellor's Research and Creative Achievement Award (1997).

[Honor-14] Fellow, IEEE (1997).

[Honor-15] Allen and Hoshall Award for Teaching and Research, Univ. of Tennessee (2003).

[Honor-16] Engineering Research Fellow Award, Univ. of Tennessee (2003).

[Honor-17] Charles E. Ferris Award, Technical Society of Knoxville (2006).

Donald W. Bouldin

MILITARY EXPERIENCE:

[Military-1] Naval R. O. T. C. , Vanderbilt University (1963-1967).

[Military-2] Shipboard Electronics Officer (1968-1969). Supervised twenty technicians in in maintaining radar, communication and electronic countermeasures equipment in U.S.S. Worden (DLG-l8), Guided Missile Frigate based in San Diego, CA and operated in the Western Pacific Ocean (off Vietnam).

[Military-3] Squadron Electronics Officer (1969-1971). Provided guidance to electronics officers of combatant ships; implemented and supervised testing and evaluation of experimental electronic equipment; Staff, Commander Destroyer Squadron Fourteen based in Mayport, FL and operated in the Mediterranean Sea.

[Military-4] Naval Training Advisor (1971-1972). Provided liaison to foreign military officers for the purpose of improving technical training of South Vietnamese Navy at the Naval Training Center, Saigon, Republic of Vietnam.

[Military-5] Naval Reserve Research Unit, Vanderbilt University (1972-1975).

[Military-6] Naval Reserve Standby Unit (1975-1987). Retired as Lieutenant Commander with Honorable Discharge.

Donald W. Bouldin

DOCTORAL DISSERTATIONS SUPERVISED:

[Dissertation-1] Jatko, W. B., "A VLSI-based System for Stamp Inspection" (May 1990).

[Dissertation-2] Mukund, P. R., "Optimal Clock Distribution in VLSI Systems" (December 1990).

[Dissertation-3] Takla, M. B., "A Quantitative Approach for Managing the Multi-Dimensional Design Space of VLSI" (May 1992).

[Dissertation-4] Dehkordi, P. K., "Design for Packagability–The Impact of Bonding and Interconnection Technology on the Design of VLSI Dies" (May 1992).

[Dissertation-5] Casey, M. E., "An Analysis of Counting Losses in Positron Emission Tomography" (December 1992).

[Dissertation-6] Newport, D. F., "Architectural Considerations in Using VLSI" (December 1995).

[Dissertation-7] Chandra, T., "Intrinsic Area-Array Placement and Routing of ICs" (May 1997).

[Dissertation-8] Ramamurthi, Karthi, "Optimal Partitioning of Microelectronic Systems for Multi-Chip Modules" (May 1999).

[Dissertation-9] Kerkiz, N., "Multi-FPGA Partitioning for Adaptive Computing Systems" (December 2000).

[Dissertation-10] Clonts, L. G., "Development of a Simulation Backplane with Dynamic Configurability" (May 2001).

[Dissertation-11] Ong, S. W., "Data Flow Synchronization for Adaptive Computing System Applications" (May 2001).

[Dissertation-12] Karakaya, F., "Automated Exploration of the ASIC Design Space for Minimum Power-Delay-Area Product at the Register Transfer Level" (May 2004).

[Dissertation-13] Earl, D., "Development of an FPGA-based Hardware Evaluation System for Use with GA-designed Artificial Neural Networks" (May 2004).

[Dissertation-14] Du, H., "Efficient Image Processing in Resource-constrained Visual Sensor Networks" (Dec. 2006)

Donald W. Bouldin

MASTER'S THESES SUPERVISED:

[Thesis-1] Davies, D. L., "Edge Detection in Digital Images Using Small Mask and Vector Operators and the Method of Polar Histograms" (December 1978).

[Thesis-2] Bryant, D. J., "Evaluation of Edge Operators Using Relative and Absolute Grading" (December 1978).

[Thesis-3] Charirnwanit, S., "Techniques for Generating Stereoscopic Displays with a Minicomputer" (December 1978).

[Thesis-4] Saeed, I. M., "A Low-Cost Microprogram Development and Learning Kit" (March 1980).

[Thesis-5] Barker, L. W., "Development of a Microcomputer-Based Flowmeter for Liquid Volume Flow in Partially Full Pipes" (June 1980).

[Thesis-6] Eason, R. O., "Development and Comparison of Algorithms for Generating a Scan Sequence for a Random Access Scanner" (August 1980).

[Thesis-7] Gilbert, G. R., "Development of a Procedure and Design of an Instrument to Correct for Pulse Pile-up Distortion" (June 1981).

[Thesis-8] Aimthikul, Y., "Computer-Generated Speech" (December 1981).

[Thesis-9] Eldridge, E. M., "Microcomputer Control for Feeding Material Into a Chemical Process" (December 1981).

[Thesis-10] Jones, D. C., "A Microprocessor-Based Controller for Radioteletype Communications" (August 1982).

[Thesis-11] Hsu, J. A., "Design of an Interface Between a Shorthand Machine and a Word Processing Microcomputer" (December 1982).

[Thesis-12] Rowe, J. C., "A Microcomputer-Based Flowmeter for Determining Average Liquid Phase Flow in a Two-Phase Fluid" (December 1982).

[Thesis-13] Raible, L. A., "An Image Processor for a MMW Radar Seeker" (December 1982).

[Thesis-14] Syed, N. U., "Minicomputer Controlled Fast Expansion of Speech Signals for Improving Intelligibility" (March 1983).

[Thesis-15] Kim, Y. P., "Computer-Aided Design of Digital Systems Using Pattern Recognition and Menu Selection Techniques" (December 1983).

MASTER'S THESES SUPERVISED (continued):

[Thesis-16] Manges, W. M., "Development of an Integrated Control and Measurement System" (March 1984).

[Thesis-17] Tomcik, T. M., "Computer-Aided Design of Algorithmic State Controllers" (March 1984).

[Thesis-18] Majure, R. G., "A Color Graphics System for a Power Plant Monitoring System" (March 1984).

[Thesis-19] Trivedi, M. P., "Diagnostics of VLSI Floating-Point Processors" (August 1984).

[Thesis-20] Jatko, W. B., "A Microcomputer-Based Averaging Flowmeter using the Forth Programming Language" (June 1985).

[Thesis-21] Ahsan, Z., "Asynchronous File Transfer Between the TI-990/12 Minicomputer and Other Computers" (December 1985).

[Thesis-22] Flanagan, E. B., "Development of an On-Line Monitor for Mercury" (March 1986).

[Thesis-23] Shell, M. A., "The Design, Development and Testing of a Precision Temperature Monitoring System" (June 1986).

[Thesis-24] Younkin, J. R., "Design and Implementation of an Electronic Radiographic System Using Image Processing Techniques" (June 1986).

[Thesis-25] Matheson, D. W., "Production Test Station Networking and Collection of Test Results" (June 1986).

[Thesis-26] Sharp, R. J., "Low-Cost, Three-Dimensional Computer Vision System for Part Positioning" (December 1986).

[Thesis-27] Newport, D. F., "A VLSI Coprocessor Design Frame" (December 1986).

[Thesis-28] Hussain, S. K., "A Computer-Aided Design Software Package for Logic Diagram Generation" (December 1987).

[Thesis-29] Butler, P. L., "Design and Implementation of a Parallel Processing Machine for Artificial Intelligence Applications" (December 1987).

[Thesis-30] Foy, J. A., "An Expert System for Diagnostic Interpretation and Relay Ladder Logic Test Generation for Programmable Logic Controllers" (June 1988).

[Thesis-31] Crutcher, R. I., "Analysis of a Data Isolation Technique for a Broadband Local Area Network" (June 1988).

MASTER'S THESES SUPERVISED (continued):

[Thesis-32] Bryson, D. A., "Implementation of a Dynamic Matrix Control Algorithm with Constraints" (August 1988).

[Thesis-33] Hilger, J. E., "Hierarchical Clustering of Digital Circuits" (August 1988).

[Thesis-34] Kumar, R. R., "A VLSI Robotic Controller" (August 1988).

[Thesis-35] Rinehart, K. A., "Design and Development of an Intelligent Quad Video Frame Buffer" (December 1988).

[Thesis-36] Sitter, M. S., "Hardware Design of TMS 9995 Interface Pod" (December 1988).

[Thesis-37] Linehan, D. E., "An Application-Specific Design of a Self-Diagnosing Encoder Counter" (May 1989).

[Thesis-38] Mathai, G. A., "Automated Methods for Signal Validation and Anomaly Detection" (May 1989).

[Thesis-39] Rochelle, R. B., "A Programmable High-Speed Data Acquisition Controller" (May 1989).

[Thesis-40] Hoffheins, B. F., "Using Sensor Arrays and Pattern Recognition to Identify Organic Compounds" (August 1989).

[Thesis-41] Armstrong, G. A., "Design and Implementation of a Moment Invariant Algorithm in VLSI for Pattern Recognition Applications" (December 1989).

[Thesis-42] Cox, R. H., "Final Manufacturing Test of a Resolver Position Tracker" (May 1990).

[Thesis-43] Broadaway, E. V., "A Transportable, Knowledge-Based Assistant for Troubleshooting Industrial Electronic Equipment" (May 1990).

[Thesis-44] Luchuk, A. A., "A Study of Vector and Parallel Processing" (August 1991).

[Thesis-45] Bass, R. M., "Design and Implementation of a Microcomputer-Based Video Analysis System" (May 1992).

[Thesis-46] Gleason, S. S., "Design and Implementation of a Perforation Registration System" (May 1992).

[Thesis-47] Patel, N. D., "Development and Automation of a Procedure for Improved Timing Analysis of Field-Programmable Gate Arrays" (May 1992).

[Thesis-48] Perry, T. O., "Design and Implementation of a Gate Array for Interfaces" (December 1992).

MASTER'S THESES SUPERVISED (continued):

[Thesis-49] Zimmerman, S. L., "A Real-Time Omni-direction Image Processing System" (December 1992).

[Thesis-50] Clonts, L. G., "Design and Synthesis of an Intel 80C51-compatible Microprocessor Optimized for Reduced Instruction Time (RIT) Execution" (May 1993).

[Thesis-51] Sawan, T. E., "An Investigation of Leafcell Design Methodologies" (Dec. 1993).

[Thesis-52] Tolnas, B. E., "Multi-objective Optimization of VLSI Design Space" (April 1995).

[Thesis-53] Horner, R. N., "Design and Characterization of Monolithic Digital-to-Analog Converter Structures" (August 1995).

[Thesis-54] Chattapadhyay, S., "MCM Placement Considering Area and Thermal Constraints Simultaneously" (August, 1995).

[Thesis-55] Powell, T., "Performance Comparison of MCM-D and SMT Packaging Technologies for a DSP Subsystem" (Dec. 1995).

[Thesis-56] Quinn, D. A., "Simultaneous Hierarchical Physical Design of Integrated Circuits and Multi-Chip Modules" (Dec. 1995).

[Thesis-57] Shen, Z., "Development of an Environment for Reconfigurable Computing" (Dec. 1996).

[Thesis-58] York, J., "Enhancment of MCM Testability Using an On-Substrate FPGA" (August 1997).

[Thesis-59] Chokhavala, A., "Architectural Tradeoffs for Malleable Signal Processing" (Dec. 1997).

[Thesis-60] Levine, B., "A System for the Implementation of Image Processing Algorithms on Configurable Computing Hardware" (August 1999).

[Thesis-61] Natarajan, S., "Development and Verification of Library Cells for Reconfigurable Logic" (August 1999).

[Thesis-62] Kelly, M., "Verification of Portable Intellectual Property Blocks for FPGAs" (Dec. 1999).

[Thesis-63] Clonts, L., "A Simulation Backplane with Dynamic Configurability for the Simulation of MEMS" (Dec. 2000).

[Thesis-64] Xie, J., "Automated Verification of Synthesizable and Portable Virtual Components" (Dec. 2001).

MASTER'S THESES SUPERVISED (continued):

[Thesis-65] Royer, M, "ASIC Technology Migrations: A design guide for first-pass success" (Dec. 2001).

[Thesis-66] Srijanto, B., "Implementing Neural Network-Based Face Detection onto a Reconfigurable Computing System Using CHAMPION" (Aug. 2002).

[Thesis-67] Koay, T., "Verification of Intellectual Property Blocks Using Reconfigurable Hardware" (Aug. 2002).

[Thesis-68] Ku, C., "Size, Speed and Power Analysis for Application-specific Integrated Circuits Using Synthesis" (Dec. 2002)

[Thesis-69] Miller, A., "Development and Verification of Parameterized Digital Signal Processing Macros for Microelectronic Systems" (Aug. 2003).

[Thesis-70] Fu, X., "Design and Verification of the Data Encryption Standard for ASICs and FPGAs" (Aug. 2003).

[Thesis-71] Devalapalli, S., "Development of SystemC Modules from HDL for System-on-Chip Applications" (May 2004).

[Thesis-72] Patel, K., "Quality and Versatility of Automatic Leafcell Generation" (May 2004).

[Thesis-73] Raghuraman, N., "Animating Logic Simulations" (May 2004).

[Thesis-74] Balakrishnan, A., "An Experimental Study of the Accuracy of Multiple Power Estimation Methods" (Aug. 2004).

[Thesis-75] Srivastava, R., "An Open Core System-on-Chip Platform" (Aug. 2004).

[Thesis-76] Polisetty, S., "Hardware Acceleration of the Embedded Zerotree Wavelet Algorithm" (Dec. 2004).

[Thesis-77] Wala, M., "Using Platform Express for System-on-Chip Design" (May 2005).

[Thesis-78] Jiang, W., "Enhancing System-on-Chip Verification Using Embedded Test Structures" (Dec. 2005)

[Thesis-79] Fields, S., "Hardware Design and Implementation of Role-Based Cryptography" (Dec. 2005)

[Thesis-80] Chereches, G., "Design and Verification of a Reusable Self-Reconfigurable Gate Array Architecture" (Dec. 2005)

MASTER'S THESES SUPERVISED (continued):

[Thesis-81] Khor, C., "Tutorials for the Xilinx XUP Board" (Dec. 2005)

[Thesis-82] Veluri, P., "MS Comprehensive Exam" (Dec. 2005)

[Thesis-83] Stinson, B., "Design and Test of an Event Detector and Locator for the ReflectoActive Seals System" (May. 2006)

[Thesis-84] Marwah, T., "System-on-Chip Design and Test with Embedded Debug Capabilities" (Aug. 2006)

[Thesis-85] Turnmire, J., "Automated Design Space Exploration for Digital Hardware" (Aug. 2006)

[Thesis-86] Dennis, N., "Power Spectral Density Estimation on an FPGA" M.S. 501 Project (Aug. 2006)

[Thesis-87] Mallette, C., "High Performance Computer Operating Systems: Windows vx. Linux" M.S. 501 Project (Aug. 2006)

[Thesis-88] Carroll, N. "Source Code Revision Control" M.S. 501 Project (Dec. 2006)

[Thesis-89] Girinathan, V. "Automation for Hardware Acceleration of Post-Layout Simulation of Integrated Circuits" M.S. 501 Project (Dec. 2006)

[Thesis-90] Jain, A. "FPGA-Based Image Processing" M.S. 501 Project (Dec. 2006)

[Thesis-91] Subramanian, K., "MS Comprehensive Exam" (Dec. 2006)

[Thesis-92] Shaik, I., "MS Comprehensive Exam" (Dec. 2006)

[Thesis-93] Chimakurthy, P. "Using Physical Compilation to Implement a SoC Platform" (Dec. 2006)

[Thesis-94] Liang, G. "Optimization of Digital Filter Design Using Hardware Accelerated Simulation" (May, 2007)

[Thesis-95] Yelagondanahalli, V., "Simulink to Silicon" M.S. 501 Project (Aug. 2007)

[Thesis-96] Sundaramurthy, K., "ATPG and Scan Chain Diagnostics for Failure Analysis of Integrated Circuits" M.S. 501 Project (Aug. 2007)

[Thesis-97] Parla, P., "MS Comprehensive Exam" (Dec. 2006)

[Thesis-98] Sharafat, M., "FPGA-based Image Analysis System for Cotton Classing" (Dec. 2007)

Donald W. Bouldin

PUBLICATIONS:

[Publication-1] Bouldin, D. W. and J. R. Bourne, "A Hybrid Analog-Digital System for Generation of Dynamic Random Dot Stereograms", *Proceedings of IEEE SoutheastCon-74*, Orlando, FL, pp. 188-190 (May 1974).

[Publication-2] Bouldin, D. W. and J. R. Bourne, "A Minicomputing System for Simultaneous Random Dot Stereogram Generation and Evoked Potential Analysis", *Proceedings of the 27th Annual Conference on Engineering in Medicine and Biology*, Philadelphia, PA, p. 227 (October 1974).

[Publication-3] Bouldin, D. W. and G. E. Cook, "Dual Input Describing Function for Multi-Valued Nonlinearities Subjected to Sine Wave Plus Random Dither", *Proceedings of the 17th Midwest Symposium on Circuits and Systems*, Lawrence, KS, pp. 5l-62 (September 1974).

[Publication-4] Bouldin, D. W., Bourne, J. R. and R. Fox, "Visually Evoked Cortical Potentials in Cyclopean Vision", *Program the University of Tennessee Fall Neuroscience Meeting*, Memphis, TN, p. 45 (December 1974).

[Publication-5] Bouldin, D. W., Bourne, J. R. and R. Fox, "Lambda Waves Elicited by Cyclopean Contour Movement", *Program of the Spring Meeting of the Association for Research in Vision and Ophthalmology*, Sarasota, FL, p. 90 (May 1975).

[Publication-6] Moore, M. L., Bouldin, D. W., Fox, R. and J. R. Bourne, "Acquisition and Analysis of Psychophysical Data Obtained in Response to Stereoscopic Stimuli", *Proceedings of IEEE SoutheastCon-75*, Charlotte, NC, pp. ID-2-1 thru ID-2-4 (April 1975).

[Publication-7] Moore, M. L., D. W. Bouldin, R. Fox and J. R. Bourne, "Minicomputer Utilization in Psychophysical Investigations of Binocular Depth Perception", *Proceedings of ACM Southeast Region Meeting*, Chapel Hill, NC, pp. 341-350 (May 1975).

[Publication-8] Bouldin, D. W., "Visual Evoked Cortical Potentials Elicited by Dynamic Random Dot Stereograms", Ph.D. Dissertation, Vanderbilt University, Ann Arbor, MI: University Microfilms (August 1975).

[Publication-9] Bouldin, D. W., "Minicomputing System for Testing of Binocular Vision", *Proceedings of the 8th Annual Southeastern Symposium on System Theory*, Knoxville, TN, pp. 164-167 (April 1976).

[Publication-10] Christophorou, L. G., James, D. R., Pai, R. Y., Pace, M. O., Mathis, R. A. and D. W. Bouldin, "High Voltage Research (Breakdown Strength of Gaseous and Liquid Insulators)", ORNL/TM-5604, (April - June 1976).

PUBLICATIONS (continued):

[Publication-11] Christophorou, L. G., James, D. R., Pai, R. Y., Pace, M. O., Mathis, R. A. and D. W. Bouldin, "High Voltage Research (Breakdown Strength of Gaseous and Liquid Insulators)", ORNL/TM-5713, (July - September 1976).

[Publication-12] Christophorou, L. G., James, D. R., Pai, R. Y., Pace, M. O., Mathis, R. A. and D. W. Bouldin, "High Voltage Research (Breakdown Strength of Gaseous and Liquid Insulators)", ORNL/TM-5806, (October - December 1976).

[Publication-13] Christophorou, L. G., James, D. R., Pai, R. Y., Pace, M. O., Mathis, R. A. and D. W. Bouldin, "High Voltage Research (Breakdown Strength of Gaseous and Liquid Insulators)", ORNL/TM-5917, (January - March 1977).

[Publication-14] Christophorou, L. G., James, D. R., Pai, R. Y., Pace, M. O., Mathis, R. A. and D. W. Bouldin, "High Voltage Research (Breakdown Strength of Gaseous and Liquid Insulators)", ORNL/TM-6113 (April - September 1977).

[Publication-15] Pace, M. O., Christophorou, L. G., James, D. R., Pai, R. Y., Mathis, R. A. and D. W. Bouldin, "Improved Unitary and Multicomponent Gaseous Insulators", *Proceedings of IEEE Conference on Electrical/Electronics Insulation*, Chicago, IL, pp. 313-317 (September 1977).

[Publication-16] James, D. R., Christophorou, L. G., Pai, R. Y., Pace, M. O., Mathis, R. A. and D. W. Bouldin, "Breakdown Voltages of Some New Unitary and Multicomponent Gas Mixtures", *1977 Annual Report of the Conference on Electrical Insulation and Dielectric Phenomena*, Colonie, NY, pp. 409-420 (October 1977).

[Publication-17] Pace, M. O., Christophorou, L. G., James, D. R., Pai, R. Y., Mathis, R. A. and D. W. Bouldin, "Improved Unitary and Multicomponent Gaseous Insulators", *IEEE Transactions on Electrical Insulation*, vol. EI-l3, no. 1, pp. 31-36 (February 1978).

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