Overview of FPGAs and ASICs

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A VARIETY OF ICS ARE POSSIBLE

- Full Custom Digital
- Custom Standard
  Cell Digital Audio
- Custom Analog
- Semi-Custom Digital
- I&C
APPLICATIONS MAY USE STANDARD ICs or FPGAs/ASICs

- **Standard IC (off-the-shelf)**
  - SSI/MSI
  - LSI/VLSI

- **ASIC (User-specified)**
  - Semicustom
    - User-programmable
      - User-programmable ASICS
        - PLDs
        - FPGAs
    - Structured ASICS
    - Standard Library Cells
  - Custom
    - Analog/Digital Mixed-Signal
      - (All Masks)

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Intel spent $3 billion to construct and equip its integrated circuit fabrication facility in Chandler, Arizona.

The foundry produces 300-mm wafers using feature sizes of 45 nanometers.

http://www.intel.com/
According to SemaTech, a mask set for 65-nm costs $3 million.
THE COST PER GATE DECREASES AS THE DENSITY OF AN I.C. INCREASES

- Microprocessors and other off-the-shelf LSI/VLSI chips are the most cost-effective because millions of gates are available in a single chip. ($0.0001/gate; 20,000 gates/pin)

- SSI/MSI glue logic chips are the least cost-effective because only a few gates are available in a single chip. ($0.01/gate; 1-3 gates/pin)
SYSTEM FUNCTIONS ARE OFTEN SPLIT BETWEEN THE CPU AND AN ASIC

- The most economical means of implementing logic functions is to use a microprocessor.
- When the microprocessor is too slow or too busy to handle some fast inputs and outputs, an ASIC can be used to implement high-speed concurrent operations.
REAL-TIME EMBEDDED SYSTEMS

- An electronic system containing a CPU without an operating system visible to the end-user.
- It interacts with peripheral devices within fixed time constraints.
- A minimum of resources are employed to perform the required tasks.
- In addition to functionality and cost, other constraints include power management, fault tolerance, quality of service, security, etc.
ECE 551-552

- **ECE 551:**
  - Pairs create project using VHDL
  - Simulate pre-synthesis and post-layout
  - Demonstrate using 200K-gate Xilinx FPGA on Spartan3 Board with I/O
  - Implement on screen only using Altera FPGA

- **ECE 552:**
  - Team of 4 will create and reuse IP blocks
  - Programmable SoC design with DSP
  - Demonstrate using 1M-gate Virtex2-Pro/XUP
  - Lectures on alternate weeks
ECE 651 - 652

• ECE 651:
  – Perform custom IC design (but not submit for fab)
  – Compare manual design vs. automated tools
  – Study nanometer design issues (cross-talk, power)

• ECE 652:
  – Extend our System-on-Chip platform
  – Design Testable ASIC for nanometer process
  – Optimize SoC at both synthesis and physical levels
  – Lectures on alternate weeks
PROGRAMMABLE LOGIC DEVICES ARE BEST FOR SMALL DESIGNS WITH I/O

- Vendor prefabricates multiple sets of ANDs and ORs with programmable connections
- User specifies connections to implement desired logic functions
- Replaces 200 to 8,000 gates with single package of 20-84 pins
- Electrically programmable (and erasable) by the user one at a time within minutes
- PC-based development system costs $1K
The internal logic and interconnect of a reconfigurable component (FPGA) may be specified by the user and changed at any time.
STRUCTURED ASICS

- Choose Slice and RapidReady IP
- Design System RTL (RapidBuilder, RapidView)
- Physical RTL Optimization (RapidPro)
- Physical Synthesis
- Amplify RapidChip, RapidChecks
- Handoff to LSI Logic
- Design Completion
- Manufacture

- Match Slice to IP, gate count, memory, and I/O requirements
- Generate and integrate memory, I/O and clock RTL with customer logic
- Optimize RTL code for physical implementation
- Chip-level synthesis of RTL to placed gates
- Clock tree synthesis, detailed route, and test generation
- Metal Layer Manufacturing, Packaging and Test

- Clock
- Configurable IO's
- HyperPHY Standard x20
- HyperPHY x4
- GigaBlaze x8
- GigaBlaze x4
- Control IO's
- Configurable IO's

- Diffused Memories
- Transistor Fabric

http://www.rapidchip.com/ → Available from Fujitsu
STANDARD-CELLS ARE BEST FOR HIGH-QUANTITY APPLICATIONS WITH RAM

- Vendor develops library disk files of logic functions (and internal RAM or cache).
- User selects cells and specifies two layers of interconnections.
- After place & route, masks are made for all layers.
- Replaces 20,000 to 2,000,000 gates (or more).
- Workstation-based development system costs more than $200K.
- Turnaround time for prototypes is 8 weeks.
STANDARD-HEIGHT CELL CHIPS CAN ALSO USE EMBEDDED RAM

Space between rows for wiring can be varied as needed.
SPECIAL TECHNIQUES ARE USED FOR LAYOUT OF ANALOG CIRCUITS

- Layouts use multi-gate fingers and common-centroid symmetry to improve matching of devices.
- Poly2-Poly1 capacitors save space.
- Switched-capacitor circuits replace large resistors.
- Guard rings reduce noise.
SHARING MASK/WAFTER COSTS

http://www.ssec.honeywell.com/

http://www.mosis.org/
MIXED-SIGNAL ICS USE BOTH ANALOG AND DIGITAL CIRCUITS

- Solar cells provide power.
- Analog circuit detects when sufficient energy is available.
- Digital circuit provides for series of pulses.
- Infrared LEDs emit output that is detectable 1 mile away.
MICROELECTRONIC SYSTEM DESIGN CONSISTS OF ITERATIVE REFINEMENTS OF SYNTHESIS AND VERIFICATION
CUSTOM IC DESIGN FLOW

1--SCHEMATIC

2--PRE-LAYOUT LOGIC SIMULATION

TimeA = 0(0) ns
Sim End = 1224 ns
Cur2-Cur1 = 0 ns
Cursor1 = 0(0) ns
Cursor2 = 0 ns
TimeA = 0(0) ns
0

3—MANUAL LAYOUT

4--POST-LAYOUT TRANS. SIMULATION
SEMI-CUSTOM DESIGN FLOW OF DIGITAL FPGAS/ASICS

1—HDL

CASE w IS
  WHEN "00" => y <= "1000" ;
  WHEN "01" => y <= "0100" ;
  WHEN "10" => y <= "0010" ;
  WHEN OTHERS => y <= "0001" ;
END CASE ;

2--PRE-SYNTHESIS SIMULATION

3—SYNTHESIS/AUTO LAYOUT

4--POST-LAYOUT SIMULATION
A HARDWARE DESCRIPTION LANGUAGE CAN BE SYNTHESIZED

• The desired functionality and timing may be described using a hardware description language such as VHDL or Verilog and then synthesized into the structural level for a specified device.

• Synthesis involves:
  (1) translation into Boolean equations,
  (2) optimization for area/delay, and then
  (3) mapping to a FPGA or ASIC process (library).

• The physical level is then implemented automatically using a placement and routing program.
HDL DESIGNS CAN BE TARGETED TO MULTIPLE LAYOUTS

HDL architecture behavior of control is:
if left_paddle then
  n_state <= hit_state
elsif n_state <= miss_state
  end if;

SYNPLIFY

SCHEMATIC--A

TECH A

AND

AND

OR

ALTERA
PLACE & ROUTE

PHYSICAL LAYOUT

SCHEMATIC--B

TECH B

OR

AND

OR

XILINX
PLACE & ROUTE

PHYSICAL LAYOUT

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INTELLECTUAL PROPERTY BLOCKS

Design #1 without Planned Reuse

Design #2 without Planned Reuse

Design #3 without Planned Reuse

Design #1 For Reuse

Design #2 WITH IP

Design #3 WITH IP

IP blocks should have well-defined interfaces

Often, IP are more like patches that must be stitched together like a quilt
COLLABORATIVE DESIGN

Collaborative Design of a System-on-Chip
http://www.cs.wright.edu/~tkprasad/courses/soc.html

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PROGRAMMABLE SYSTEM-ON-CHIP

- CPU integrated inside the FPGA package
  - Replaces board with separate CPU and FPGA packages
  - Higher bandwidth and lower latency
  - CPU performs control functions
  - CPU may lack floating-point capability
  - Programmable System-on-Chip (SoC) Platform
  - Can prototype ASIC SoC or an embedded system

http://www.xilinx.com/
• Wire load models were previously used by synthesis to predict layout capacitance accurately. However, these models are failing today.

• Now that wire delays dominate gate delays in nanometer processes, synthesis must be coupled with physical floorplanning to achieve the desired timing goals.

http://www.synopsys.com/
SIGNAL INTEGRITY AND POWER ISSUES ARE ESCALATING

Effects of Crosstalk: Delay Uncertainty

Thresholds

min  nom  max

Series1

Series2

Series3

Series4

Series5

Series6

Series7

Time (ps)

Voltage (V)

http://vlsicad.ucsd.edu/  http://www.tomshardware.com/

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SYSTEM-ON-CHIP REQUIRES CO-DESIGN OF SW AND HW

- Traditional co-design uses C and HDL separately.
- Integration is performed on prototypes after using separate simulators with limited linkage.
- SystemC is now being used for co-simulation at the behavioral level.
- The hardware portion is then automatically translated into HDL.
- The same test bench is used at every level.

http://www.SystemC.org/
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