SCHEMATIC

AND

OR

HDL

SYNTHESIS

PLACE & ROUTE

PHYSICAL LAYOUT

n_state <= hit_state;

elsif n_state <= miss_state

end if;

PHYSICAL LAYOUT

ECE 651
FALL 2001

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COURSE OUTLINE

• Overview
• Digital Logic Using MOSFETs
• Physical Layout Styles
• Physical Placement and Routing
• Using Simulation Wisely
• Digital Circuit Design and Layout
• Homework and MOSIS Projects
A VARIETY OF ASICS ARE POSSIBLE
IMPACT OF VLSI INTEGRATION

• In this application, the same functionality provided by a board with 24 packaged parts has been integrated into one new VLSI chip plus two other parts and placed on a new board.

• The new board uses only 1/5 the board space, costs only 1/2 as much and consumes only 1/4 the power.
VLSI FABRICATION REQUIRES AN EXPENSIVE CAPITAL INVESTMENT

- Clean rooms provide a highly sterile environment.
- Wafers are processed in batches.
- Layers of various materials are stacked vertically like a cake to form transistors and wires.
EACH WAFER CONTAINS MANY DIES
BUT SOME WILL BE DEFECTIVE
SHARING MULTI-PROJECT MASKS AND WAFERS SAVES MONEY
THE INTEL 386 MICROPROCESSOR USED THREE LAYOUT STYLES

- Datapath or bit-slice cells are used for the ALU.
- Memory cells have been tiled into 2-D arrays.
- Row-based layout of standard-height cells provide random functions.
APPLICATIONS MAY USE STANDARD ICs or FPGAs/ASICs

- **Standard IC (off-the-shelf)**
  - SSI/MSI
  - LSI/VLSI

- **ASIC (User-specified)**
  - Semicustom
    - User-programmable
      - PLDs
      - FPGAs
    - Gate Arrays
    - Standard Library Cells
  - Custom
    - Bit-Slice Data Paths
    - Analog/Digital Mixed Technologies (All Masks)
A MASK GATE ARRAY CAN BE STOCKPILED AND THEN PERSONALIZED

- The fabricator provides basic gates with space for interconnect.
- The application designer submits a logic net-list which defines the interconnect layers.
A MASK GATE ARRAY MAY CONTAIN EMBEDDED RAM
STANDARD-HEIGHT CELL DESIGNS REQUIRE ALL MASKS FOR FABRICATION

- Only logic cells which are needed are fabricated.
- Higher performance and less area can be achieved but fabrication takes longer.
STANDARD-HEIGHT CELL CHIPS CAN ALSO USE EMBEDDED RAM

Space between rows for wiring can be varied as needed.
DATAPATH OR BIT-SLICE LAYOUT IS THE MOST EFFICIENT

- The basic cell has been designed with its neighbors in mind.
- One bit has been arrayred 8 times to form a byte.
- Each byte is connected to its neighbor to form a datapath or systolic array.
BEE-TRACKING APPLICATION

- Solar cells provide power.
- Analog circuit detects when sufficient energy is available.
- Digital circuit provides for series of pulses.
- Infrared LEDs emit output that is detectable 1 mile away.
MICROELECTRONIC SYSTEM DESIGN CONSISTS OF ITERATIVE REFINEMENTS OF SYNTHESIS AND VERIFICATION

Requirements

Architectural Specifications

Behavioral Description

Logic Synthesis

Physical Implementation

Prototype

Design Review

Behavioral Simulation

Logical-Level Simulation

Switch-Level Simulation

Measurement
SYNTHESIS AND PLACE & ROUTE SOFTWARE CAN BE USED TO GENERATE THE IMPLEMENTATION
DIGITAL LOGIC USING MOSFETS

• General Modes of Operation of Transistors.
• Digital vs. Analog Demands on Fabrication, Modeling and Simulation.
• Basic MOSFET Operation for nfets and pfets.
• Transistor Sizing for Drive and Speed.
• Building Digital Logic Circuits Using MOSFETs.
TRANSISTOR MODES OF OPERATION

OFF

RESISTIVE (ANALOG)

threshold

OFF

ON (saturated)

VDD

V_{DS}
DIGITAL BEHAVIOR IS LESS DEMANDING OF THE FABRICATION PROCESS THAN ANALOG

• For *analog* designs, we intentionally bias the transistors to operate in the resistive region but this requires that the fabrication process be very precise.

• For *digital* designs, we operate the transistors using only the OFF and SATURATED modes to act like ideal switches.

• Thus, the manufacturing yield for digital transistors is higher and the cost is cheaper.

• Also, switch-level modeling is simpler, so simulation is easier and faster.

• With robust behavior of cheap devices, digital designs can contain millions of transistors.

• There is an economic incentive to maximize the use of digital circuits and then be first to market.
OPERATING A FET IN A DIGITAL MODE

With $V_{ds}$ below threshold, the Nfet is OFF—nonconducting

With $V_{ds} = V_{dd}$, the nfet conducts and becomes SAT
CMOS USES BOTH NFETS AND PFETS
• The channel length, L, is the distance the charge carriers must traverse.

• The width, W, of the transistor determines how many charge carriers traverse the channel in parallel.

• If the fets have identical W/L, the nfet is 2.5x faster than a pfet due to their mobility differences.
CMOS INVERTER OPERATION

When the input is 1:
- Pfet is OFF
- Nfet is ON
- Output is 0

When the input is 0:
- Pfet is ON
- Nfet is OFF
- Output is 1
PHYSICAL LAYOUT STYLES

- CUSTOM CMOS LAYOUT
- STANDARD-HEIGHT CELLS
- DATAPATH BIT-SLICE CELLS
- MEMORY CELLS/PROCESSES
BIT-SLICE CELLS CAN BE ARRAYED AND USED IN A DATAPATH

- A datapath is often used for ALU operations.
 BIT-SLICE CELLS CAN BE ARRAYED FOR N BITS

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A BIT-SLICE CELL KNOWS ITS NEIGHBOR
IN ONE DIMENSION

• Vdd/GND, Control and Ripple Signals are aligned vertically in anticipation of being arrayed.
CHIP WITH NINE ROWS
OF STANDARD-HEIGHT CELLS
LAYOUT OF CMOS INVERTER
ROW OF STANDARD-HEIGHT CELLS
STANDARD-HEIGHT CELL CONSTRUCTION

STEP 1: INPUTS AND FETS
STANDARD-HEIGHT CELL CONSTRUCTION
STEP 2: WIRES, VDD, GND & PLUGS
FINAL LAYOUT OF AND-OR-INVERTER
STANDARD-HEIGHT CELL CONSTRUCTION

SUMMARY
PLACEMENT AND ROUTING

• The goal of placement and routing is to map optimally the structural interconnection of components expressed in a schematic onto the target physical architecture.

• Thus, placement and routing is seeks to minimize the cost of the chip by packing the logic and wires into the smallest possible area.

• The software also tries to minimize the time delays of critical paths so the chip will run fast.

• A combination of area and delay can be expressed as total wire length.

• Since hundreds of components and nets are involved, the task is formidable for humans and very difficult even for clever software.

• The task is highly order dependent so it can be directed by the designer assigning weights to critical nets. Multiple solutions should be obtained and evaluated since they may vary by 30%-50%.
• Since the full task of finding the optimal solution is so formidable, we generally divide and conquer by breaking it into three phases.

• We solve each phase as best we can and then move on to the next phase.

• Similar to the NCAA playoffs with regional matchups and then the Finals, this approach may skip over the true optimum.

The three phases are:

- Placement
- Channel Allocation
- Final Routing
THREE ROWS OF STANDARD-HEIGHT CELLS
THE ORDER OF PLACEMENT AFFECTS THE FINAL RESULT

Sol. # 1

Sol. # 2

Sol. # 3
THE ORDER OF PLACEMENT AFFECTS THE FINAL RESULT

Order = ABC

Area = 125

Order = ABC

Area = 260

Order = ABC

Area = 250
TWO WIRING CHANNELS BETWEEN ROWS
CHANNEL ALLOCATION AND FINAL ROUTING

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## INITIAL ASSESSMENT OF ROUTES NEEDED

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FINAL ROUTING REQUIRES ANOTHER CHANNEL
CHANNEL ALLOCATION AND FINAL ROUTING EXAMPLE
MEMORY CELLS ARE TILED INTO TWO-DIMENSIONAL ARRAYS

- A memory cell knows its neighbors in both directions.
- Internal cache memories use a logic-optimized process.
- Larger external memories use a memory-optimized process.