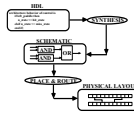
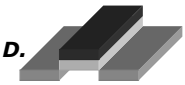
DESIGNING FPGAS & ASICS



Using Synthesis



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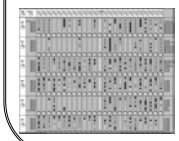
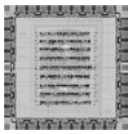
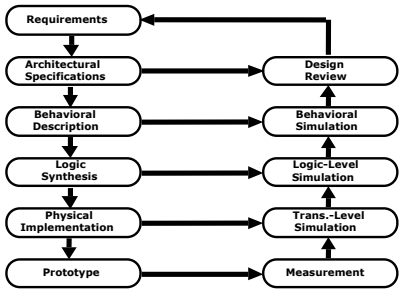




COURSE OUTLINE

- **Overview of FPGAs and ASICs**
- **Using Synthesis**
- **HDL Examples**
- **Simulation and Testing**
- **Physical Place and Route**
- **Testing ASICs**
- **Component Reuse**

MICROELECTRONIC SYSTEM DESIGN CONSISTS OF ITERATIVE REFINEMENTS OF SYNTHESIS AND VERIFICATION



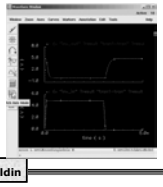
CUSTOM IC DESIGN FLOW

1--SCHEMATIC

2--PRE-LAYOUT LOGIC SIMULATION

3—MANUAL LAYOUT

4--POST-LAYOUT TRANS. SIMULATION



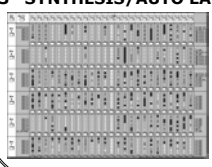
SEMI-CUSTOM DESIGN FLOW OF DIGITAL FPGAS/ASICS

1—HDL

```
CASE w IS
   WHEN "00" => y <= "1000" ;
   WHEN "01" => y <= "0100" ;
   WHEN "10" => y <= "0010" ;
   WHEN OTHERS => y <= "0001";
END CASE ;
```

2--PRE-SYNTHESIS SIMULATION

3—SYNTHESIS/AUTO LAYOUT

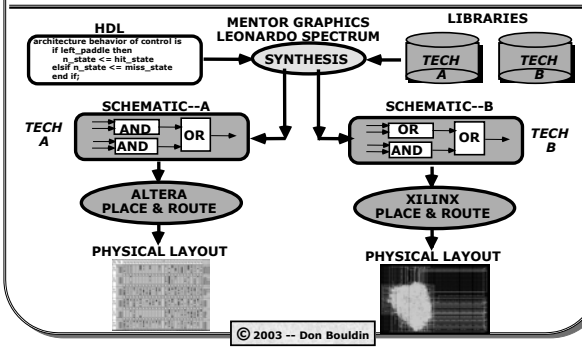


4--POST-LAYOUT SIMULATION

A HARDWARE DESCRIPTION LANGUAGE CAN BE SYNTHESIZED

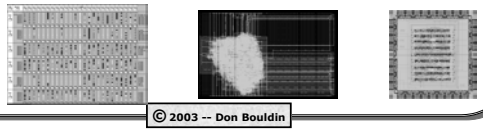
- **The desired functionality and timing may be described using a *hardware description language* such as VHDL or Verilog and then *synthesized* into the structural level for a specified device.**
- ***Synthesis* involves:**
  (1) translation into Boolean equations,
  (2) optimization for area/delay, and then
  (3) mapping to a FPGA or ASIC process (library).
- **The physical level is then implemented automatically using a placement and routing program.**

HDL DESIGNS CAN BE TARGETED TO MULTIPLE LAYOUTS

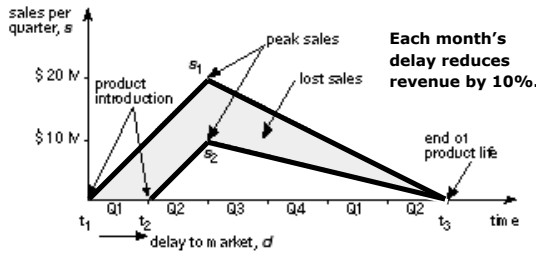


SYNTHESIS AND FPGAS CAN REDUCE TIME-TO-MARKET

- Synthesis can reduce the design time required to achieve and verify a given functionality since many candidate solutions can be constructed quickly and accurately.
- Simulation is required for verification and risk reduction but is time-consuming and may not be entirely representative of the full system environment.
- Prototyping with FPGAs can speed verification and reduce risk.
- Synthesis facilitates retargeting a design from one FPGA to another or to an ASIC when the requirements are frozen and the production quantity is sufficient.



TIME-TO-MARKET AFFECTS PRODUCT REVENUE



Each month's delay reduces revenue by 10%.

Fig. 1.13, Page 24 ASICs by M. Smith © 1997 A-D-W, Inc. Used by permission.

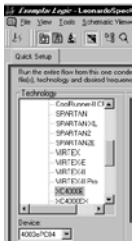
REDUCTION IN TIME-TO-MARKET INCREASES PROFITS

METHODOLOGY	Design Capture	Design Verification	Production and Profit
TRADITIONAL:	CAP	VER	$$$
SYNTHESIS:	CAP	VER	$$$$$$$$$
SYNTHESIS AND FPGAs:	CAP	VER	$$$$$$$$$$$$$$$$

USE HDL AND GRAPHICS WISELY

- Use HDL:
  - Most straightforward transcription of control (if-then).
  - Can be technology-independent.
  - Can be optimized and retargeted by synthesis.
  - Can be used to describe structure if needed.
- Use Graphics:
  - Most straightforward transcription of structure/flow.
  - Best for visualization and even animation.
  - May be slower to enter/modify.
  - May be more difficult to manage large designs.
- Capture design using either and then convert to the other.

DRIVING THE DESIGN FLOW



- Graphical User Interface (GUI)
  - Presents only valid choices and can guide user.
  - May improve productivity by reducing errors.
  - May degrade productivity by taking longer to enter.
- Command Line Interface (CLI)
  - Command lines (script) are generally faster.
  - Can use old script as a guide.
  - Best for iterations.
  - *vsim -coverage Seq_TestBench -do stim.do*
  - *spectrum -file seq_gen_altera.tcl*

PRINCIPLES OF SYSTEM OPTIMIZATION

- A global figure of merit for the entire system should be determined and optimized.
- This figure of merit involves multiple dimensions including cost, area, speed, power, design time, risk, etc.
- Optimization of a particular level or component of a system may not constitute a good return on investment.
- Decisions made at the higher levels of the design are often more significant than at the lower levels.
- Designers should pinpoint and concentrate on sensitive components for which small changes yield big payoffs.

THE ORIGINAL AND PRESENT USES OF VHDL

- VHDL = VHSIC HDL = Very High-Speed Integrated Circuit Hardware Description Language
- In 1981 VHDL was developed by the US Dept. of Defense to standardize documentation for maintenance or possible redesign.
- In 1987 IEEE approved a VHDL standard.
- Since then, CAE companies have been using VHDL with enhancements for synthesis.
- In 1992, a new IEEE standard with many of these synthesis enhancements was approved.

VERILOG

- VERILOG is a hardware description language originally developed by Gateway Automation (Cadence) for verification of logic.
- Cadence and other CAE companies have been using Verilog with enhancements for synthesis.
- Most users say Verilog is easier to learn than VHDL.
- VERILOG is no longer proprietary.

HDL DESIGNS CAN BE TARGETED TO MULTIPLE LAYOUTS