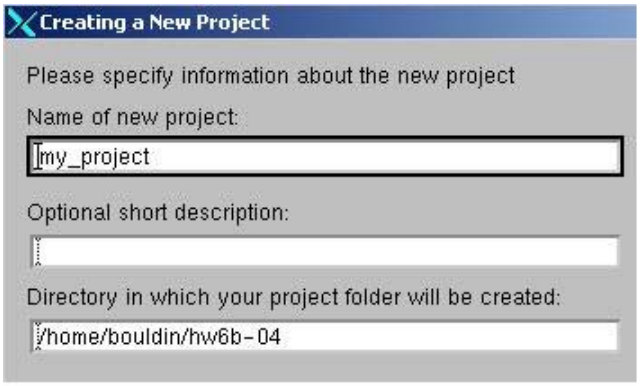
HDL2GRAPHICS

Prof. Don Bouldin – 12 Nov. 2004

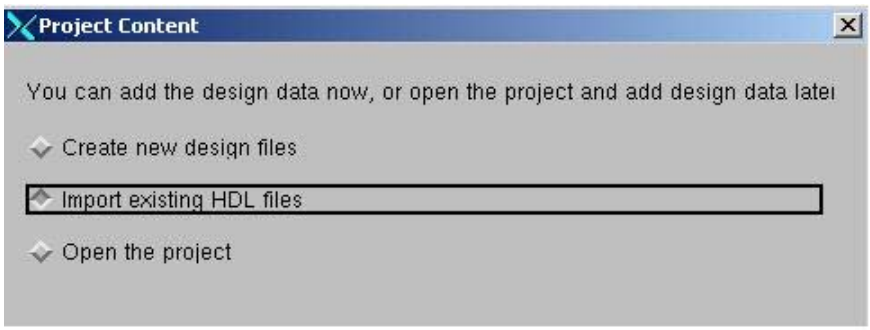
Purpose: **Generate graphics from VHDL using *fpgadvpro*.**

cd hw6b-04
mentor_tools; fpgadvpro &
create-new-project
hdl-import-vhdl
hdl-import-specify-files
hdl-import-target-convert
convert-hdl2graphics
log-conversion-complete
timer_tb (block)
timer_tester-1 (flow)
timer_tester-2 (flow)
timer_tester-3 (flow)
timer (block)
control_fsm (flow)
control_fsm-output (flow)
control_fsm-nextstate-left (flow)
control_fsm-nextstate-right (flow)
counter_struct (block)
bcdcounter (flow)

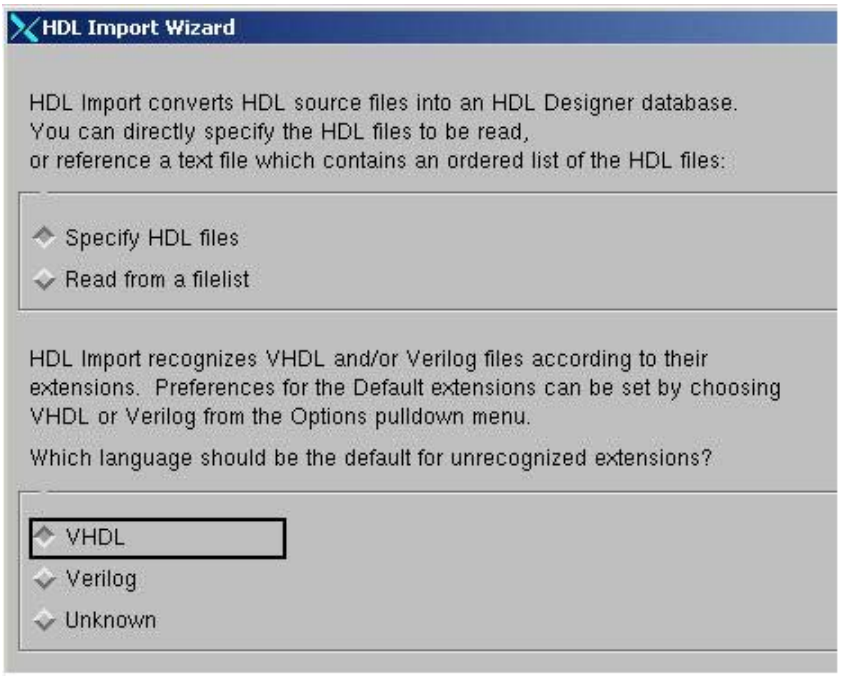
create-new-project



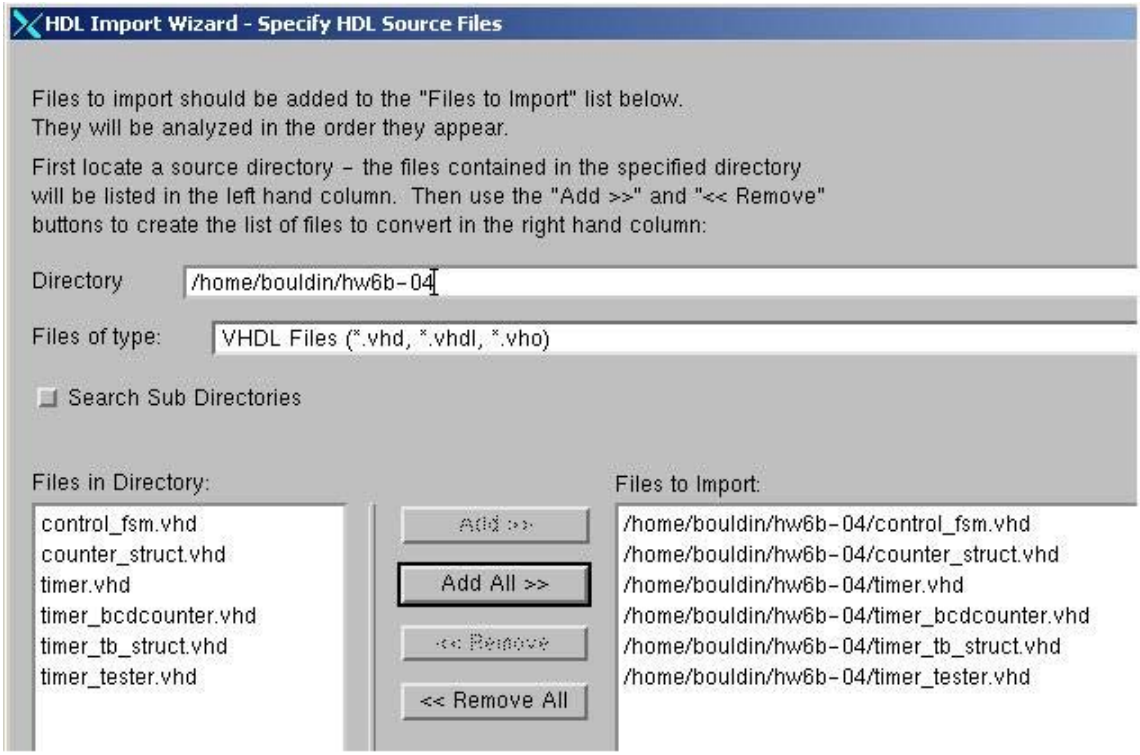
hdl-import-vhdl



hdl-import-specify-files

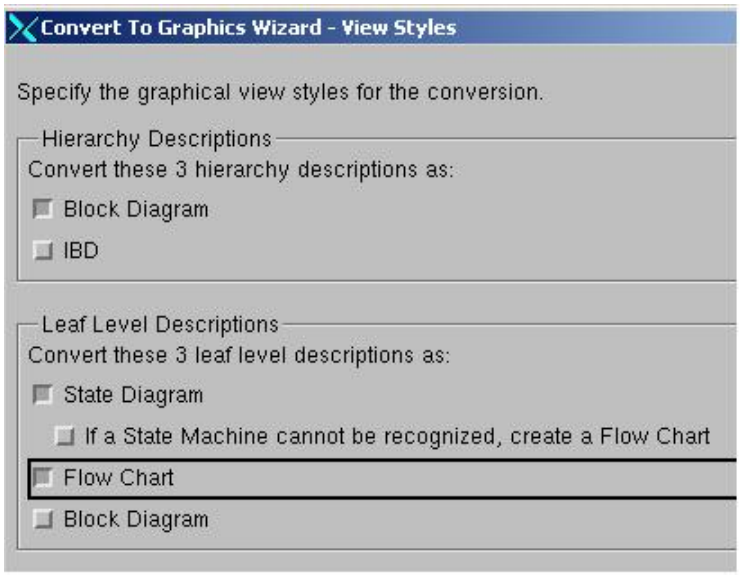


hdl-import-specify-files

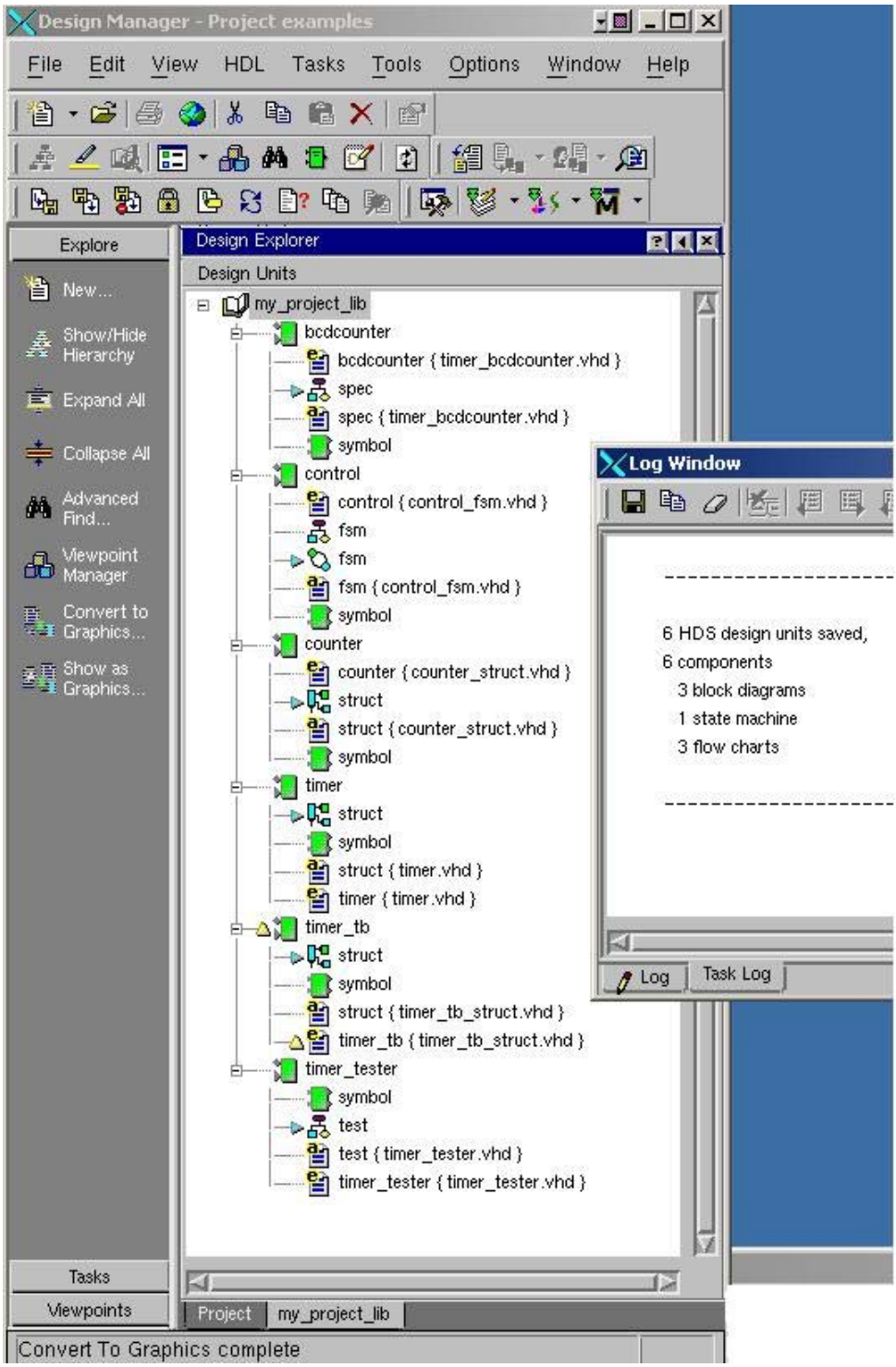


hdl-import-target-convert

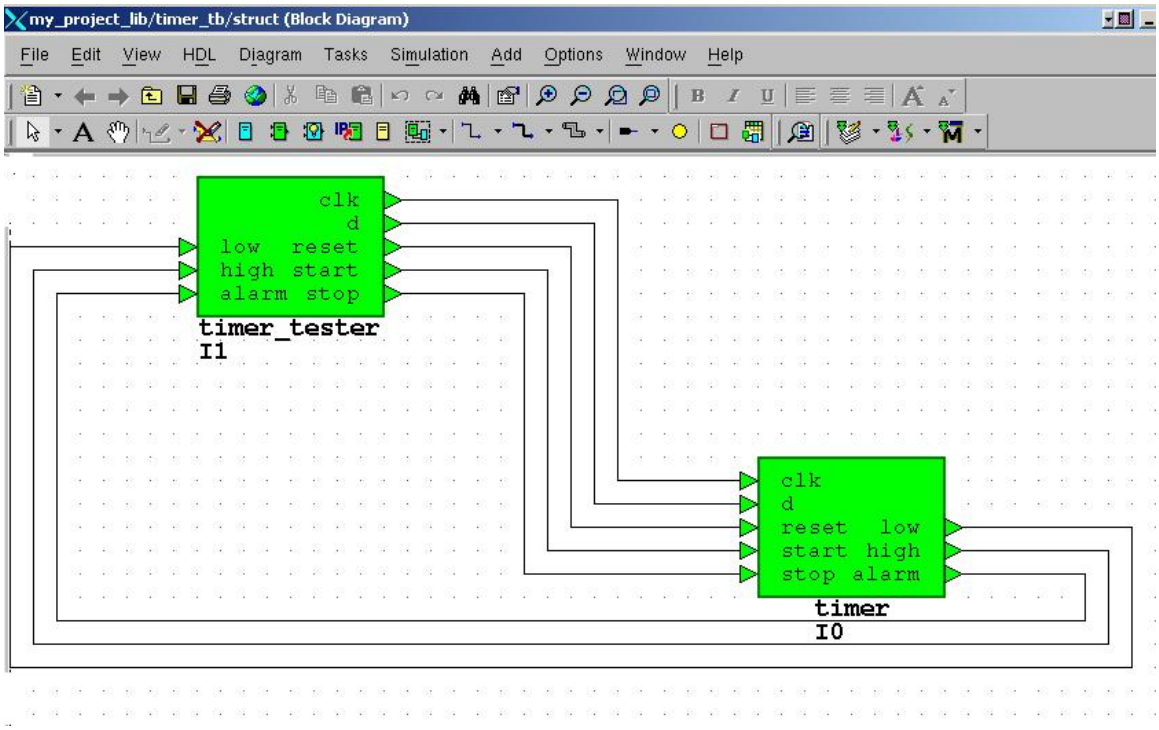
convert-hdl2graphics



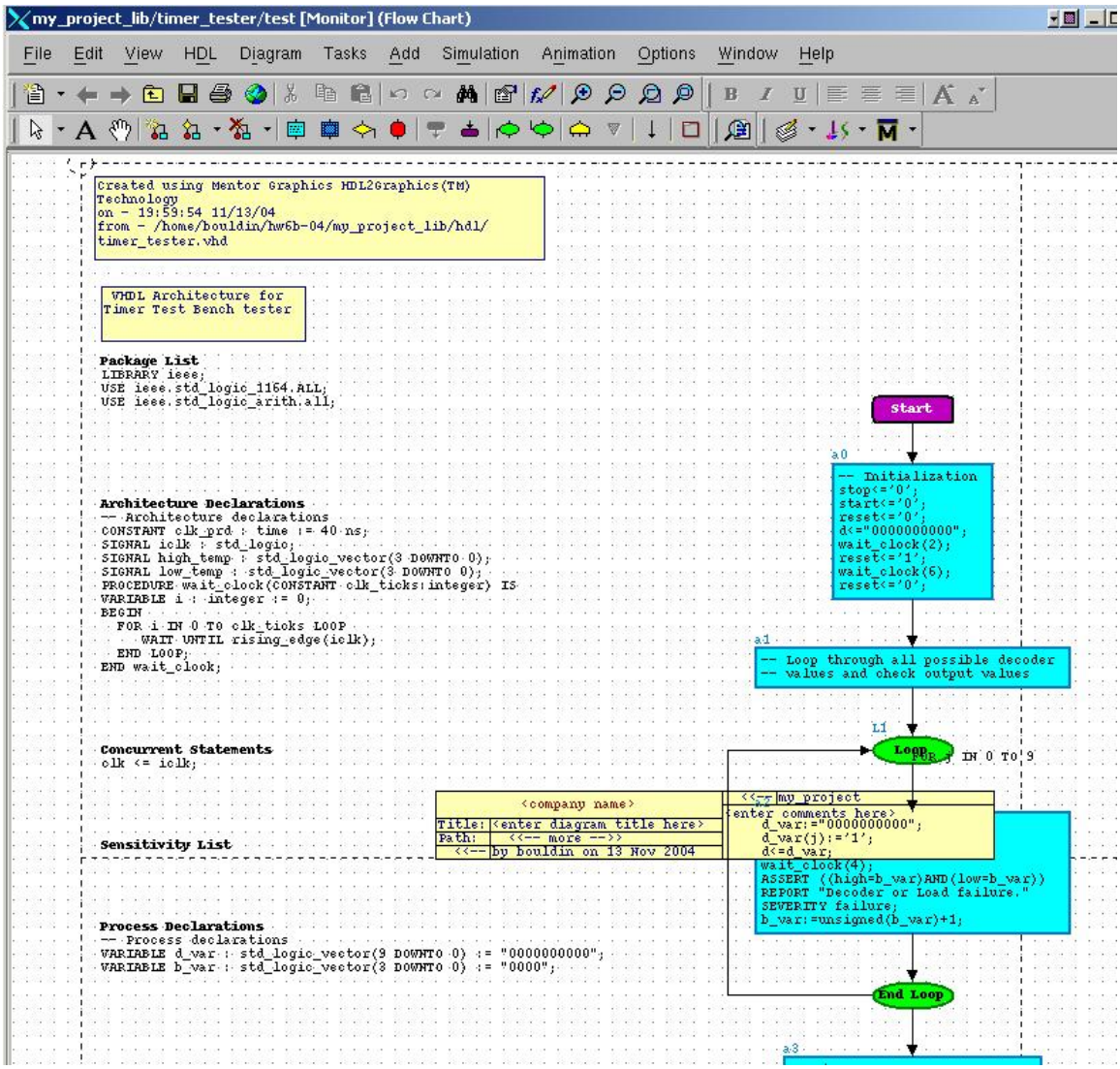
log-conversion-complete



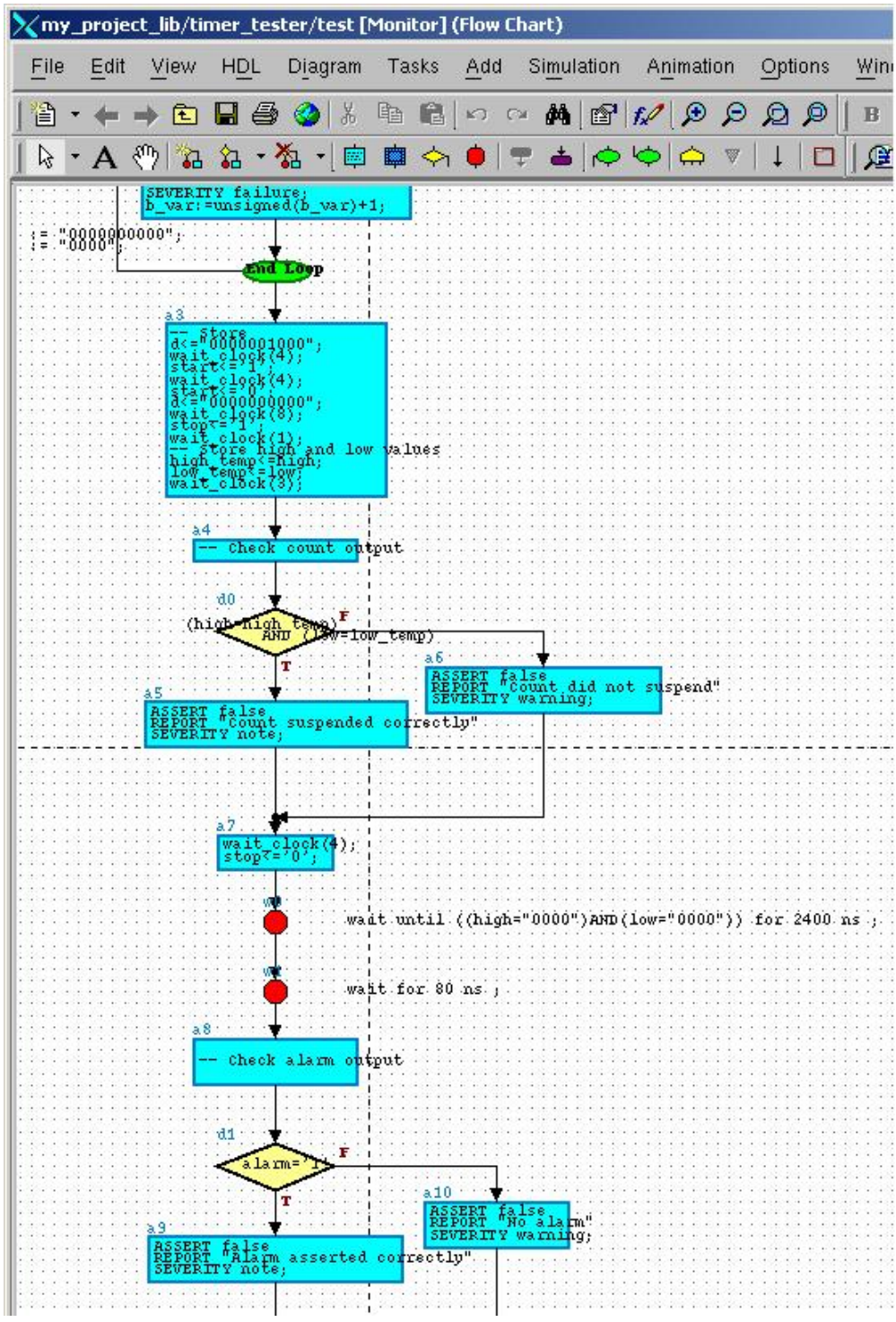
timer_tb (block)



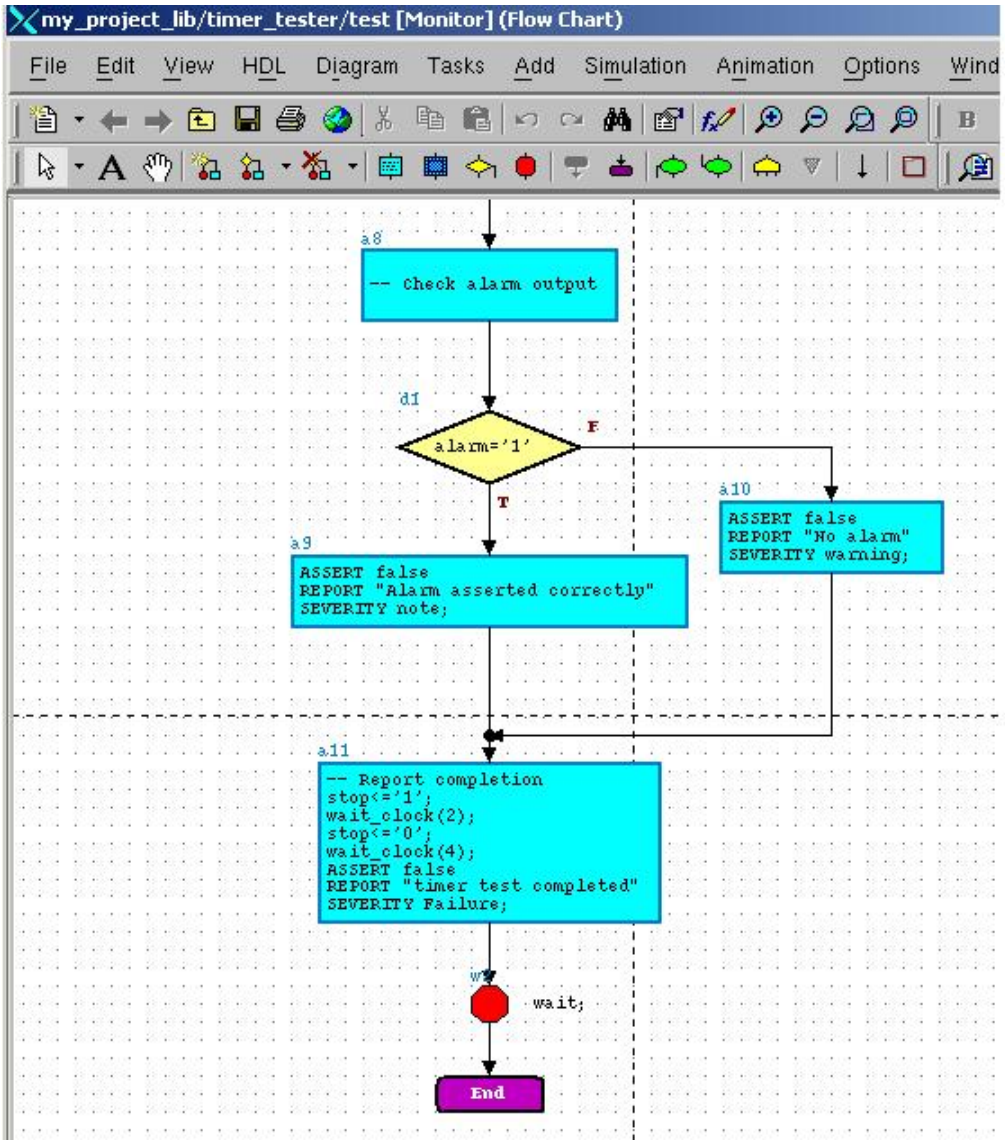
timer_tester-1 (flow)



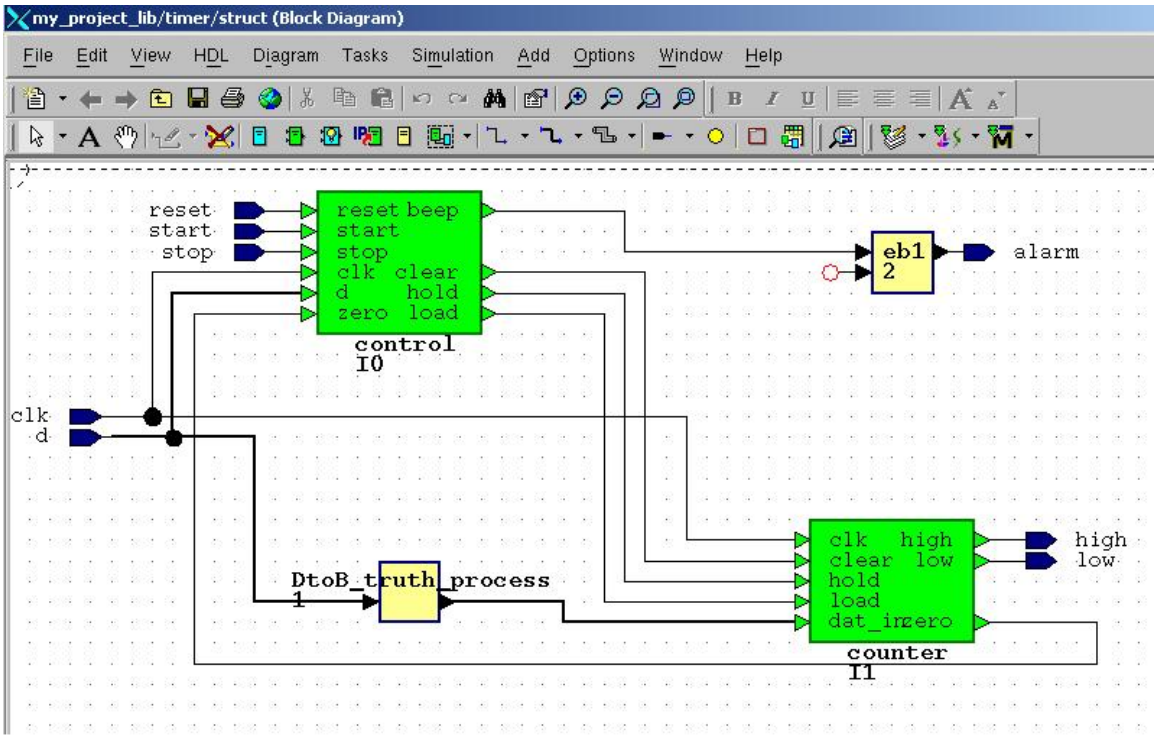
timer_tester-2 (flow)



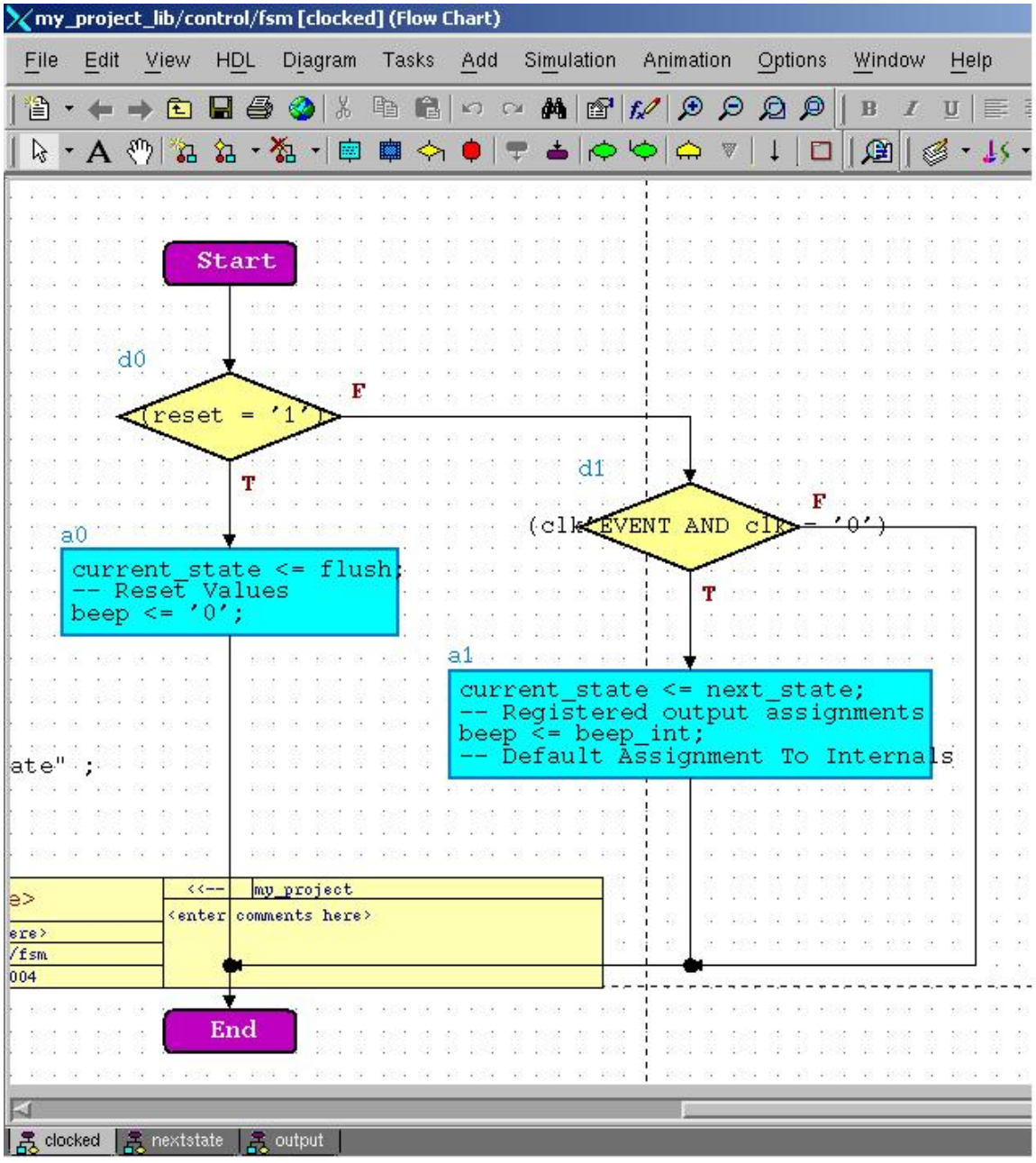
timer_tester-3 (flow)



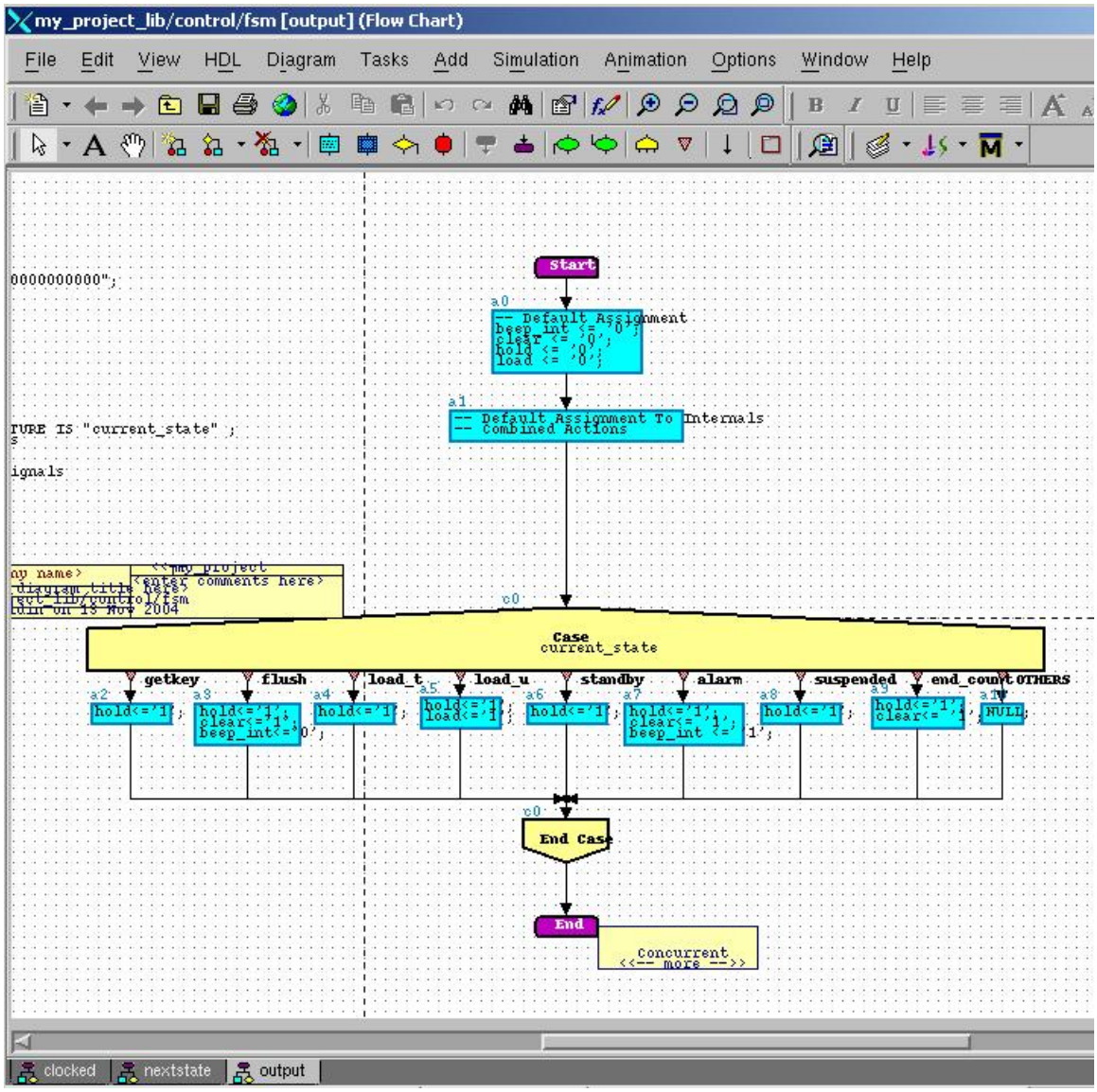
timer (block)


my_project_lib/timer/struct (Block Diagram)
File Edit View HDL Diagram Tasks Simulation Add Options Window Help
reset
start
stop
reset beep
start
stop
clk clear
d hold
zero load
control
I0
eb1
2
alarm
clk
d
clk high
clear low
hold
load
dat_iszero
high
low
counter
I1
DtoB_truth_process
1

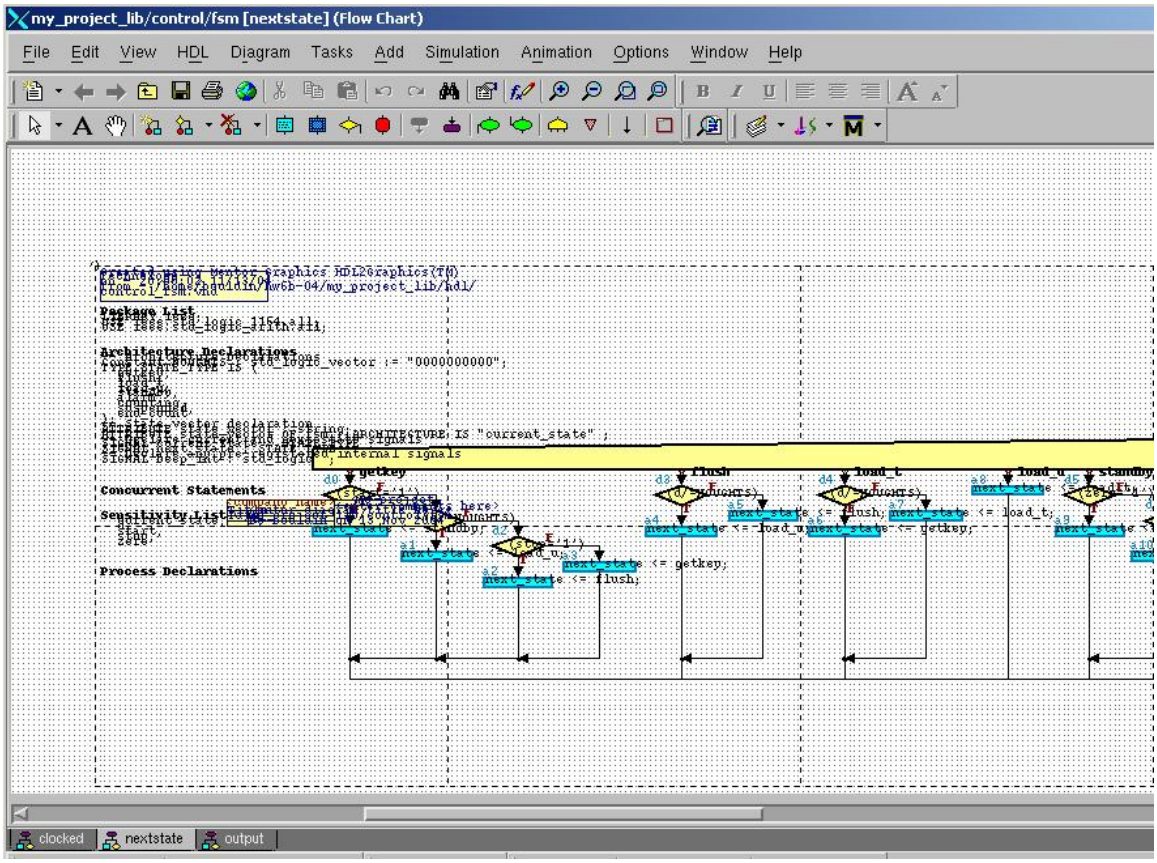
control_fsm (flow)



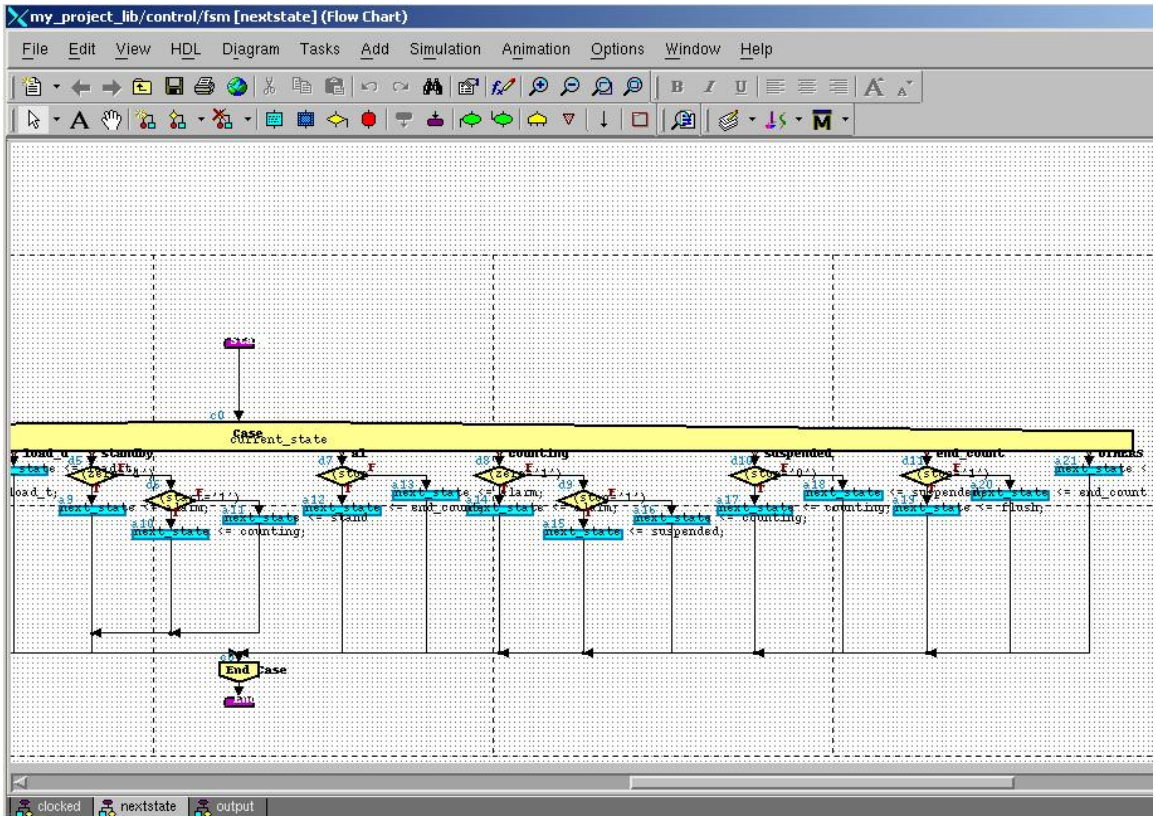
control_fsm-output (flow)



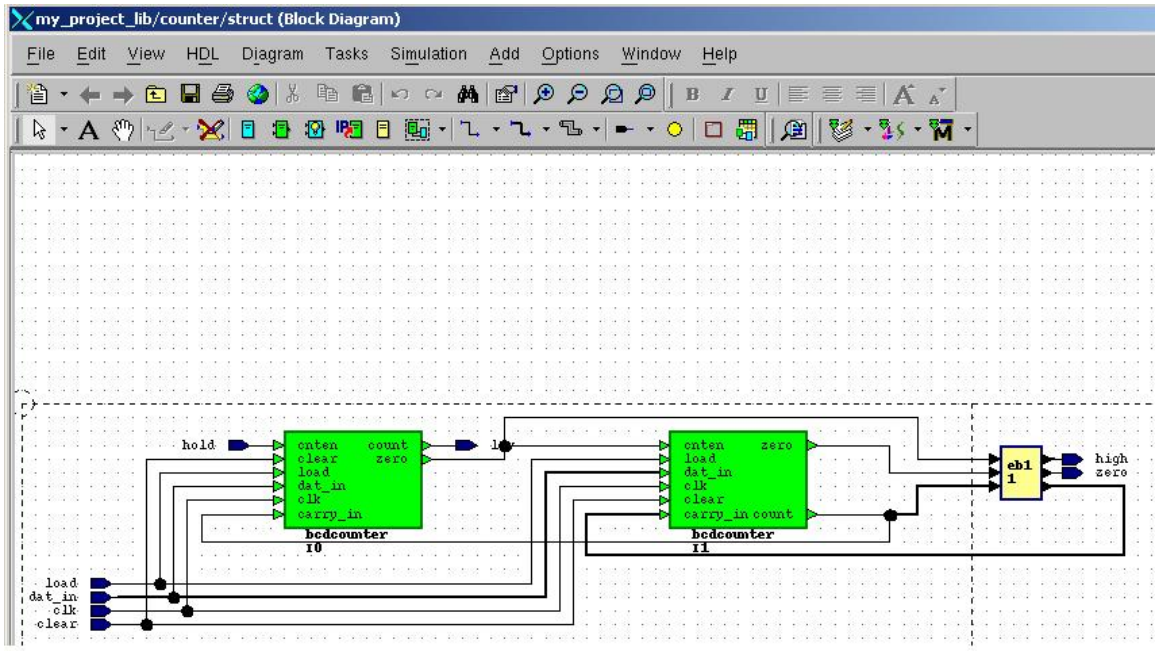
control_fsm-nextstate-left (flow)



control_fsm-nextstate-right (flow)



counter_struct (block)



bcdcounter (flow)