Cadabra User Guide

Version C-2009.09, September 2009

SYNOPSYS®

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Contents

About This Manual

This manual provides task-based instructions for working with Cadabra.

The following sections in this chapter provide a guide to this manual, as well as the other documents that comprise Cadabra's documentation suite.

Intended Audience

In order to address the manuals to the correct audience, the roles of the users of Cadabra is defined as follows:

- Design Engineer

  This role covers users who design standard cell libraries. Design engineers should be extensively familiar with layout design and SPICE netlists.

- CAD Administrator

  This role covers users who install and administer Cadabra. CAD administrators should be competent with and have requisite privileges for performing administrative tasks, such as installation, administration, and configuration, on UNIX systems.

This manual is intended for design engineers.

Revision History

This section contains a history of this document's revision history:

Revision Date	Description
September 2009	Initial publication of document for Cadabra C-2009.09.

Conventions

The following conventions are used in Synopsys documentation.

Convention	Description
`Courier`	Indicates command syntax.
`Italic`	Indicates a user-defined value, such as *`object_name`*.
Purple	▪ Within an example, indicates information of special interest. ▪ Within a command-syntax section, indicates a default value, such as: `include_enclosing = true | false`
`Bold`	▪ Within syntax and examples, indicates user input—text you type verbatim. ▪ Indicates a graphical user interface (GUI) element that has an action associated with it.
[ ]	Denotes optional parameters, such as: `write_file [-f filename]`
`...`	Indicates that parameters can be repeated as many times as necessary: *`pin1 pin2 ... pinN`*
|	Indicates a choice among alternatives, such as `low | medium | high`
\	Indicates a continuation of a command line.
/	Indicates levels of directory structure.
Edit > Copy	Indicates a path to a menu command, such as opening the Edit menu and choosing Copy.
Ctrl+C	Indicates a keyboard combination, such as holding down the Ctrl key and pressing the C key.

Related Publications

For additional information about Cadabra, see

- The documentation installed with the Cadabra software and available through the Cadabra Help menu
- The Cadabra Release Notes, available on SolvNet (see Accessing SolvNet)
- Documentation on the Web, which provides HTML and PDF documents and is available on SolvNet (see Accessing SolvNet)

You might also want to refer to the documentation for the following related Synopsys products:

- Synopsys Common Licensing
- Milkyway

Customer Support

Customer support is available through SolvNet online customer support and through contacting the Synopsys Technical Support Center.

Accessing SolvNet

SolvNet includes an electronic knowledge base of technical articles and answers to frequently asked questions about Synopsys tools. SolvNet also gives you access to a wide range of Synopsys online services, which include downloading software, viewing Documentation on the Web, and entering a call to the Support Center.

To access SolvNet:

1. Go to the SolvNet Web page at http://solvnet.synopsys.com.
2. If prompted, enter your user name and password. (If you do not have a Synopsys user name and password, follow the instructions to register with SolvNet.)

If you need help using SolvNet, click Help on the SolvNet menu bar.

Contacting the Synopsys Technical Support Center

If you have problems, questions, or suggestions, you can contact the Synopsys Technical Support Center in the following ways:

- Open a call to your local support center from the Web by going to http://solvnet.synopsys.com/EnterACall (Synopsys user name and password required).
- Send an e-mail message to your local support center.
  - E-mail support_center@synopsys.com from within North America.
  - Find other local support center e-mail addresses at http://www.synopsys.com/support/support_ctr.
- Telephone your local support center.
  - Call (800) 245-8005 from within the continental United States.
  - Call (650) 584-4200 from Canada.
  - Find other local support center telephone numbers at http://www.synopsys.com/support/support_ctr.

1

Introducing Cadabra

Describes the basic concepts of Cadabra, and introduces you to the overall Cadabra workflow.

Cadabra provides an automated solution for migrating and creating custom standard cell layouts. Cadabra allows you to migrate custom standard cell libraries to new process technologies, transistor sizes, or architectures, and create LVS and DRC correct cell layouts.

Cadabra provides three main automated processes: Migrate-GDS, ATL (Automated Transistor Layout), and Migrate-ATL.

Automated Process	Description
Migrate-GDS	Using cell netlists, GDSII files, and a target architecture and technology as input, Migrate GDS imports, compacts, finalizes, and exports cell layouts in one step.
ATL	Using cell netlists and an architecture and technology as input, ATL places, routes, compacts, finalizes, and exports cell layouts in one step.

Automated Process	Description
Migrate-ATL	Using cell netlists, GDSII files, and a target architecture and technology as input, Migrate-ATL combines the functionality of Migrate GDS and ATL in one step. Migrate-ATL runs the Migrate GDS process first, then based on your specifications, runs ATL. ATL can always be run, or run only on those cells that fail migration, or are sub-optimal after migration. The Migrate-ATL process should be used if: ▪ The source layouts for some cells in a library are not compatible with the target architecture and/or cell netlists. ▪ The Migrate GDS process on its own provides sub-optimal or infeasible results. ▪ You want to compare a migration methodology to an ATL methodology. Cadabra also allows you to run the individual steps of each automated process (import, place, route, compact, finalize, and export) for finer control. All three processes allow you to view the results as the layouts are generated. Cadabra also provides the functionality for hand-editing layouts individually. Cadabra has an easy-to-use graphical user interface (GUI). Advanced users also have the option of using Cadabra's own Application Language (AL) to run the tool. Cadabra provides the Generic Portfolio, which contains a set of built-in files that are the foundation for creating cell architectures in any process. You can use the provided templates and customize the property values. Cadabra's Architecture Builder can be used to configure and register devices, custom design steps, callbacks, and exporters that are contained within the Generic Portfolio. Migration refers to converting existing GDSII layouts to new GDSII layouts by mapping the original layout to new technology process rules or architectures. Migration applies to GDSII formatted libraries only.

This section covers the following topics:

Introduction to Cadabra Workflow

Using Cadabra to migrate and/or create cell layouts involves three stages: defining the target architecture, initializing the library, and migrating and/or creating the cells. Defining the architecture requires entering the design rules for your target technology and specifying the cell architecture and layout options for your target architecture. Initializing the library requires adding cell netlists. If using migration, you must also add GDSII layouts and map them to the netlists. Migrating and/or creating the cells requires running one of three processes: Migrate GDS, Automated Transistor Layout (ATL), or Migrate-ATL.

Cadabra automatically migrates and/or creates a final layout and displays cell completion and quality data. The cells can then be saved as a Cadabra-formatted library or exported to GDSII files.

Working with Cadabra Workflow

When working with Cadabra, Synopsys recommends the following workflow:

- Define Target Architecture
- Initialize the Library
- Migrate and Create Cells

Define Target Architecture

This section covers the following topics:

- Build a technology
- Build an architecture

Build a technology

Build a target technology by setting up your layers and process design rules through the Technology Builder. The physical and electrical design rules govern the behavior of the layout features. Cadabra's Technology Builder provides an easy-to-use graphical user interface for entering your design rules.

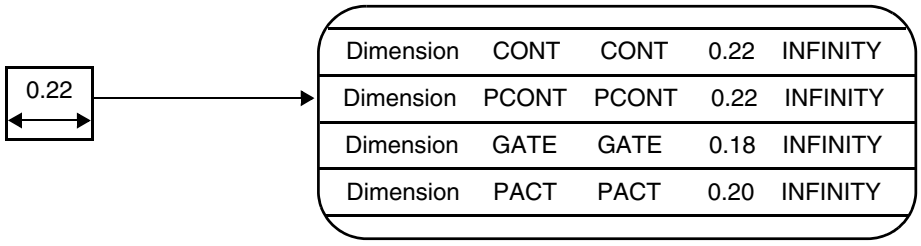


Figure 1 Sample Technology Builder Interface

Note: You can use the PLAN utility to define the technology and architecture. This allows you to explore architectures without acquiring a synthesis license.

Build an architecture

Build an architecture by setting up your cell architecture elements, layout styles, importer and exporter options through the Architecture Builder. The architecture is based on your technology, which can be edited and exported into the architecture with any late changes. The architecture describes the behavior of the devices in the layout and the style preferences for cell migration and creation.

The Architecture Builder provides graphical feedback of the cell architecture by displaying a view of the layout features (such as the position of the well, the cell boundary size, the position of power rails, or the shape of various contacts).

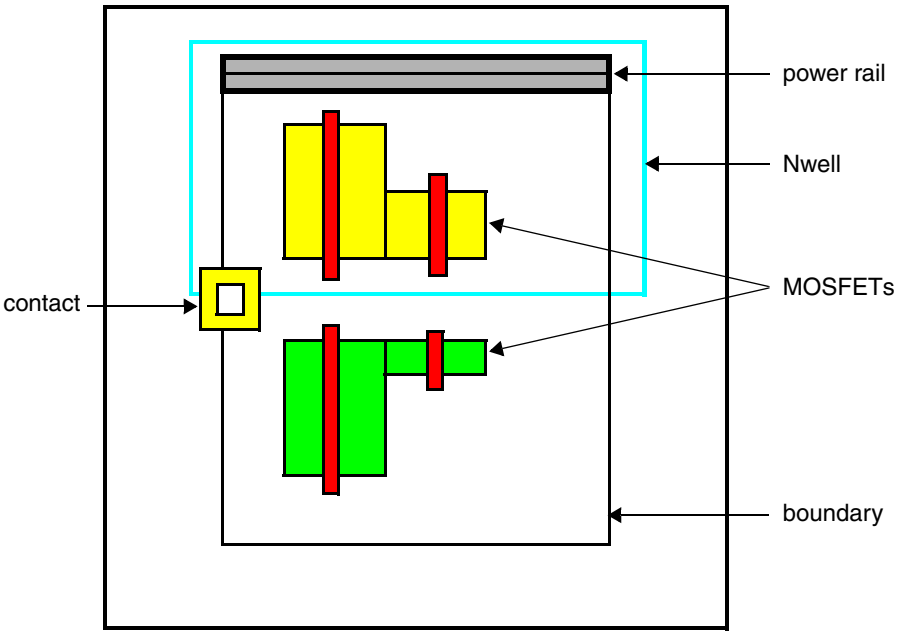


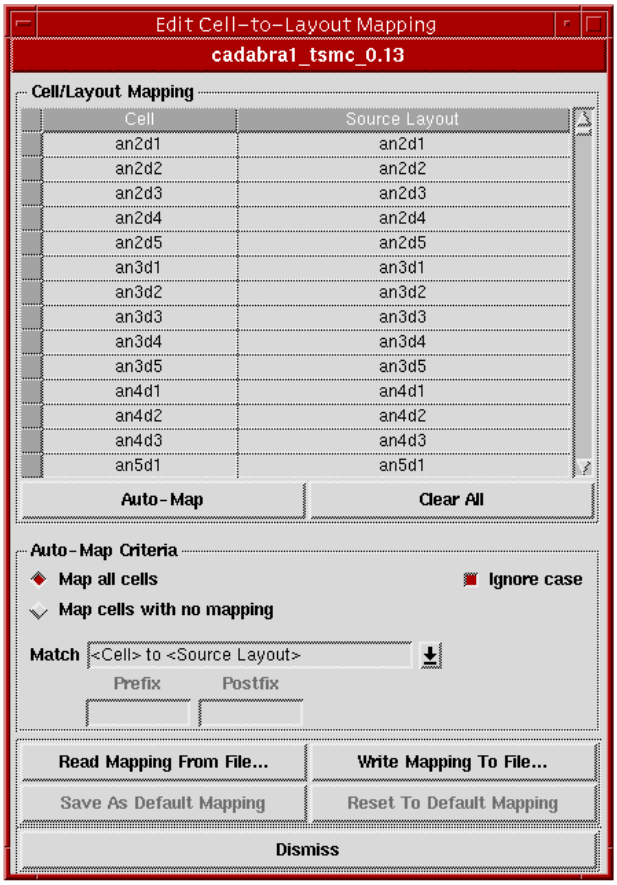
Figure 2 Sample Architecture Builder Interface

All cells in a library are based on the same architecture.

Initialize the Library

From the Cadabra main window, create an empty library file based on a target architecture file. Then add the cells to the library, either individually by entering a netlist filename, or as a set by specifying a directory which contains all the netlists for the cells to be added.

If you are migrating a library, input a GDSII formatted cell library file and add the GDSII layouts that are to be mapped to the cells. Layouts can be added individually, or as a set by specifying the directory in which the GDSII files reside. Finally, map the cells to their corresponding GDSII layouts.



Note: More than one cell can be mapped to the same GDSII layout. However, a cell can only be mapped to one layout at any given time.

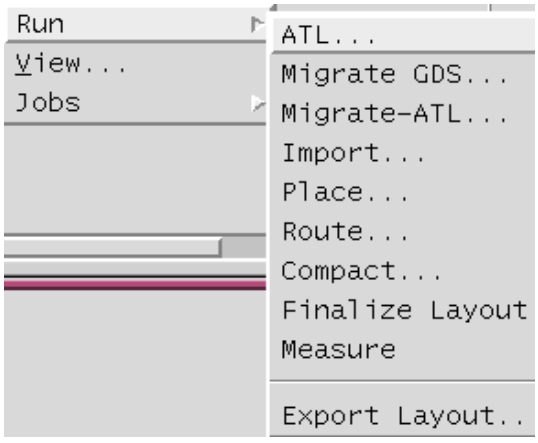
Migrate and Create Cells

This section covers the following topics:

- Migrate cells
- Create cells
- Migrate and create cells
- View the results
- Export the layouts

Migrate cells

Run the cells through the entire migration flow by selecting the Migrate GDS process or its individual steps (Import, Compact, and Finalize Layout) by selecting each process separately.



Create cells

Run the cells through the automated transistor layout flow by selecting ATL or its individual steps (Place, Route, Compact, and Finalize Layout) by selecting each process separately.

Migrate and create cells

Run the cells through the entire migration and automated transistor layout flows by selecting Migrate-ATL. Depending on your specifications, ATL may not always be run.

Multiple users can access and work on cells in the same library simultaneously. Locks on individual cells prevent any user conflict.

View the results

View the results of the Migrate GDS, ATL or Migrate-ATL processes in the main Cadabra window by monitoring the cell completion and quality data.Cadabra highlights the design point of the best layout created with a yellow marker in the Cell Browser. The achieved cell width is compared to the target width (if given). You can open the marked design point to view the final layout. If any cells were unable to complete, you can easily hand-edit them using the Cell Editor.

Note: You can use the VIEW utility to view library data. This allows you to monitor library development without acquiring a synthesis license.

Export the layouts

The final layouts can be exported to GDSII as part of the Migrate GDS, ATL or Migrate-ATL process, or manually, once the final layouts have been viewed.

2

Launching Cadabra

Describes how you can launch Cadabra; includes details about environment variables and available launching options.

Once the software has been installed and the license server setup, you can get started. First, you must set the CADABRAHOME environment variable and any optional environment variables, and then you can launch the tool.

This section covers the following topics:

Environment Variables

Some environment variables can be set to help organize your library files. We recommend you set the first two of the following:

- `CADABRAPROJECT` sets the location of input files for a project.

  If you are working in sh, ksh, or bash, type:
  ```
  export CADABRAPROJECT=/home/$USER/this_project/
  ```

  If you are working in csh or tcsh, type:
  ```
  setenv CADABRAPROJECT /home/$USER/this_project/
  ```

  Note: If any of the directories included in `CADABRAPROJECT` contain subdirectories named RSK, then those subdirectories will also be included in the search path. These subditectories are included immediately after the named directories that contain them.

If your design environment includes a directory titled RSK, then the path to that directory is automatically added to CADABRAPROJECT.

- CADABRAWORKING sets the location of output files for this project.

  If you are working in sh, ksh, or bash, type:
  `export CADABRAWORKING=/home/$USER/this_project/output/`

  If you are working in csh or tcsh, type:
  `setenv CADABRAWORKING /home/$USER/this_project/output/`

- CADABRALOG sets the location where log files should be stored. By default, the log files are placed in /log/ under the current directory.

  If you are working in sh, ksh, or bash, type:
  `export CADABRALOG=/home/$USER/log/`

  If you are working in csh or tcsh, type:
  `setenv CADABRALOG /home/$USER/log/`

- CADABRA_LICENSE_UNAVAILABLE_EXIT_CODE sets the tool exit code on failure. This code can be caught by other applications, such as the LSF job scheduling software.

  If you are working in sh, ksh, or bash, type:
  `export CADABRA_LICENSE_UNAVAILABLE_EXIT_CODE=<code>`

  If you are working in chs or tsch, type:
  setenv `CADABRA_LICENSE_UNAVAILABLE_EXIT_CODE <code>`

- CADABRAPANICLIB determines if a panic library should be saved. Acceptable values are 1 and 0. If `CADABRAPANICLIB = 1`, then the panic library is saved; if set to 0, then no panic library is saved.

- CADABRA_CHECK_LCA determines whether keys that are not part of the Cadabra's bill of features are checked for. This environment variable is particularly relevant when you want to control Beta or debug functionalities using license keys. Acceptable values are 1 and 0. If `CADABRA_CHECK_LCA = 1`, then Cadabra checks for keys that are not part of Cadabra's bill of features; if set to 0, then Cadabra does perform the check.

- CADABRA_LICENSE_WAIT determines Cadabra support for queuing with regard to license servers. Acceptable values are 1 and 0. If `CADABRA_LICENSE_WAIT = 1`, then Cadabra supports queuing for license servers; if set to 0, then Cadabra does not support the queuing functionality.

Launching Options

Depending on the options used to launch the tool, Cadabra can be opened in planning or synthesis modes. When you need to switch modes, you must re-launch the tool. If you do not specify any options on launch, Cadabra opens with all the available licenses. Following are the Cadabra launching options:

- -view

  Cadabra launches in viewing mode. You can initialize libraries, browse libraries and cells, edit cell properties, and set up job scheduling. However, you cannot migrate or create cell libraries.

- -1 *<logDirectory>*

  The log file's directory path is set, overriding `CADABRALOG`.

  Note: Ensure that the log directory, whose path is set here, exists. Cadabra does not create this directory automatically for you. If the specified directory does not exist, log files are not created.

- -nl

  Logging is turned off. No log files are produced.

- -nw

  Cadabra launches in ``no windows" mode and uses a terminal window to accept AL commands. The main Cadabra window does not appear. This option cannot be used with the -view option. Log files are not created in this mode.

- -version

  Cadabra displays the version information.

- -help

  A summary of Cadabra's command line options are displayed.

You can also append a list of library or AL files to be opened with the tool at the end (except when using `-nw`), as in the example:

```
cadabra -view /home/$USER/working/myLib.lib
```

To launch Cadabra

To launch Cadabra, do the following:

1. Set the CADABRAHOME environment variable to the Cadabra directory.

   If you are working in sh, ksh, or bash, type:
   `export CADABRAHOME=/home/cadabra/`

   If you are working in csh or tcsh, type:
   `setenv CADABRAHOME /home/cadabra/`

2. Set the optional Environment Variables.

3. Launch Cadabra by typing: `$CADABRAHOME/bin/cadabra` To launch Cadabra

   The main Cadabra window appears. The available functionality depends on the options used to launch Cadabra.

   Note: When you first launch Cadabra, it automatically creates default configuration files in ~/.cadabra. You can configure Cadabra to customize your setup.

3

Setting Architectures

Describes how to create technologies and architectures in Cadabra.

Before you can create a library, you need to set up its layers, design rules, cell architecture, and layout options. If you are migrating a library, you must set the GDSII importer options. If you plan on exporting the final layouts of the library in GDSII format, you also need to set up the GDSII exporter options.

The layers and design rules are defined in a technology file. The cell architecture, layout options, GDSII importer and GDSII exporter are defined in an architecture file.

Cadabra's Technology Builder and Architecture Builder allow you to set up your technology and architecture through a graphical user interface.

The technology must be created first. However, you can go back and edit your technology file while simultaneously working on your architecture.

This section covers the following topics:

- Architecture Status
- To view element messages
- Working with Architectural Elements
- Architecture Details
- To integrate custom AL files
- To manage design steps, callbacks, and exporters
- Setting Layout Options
- To set the optimization goal
- Working with Placement Styles
- Working with Routing Styles
- Working with Compaction Styles
- Working with Electromigration Styles
- Working with Text Annotation
- To set path layers
- Working with Measurement Metrics
- Working with Importers
- Working with Exporters
- Customizing an Architecture
- To save an architecture

Setting a Technology

A technology is a collection of layers and design rules governing the interaction of those layers. Cadabra's Technology Builder allows you to define a technology through a graphical user interface.

There is no specific method for defining a technology, however, Synopsys recommends the following workflow:

Create Technology: Create a technology and define the manufacturing grid (in microns). This grid is the finest granularity of the layout on which devices can be placed. All design rule intervals must be a multiple of the manufacturing grid. In addition, define the lateral diffusion (if used).

Add the layers that are to be used in the architecture. Each layer must have a unique name. The appearance of each layer can be customized. Shapes that are created on this layer will be displayed in a layout with this appearance. Color and pattern can be varied. A set of predefined base layers is present in every technology. These layers are used to display information such as the IO grid. The predefined layers can be hidden from view while creating a technology.

Add design rules on and between layers. Design rules enforce allowed distances between objects on those layers. Design rules can be physical rules (which govern the distance between objects) and electrical rules (which govern the interactions of electrically similar objects). Certain design rules may have conditions associated with them that describe special situations when a certain spacing is in effect. When the condition is fulfilled, the conditional spacing is used. Otherwise, the default spacing is used.

Verify the technology. Once all layers and design rules have been added, the technology should be verified to ensure that routable layers are available and that interactions between layers are properly described.

Save the technology. The technology is saved in a file that can be used to build an architecture, which is the basis for a library.

To create a new technology

To create a new technology, do the following:

1. In the Cadabra window, select Tools > Technology Builder > Create/Edit Technology.
   The Technology Builder dialog box appears.
2. Select File > New.
   The Technology Properties dialog box appears.
3. Enter a name for the technology in Name.
4. Enter a value in Manufacturing Grid.

   Caution: The value for the manufacturing grid cannot be larger than 8 microns.

5. Set the option:

Lateral Diffusion The delta between the drawn and effective widths caused by encroachment of field oxide over the device well.

6. Click OK.
   The Technology Properties dialog box closes and the new technology is created.

To open a technology

You can open a technology in the following ways:

- With an existing architecture
- Without an architecture

With an existing architecture

To open a technology with an existing architecture, do the following:

1. In the Cadabra window, select Tools > Technology Builder > Edit Technology from Architecture.
   The File Browser appears.
2. Select an architecture file.
   The selected architecture appears in the Architecture Builder window and its technology appears in a Technology Builder window.

Without an architecture

To open a technology without an existing architecture, do the following:

1. In the Cadabra window, select Tools > Technology Builder > Create/Edit Technology.
   The Technology Builder dialog box appears.
2. Select File > Open *or* File > Open in New Window.
   The File Browser appears.
3. Select a technology file.

   Note: A technology file written in Cadabra's Application Language ends with an.al extension.

4. Click OK.
   The selected technology appears in the existing or a new Technology Builder window.

To open a Milkyway technology

To open a Milkyway technology, do the following:

1. In the Cadabra window, select Tools > Technology Builder > Create/Edit Technology.
   The Technology Builder dialog box appears.
2. Select File > From Milkyway.
   The Directory Browser appears.
3. Browse to the directory that contains the Milkyway library.

   Note: A Milkyway technology is specified by a Milkyway library, not by a specific filename or extension.

4. Click OK.
   The Milkyway technology appears in the Technology Builder window.

   Caution: A warning message will appear if there are conflicting rule values within the Milkyway technology file. It is recommended that you review these values in the Technology Builder before proceeding.

To edit technology properties

To edit technology properties, do the following:

1. In the Technology Builder dialog box, select Edit > Technology Properties.
   The Technology Properties dialog box appears.
2. Edit the technology properties.
3. Click OK.
   The Technology Properties dialog box closes and the technology properties are updated.

Technology Properties Options

Name: The name of the technology.

Manufacturing Grid: The manufacturing grid size in microns. This value cannot be larger than 8 microns.

Lateral Diffusion: The delta between the drawn and effective widths caused by encroachment of field oxide over the device well.

This section covers the following topics:

Lateral Diffusion

The delta between the drawn and effective widths caused by encroachment of field oxide over the device well.

This section covers the following topics:

Why set this option?

If MOSFETs are folded and unfolded multiple times, you must account for the area of encroachment. Otherwise, the effective widths of the MOSFETs will be greater than the drawn widths.

Lateral Diffusion Option Details

Lateral diffusion refers to the delta between the drawn and effective widths caused by encroachment of field oxide over the device well as shown in the figure below. This encroachment is also referred to as the “bird's-beak effect.”

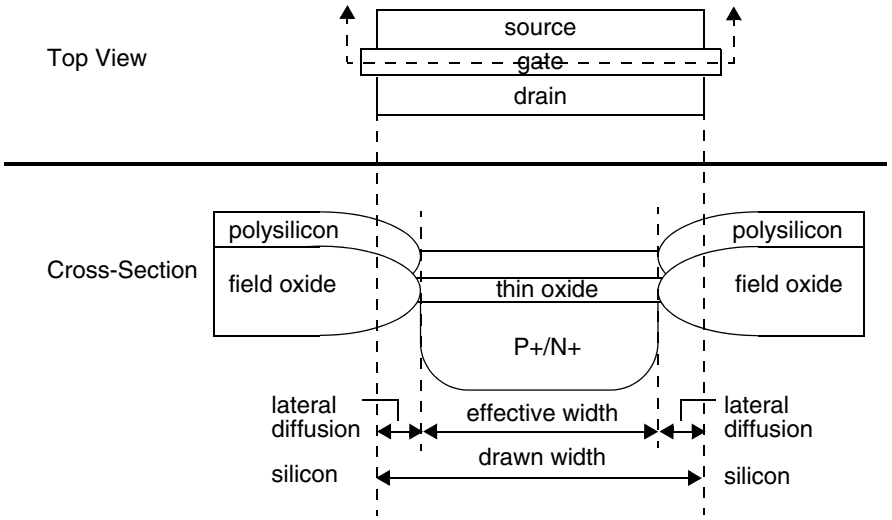


Figure 3 Lateral Diffusion - Bird's Beak Effect

Although this difference is a small percentage of the entire MOSFET width, lateral diffusion can become significant if the MOSFET is folded or unfolded multiple times. The figure below demonstrates the effect of lateral diffusion during unfolding.

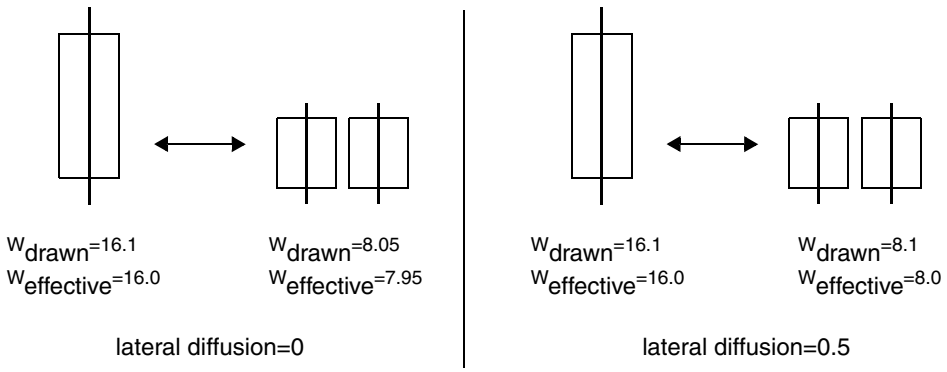


Figure 4 Effect of Lateral Diffusion During Unfolding

To correctly calculate the drawn width of MOSFETs during folding/unfolding, the lateral diffusion is initially removed from the MOSFETs and then added

back once the MOSFETs are folded/unfolded. This will give the correct drawn width. Cadabra assumes that the initial input width includes the lateral diffusion.

To add a new layer

To add a new layer, do the following:

1. In the Technology Builder dialog box, select Layers > Add.
   The Add New Layer dialog box appears.
2. Enter a name for the new layer.
3. Set the options.
4. Click OK.
   The Add New Layer dialog box closes. The new layer is added to the technology and dimension and separation rules are automatically created for the new layer.

To edit a layer

To edit a layer, do the following:

1. In the Technology Builder dialog box, select Layers > Edit.
   The Edit Layers dialog box appears.
2. Select the layer you would like to edit from Layer Name.
3. Edit the options.
4. Click OK.
   The Edit Layers dialog box closes and the layers' properties are updated.

Add/Edit Layer Options

Layer Name: The name for the layer that is added or edited.

Inherit from Layer: The existing layer from which properties are inherited. Inherited layer properties include both physical appearance (color, stipple,

drawing order) and design rules and any associated conditions. This option is only available when creating a new layer.

Routable: The layer is routable. Cadabra will only look at “routable” layers during routing.

Use Appearance of: The appearance of the selected layer is used as a template for creating the new layer.

Stipple The stipple pattern for the layer.

Fill: The color for the layer. Click on a color block or customize the color.

Outline: The outline color for the layer. Click on a color block or customize the color.

Boundary Distances: The minimum space between the cell boundary edge and any shape on this layer that is contained within the boundary. You can use default values or manually specify the left, right, top, and bottom distances.

Preview with: An existing layer to view the new layer with.

Over: The preview layer is placed over the new layer.

Under: The preview layer is placed under the new layer.

This section covers the following topics:

Stipple

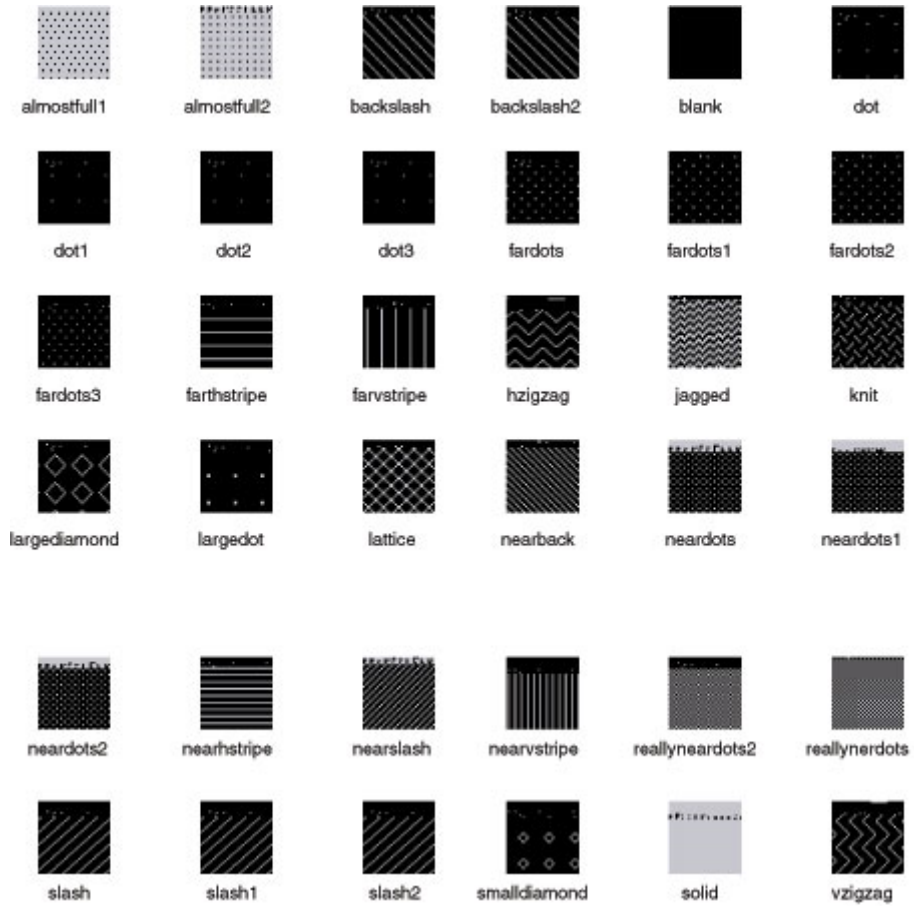
The stipple pattern of the layer.

This section covers the following topics:

Why set this option?

The chosen pattern helps distinguish this new layer from the other layers of the technology in a symbolic layout.

Cadabra provides the following stipple patterns:



To customize a layer color

To customize a layer color, do the following:

1. In the Add New Layer or Edit Layer dialog box, select Customize.
   The Choose Color dialog box appears.
2. Enter a Red, Green and Blue value for the color or adjust the respective scales.
3. Click OK.
   The Choose Color dialog box closes and the specified color appears in the Add New Layer dialog box.

To delete a layer

To delete a layer, do the following:

1. In the Technology Builder, select Layers > Delete.
   The Delete Layers dialog box appears.
2. Select the layer(s) you would like to delete.
3. Click Delete.
   A Question dialog box appears to confirm the removal.

   Caution: If you delete a layer, all of the associated design rules will also be deleted.

4. Click Yes.
   The selected layer(s) and their associated design rules are removed.

Predefined Layers

Each technology has a set of predefined layers. Predefined layers set the color and stipple patterns for system graphics. Currently, there are five predefined layers:

1. @annotate

   This layer is used to select the color for the net name annotation.

2. @error

   This layer is used to select the color for annotating errors.

3. @compaction

   This layer is used by Cadabra's Gate Bend Balancer and Gate Bend Centering devices, and Minimum Area shape behavior.

4. @group

   This layer is used to select the color for the rectangle that surrounds devices which are in a group.

5. @iogrid

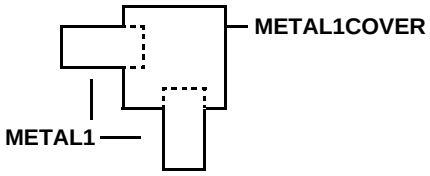
   This layer is used to select the color for the I/O grid.

Note: The predefined layers can be hidden in the Layers list by selecting Edit > Hide Predefined Layers. Deselecting this option displays the predefined layers.

Representative Layers

Representative layers define a set of logical layers as the same physical mask layer. They are used to support different design rules against the physical layer. They also help determine which shape edges are affected by the design rules. When two layers are considered representative, the shapes on those layers are grouped together and process design rules are only enforced against the outermost contours of the group.

For example, if METAL1Cover is representative of METAL1 and the placement shown in the figure below occurs, the minimum separation between the wires is not enforced and connectivity is maintained during compaction.



Since METAL1 and METAL1Cover are considered to be the same physical mask layer, some edges of the METAL1 shapes will be “contained” and, therefore, will not make constraints with any other METAL1 or METAL1Cover shapes that may exist outside the perimeter of this shape island. If the shapes were not representative, then the METAL1 wire shapes would make separation constraints to other METAL1 wire shapes that they otherwise would have been masked from by the METAL1Cover shape.

This section covers the following topics:

- To set representative layers
- To unset representative layers
- To set the layer drawing order

To set representative layers

Setting representative layers allows you to mark a group of layers as the same physical layer. To set representative layers, do the following:

1. In the Technology Builder dialog box, select Layers > Set Representatives.
   The Representative dialog box appears.
2. Select the layer to be the representative layer from the Layers list.
3. Click Set Representative.
   The selected layer appears under the Representative heading on the dialog box.
4. Select the layer to be the constituent layer from the Layers list.
5. Click Set Constituent.
   The selected layer is moved under the set representative layer in the Layers list.
6. Repeat steps 2-5 until you have set all the required representative layers.
7. Click OK.
   The Representatives dialog box closes.

   Shortcut: The representative layers can also be set by dragging and dropping the constituent layer on top of the representative layer.

To unset representative layers

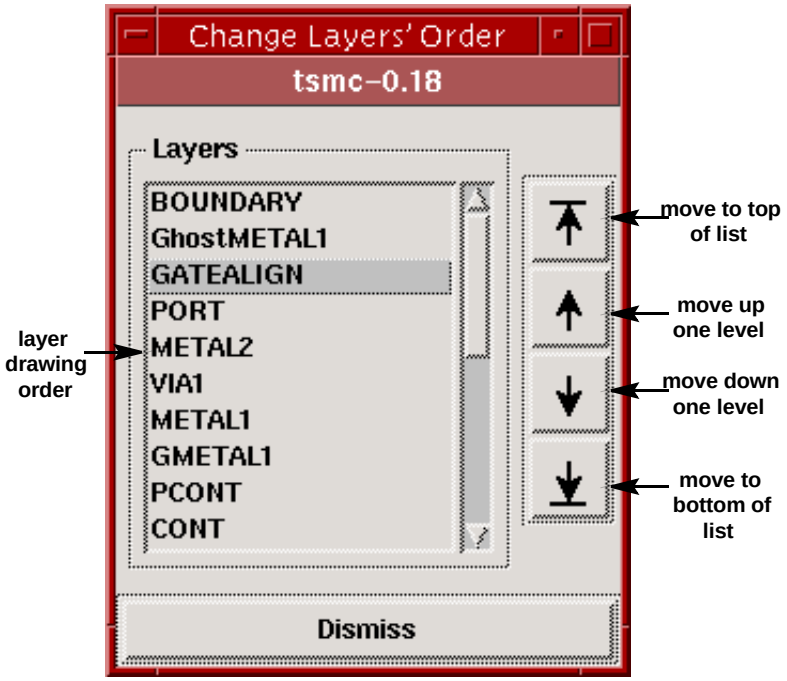
To unset representative layers, do the following:

1. In the Technology Builder dialog box, select Layers > Set Representatives.
   The Representative dialog box appears.
2. Select the constituent layer to be unset.
3. Click Unset Constituent.
   The constituent layer is moved out from under its representative layer and returned to the parent level.
4. Click OK.
   The Representatives dialog box closes.

To set the layer drawing order

To set the layer drawing order, do the following:

1. In the Technology Builder dialog box, select Layers > Change Drawing Order.
   The Change Layers' Order dialog box appears.



2. Select the layer(s) you would like to move and use the appropriate buttons to shift the layer(s) up or down.

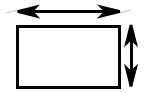
   Note: The first layer in the list is drawn first and the second layer is drawn over the first, and so forth.

3. Click OK.
   The Change Layers' Order dialog box closes and the Layers list in the Technology Builder dialog is updated.

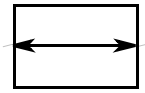
Design Rules

Design rules determine the behavior of shapes and devices on each of the layers. There are two types of design rules you can set: physical design rule and electrical design rule.

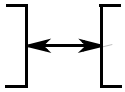
The following design rules are supported by Cadabra:



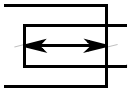
Area Rule



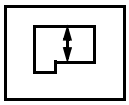
Dimension Rule



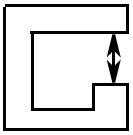
Separation Rule



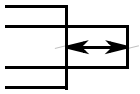
Overlap Rule



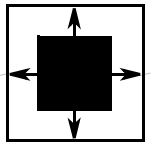
Enclosed Separation Rule



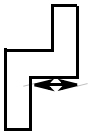
Net Separation Rule



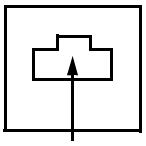
Extension Rule



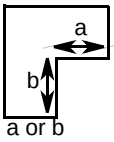
Contact Extension Rule



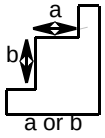
Minimum Edge Length Rule



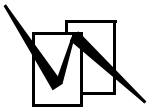
Enclosed Area Rule



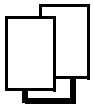
Concave Corner Edge Length Rule



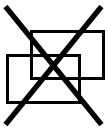
Convex Corner Edge Length Rule



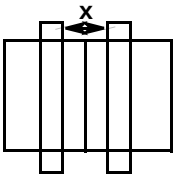
Connectivity Rule



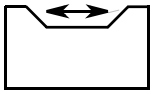
Net Avoidance Rule

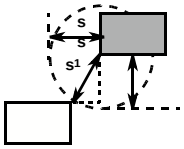


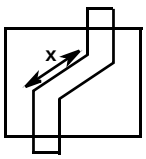
Avoidance Rule



Gate-to-Gate Separation







Spanned Edge Rule | Radial Distance at Corners Rule | Minimum/Maximum Bend Length Rule

Certain design rules are required for a technology. Cadabra prompts you with an error message if you attempt to save or verify a technology that does not have all the required design rules. For a list of these rules, refer to Verification Conditions on page 78.

A preferred minimum can be also used for design rules in the final layout when possible. For more information, refer to Preferred Rule on page 64.

The spacing intervals set for design rules can be altered if certain conditions are met. Refer to the Design Rule Conditions on page 67 for more information on creating and using design rule conditions.

Area Rule

The area rule adds a minimum area rule to the technology. The area rule requires that the area of shape(s) on the specified layer be larger than the specified minimum. This rule may apply to isolated diffusion or metal regions. These regions must be larger than a minimum area, as shown in the first figure above. The minimum width distance depends on the length of the edge being checked. This rule can only be applied to rectangular shapes.

The area rule is supported by the compactor, but the constraints must be generated by a symbolic device. The devices enforce an *approximation* of the minimum area. That is, the area could be a bit more than the minimum, as shown in the second figure above.

This section covers the following topics:

- To add an area design rule
- To edit an area design rule
- Add/Edit Area Design Rule Options

To add an area design rule

To add an area design rule, do the following:

1. In the Technology Builder dialog box, select Design Rules > Add > Area. The Add Area Rule dialog box appears.

Important: Select an existing design rule on the Technology Builder dialog and click Add to have the values of the rule displayed in the New Design Rule dialog box.

2. Set the options (refer to Add/Edit Area Design Rule Options on page 31).
3. Click OK.
   The Add Area Rule dialog box closes and the new rule appears in the Technology Builder dialog box.

To edit an area design rule

To edit an area design rule, do the following:

1. From the table of design rules on the Technology Builder dialog box, select the area design rule you would like to edit.
2. Select Design Rules > Edit.
   The Edit Area Rule dialog box appears.

   Note: Double-clicking the selected design rule also opens the Edit Area Rule dialog box.

3. Edit the options (refer to Add/Edit Area Design Rule Options on page 31).
4. Click OK.
   The Edit Area Rule dialog box closes and the design rule is updated.

   Shortcut: You can edit a design rule's Min and Max spacing values by directly entering the values in the table on the Technology Builder dialog box.

   Note: You can enter comments for the design rules directly in the table on the Technology Builder dialog box.

Add/Edit Area Design Rule Options

Layer: The layer the design rule applies to.

Min: The minimum spacing interval of the rule.

Comment: Any comments you would like to add to the design rule.

Caution: The minimum spacing interval value must be equal to or more than the epsilon value. It must also be a multiple of the manufacturing grid, otherwise, the design rule will appear in red in the table on the Technology Builder dialog box.

Dimension Rule

The dimension rule sets the minimum dimension of shapes on the specified layer. No two external edges can be any closer than the minimum value in this rule.

Every layer must have a dimension rule. Therefore, whenever a new layer is added to a technology, an associated dimension rule is automatically created for that layer.

After the dimension rule is created, it can be edited and a preferred minimum value can be specified, creating a preferred rule. The preferred minimum, which is greater than the dimension rule's minimum, is applied in the final layout when possible.

This section covers the following topics:

To edit a dimension design rule

To edit a dimension design rule, do the following:

1. From the table of design rules on the Technology Builder dialog box, select the dimension design rule you would like to edit.
2. Click Design Rules > Edit.
   The Edit Dimension Rule dialog box appears.

   Note: Double-clicking a dimension design rule in the Technology Builder also opens the Edit Dimension Rule dialog box.

3. Edit the options (refer to Edit Dimension Design Rule Options on page 33).
4. Click OK.
   The Edit Dimension Rule dialog box closes and the design rule is updated.

Shortcut: You can edit a design rule's Min and Max spacing values by directly entering the values in the table on the Technology Builder dialog box.

Note: You can enter comments for the design rules directly in the table on the
Technology Builder dialog box.

Edit Dimension Design Rule Options

Layer: The layer the design rule applies to.

Min: The minimum spacing interval of the rule.

Max: The maximum spacing interval of the rule.

Preferred Rule: A preferred rule is set for the design rule. To specify a preferred rule for a design rule, click Add to open the Add Preferred Rule dialog box. Set the following options, then click OK.

Min: The preferred minimum spacing for the rule.

Priority: The priority of use for the rule. Select a value from the drop-down list.

Distribute: Whether or not the preferred rule is distributed evenly. If multiple preferred rules are used, this option must be set to No.

To add multiple preferred rules, repeat the steps above until all of the preferred rules are added.

Note: To delete a preferred rule, select the rule in the Preferred Rule(s) table and click Delete.

Note: Design rules that have a preferred rule are noted in the Pref. Rule (preferred rule) table column in the Technology Builder. Multiple preferred rules are noted by the text “Multiple”.

Comment: Any comments you would like to add to the design rule.

Caution: The Min and Max spacing interval values must be equal to or more than the epsilon value. They must also be a multiple of the manufacturing grid, otherwise, the design rule will appear in red in the table on the Technology Builder dialog box.

Separation Rule

The separation rule sets the minimum spacing between two shapes on two layers. However, a layer must also have a separation rule against itself. For example, there is a METAL-METAL separation rule. Whenever a new layer is added, appropriate separation rules are automatically added to the technology. The separation rules that are automatically created can be further edited to add dead zones and preferred rules. Additional separation rules can also be added manually to the technology, as they are required.

Multiple minimum and maximum intervals can be specified for a separation rule. For example, two intervals may be specified to accommodate a dead zone where the edge of a device may not exist.

A preferred minimum can also be specified for a separation rule, creating a preferred rule. The preferred minimum, which is greater than the separation rule's minimum, is applied in the final layout when possible.

This section covers the following topics:

To add a separation design rule

To add a separation design rule, do the following:

1. In the Technology Builder dialog box, select Design Rule > Add > Separation.
   The Add Separation Rule dialog box appears.

   Important: Select an existing separation design rule on the Technology Builder dialog to have the values of that rule displayed in the Add Separation Rule dialog box.

2. Set the options (refer to Add/Edit Separation Design Rule Options on page 35).
3. Click OK.
   The Add Separation Rule dialog box closes and the new rule appears in the Technology Builder dialog box.

To edit a separation design rule

To edit a separation design rule, do the following:

1. From the table of design rules on the Technology Builder dialog box, select the separation design rule you would like to edit.
2. Click Edit.
   The Edit Separation Rule dialog box appears.

   Note: Double-clicking the selected separation design rule also opens the Edit Design Rule dialog box.

3. Edit the options (refer to Add/Edit Separation Design Rule Options on page 35).
4. Click OK.
   The Edit Separation Rule dialog box closes and the design rule is updated.

   Shortcut: You can edit a design rule's Min and Max spacing values by directly entering the values in the table on the Technology Builder dialog box.

   Note: You can enter comments for the design rules directly in the table on the
   Technology Builder dialog box.

Add/Edit Separation Design Rule Options

Layer 1: The layer the design rule applies to.

Layer 2: The second layer the design rule applies to.

Min: The minimum spacing interval of the rule.

Max: The maximum spacing interval of the rule.

Preferred Rule: A preferred rule is set for the design rule. To specify a preferred rule for a design rule, click Add to open the Add Preferred Rule dialog box. Set the following options, then click OK.

Min: The preferred minimum spacing for the rule.

Priority: The priority of use for the rule. Select a value from the drop-down list.

Distribute: Whether or not the preferred rule is distributed evenly. If multiple preferred rules are used, this option must be set to No.

To add multiple preferred rules, repeat the steps above until all of the preferred rules are added.

Note: To delete a preferred rule, select the rule in the Preferred Rule(s) table and click Delete.

Note: Design rules that have a preferred rule are noted in the Pref. Rule (preferred rule) table column in the Technology Builder. Multiple preferred rules are noted by the text “Multiple”.

Dead Zone Interval A dead zone is set for the design rule. You must specify the minimum and maximum spacing required to create the dead zone.

Comment: Any comments you would like to add to the design rule.

Caution: The Min and Max spacing interval values must be equal to or more than the epsilon value. They must also be a multiple of the manufacturing grid, otherwise, the design rule will appear in red in the table on the Technology Builder dialog box.

Overlap Rule

The overlap rule sets the amount by which two layers must extend onto each other. This rule is similar to the extension rule, but the area of interest is the overlap region of both layers, rather than the extension region of one layer beyond another.

Cadabra does not automatically support the overlap rule in the compactor. The device that contains overlapping shapes uses the value from the technology to support the overlap rule.

This section covers the following topics:

- To add an overlap design rule
- To edit an overlap design rule
- Add/Edit Overlap Design Rule Options

To add an overlap design rule

To add an overlap design rule, do the following:

1. In the Technology Builder dialog box, click Design Rule > Add > Overlap.
   The Add Overlap Rule dialog box appears.

   Important: Select an existing overlap design rule on the Technology Builder dialog to have the values of that rule displayed in the Add Overlap Rule dialog box.

2. Set the options (refer to Add/Edit Overlap Design Rule Options on page 38).
3. Click OK.
   The Add Overlap Rule dialog box closes and the new rule appears in the Technology Builder dialog box.

To edit an overlap design rule

To edit an overlap design rule, do the following:

1. From the table of design rules on the Technology Builder dialog box, select the overlap design rule you would like to edit.
2. Click Edit.
   The Edit Overlap Rule dialog box appears.

   Note: Double-clicking the selected overlap design rule also opens the Edit Overlap Rule dialog box.

3. Edit the options (refer to Add/Edit Overlap Design Rule Options on page 38).
4. Click OK.
   The Edit Overlap Rule dialog box closes and the design rule is updated.

   Shortcut: You can edit a design rule's Min and Max spacing values by directly entering the values in the table on the Technology Builder dialog box.

   Note: You can enter comments for the design rules directly in the table on the
   Technology Builder dialog box.

Add/Edit Overlap Design Rule Options

Layer 1: The layer the design rule applies to.

Layer 2: The second layer the design rule applies to.

Min: The minimum spacing interval of the rule.

Max: The maximum spacing interval of the rule.

Comment: Any comments you would like to add to the design rule.

Caution: The Min and Max spacing interval values must be equal to or more than the epsilon value. They must also be a multiple of the manufacturing grid, otherwise, the design rule will appear in red in the table on the Technology Builder dialog box.

Enclosed Separation Rule

The enclosed separation rule sets the minimum spacing between two edges of an enclosed area (a hole) on one layer.

Multiple spacing intervals can be specified for a separation rule. For example, two intervals may be specified to accommodate a dead zone where the edge of the enclosed area may not exist.

A preferred minimum can also be specified, creating a preferred rule. The preferred minimum, which is greater than the enclosed separation rule's minimum, is applied in the final layout when possible.

The compactor enforces this rule natively.

This section covers the following topics:

To add an enclosed separation design rule

To add an enclosed separation design rule, do the following:

1. In the Technology Builder dialog box, click Design Rule > Add > Enclosed Separation.
   The Add Enclosed Separation Rule dialog box appears.

   Important: Select an existing enclosed separation design rule on the Technology Builder dialog to have the values of that rule displayed in the Add Enclosed Separation Rule dialog box.

2. Set the options (refer to Add/Edit Enclosed Separation Design Rule Options on page 40).
3. Click OK.
   The New Enclosed Separation Rule dialog box closes and the new rule appears in the Technology Builder dialog box.

To edit an enclosed separation design rule

To edit an enclosed separation design rule, do the following:

1. From the table of design rules on the Technology Builder dialog box, select the enclosed separation design rule you would like to edit.
2. Click Edit.
   The Edit Enclosed Separation Rule dialog box appears.

   Note: Double-clicking the selected enclosed separation design rule also opens the Edit Enclosed Separation Rule dialog box.

3. Edit the options (refer to Add/Edit Enclosed Separation Design Rule Options on page 40).
4. Click OK.
   The Edit Enclosed Separation Rule dialog box closes and the design rule is updated.

   Shortcut: You can edit the Min spacing value by directly entering the value in the table on the Technology Builder dialog box.

Note: You can enter comments for the design rules directly in the table on the Technology Builder dialog box.

Add/Edit Enclosed Separation Design Rule Options

Layer 1: The layer the design rule applies to.

Layer 2: The second layer the design rule applies to.

Min: The minimum spacing interval of the rule.

Max: The maximum spacing interval of the rule.

Preferred Rule: A preferred rule is set for the design rule. To specify a preferred rule for a design rule, click Add to open the Add Preferred Rule dialog box. Set the following options, then click OK.

Min: The preferred minimum spacing for the rule.

Priority: The priority of use for the rule. Select a value from the drop-down list.

Distribute: Whether or not the preferred rule is distributed evenly. If multiple preferred rules are used, this option must be set to No.

To add multiple preferred rules, repeat the steps above until all of the preferred rules are added.

Note: To delete a preferred rule, select the rule in the Preferred Rule(s) table and click Delete.

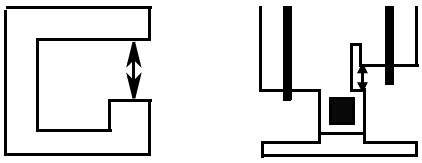
Note: Design rules that have a preferred rule are noted in the Pref. Rule (preferred rule) table column in the Technology Builder. Multiple preferred rules are noted by the text “Multiple”.

Dead Zone Interval: A dead zone is set for the design rule. You must specify the minimum and maximum spacing required to create the dead zone.

Comment: Any comments you would like to add to the design rule.

Caution: The Min and Max spacing interval values must be equal to or more than the epsilon value. They must also be a multiple of the manufacturing grid, otherwise, the design rule will appear in red in the table on the Technology Builder dialog box.

Net Separation Rule



The net separation rule sets a separation between layers on the same net.

When the compactor encounters non-overlapping layers, it will enforce the appropriate separation rule between them. However, if the two layers are on the same net, the compactor first checks for a net separation rule between the two layers. If one exists, the interval set in the net separation rule overrides the one set in the separation rule.

The minimum interval for a net separation rule is often set to a negative value or 0. A negative value causes the two layers to overlap, while a value of 0 fills in the notch between the two layers.

For example, a tie may force a separation with a MOSFET, as shown in the second figure above. For other examples where a net separation rule may be used, refer to Optimizing Your Technology on page 80.

Multiple minimum and maximum ranges can be specified for a net separation rule. For example, two ranges may be specified to accommodate a dead zone where the edge of a device may not exist.

A preferred minimum can also be specified for a net separation rule, creating a preferred rule. The preferred minimum, which is greater than the net separation rule's minimum, is applied in the final layout when possible.

This section covers the following topics:

- To add a net separation design rule
- To edit a net separation design rule
- Add/Edit Net Separation Design Rule Options

To add a net separation design rule

To add a net separation design rule, do the following:

1. In the Technology Builder dialog box, click Design Rule > Add > Net Separation.

Result: The Add Net Separation Rule dialog box appears.

Note: Select an existing net separation design rule on the Technology Builder dialog to have the values of that rule displayed in the Add Net Separation Rule dialog.

2. Set the options (refer to Add/Edit Enclosed Separation Design Rule Options on page 40).
3. Click OK.

   Result: The Add Net Separation Rule dialog box closes and the new rule appears in the Technology Builder dialog box.

To edit a net separation design rule

To edit a net separation design rule, do the following:

1. From the table of design rules on the Technology Builder dialog box, select the net separation design rule you would like to edit.
2. Click Edit.
   The Edit Net Separation Rule dialog box appears.

   Note: Double-clicking the selected design net separation rule also opens the Edit Net Separation Rule dialog box.

3. Edit the options (refer to Add/Edit Enclosed Separation Design Rule Options on page 40).
4. Click OK.
   The Edit Net Separation Rule dialog box closes and the design rule is updated.

   Shortcut: You can edit a design rule's Min and Max spacing values by directly entering the values in the table on the Technology Builder dialog box.

   Note: You can enter comments for the design rules directly in the table on the Technology Builder dialog box.

Add/Edit Net Separation Design Rule Options

Layer 1: The layer the design rule applies to.

Layer 2: The second layer the design rule applies to.

Min: The minimum spacing interval of the rule.

Max: The maximum spacing interval of the rule.

Preferred Rule: A preferred rule is set for the design rule. To specify a preferred rule for a design rule, click Add to open the Add Preferred Rule dialog box. Set the following options, then click OK.

Min: The preferred minimum spacing for the rule.

Priority: The priority of use for the rule. Select a value from the drop-down list.

Distribute: Whether or not the preferred rule is distributed evenly. If multiple preferred rules are used, this option must be set to No.

To add multiple preferred rules, repeat the steps above until all of the preferred rules are added.

Note: To delete a preferred rule, select the rule in the Preferred Rule(s) table and click Delete.

Note: Design rules that have a preferred rule are noted in the Pref. Rule (preferred rule) table column in the Technology Builder. Multiple preferred rules are noted by the text “Multiple”.

Dead Zone Interval: A dead zone is set for the design rule. You must specify the minimum and maximum spacing required to create the dead zone.

Comment: Any comments you would like to add to the design rule.

Caution: The Min and Max spacing interval values must be equal to or more than the epsilon value. They must also be a multiple of the manufacturing grid, otherwise, the design rule will appear in red in the table on the Technology Builder dialog box.

Extension Rule

The extension rule sets the amount by which one layer must extend past another. There cannot be a connectivity rule between the two layers of an extension rule. If a connectivity rule exists between the two layers specified for the extension rule, the rule defaults to a Contact Extension Rule.

You must set a corresponding extension rule for any asymmetrical extension rule you set. However, the extension rule must have the smaller value of the two. Otherwise, the larger extension may be enforced rather than the smaller one. This is because the compactor automatically enforces the extension rule while the device is meant to enforce the asymmetrical extension rule.

A preferred minimum can also be specified for an extension rule, creating a preferred rule. The preferred minimum, which is greater than the extension rule's minimum, is applied in the final layout when possible.

This section covers the following topics:

To add an extension design rule

To add an extension design rule, do the following:

1. In the Technology Builder dialog box, click Design Rule > Add > Extension.
   The Add Extension Rule dialog box appears.

   Important: Select an existing extension design rule on the Technology Builder dialog to have the values of that rule displayed in the Add Extension Rule dialog box.

2. Set the options (refer to Add/Edit Extension Design Rule Options on page 45).
3. Click OK.
   The Add Extension Rule dialog box closes and the new rule appears in the Technology Builder dialog box.

To edit an extension design rule

To edit an extension design rule, do the following:

1. From the table of design rules on the Technology Builder dialog box, select the extension design rule you would like to edit.
2. Click Edit.
   The Edit Extension Rule dialog box appears.

Note: Double-clicking the selected extension design rule also opens the Edit Extension Rule dialog box.

3. Edit the options (refer to Add/Edit Extension Design Rule Options on page 45).
4. Click OK.
   The Edit Extension Rule dialog box closes and the design rule is updated.

   Shortcut: You can edit a design rule's Min and Max spacing values by directly entering the values in the table on the Technology Builder dialog box.

   Note: You can enter comments for the design rules directly in the table on the
   Technology Builder dialog box.

Add/Edit Extension Design Rule Options

Layer 1: The layer the design rule applies to.

Layer 2: The second layer the design rule applies to.

Min: The minimum spacing interval of the rule.

Max: The maximum spacing interval of the rule.

Preferred Rule: A preferred rule is set for the design rule. To specify a preferred rule for a design rule, click Add to open the Add Preferred Rule dialog box. Set the following options, then click OK.

Min: The preferred minimum spacing for the rule.

Priority: The priority of use for the rule. Select a value from the drop-down list.

Distribute: Whether or not the preferred rule is distributed evenly. If multiple preferred rules are used, this option must be set to No.

To add multiple preferred rules, repeat the steps above until all of the preferred rules are added.

Note: To delete a preferred rule, select the rule in the Preferred Rule(s) table and click Delete.

Note: Design rules that have a preferred rule are noted in the Pref. Rule (preferred rule) table column in the Technology Builder. Multiple preferred rules are noted by the text “Multiple”.

Comment: Any comments you would like to add to the design rule.

Caution: The Min and Max spacing interval values must be equal to or more than the epsilon value. They must also be a multiple of the manufacturing grid, otherwise, the design rule will appear in red in the table on the Technology Builder dialog box.

Contact Extension Rule

The contact extension rule is a combination of symmetrical and asymmetrical extension rules, which are based on the extension rule. The contact extension rule sets the constraints for contact devices by modifying an existing extension rule. However, contact extension rules differ from extension rules in that there must be a connectivity rule between the layers and that they can only be applied to contact devices.

The contact extension rule is supported by the compactor, but the constraints must be generated by a symbolic device. Both of the symmetrical and asymmetrical contact extension rules can only be applied to rectangular shapes and against pairs of parallel edges.

The symmetrical and asymmetrical contact extension rules are created using the Add Contact Extension Rule dialog box. A symmetrical contact extension rule can also be created by adding a connectivity rule between the two layers of an existing extension rule. Conversely, if a connectivity rule between the two layers of a symmetrical contact extension rule is deleted, the contact extension rule is changed to an Extension Rule.

A preferred minimum can also be specified for contact extension rules, creating a preferred rule. The preferred minimum, which is greater than the contact extension rule's minimum, is applied in the final layout when possible.

This section covers the following topics:

- To add a contact extension design rule
- To edit a contact extension design rule
- Add/Edit Contact Extension Design Rule Options

To add a contact extension design rule

To add a contact extension design rule, do the following:

1. In the Technology Builder dialog box, click Design Rule > Add > Contact Extension.
   The Add Contact Extension Rule dialog box appears.

   Important: Select an existing design rule on the Technology Builder dialog to have the values of that rule displayed in the Add Contact Extension Rule dialog box.

2. Set the options (refer to Add/Edit Contact Extension Design Rule Options on page 48).
3. Click OK.
   The Add Contact Extension Rule dialog box closes and the new rule appears in the Technology Builder dialog box.

To edit a contact extension design rule

To edit a contact extension design rule, do the following:

1. From the table of design rules on the Technology Builder dialog box, select the contact extension design rule you would like to edit.
2. Click Edit.
   The Edit Contact Extension Rule dialog box appears.

   Note: Double-clicking the selected design rule also opens the Edit Contact Extension Rule dialog box.

3. Edit the options (refer to Add/Edit Contact Extension Design Rule Options on page 48).
4. Click OK.
   The Edit Contact Extension Rule dialog box closes and the design rule is updated.

   Shortcut: You can edit a design rule's Min and Max spacing values by directly entering the values in the table on the Technology Builder dialog box.

   Note: You can enter comments for the design rules directly in the table on the Technology Builder dialog box.

Add/Edit Contact Extension Design Rule Options

Before a symmetrical or asymmetrical contact extension rule can be created between two layers, the two layers must first have a Connectivity Rule between them.

Cover Layer: The contact cover layer the design rule applies to.

Contact Cut Layer: The contact cut layer the design rule applies to.

Symmetrical: The contact extension is applied symmetrically between the specified contact layers.

Extension:

Min: The minimum spacing interval for the extension.

Max: The maximum spacing interval for the extension.

Asymmetrical: The contact extension is specified as two values: a short extension and a long extension and it is applied asymmetrically between the specified contact layers.

Short Extension:

Min: The minimum spacing interval for the short extension.

Max: The maximum spacing interval for the short extension.

Long Extension:

Min: The minimum spacing interval for the long extension.

Max: The maximum spacing interval for the long extension.

Note: The values for the short extension must be less than the values for the extension, which in turn must be less than the values for the long extension.

Preferred Rule: A preferred rule can be set for each of the symmetrical and asymmetrical contact extensions. To specify a preferred rule for a contact extension, click Add to open the Add Preferred Rule dialog box. Set the following options, then click OK.

Min: The preferred minimum spacing for the rule.

Priority: The priority of use for the rule. Select a value from the drop-down list.

Distribute: Whether or not the preferred rule is distributed evenly. If multiple preferred rules are used, this option must be set to No.

To add multiple preferred rules, repeat the steps above until all of the preferred rules are added.

Note: To delete a preferred rule, select the rule in the Preferred Rule(s) table and click Delete.

Note: Design rules that have a preferred rule are noted in the Pref. Rule (preferred rule) table column in the Technology Builder. Multiple preferred rules are noted by the text “Multiple”.

Comment: Any comments you would like to add to the design rule.

Caution: The Min and Max spacing interval values must be equal to or more than the epsilon value. They must also be a multiple of the manufacturing grid, otherwise, the design rule will appear in red in the table on the Technology Builder dialog box.

Minimum Edge Length Rule

The minimum edge length rule sets the minimum length for all edges on a layer.

A preferred minimum can also be specified for a minimum edge length rule, creating a preferred rule. The preferred minimum, which is greater than the minimum edge length rule’s minimum, is applied in the final layout when possible.

This section covers the following topics:

To add a minimum edge length design rule

To add a minimum edge length design rule, do the following:

1. In the Technology Builder dialog box, click Design Rule > Add > Minimum Edge Length.
   The Add Minimum Edge Length Rule dialog box appears.

Important: Select an existing minimum edge length design rule on the Technology Builder dialog to have the values of that rule displayed in the Add Minimum Edge Length Rule dialog box.

2. Set the options (refer to Add/Edit Minimum Edge Length Design Rule Options on page 50).
3. Click OK.
   The New Minimum Edge Length Rule dialog box closes and the new rule appears in the Technology Builder dialog box.

To edit a minimum edge length design rule

To edit a minimum edge length design rule, do the following:

1. From the table of design rules on the Technology Builder dialog box, select the minimum edge length design rule you would like to edit.
2. Click Edit.
   The Edit Minimum Edge Length Rule dialog box appears.

   Note: Double-clicking the selected minimum edge length design rule also opens the Edit Minimum Edge Length Rule dialog box.

3. Edit the options (refer to Add/Edit Minimum Edge Length Design Rule Options on page 50).
4. Click OK.
   The Edit Minimum Edge Length Rule dialog box closes and the design rule is updated.

   Shortcut: You can edit a design rule's Min and Max spacing values by directly entering the values in the table on the Technology Builder dialog box.

   Note: You can enter comments for the design rules directly in the table on the Technology Builder dialog box.

Add/Edit Minimum Edge Length Design Rule Options

Layer 1: The layer the design rule applies to.

Layer 2: The second layer the design rule applies to.

Min: The minimum spacing interval of the rule.

Max: The maximum spacing interval of the rule.

Preferred Rule: A preferred rule is set for the design rule. To specify a preferred rule for a design rule, click Add to open the Add Preferred Rule dialog box. Set the following options, then click OK.

Min: The preferred minimum spacing for the rule.

Priority: The priority of use for the rule. Select a value from the drop-down list.

Distribute: Whether or not the preferred rule is distributed evenly. If multiple preferred rules are used, this option must be set to No.

To add multiple preferred rules, repeat the steps above until all of the preferred rules are added.

Note: To delete a preferred rule, select the rule in the Preferred Rule(s) table and click Delete.

Note: Design rules that have a preferred rule are noted in the Pref. Rule (preferred rule) table column in the Technology Builder. Multiple preferred rules are noted by the text “Multiple”.

Comment: Any comments you would like to add to the design rule.

Caution: The Min and Max spacing interval values must be equal to or more than the epsilon value. They must also be a multiple of the manufacturing grid, otherwise, the design rule will appear in red in the table on the Technology Builder dialog box.

Enclosed Area Rule

This rule adds a minimum enclosed area rule to the technology. It requires that the enclosed area (a hole) on the specified layer be larger than a specified minimum. Note that the entire diffusion island plus the rail straps are counted together in the enclosed minimum area check.

This rule is automatically supported by the compactor with a built-in device called “Enclosed Area Device”. The enforced area could be a little larger than the minimum due to approximation.

This section covers the following topics:

To add an enclosed area design rule

To add an enclosed area design rule, do the following:

1. In the Technology Builder dialog box, click Design Rule > Add > Enclosed Area.
   The Add Enclosed Area Rule dialog box appears.

   Important: Select an existing enclosed area design rule on the Technology Builder dialog to have the values of that rule displayed in the Add Enclosed Area Rule dialog box.

2. Set the options (refer to Add/Edit Enclosed Area Design Rule Options on page 53).
3. Click OK.
   The New Enclosed Area Rule dialog box closes and the new rule appears in the Technology Builder dialog box.

To edit an enclosed area design rule

To edit an enclosed area design rule, do the following:

1. From the table of design rules on the Technology Builder dialog box, select the enclosed area design rule you would like to edit.
2. Click Edit.
   The Edit Enclosed Area Rule dialog box appears.

   Note: Double-clicking the selected enclosed area design rule also opens the Edit Enclosed Area Rule dialog box.

3. Edit the options (refer to Add/Edit Enclosed Area Design Rule Options on page 53).
4. Click OK.
   The Edit Enclosed Area Rule dialog box closes and the design rule is updated.

Shortcut: You can edit the Min spacing value by directly entering the value in the table on the Technology Builder dialog box.

Note: You can enter comments for the design rules directly in the table on the Technology Builder dialog box.

Add/Edit Enclosed Area Design Rule Options

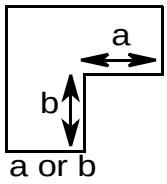
Layer: The layer the design rule applies to.

Min: The minimum spacing interval of the rule.

Comment: Any comments you would like to add to the design rule.

Caution: The Min spacing interval value must be equal to or more than the epsilon value. It must also be a multiple of the manufacturing grid, otherwise, the design rule will appear in red in the table on the Technology Builder dialog box.

Concave Corner Edge Length Rule



The concave corner edge length rule sets the minimum length for at least one edge of a concave corner on a specified layer. This rule does not apply to corners which involve 45 degree edges.

This section covers the following topics:

To add a concave corner edge length design rule

To add a concave corner edge length design rule, do the following:

1. In the Technology Builder dialog box, click Design Rule > Add > Concave Corner Edge Length.
   The Add Concave Corner Edge Length Rule dialog box appears.

   Important: Select an existing concave corner edge length design rule on the Technology Builder dialog to have the values of that rule displayed in the Add Concave Corner Edge Length Rule dialog box.

2. Set the options (refer to Add/Edit Concave Corner Edge Length Design Rule Options on page 55).
3. Click OK.
   The New Concave Corner Edge Length Rule dialog box closes and the new rule appears in the Technology Builder dialog box.

To edit a concave corner edge length design rule

To edit a concave corner edge length design rule, do the following:

1. From the table of design rules on the Technology Builder dialog box, select the concave corner edge length design rule you would like to edit.
2. Click Edit.
   The Edit Concave Corner Edge Length Rule dialog box appears.

   Note: Double-clicking the selected concave corner edge length design rule also opens the Edit Concave Corner Edge Length Rule dialog box.

3. Edit the options (refer to Add/Edit Concave Corner Edge Length Design Rule Options on page 55).
4. Click OK.
   The Edit Concave Corner Edge Length Rule dialog box closes and the design rule is updated.

   Shortcut: You can edit a design rule's Min and Max spacing values by directly entering the values in the table on the Technology Builder dialog box.

Note: You can enter comments for the design rules directly in the table on the Technology Builder dialog box.

Add/Edit Concave Corner Edge Length Design Rule Options

Layer: The layer the design rule applies to.

Min: The minimum spacing interval of the rule.

Comment: Any comments you would like to add to the design rule.

Caution: The Min spacing interval value must be equal to or more than the epsilon value. It must also be a multiple of the manufacturing grid, otherwise, the design rule will appear in red in the table on the Technology Builder dialog box.

Convex Corner Edge Length Rule

The convex corner edge length rule sets the minimum length for at least one edge of a convex corner on a specified layer. This rule does not apply to corners which involve 45 degree edges.

This section covers the following topics:

To add a convex corner edge length design rule

To add a convex corner edge length design rule, do the following:

1. In the Technology Builder dialog box, click Design Rule > Add > Convex Corner Edge Length.
   The Add Convex Corner Edge Length Rule dialog box appears.

Important: Select an existing convex corner edge length design rule on the Technology Builder dialog to have the values of that rule displayed in the Add Convex Corner Edge Length Rule dialog box.

2. Set the options (refer to Add/Edit Convex Corner Edge Length Design Rule Options on page 57).
3. Click OK.
   The New Convex Corner Edge Length Rule dialog box closes and the new rule appears in the Technology Builder dialog box.

To edit a convex corner edge length design rule

To edit a convex corner edge length design rule, do the following:

1. From the table of design rules on the Technology Builder dialog box, select the convex corner edge length design rule you would like to edit.
2. Click Edit.
   The Edit Convex Corner Edge Length Rule dialog box appears.

   Note: Double-clicking the selected convex corner edge length design rule also opens the Edit Convex Corner Edge Length Rule dialog box.

3. Edit the options (refer to Add/Edit Convex Corner Edge Length Design Rule Options on page 57)..
4. Click OK.
   The Edit Convex Corner Edge Length Rule dialog box closes and the design rule is updated.

   Shortcut: You can edit a design rule's Min and Max spacing values by directly entering the values in the table on the Technology Builder dialog box.

   Note: You can enter comments for the design rules directly in the table on the Technology Builder dialog box.

Add/Edit Convex Corner Edge Length Design Rule Options

Layer: The layer the design rule applies to.

Min: The minimum spacing interval of the rule.

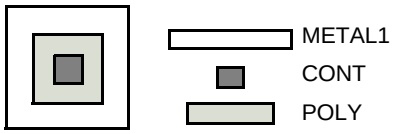
Comment: Any comments you would like to add to the design rule.

Caution: The Min spacing interval value must be equal to or more than the epsilon value. It must also be a multiple of the manufacturing grid, otherwise, the design rule will appear in red in the table on the Technology Builder dialog box.

Connectivity Rule

The connectivity rule specifies that two layers connect electrically if they touch.

For example, there could be a connectivity rule between POLY and CONTACT, and CONTACT and METAL1, but not between POLY and METAL1 since they do not connect directly, as shown in the figure below.



Note: If you add a connectivity rule between two layers that are used for an Extension Rule, the extension rule is changed to a Contact Extension Rule. Conversely, if you remove a connectivity rule between two layer that are used for a contact extension rule, the connectivity rule is changed to an extension rule.

This section covers the following topics:

To add a connectivity design rule

To add a connectivity design rule, do the following:

1. In the Technology Builder dialog box, click Design Rule > Add > Electrical Connectivity.
   The Add Connectivity Rule dialog box appears.

   Important: Select an existing design rule on the Technology Builder dialog to have the values of that rule displayed in the Add Connectivity Rule dialog box.

2. Set the options (refer to Add/Edit Connectivity Design Rule Options on page 58).
3. Click OK.
   The Add Connectivity Rule dialog box closes and the new rule appears in the Technology Builder dialog box.

To edit a connectivity design rule

To edit a connectivity design rule, do the following:

1. From the table of design rules on the Technology Builder dialog box, select the connectivity design rule you would like to edit.
2. Click Edit.
   The Edit Connectivity Rule dialog box appears.

   Note: Double-clicking the selected connectivity design rule also opens the Edit Connectivity Rule dialog box.

3. Edit the options (refer to Add/Edit Connectivity Design Rule Options on page 58).
4. Click OK.
   The Edit Connectivity Rule dialog box closes and the design rule is updated.

   Note: You can enter comments for the design rules directly in the table on the Technology Builder dialog box.

Add/Edit Connectivity Design Rule Options

Layer 1: The layer the design rule applies to.

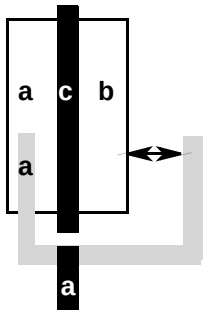
Layer 2: The second layer the design rule applies to.

Comment: Any comments you would like to add to the design rule.

Net Avoidance Rule

The net avoidance rule specifies that two layers must avoid one another unless they carry the same net.

For example, the net avoidance rule can be used to prevent LI from connecting to POLY or ACTIVE unless they are on the same net, as shown in the figure below.



This section covers the following topics:

- To add a net avoidance design rule
- To edit a net avoidance design rule
- Add/Edit Net Avoidance Design Rule Options

To add a net avoidance design rule

To add a net avoidance design rule, do the following:

1. In the Technology Builder dialog box, click Design Rule > Add > Electrical Net Avoidance.
   The Add Net Avoidance Rule dialog box appears.

   Important: Select an existing net avoidance design rule on the Technology Builder dialog to have the values of that rule displayed in the Add Net Avoidance Rule dialog box.

2. Set the options (refer toAdd/Edit Net Avoidance Design Rule Options on page 60).

3. Click OK.
   The Add Net Avoidance Rule dialog box closes and the new rule appears in the Technology Builder dialog box.

To edit a net avoidance design rule

To edit a net avoidance design rule, do the following:

1. From the table of design rules on the Technology Builder dialog box, select the net avoidance design rule you would like to edit.
2. Click Edit.
   The Edit Net Avoidance Rule dialog box appears.

   Note: Double-clicking the selected net avoidance design rule also opens the Edit Net Avoidance Rule dialog box.

3. Edit thoptions (refer toAdd/Edit Net Avoidance Design Rule Options on page 60).
4. Click OK.
   The Edit Net Avoidance Rule dialog box closes and the design rule is updated.

   Note: You can enter comments for the design rules directly in the table on the Technology Builder dialog box.

Add/Edit Net Avoidance Design Rule Options

Layer 1: The layer the design rule applies to.

Layer 2: The second layer the design rule applies to.

Comment: Any comments you would like to add to the design rule.

Avoidance Rule

The avoidance rule prevents the router and compactor from placing one layer on top of another, even if the shapes involved carry the same net.

However, two avoidance layers can abut, if there is also a connectivity rule and separation rule of 0 between them, as shown in the figure below.

This section covers the following topics:

To add an avoidance design rule

To add an avoidance design rule, do the following:

1. In the Technology Builder dialog box, click Design Rule > Add > Electrical Avoidance.
   The Add Avoidance Rule dialog box appears.

   Important: Select an existing avoidance design rule on the Technology Builder dialog to have the values of that rule displayed in the Add Avoidance Rule dialog box.

2. Set the options (refer to Add/Edit Avoidance Design Rule Options on page 62).
3. Click OK.
   The Add Avoidance Rule dialog box closes and the new rule appears in the Technology Builder dialog box.

To edit an avoidance design rule

To edit an avoidance design rule, do the following:

1. From the table of design rules on the Technology Builder dialog box, select the avoidance design rule you would like to edit.
2. Click Edit.
   The Edit Avoidance Rule dialog box appears.

   Note: Double-clicking the selected avoidance design rule also opens the Edit Avoidance Rule dialog box.

3. Edit the options (refer to Add/Edit Avoidance Design Rule Options on page 62).
4. Click OK.
   The Edit Avoidance Rule dialog box closes and the design rule is updated.

Note: You can enter comments for the design rules directly in the table on the Technology Builder dialog box.

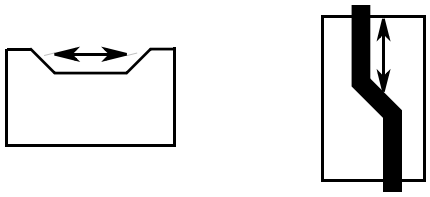
Add/Edit Avoidance Design Rule Options

Layer 1: The layer the design rule applies to.

Layer 2: The second layer the design rule applies to.

Comment: Any comments you would like to add to the design rule.

Spanned Edge Rule



The spanned edge rule modifies an existing design rule between two edges that are connected by a common edge.

In Cadabra, spanned edge rules are implemented by adding conditions to existing design rules.

For example, the spanned edge rule would be enforced in the second figure above by adding a condition with an edge 90 to edge 45 configuration and vertical orientation to the POLY-Diffusion extension rule.

For other examples where a spanned edge rule may be used, refer to Optimizing Your Technology on page 80.

Radial Distance at Corners Rule

The radial distance at corners rule sets a different separation for layers between two corners.

In Cadabra, you can set radial distance at corner rules by adding corner conditions to your separation design rules.

Minimum/Maximum Bend Length Rule

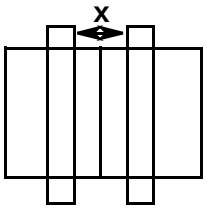
The minimum/maximum bend length rule sets dimension rules for gate bends.

In Cadabra, minimum/maximum bend lengths are set in the Architecture Builder. When adding a MOSFET to your architecture, you can select the Allow gate bends option and then specify the minimum and maximum lengths for the gate bends. You can also specify other gate bend properties at this time.

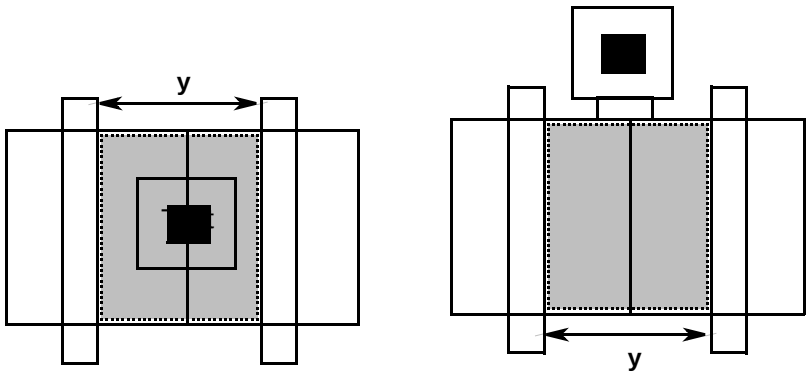
Gate-to-Gate Separation

When there is a device between two MOSFET gates, a different separation distance may need to be enforced between the two gates than when there is not.

For example, if there is no device between the two adjacent gates, then the standard gate-to-gate separation rule is enforced as shown in the figure below.



However, if there is a contact in the vertical column between two adjacent gates the Gate Separator device is placed between the two gates to enforce a different separation distance as shown in the figure below.



Gate Separator Device added to enforce rules in special cases

The Gate Separator device is available with Cadabra's Generic Portfolio. When setting up your MOSFET elements in your architecture, you can select Enforce extra separation when diffusion contains contacts to have Cadabra use the Gate Separator device when necessary.

Preferred Rule

A preferred rule is set for the design rule. You must specify the preferred minimum spacing, the priority of its use, and whether or not it is evenly distributed. The preferred minimum must be a value within the design rule's specified interval (that is, greater than the minimum and lesser than the maximum).

Preferred rules can only be set for the dimension, extension, asymmetrical extension, separation, and net separation rules and are only enforced when the Advanced Cell Compact design step is run. Preferred rules cannot be set for the separation and net separation rules if a dead zone has been set. Also, preferred rules cannot be set for design rule conditions.

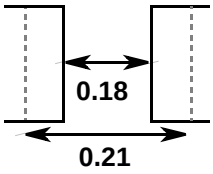
This section covers the following topics:

- Why set this option?

Why set this option?

Preferred rules allow a second, greater value to be used in the final layout for the specific design rule when possible. At the same time, the main objectives are met.

For example, a separation rule can be set using a minimum of 0.18 and a preferred minimum of 0.21. In the final layout, if possible, the preferred minimum is applied, as shown in the figure below.



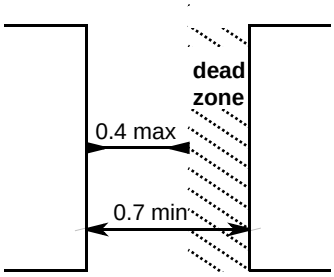
If a preferred rule is also set to be evenly distributed, whenever the preferred minimum spacing is met, the objects which apply to the design rule are distributed in an even fashion in the layout.

Dead Zone Interval

A dead zone is set for the design rule. You must specify the minimum and maximum spacing required to create the dead zone. This second spacing interval for the design rule cannot overlap with its first interval, otherwise a dead zone is not created. A dead zone is the space between the two spacing intervals. The edge of a shape cannot exist in the dead zone.

For example, as illustrated in the figure below, a separation rule can be set between POLY and GATE with a minimum spacing of 0.1 microns, and a maximum spacing of 0.4 microns. Then, a dead zone interval of 0.7 (minimum) and 0.9 (maximum) can be added. As a result, the edges of the two shapes can

exist in the regions 0.1 - 0.4 and 0.7 - 0.9. However, the region 0.4 - 0.7 is a dead zone and the edge of a shape cannot appear in this zone.



Dead zones can only be set for the separation, net separation, and enclosed separation rules and only if a preferred rule has not been set.

To filter design rules for viewing

Filtering the layers and design rules on the Technology Builder dialog allows you to view a specific group of rules. To filter design rules for viewing, do the following:

1. In the Technology Builder dialog box, select the layers you would like to view the design rules for from the Layers listbox.
   All the design rules for the selected layers appear in the bottom table.
2. Select Hide unselected layers if you would only like to view design rules that only contain the selected layers in both Layer 1 and Layer 2. Otherwise, all design rules that have the selected layers in either Layer 1 or Layer 2 are displayed.
   All the design rules for the selected layers appear in the bottom table.
3. Select the design rules you would like to view.
   The selected design rules for the specified layers appear in the bottom table.

   Caution: Design rules appearing in red indicate that the rule has an interval value
   that is not a multiple of the manufacturing grid. Since all edges must lay
   on a manufacturing line, interval values should be a multiple of the
   manufacturing grid.

To sort design rules for viewing

Sorting the design rules in the Technology Builder dialog allows you to alter the viewing order of the rules. Design rules can be sorted in ascending and descending order based on the column headers in the design rule table that appears at the bottom of the Technology Builder dialog box. To sort design rules for viewing, do the following:

1. In the Technology Builder dialog box, click the design rule table column header you would like to sort the design rules by.
   A “t” button appears on the right side of the column header.
2. Click the “t” button to sort the design rules in descending order.
   A “s” button replaces the “t” button in the column header and the design rules are sorted based on the values in the selected column.
3. Click the “s” button to sort the design rules in ascending order.
   The design rules are re-sorted based on the values in the selected column.

To delete a design rule

To delete a design rule, do the following:

1. From the table of design rules on the Technology Builder dialog box, select the design rule(s) you would like to delete.
2. Click Delete.
   A Question dialog box appears to confirm the removal.
3. Click Yes.
   The selected design rule(s) are removed.

Design Rule Conditions

Design rule conditions alter the specified spacing of design rules if certain conditions are met. There are four types of design rule conditions that you can set:

- Simple Condition
- Common Run Condition

- Width Dependent Condition
- Common Run and Width Dependent Condition

Note: The common run and common run and width dependent conditions can only be applied to separation design rules. The width dependent condition can be applied to both separation and extension design rules.

Simple Condition

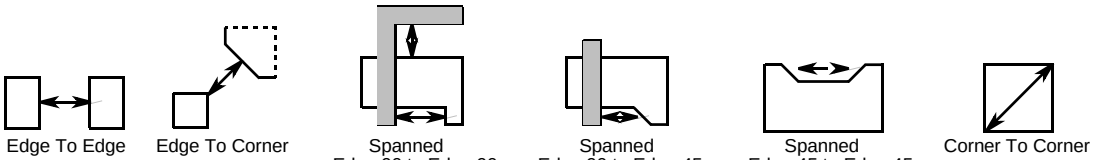
A simple condition is based on the configuration and orientation of two edges. Both the specified configuration and orientation must be met before the conditional rule is enforced.

This section covers the following topics:

- Configuration Conditions
- Orientation Conditions
- To add a simple design rule condition
- To edit a simple design rule condition
- Add/Edit Simple Condition Options

Configuration Conditions

A conditional rule is only enforced if the edges meet a specific configuration between two shapes before the design rule condition will be applied. The configurations that might be required are shown below.



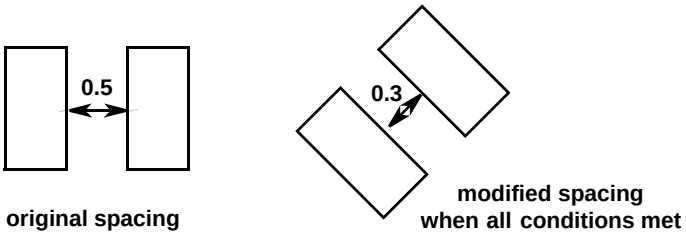
Note: If a spanned Edge 90 to Edge 90 configuration condition is added to a Separation Rule or Net Separation Rule, a dead zone interval can also be added to the condition.

Orientation Conditions

A conditional rule is only enforced if the edges that meet the configuration criteria are aligned in a certain way. The orientations that might be required are shown below.

You can set as many conditions as necessary on a design rule. However, the conditions of *all* of the conditions must be met before the specified spacing of the design rule will be replaced by those of the condition.

For example, you can set a separation rule of 0.5 microns between two devices. Then, you can set an edge to edge configuration condition and a diagonal orientation condition on that separation rule and set the altered spacing at 0.3 microns. The altered spacing (0.3 microns) will only be applied to the two devices if both the edge to edge configuration *and* the diagonal orientation conditions are met. If only one condition is met, then the original spacing (0.5 microns) will be applied.



To add a simple design rule condition

To add a simple design rule condition, do the following:

1. In the Technology Builder dialog box, select the design rule you would like to add a condition to.
2. Click Add/Edit Condition.
   The Design Rule Conditions dialog box appears.
3. Click Add.
   A pop-up menu displaying the conditions available for the selected design rule appears.

4. Click Simple from the pop-up menu.
   The Add Simple Condition dialog box appears.
5. Set the options (refer to Add/Edit Simple Condition Options on page 70).
6. Click OK.
   The Add Simple Condition dialog box closes and the condition is added to the table on the Design Rule Conditions dialog box.
7. Click OK.
   The Design Rule Conditions dialog box closes.

To edit a simple design rule condition

To edit a simple design rule condition, do the following:

1. In the Technology Builder dialog box, select the design rule you would like to edit a condition for.

   Note: Design rules that have a condition are marked with an asterisk (*) in the Cond (condition) table column in the Technology Builder.

2. Click Add/Edit Condition.
   The Design Rule Conditions dialog box appears.
3. Select the condition you would like to edit.
4. Click Modify.
   The Modify Simple Condition dialog box appears.
5. Edit the options (refer to Add/Edit Simple Condition Options on page 70).
6. Click OK.
   The Modify Simple Condition dialog box closes and the changes appear in the table on the Design Rule Conditions dialog box.
7. Click OK.
   The Design Rule Conditions dialog box closes.

Add/Edit Simple Condition Options

Configuration: The configuration required for the modified spacing to be applied.

Orientation: The orientation required for the modified spacing to be applied.

Minimum: The minimum separation interval to be used if the specified configuration and orientation are met.

Maximum: The maximum separation interval to be used if the specified configuration and orientation are met.

Comment: Any comments you would like to add to the condition.

Common Run Condition

A common run condition sets a different separation between two device edges if the edges have a common run greater than or equal to a certain length. Common run conditions can only be applied to separation rules.

For example, the METAL1 to METAL1 separation rule could be set at 0.2 microns (x1). However, a common run condition can be applied to that rule in which a separation of 0.22 microns (x2) is used when two METAL1 edges have a common run greater than 1.0 microns, as shown in the figure above.

This section covers the following topics:

To add a common run design rule condition

To add a common run design rule condition, do the following:

1. In the Technology Builder dialog box, select the separation design rule you would like to apply the condition to.
2. Click Add/Edit Condition.
   The Design Rule Conditions dialog box appears.
3. Click Add.
   A menu displaying the conditions you can apply to the selected design rule appears.
4. Select Common Run.
   The Add Common Run Condition dialog box appears.

5. Set the options (refer to Add/Edit Common Run Condition Options on page 72).
6. Click OK.
   The Add Common Run Condition dialog box closes and the condition is added to the table on the Design Rule Conditions dialog box.
7. To add additional common run conditions for the selected separation rule, repeat steps 3 to 6 until all of the conditions are added.
8. Click OK.
   The Design Rule Conditions dialog box closes.

To edit a common run design rule condition

To edit a common run design rule condition, do the following:

1. In the Technology Builder dialog box, select the separation design rule you would like to edit the condition for.

   Note: Design rules that have a condition are marked with an asterisk (*) in the Cond (condition) column on the Technology Builder dialog box.

2. Click Add/Edit Condition.
   The Design Rule Conditions dialog box appears.
3. Select the common run condition you would like to edit.
4. Click Modify.
   The Modify Common Run Condition dialog box appears.
5. Edit the options (refer to Add/Edit Common Run Condition Options on page 72).
6. Click OK.
   The Modify Common Run Condition dialog box closes and the changes appear in the table on the Design Rule Conditions dialog box.
7. Click OK.
   The Design Rule Conditions dialog box closes.

Add/Edit Common Run Condition Options

Minimum Common Run: The minimum common run length.

Minimum Separation: The minimum separation interval to be used if the specified minimum common run length is met.

Comment: Any comments you would like to add to the condition.

Width Dependent Condition

When applied to a separation rule, a width dependent condition sets a different separation between two device edges if one device is greater than or equal to a given minimum width. A width dependent condition can be applied to a separation rule for devices that exist on the same layer, or on different layers, however, one of the two layers must be identified as the layer the condition depends on.

For example, the METAL1 to METAL1 separation rule could be set at 0.5 microns. However, a width dependent condition can be applied to that rule in which a separation of 0.58 microns is used when the width of one of the METAL1 devices is greater than or equal to the given minimum width.

When applied to an extension rule, if a shape on one layer (A) touches a shape on a second layer (B), a width dependant conditions sets a different extension between the two shape edges if the shape on layer A is greater than or equal to a given minimum width. With extension rules, the width dependant condition is always dependant on the first layer.

For example, a METAL1 to PCONT extension rule could be set at 0.1 microns. However, a width dependant condition can be applied to that rule in which an extension of 0.15 microns is used when the width of the METAL1 device is greater than or equal to the given minimum width.

Width dependent conditions can only be applied to separation or extension design rules.

This section covers the following topics:

To add a width-dependent design rule condition

To add a width-dependant design rule condition, do the following:

1. In the Technology Builder dialog box, select the separation or extension design rule you would like to apply a condition to.
2. Click Add/Edit Condition.
   The Design Rule Conditions dialog box appears.
3. Click Add.
   A menu displaying the conditions you can apply to the selected design rule appears.
4. Select Width Dependent.
   The Add Width Dependent Condition dialog box appears.
5. Set the options (refer to Add/Edit Width Dependent Condition Options on page 75).
6. Click OK.
   The Add Width Dependent Condition dialog box closes and the condition is added to the table on the Design Rule Conditions dialog box.
7. To add additional width dependent conditions for the selected separation or extension rule, repeat steps 3 to 6 until all of the conditions are added.
8. Click OK.
   The Design Rule Conditions dialog box closes.

To edit a width-dependent design rule condition

To edit a width-dependent design rule condition, do the following:

1. In the Technology Builder dialog box, select the design rule you would like to edit a condition for.

   Note: Design rules that have a condition are marked with an asterisk (*) in the Cond (condition) column on the Technology Builder dialog box.

2. Click Add/Edit Condition.
   The Design Rule Conditions dialog box appears.
3. Select the width dependent condition you would like to edit.

4. Click Modify.
   The Modify Width Dependent Condition dialog box appears.
5. Edit the options (refer to Add/Edit Width Dependent Condition Options on page 75).
6. Click OK.
   The Modify Width Dependent Condition dialog box closes and the changes appear in the table on the Design Rule Conditions dialog box.
7. Click OK.
   The Design Rule Conditions dialog box closes.

Add/Edit Width Dependent Condition Options

Minimum Width: The minimum width of the device.

Layer: The layer the condition depends on.

Minimum Separation: The minimum separation interval to be used if the specified minimum width value is met.

Comment: Any comments you would like to add to the condition.

Common Run and Width Dependent Condition

A common run and width dependent condition sets a different separation between two device edges if the edges have a common run greater than or equal to a certain length and one of the devices has a width greater than or equal to a given width. Common run and width dependent conditions can only be applied to separation rules either on the same layer, or on different layers, however, one of the two layers must be identified as the layer the condition depends on.

For example, the METAL1 to METAL1 separation rule could be set at 0.3 microns. However, a common run and width dependent condition can be added to that rule in which a separation of 0.35 microns is used when two METAL1 edges have a common run greater than or equal to 1.0 microns and the width of one of the devices is greater than or equal to the given minimum width.

This section covers the following topics:

- To add a common run and width-dependent design rule condition
- To edit a common run width-dependent design rule condition
- Add/Edit Common Run and Width Dependent Condition Options

To add a common run and width-dependent design rule condition

To add a common run and width-dependent design rule condition, do the following:

1. In the Technology Builder dialog box, select the separation design rule you would like to apply the condition to.
2. Click Add/Edit Condition.
   The Design Rule Conditions dialog box appears.
3. Click Add.
   A menu displaying the conditions you can apply to the selected design rule appears.
4. Select Common Run and Width Dependent.
   The Add Common Run and Width Dependent Condition dialog box appears.
5. Set the options (refer to Add/Edit Common Run and Width Dependent Condition Options on page 77).
6. Click OK.
   The Add Common Run and Width Dependent Condition dialog box closes and the condition is added to the table on the Design Rule Conditions dialog box.
7. To add additional common run and width dependent conditions for the selected separation rule, repeat steps 3 to 6 until all of the conditions are added.
8. Click OK.
   The Design Rule Conditions dialog box closes.

To edit a common run width-dependent design rule condition

To edit a common run width-dependent design rule condition, do the following:

1. In the Technology Builder dialog box, select the separation design rule you would like to edit the condition for.

   Note: Design rules that have a condition are marked with an asterisk (*) in the Cond (condition) column on the Technology Builder dialog box.

2. Click Add/Edit Condition.
   The Design Rule Conditions dialog box appears.
3. Select the common run and width dependent condition you would like to edit.
4. Click Modify.
   The Modify Common Run and Width Dependent Condition dialog box appears.
5. Edit the options (refer to Add/Edit Common Run and Width Dependent Condition Options on page 77)..
6. Click OK.
   The Modify Common Run and Width Dependent Condition dialog box closes and the changes appear in the table on the Design Rule Conditions dialog box.
7. Click OK.
   The Design Rule Conditions dialog box closes.

Add/Edit Common Run and Width Dependent Condition Options

Minimum Common Run: The minimum common run length.

Minimum Width: The minimum width of the device.

Layer: The layer the condition depends on.

Minimum Separation: The minimum separation interval to be used if the specified minimum common run length and minimum width are met.

Comment: Any comments you want to add to the condition.

To delete a design rule condition

To delete a design rule condition, do the following:

1. In the Technology Builder dialog box, select the design rule you would like to remove a condition for.
2. Click Add/Edit Condition.
   The Add Design Rule Conditions dialog box appears.
3. Select the condition(s) you would like to delete.
4. Click Delete.
   A Question dialog box appears to confirm the removal.
5. Click Yes.
   The selected condition(s) are removed.

To verify a technology

To verify a technology, do the following:

- In the Technology Builder dialog box, select File > Verify.
  The Verify Technology dialog box appears, indicating whether or not the verification was successful.

Verification Conditions

The verification process runs a consistency check on the technology, verifying that all the basic requirements for a technology have been met.

Specifically, the verification process checks for the following conditions:

- There is at least one routing layer.
- Each layer has a positive dimension rule.
- Each layer has a separation rule against itself.
- Each pair of layers that has a connectivity rule also has an extension rule.

- Each pair of layers that has an overlap rule also has a separation rule.
- Each representative layer has a connectivity rule with each of its constituents.

If any of the above conditions are not met, an error message explaining the problem is displayed when you try to either verify or save the technology.

To view a technology report

To view a technology report, do the following:

- In the Technology Builder dialog box, select File > Report.
  The Technology Summary dialog box appears.

  Important: You can print the report by clicking Print and entering the correct Printer Command.

  Important: You can save the report by clicking Save and entering a file name and selecting directory in the File Browser dialog box.

To save a technology

To save a technology, do the following:

1. In the Technology Builder dialog box, select File > Save *or* Save As.
   If the technology has not been saved yet or if you select Save As, then the Save Technology dialog box appears. If you select Save, the technology is automatically saved to the same file it was loaded from.
2. Enter the filename for the technology *or* click Browse to open a file browser.
3. Click OK.
   The technology is verified and saved. If the technology does not meet the verification conditions, then an error dialog box appears.

Optimizing Your Technology

When setting up your technology, there are some specific design rules and layers you can set to optimize the quality of your technology with Cadabra. Following is a description of these rules and layers.

This section covers the following topics:

Asymmetrical Extension Rules

When adding asymmetrical extension rules, the corresponding extension rule must have the smaller value. Otherwise, the larger extension may be enforced rather than the smaller one. This is because the compactor automatically enforces the extension rule while the device enforces the asymmetrical rule.

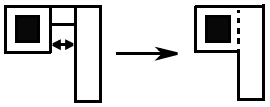
Negative Net Separation Rules

Negative net separation rules should be set between contact layers and their cover layers. A good value to use is the negative of the dimension rule of the contact layer. Using a smaller value can cause DRC errors.

negative net separation rule enforced

Negative Spanned Edge Rules

Negative spanned edge rules should be set for each layer that is used for wire and/or contact cover layers. A good value to use is the negative of the dimension rule of the layer to itself. This would allow edges of the same shape island to fall in on each other, as shown in the figure below.



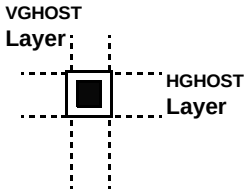
negative spanned edge rule enforced

If only manhattan orientations are possible, then negative spanned edge-to-edge rules are sufficient. If 45 degree wires are also going to be used, then negative spanned edge-to-edge 45 rules are recommended as well.

Rules on Ghost Layers

Separation rules and avoidance rules should be set between any ghost layers and the layers that the ghost layers are meant to block (i.e. keep out of a region of the layout during routing or compaction.

For example, vertical and/or horizontal ghost layers can be used for ports to block any other shape from being placed in the same vertical and/or horizontal channel as the port.



However, for the ghost layers to be effective, they need to have separation rules and avoidance rules with the “real” layers that they are trying to keep out. The values for the separation rules are generally the same as those used by the “real” layers against themselves.

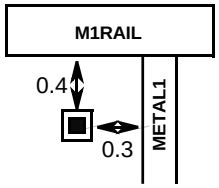
Net separation rules and net avoidance rules may also be necessary depending on the function of the ghost layer. For example, a ghost layer can be used to block a region from METAL2 that is not connected to the device the shape belongs to. In this case, a negative net separation rule and net

avoidance rule should be set in addition to a separation rule and avoidance rule between METAL2GHOST and MaETAL2.

Different Layers

Different layers can be used to support a technology that has different rules for certain situations.

For example, if the separation between METAL1 and CONT is different depending on whether the METAL1 shape is a power rail or wire, you can enforce the different separations by creating another layer for METAL1, such as M1RAIL.



However, METAL1Rail should be set as a representative layer of METAL1, so that the two layers interact as the same layer when they are connected.

As well, all the rules that METAL1 has against itself should also be set for METAL1RAIL using the same values. The METAL1RAIL rules should include:

- a dimension rule,
- separation rules to itself and METAL1,
- spanned edge to edge rules to itself and METAL1 (if METAL1 has any), and
- net separation rules (if METAL1 has any).

Rules for Wells and Implants

When adding rules for the well and implant layers, there are certain conditions that must be met. Following is a description of these conditions:

- A design rulebook often lists only one rule and its complimentary rules are assumed. However, all of the rules must be entered explicitly in Cadabra. For example, if the design rulebook lists a requirement for a 0.5 overlap rule of N-well over P-ACT, you should also set a 0.5 spacing rule between P-well and P-ACT. The same applies to the rules for the implant layers.
- The separation between P-ACT and N-ACT must be large enough to accommodate the space and extension of the well and implant layers.
- If your architecture allows dynamically placed substrate taps, the separation rules between the tap and MOSFET diffusion layers must ensure that you always receive the minimum dimension of the implants. For example, this generally means the space between P-tap and N-tap is calculated as:

extension P-implant over P-tap + dimension of N-implant + dimension of P-implant + extension n-implant over n-tap

Setting an Architecture

An architecture in Cadabra is defined as a collection of devices, layout styles, and GDSII importer and exporter options. Cadabra's Architecture Builder allows you to define an architecture through a graphical user interface.

There is no specific method for defining an architecture, however, Synopsys recommends the following workflow:

1. Create an architecture using a technology as the input. The technology is an AL file.

   Refer to To create a new architecture on page 86.

2. Set the cell architecture by adding the architectural elements from the Setup tab. Some architectural elements, such as contacts, can be defined multiple times and must have unique names. As each architectural element is added, the properties of other elements may be affected. Icons will indicated any status change with an element.

   Refer to Setting Cell Architecture on page 88.

3. View and edit architecture details from the Advanced tab. This tab allows for the viewing and editing of the detailed information stored within the Architecture *.al file. This step is optional and is for advanced users.

   Refer to Architecture Details on page 125.

4. Integrate custom AL files for devices, design steps, callbacks, and exporters.

   Refer to To integrate custom AL files on page 130.

5. Manage design steps and callbacks.

   Refer to To manage design steps, callbacks, and exporters on page 131.

6. Set the layout options for the Migrate GDS, Automated Transistor Layout (ATL) or Migrate-ATL processes.

   Refer to Setting Layout Options on page 133.

7. Set the text annotation options for the layout.

   Refer to To set text annotation on page 153.

8. Identify the path layers for the layout.

   Refer to To set path layers on page 155.

9. Select the measurement metrics to be used when the Automated Transistor Layout (ATL), Migrate-ATL, or Measure processes are run.

   Refer to To set measurement metrics on page 155.

10. Set the import options for the GDSII Importer layer mapping if you are using the Migrate GDS or Migrate-ATL processes.

    Refer to To set the importer on page 157.

11. Set the export options for the Exporter. If you are using your own exporter, add it to the architecture by customizing the file in AL.

    Refer to To set the exporter on page 158.

12. Save the architecture. The architecture is compiled and saved in a .pspec file.

    Refer to To save an architecture on page 162.

This section covers the following topics:

Architecture Exploration

While defining your architecture, you can explore different alternatives by working with varying technologies and architectures. You must first add Path

Sets with differing setups to memory and then you can alternate between these by setting the active path in the Architecture Builder to explore the possibilities.

Editing the Technology

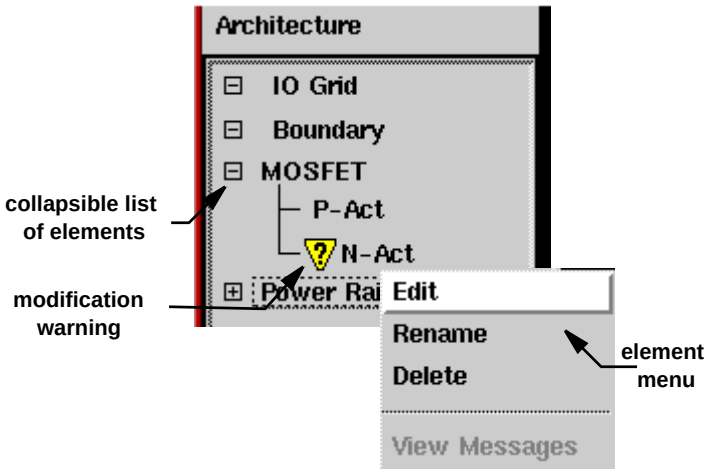
At any point during the set up of your architecture, you can go back and edit your technology. The technology can be opened from the Architecture Builder by selecting Edit > Basic Technology Rules.

Saving changes in the technology to the architecture may affect some of the existing elements. If this occurs, a warning icon will appear beside the affected elements. You must view the element message and from the message determine the appropriate course of action.

Using the Architecture Builder

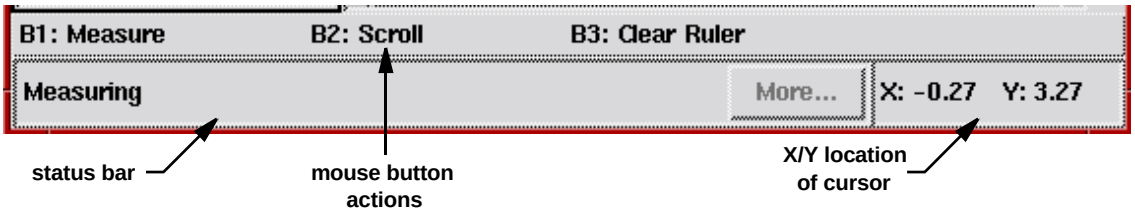
The Architecture Builder allows you to define your architecture through a graphical user interface.

As elements are added to build the cell architecture, a list of the added architectural elements appears to the left of the window in the Setup tab. You can click on the architectural element names to bring up the architectural element menu, which allows you to edit, rename, delete, or view the messages of an architectural element when its status has changed. A change in architecture status is indicated by a conflict or modification warning icon.



At the same time, a graphical representation of the architectural elements appears on the canvas. You can then zoom or measure the architectural elements on the canvas using the toolbar or Preferences and View menus.

Detailed information stored within the Architecture *.al file is displayed in the Advanced tab. From this tab you can view, edit, and customize architecture items such as properties, devices, callbacks, design steps, exporters, and properties and functions stored within the defaults database.



The bottom of the Architecture Builder window displays status information and mouse button actions for the current cursor.

To create a new architecture

To create a new architecture, do the following:

1. In the Cadabra window, select Tools > Architecture Builder.

   Result: The Architecture Builder window appears.

2. Select File > New.

   Result: The Enter a Technology dialog box appears.

3. Do one of the following:

- Enter the filename of a technology.
- Click Browse to open a file browser, and select a file.

4. Click OK.

   Result: The Enter a Technology dialog box closes and the new architecture is created.

   Explanation: You can open a new Architecture Builder window to simultaneously work on another architecture by selecting File > Open New Window.

To open an architecture

To open an architecture, do the following:

1. In the Cadabra window, select Tools > Architecture Builder.
   The Architecture Builder window appears.
2. Select File > Open.
   The Architecture Builder dialog box appears.
3. Enter the filename of an architecture *or* click Browse to open the file browser.

   Note: You can only open compiled.pspec files in the Architecture Builder.

4. Click OK.
   The Architecture Builder dialog box closes and the specified architecture appears in the Architecture Builder window.

   Important: You can open a new Architecture Builder window to simultaneously work on another architecture by selecting File > Open New Window.

To rename an architecture

To rename an architecture, do the following:

1. In the Architecture Builder window, select File > Rename Architecture.
   The Architecture dialog box appears.

2. Enter the new name for the architecture in Name.

   Caution: The following characters cannot be used in the architecture name:
   {} [] `' `` " @ $; : \

3. Click OK.
   The Architecture dialog box closes and the name is updated.

   Caution: Only the title of the architecture is renamed. If you would like to rename the file, save the architecture file under the new name.

To set the active path for the architecture

Setting the active path in the Architecture Builder allows you to switch between Path Sets with differing technology and architecture files. This allows you to explore different architectures. Path Sets consist of a project and working directory. You must first have different Path Sets defined in your alrc file for this option to be available.

To set the active path for the architecture, do the following:

- In the Architecture Builder window, select File > Set Active Path and the Path Set you would like to work with.

  Note: Once an active path has been set, any File Browser opened from the Architecture Builder will display the correct directory. For example, if you are opening an architecture, the File Browser displays the Setup directory from the active path.

Setting Cell Architecture

The cell architecture can be set up through the Architecture Builder, which supports any element in Cadabra's Generic Portfolio.

Once the IO grid and boundary are added, the minimum number of required elements are automatically added to the architecture. They are displayed in the elements list in the Setup tab. You can accept each of the elements manually, by viewing its properties and selecting OK. You can also edit the properties and

add additional elements. Architectural elements that are automatically generated and require manual acceptance are marked with a  icon.

The various architectural elements are as follows:

- **IO Grid:** The IO grid is used by Cadabra to place the ports during cell layout and by the boundary to determine its dimensions (in multiples of the IO grid pitch).

  Refer to To add the IO grid on page 91

- **Boundary:** The boundary enforces bounding dimensions on the cell layout. The dimensions are calculated based on integer multiples of the IO grid pitch and can maintain a fixed height or be flexible. Typically, the boundary is defined with a fixed height, but a variable width.

  Refer to To add the boundary on page 92

- **N-Well:** N-wells are used in a cell layout to create an opposing substrate. For example, a process on P-type substrate requires an N-type well to create complementary MOSFETs. The assumption is that the P-type substrate is used.

  Refer to To add the N-well on page 93

- **Power Rails:** Power rails are used to pass a signal over the width of the cell. Rails are usually created for a VDD and VSS net, but can also be created for other signals such as a clock or reset signal. Power rails correspond with the boundary. Any changes in the boundary dimensions directly affect the parameters of the power rails.

  Refer to To add a power rail on page 96

- **MOSFETs:** MOSFETs are used to actualize the devices and circuitry in the cell netlist. MOSFETs are comprised of two diffusion regions on the same layer and one gate region on another layer. Depending on the process rule, it may be necessary to create the endcaps on a separate layer.

  Refer to To add a MOSFET on page 98

- **Wires:** Wires are used to support specific behaviors when connecting layout geometries on the same layer for power wires and wires connected to IO ports of a cell on a routable layer.

  Refer to To add a wire on page 102

- **Contacts:** Contacts allow one layer to connect to another through a contact layer.

  Refer to To add a contact on page 104

- **Ports:** Ports allow one layer to connect to another layer through a contact layer. They also allow nets to connect to wires or input/output signals passing over the cell. Unlike contacts, ports do not make connections, however, they may reserve space for contacts.

  Refer to To add a port on page 106
- **Diodes:** Diodes are used to create junctions between P-type and N-type diffusions.

  Refer to To add a diode on page 108
- **Reserved Tracks:** Reserved tracks define areas in which specified layers cannot exist.

  Refer to To add a reserved track on page 109
- **Well/Substrate Ties:** Ties are used to connect to the substrate or well in order to properly bias the MOSFET bulk and reduce the chance of latch-up. Ties can be placed as horizontal rails of contacts or can be generated to fill in the gaps after a cell layout has been compacted.

  Refer to To add a well/substrate tie on page 111
- **Implants:** Implants determine which types of impurities must be inserted into diffusion sections, thereby, adjusting the threshold voltage of a MOSFET.

  Refer to To add implants on page 121

Note: As you add architectural elements, icons may appear beside existing elements to indicate a status change due to the new element. If this occurs, you must view the element message and from the message determine the appropriate course of action.

IO Grid

This section covers the following topics:

To add the IO grid

To add the IO grid, do the following:

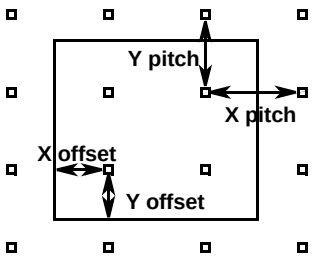
1. In the Architecture Builder window, select Add > IO Grid from the Setup tab. The Property Editor dialog box appears.
2. Click OK to accept the options as they appear in the dialog box, or edit the options (refer to IO Grid Options on page 91).
3. Click OK.
   The Property Editor dialog box closes. The IO grid appears on the canvas and its name appears in the elements list.

   Caution: You cannot delete the IO grid once it has been added.

IO Grid Options

This section covers the following topics:

Pitch



X Grid Pitch: The distance between two IO grid points in the x-direction.

Y Grid Pitch: The distance between two IO grid points in the y-direction.

Reference Layer: The reference layer used in the calculation of the grid pitch.

Calculation Method: Select one of:

Via-Via: Cadabra takes into account the reference layer and technology rules and calculates the grid pitch based on two adjacent grid points with a via on each.

Via-line: Cadabra takes into account the reference layer and technology rules and calculates the grid pitch based on two adjacent grid points, one with a via and the other with a minimum sized wire.

Offset

X Boundary Offset: The distance the boundary is offset from the IO grid in the x-direction. The offset value must be on the manufacturing grid.

Y Boundary Offset: The distance the boundary is offset from the IO grid in the y-direction. The offset value must be on the manufacturing grid.

Calculation Method: Select one of:

Half pitch: The boundary offset is set to half the grid pitch.

None: The boundary offset is set to 0.

Note: You can click Calculate to have Cadabra determine the default value for some of the options. All calculated values are displayed in black. Any values modified or input by a user are displayed in blue.

Boundary

This section covers the following topics:

To add the boundary

To add the boundary, do the following:

1. In the Architecture Builder window, select Add > Boundary from the Setup tab.
   The Property Editor dialog box appears.
2. Click OK to accept the options as they appear in the dialog box, or edit the options (refer to Boundary Options on page 93).
3. Click OK.
   The Property Editor dialog box closes. The boundary appears on the canvas and its name appears in the elements list.

Once the boundary is added, the minimum number of required elements are automatically added to the architecture. If the information for a required element cannot be automatically derived, it will be added when the information becomes available.

Caution: You cannot delete the boundary once it has been added.

Boundary Options

Layer: The layer the boundary shape is drawn on.

Cell Height in Grids: The height of the boundary in integer multiples of vertical IO grid points.

Bottom Left X Coordinate: The amount the bottom left corner of the boundary is horizontally shifted from the origin (0,0).

Bottom Left Y Coordinate: The amount the bottom left corner of the boundary is vertically shifted from the origin (0,0).

Floating height cell: The boundary is not restricted to a specific height. The set height is used only as a starting point before compaction. A floating height cell allows you to have variable height cells within a library.

N-Well

This section covers the following topics:

To add the N-well

The N-well element may be automatically added to the architecture if the appropriate settings are derived. To accept this element:

1. In the Architecture Builder window, select N-Well from the elements list in the Setup tab.
   The Property Editor dialog box appears.

2. Click OK to accept the options as they appear in the dialog box, or edit the options (refer to N-Well Options on page 94).
3. Click OK.
   The Property Editor dialog box closes. The  icon is removed from the N-well element in the list.

   Once the N-well is added, it is not possible to add an additional N-well.

   If the N-well element is not automatically added to the elements list, it can be added manually. To manually add a N-well to the architecture:
4. In the Architecture Builder window, select Add > N-Well from the Setup tab. The Property Editor dialog box appears.
5. Set the options (refer to N-Well Options on page 94).
6. Click OK.
   The Property Editor dialog box closes. The N-well appears on the canvas and its name appears in the elements list.

N-Well Options

Layer: The layer which represents the N-well region.

Complementary Layer: The layer which represents the substrate region.

Draw complementary layer: The complementary layer is drawn in the final layout.

Well Bottom: The bottom position of the N-well region in the cell layout, which is also the top position of the complementary region. If well jogs are used, the well bottom value is fixed at the side edges but is flexible within the cell.

Top Overhang: The amount the N-well region extends past the top of the boundary.

Bottom Overhang: The amount the complementary region extends past the bottom of the boundary.

Side Overhang: The amount the N-well and complementary regions extend past the sides of the boundary.

Allow well jogs: The bottom of the N-well is flexible depending on the position and size of its MOSFETs.

Note: You can click Calculate to have Cadabra determine the default value for some of the options. All calculated values are displayed in black. Any values modified or input by a user are displayed in blue.

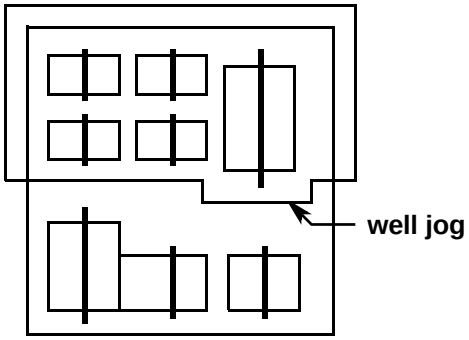
Allow well jogs

The bottom of the N-well is flexible depending on the position and size of its MOSFETs. The well edges remain fixed (relative to the boundary).

Why set this option?

For the more advanced layouts which have complex MOSFET placements or large MOSFETs that do not contain enough gate bends, well jogs allow you to fit transistors without folding them.

For example, as shown in the figure below, if a cell has a large P-MOSFET, a well jog can be used to fit the MOSFET within the N-well region.



Power Rail

This section covers the following topics:

- To add a power rail
- Power Rail Options

To add a power rail

Two power rail elements, one VDD and one VSS, are automatically added to the architecture if the appropriate settings can be derived. To accept these elements:

1. In the Architecture Builder window, select a Power Rail from the elements list in the Setup tab.
   The Property Editor dialog box appears.
2. Click OK to accept the options as they appear in the dialog box, or edit the options (refer to Power Rail Options on page 97).
3. Click OK.
   The Property Editor dialog box closes. The N icon is removed from the power rail element in the list.
4. Repeat these steps to accept the second power rail.

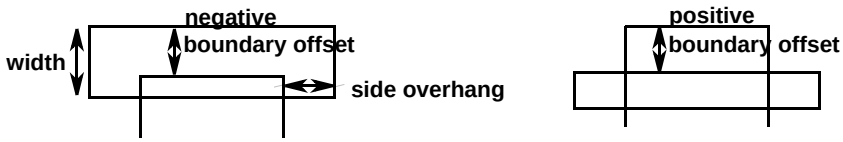
   If the power rails are not added automatically, or if additional rails are required, they can be added manually. To manually add a power rail to the architecture:

5. In the Architecture Builder window, select Add > Power Rail from the Setup tab.
   The Element Name dialog box appears.
6. Enter a name for the power rail.

   Caution: The following characters cannot be used in the name:
   {}[] `' `` " @ $; : \

7. Click OK.
   The Element Name dialog box closes and the Property Editor dialog box appears.
8. Set the options (refer to Power Rail Options on page 97).
9. Click OK.
   The Property Editor dialog box closes. The power rail appears on the canvas and its name appears in the elements list.

Power Rail Options



Layer: The layer the power rail is on.

Net: The net connected to the power rail.

Width: The width of the power rail.

Offset: The amount the power rail is vertically shifted from the boundary edge. A positive value indicates a shift to the outside of the cell while a negative value indicates a shift to the inside of the cell (e.g. inset rails).

Overhang: The amount the power rail extends past the sides of the cell.

Reference Position: The placement of the power rail on the cell. Rails connected to VDD nets are usually placed at the top while rails connected to VSS nets are usually placed at the bottom.

Note: You can click Calculate to have Cadabra determine the default value for some of the options. All calculated values are displayed in black. Any values modified or input by a user are displayed in blue.

MOSFET

This section covers the following topics:

To add a MOSFET

P and N MOSFET elements are automatically added to the architecture if the appropriate settings can be derived. To accept these elements:

1. In the Architecture Builder window, select one of the MOSFETs from the elements list in the Setup tab.
   The Property Editor dialog box appears.
2. Click OK to accept the options as they appear in the dialog box, or edit the options (refer to MOSFET Options on page 98).
3. Click OK.
   The Property Editor dialog box closes. The N icon is removed from the MOSFET element in the list.
4. Repeat for the second MOSFET element.

   If the MOSFETs are not added automatically, or if additional MOSFETs are required, they can be added manually. To manually add a MOSFET element to the architecture:
5. In the Architecture Builder window, select Add > Mosfet from the Setup tab.
   The Element Name dialog box appears.
6. Enter a name for the MOSFET.

   Caution: The following characters cannot be used in the name:
   {} [] `' `` " @ $; : \
7. Click OK.
   The Element Name dialog box closes and the Property Editor dialog box appears.
8. Set the options (refer to MOSFET Options on page 98).
9. Click OK.
   The Property Editor dialog box closes. The MOSFET appears on the canvas and its name appears in the elements list.

MOSFET Options

This section covers the following topics:

- General tab
- Gate Characteristics tab
- Gate Extensions tab

General tab

Type: The type of MOSFET element.

Model Name(s): The device model names in the cell netlist(s). A single MOSFET can be mapped to multiple MOSFET models, but a single model can only be mapped to one MOSFET.

Layers:

Source/Drain Layer: The source/drain layer of the MOSFET.

Gate Layer: The gate layer of the MOSFET.

Endcap Layer: The layer of the extension beyond the MOSFET's active region.

Width:

Maximum Width: The maximum channel width of a single MOSFET in the final layout, despite any bends.

Minimum Width: The minimum channel width of a single MOSFET in the final layout.

Width Tolerance Control:

Tolerance: The amount by which MOSFETs can vary their width. The tolerance can be an absolute or percentage value. Indicate percentages with a percent (%) sign.

Input: The policy on how MOSFETs on how input nets will react to a width tolerance. They can shrink to the minimum, grow to the maximum, or converge to the netlist channel width.

Internal: The policy on how MOSFETs on how internal nets will react to a width tolerance. They can shrink to the minimum, grow to the maximum, or converge to the netlist channel width.

Output: The policy on how MOSFETs on how output nets will react to a width tolerance. They can shrink to the minimum, grow to the maximum, or converge to the netlist channel width.

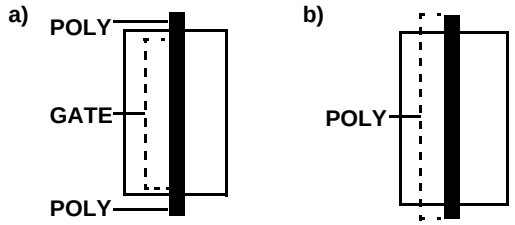
Endcap Layer

The layer of the extension beyond the MOSFET's active region.

Why set this option?

There may be particular spacing rules against the channel region of the MOSFET that do not apply to the endcap region. In this case, a different layer than the default gate layer, should be set for the endcaps.

Typically, the endcap layer is set to POLY and the gate layer is set to GATE, as shown in figure a) below. This is because the channel region of the MOSFET, which is represented by GATE, tends to have special rule constraints. However, if there are no particular spacing rules against the channel, then both the endcap and gate layers are set to POLY, as shown in figure b).



Gate Characteristics tab

Allow gate bends: The MOSFETs can have gate bends.

Require balanced gate bend edges: Balanced gate bends are used. For more information on the background device used, refer to Gate Bend Balancer.

Default bend angle: The angle of the gate bends.

Max Number of Bends: The maximum number of gate bends the MOSFET can have.

Bend Length: The distance between the source diffusion and the drain diffusion for the diagonal of a bend. The default is the gate length.

Min Bend Edge Length: The minimum distance of the bend.

Max Bend Edge Length: The maximum distance of the bend.

Bend Separation: The distance between two gate bends.

Enforce extra separation when diffusion contains contacts: Extra space is enforced between MOSFET gates when there are contacts in the diffusion region between them. The extra space eases the signal flows.

Layer: The layer on which to enforce extra space. This option is only available if *Enforce extra separation when diffusion contains contacts* is selected.

Gate Extensions tab

Layer: The gate extension layer. Extra shapes at the ends of the MOSFETs are added to this layer.

Perpendicular extensions: Perpendicular gate extensions are used.

Width: The distance between the two ends of the perpendicular gate extensions.

Length: The distance between the two sides of the perpendicular gate extensions.

Aligned extensions: Aligned gate extensions are used.

Width: The distance between the two ends of the aligned gate extensions.

Length: The distance between the two sides of the aligned gate extensions.

Note: You can click Calculate to have Cadabra determine the default value for some of the options. All calculated values are displayed in black. Any values modified or input by a user are displayed in blue.

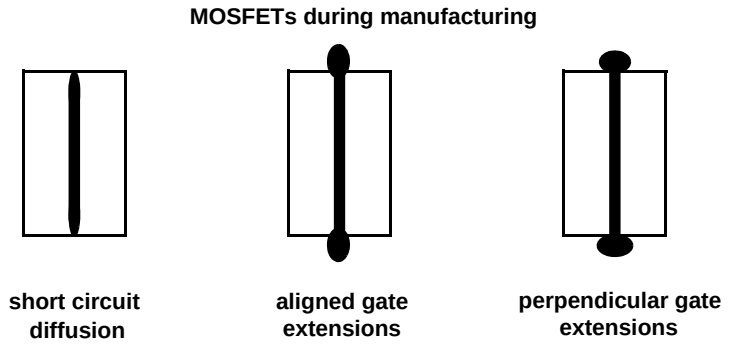
Perpendicular and Aligned Gate Extensions

The gate ends can extend over the diffusion region.

Why set this option?

Unless the MOSFET gates are connected, they may not extend far enough over the transistor when the cell is manufactured. This could result in a short circuit.

Extensions ensure that the gates that are not connected extend past the transistor.



Wire

This section covers the following topics:

To add a wire

Wire elements are automatically added to the architecture if the appropriate settings can be derived. There should be at least:

- a wire for each MOSFET diffusion layer,
- a wire for each POLY layer, and
- a wire for the base METAL layer.

To accept these elements:

1. In the Architecture Builder window, select one of the Wires from the elements list in the Setup tab.
   The Property Editor dialog box appears, set to the Default tab.
2. To accept the options as they appear in the dialog box, proceed to step 5 or edit the options (refer to Wire Options on page 103).
3. Click Advanced if you want to set alternate values for Internal, Port and Power wires.
   The Internal, Port, and Power tabs appear on the Property Editor dialog box.
4. Set the options on each of the tabs (refer to Wire Options on page 103).

   Note: Any values specified in the Default tab override the settings in the Internal, Port, and Power tabs.

5. Click OK.
   The Property Editor dialog box closes. The  icon is removed from the wire element in the list.
6. Repeat until you have accepted all of the wire elements.

   If all of the necessary wires are not added automatically, or if additional wires are required, they can be added manually. To manually add a wire to the architecture:

7. In the Architecture Builder window, select Add > Wire from the Setup tab. The Element Name dialog box appears.
8. Enter a name for the wire.

   Caution: The following characters cannot be used in the name: {}[] `' `` " @ $; : \
9. Click OK.
   The Element Name dialog box closes and the Property Editor dialog box appears, set to the Default tab.
10. Click Advanced if you want to set alternate values for Internal, Port and Power wires.
    The Internal, Port, and Power tabs appear on the Property Editor dialog box.
11. Set the options on each of the tabs (refer to Wire Options on page 103).

    Note: Any values specified in the Default tab override the settings in the Internal, Port, and Power tabs.
12. Click OK.
    The Property Editor dialog box closes. The wire appears on the canvas and its name appears in the elements list.

Wire Options

The following options can be set on the Default, Internal, Port, and Power tabs.

Layer: The layer the wire is on.

Snap Horizontal: The wire is snapped in the horizontal direction.

Snap Vertical: The wire is snapped in the vertical direction.

Width:

Min: The minimum width of the wire.

Preferred Min: The preferred minimum width of the wire.

Max: The maximum width for the wire.

Note: You can click Calculate to have Cadabra determine the default value for some of the options. All calculated values are displayed in black. Any values modified or input by a user are displayed in blue.

Contact

This section covers the following topics:

To add a contact

Contact elements are automatically added to the architecture if the appropriate settings can be derived. There should be at least three contacts:

- one for the P-MOSFET diffusion,
- one for the N-MOSFET diffusion, and
- one for the POLY diffusion.

To accept these elements:

1. In the Architecture Builder window, select one of the Contacts from the elements list in the Setup tab.
   The Property Editor dialog box appears, set to the Default tab.
2. Proceed to step 5 to accept the options as they appear in the dialog box, or edit the options (refer to Contact Options on page 105).
3. Click Advanced if you want to set alternate values for Internal, Port and Power contacts.
   The Internal, Port, and Power tabs appear on the Property Editor dialog box.

   Note: Any values specified in the Default tab override the settings in the Internal, Port, and Power tabs.

4. Set the options on each of the tabs (refer to Contact Options on page 105).
5. Click OK.
   The Property Editor dialog box closes. The  icon is removed from the contact element in the list.
6. Repeat until you have accepted all of the contact elements.

   If all of the necessary contacts are not added automatically, or if additional contacts are required, they can be added manually. To manually add a contact to the architecture:

7. In the Architecture Builder window, select Add > Contact from the Setup tab. The Element Name dialog box appears.
8. Enter a name for the contact.

   Caution: The following characters cannot be used in the name: {}[] `' `` " @ $; : \
9. Click OK.
   The Element Name dialog box closes and the Property Editor dialog box appears, set to the Default tab.
10. Set the options (refer to Contact Options on page 105).
11. Click Advanced if you want to set alternate values for Internal, Port and Power contacts.
    The Internal, Port, and Power tabs appear on the Property Editor dialog box.

    Note: Any values specified in the Default tab override the settings in the Internal, Port, and Power tabs.
12. Set the options on each of the tabs (refer to Contact Options on page 105).
13. Click OK.
    The Property Editor dialog box closes. The contact appears on the canvas and its name appears in the elements list.

Contact Options

The following options can be set on the Default, Internal, Power, and Port tabs.

- *Layers:* The layers for the contact in the order: cover1 layer, contact layer, cover2 layer.
- *Snap Horizontal:* The contact is snapped in the horizontal direction.
- *Snap Vertical:* The contact is snapped in the vertical direction.
- *Min:* The minimum number of contact cuts.
- *Max:* The maximum number of contact cuts.
- *Minimum Space Between Cuts:* The contact cuts in the final layout are spaced at the minimum space or have the flexibility to be spaced at larger interval.
- *Grow Contact Objective:* The objectives used by the compactor dealing with contact growth.

- *Grow Contact Objective Stage 1:* The objectives used by the compactor dealing with contact growth during stage 1.
- *Grow Contact Objective Stage 2:* The objectives used by the compactor dealing with contact growth during stage 2.
- *Growth Direction:* The policy and direction for contact growth.
- *Cover Orientation:* The growth direction of the cover layer(s). Available options are:
  - Vertical
  - Horizontal
  - No preference

  Once you select the Layers, their names appear above the Cover Orientation options.

Port

This section covers the following topics:

To add a port

The port element is automatically added to the architecture if the appropriate settings can be derived. There should be at least one port for the base METAL layer. To accept this element:

1. In the Architecture Builder window, select Port from the elements list in the Setup tab.
   The Property Editor dialog box appears, set to the Default tab.
2. Proceed to step 5 to accept the options as they appear in the dialog box, or edit the options (refer to Port Options on page 107).
3. Click Advanced if you want to set alternate values for Input and Output ports.
   The Input and Output tabs appear on the Property Editor dialog box.
4. Set the options on each of the tabs (refer to Port Options on page 107).

Note: Any values specified in the Default tab override the settings in the Input and Output tabs.

5. Click OK.
   The Property Editor dialog box closes. The N icon is removed from the port element in the list.
6. Repeat until you have accepted all of the port elements.

   If the port is not added automatically, or if additional ports are required, they can be added manually. To manually add a port to the architecture:
7. In the Architecture Builder window, select Add > Port from the Setup tab. The Element Name dialog box appears.
8. Enter a name for the port.

   Caution: The following characters cannot be used in the name: {}[] `' `` " @ $; : \
9. Click OK.
   The Element Name dialog box closes and the Property Editor dialog box appears, set to the Default tab.
10. Set the options (refer to Port Options on page 107).
11. Click Advanced if you want to set alternate values for Input and Output ports. The Input and Output tabs appear on the Property Editor dialog box.
12. Set the options on each of the tabs (refer to Port Options on page 107).

    Note: Any values specified in the Default tab override the settings in the Input and Output tabs.
13. Click OK.
    The Property Editor dialog box closes. The port appears on the canvas and its name appears in the elements list.

Port Options

Layers: The layers for the port. The port can be on a single layer, or on a set of layers in the order: cover1 layer, contact layer, cover2 layer.

Marker Layer: A colored layer used to identify the ports.

Keep in layout: The selected layers are drawn in the final layout.

The following options can be set on the Default, Input, and Output tabs.

- *Cover Orientation:* The growth direction of the cover layer(s). Available options are:
  - Vertical
  - Horizontal
  - No Preference

  Once you select the Layers, their names appear above the Cover Orientation options.

  From the fields below the layer names, you can specify whether the cover orientation option is a preferred or a required value by selecting the appropriate item.
- *Hitpoint Expansion:* The minimum and maximum number of IO pin hitpoints.
- *Expand Ports:* The direction in which the ports are expanded.
- *Grow Port Objective:* The objective used by the compactor dealing with port growth.
- *Unique Grid Location:* The direction in which no other port can be placed on the grid that the port is placed on.

Diode

This section covers the following topics:

To add a diode

To add a diode, do the following:

1. In the Architecture Builder window, select Add > Diode from the Setup tab. The Property Editor dialog box appears.
2. Set the options (refer to Diode Options on page 109).

3. Click OK.
   The Property Editor dialog box closes. The diode(s) appear on the canvas and its name appears in the elements list.

Diode Options

The following options are set for both P- and N-Diodes.

Layers: The layers for the diode.

Marker Layer: A colored layer used to identify the diode.

Region: The region of a cell in which diodes can be placed.

Min Y: The minimum value for the region in the Y direction.

Max Y: The maximum value for the region in the Y direction.

Usage Priority: The degree of preference of one diode type over another.

Note: You can click Calculate to have Cadabra determine the default value for some of the options. All calculated values are displayed in black. Any values modified or input by a user are displayed in blue.

Reserved Track

This section covers the following topics:

To add a reserved track

To add a reserved track, do the following:

1. In the Architecture Builder window, select Add > Reserved Track from the Setup tab.
   The Property Editor dialog box appears.
2. Set the options (refer to Reserved Track Options on page 110).

3. Click OK.
   The Property Editor dialog box closes. The track appears on the canvas and its name appears in the elements list.

Reserved Track Options

Layer: The layer the track is on.

Keep in final layout: The track layer is drawn in the final layout.

Width: The width of the track.

Overhang: The amount the track extends past the sides of the cell.

Grid location(s): The track is placed and snapped to the IO grid at the specified location(s).

Offset in microns: The track is offset from the bottom of the boundary by the specified distance.

Location: If Grid location(s) is selected, the location(s) at which to place the track. Specifying multiple locations creates multiple reserved tracks. If Offset in microns is selected, the distance by which to offset the track from the bottom of the boundary. Only one location can be specified.

Note: You can click Calculate to have Cadabra determine the default value for some of the options. All calculated values are displayed in black. Any values modified or input by a user are displayed in blue.

Well and Substrate Tie

This section covers the following topics:

To add a well/substrate tie

To add a well/substrate tie, do the following:

1. In the Architecture Builder window, select Add > Well/Substrate Tie from the Setup tab.
   The Element Name dialog box appears.
2. Enter a name for the well/substrate tie.

   Caution: The following characters cannot be used in the name: {}[] `' `` " @ $; : \
3. Click OK.
   The Element Name dialog box closes and the Property Editor dialog box appears.
4. Select the General tab.
5. Select a Tie Layer.
6. Select a Metal Layer.
7. Select the Bulk type.

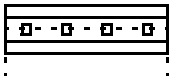
   Note: If “well” is selected, the tie is placed on the VDD net; and if “substrate” is selected, the tie is placed on the VSS net.
8. Select a Strategy from the options displayed.

   Note: Depending on the Tie Strategy you select, certain design rules must be set between the Active and Tie layers. Refer to Required Rules for Tie Strategies on page 115.
9. Select the Configure tab.
10. Set the options (refer to Tie Strategy Options on page 112).
11. Click OK.
    The tie strategy Property Editor dialog box closes.
12. Click OK.
    The Property Editor dialog box closes. The tie appears on the canvas and its name appears in the elements list.

Tie Strategy Options

Depending on the Tie Strategy and Abutment options you select, certain design rules must be set between the Active and Tie layers. Refer to Required Rules for Tie Strategies on page 115.

.



Fully Strapped Tie Rail

Width: The width of the tie.

Offset: The amount the tie is vertically shifted from the boundary edge. A positive value indicates a shift to the inside of the cell while a negative value indicates a shift to the outside of the cell.

Overhang: The amount the tie extends past the sides of the cell. If contacts can be placed on edge of the boundary, this value is usually half the tie width. If they cannot, this value is usually 0.

Match with the Metal overhangs: The metal overhangs are adjusted to at least line up with the tie overhang.

Abutment:

With contact: The tie rail can touch MOSFET diffusion using a contact.

With no contact: The tie rail can touch MOSFET diffusion without using a contact.

With and without contact: The tie rail can touch MOSFET diffusion two ways: using a contact and using no contact.

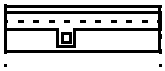
No Abutment: The tie rail cannot touch MOSFET diffusion.

Minimum Abutment Dimension: The dimension of the diffusion shape used in the abutment. The default is the minimum dimension of the diffusion layer.

Minimum Abutment Length: The length of the common overlap between the tie and MOSFET diffusion shapes. The default is the minimum dimension of the diffusion layer.

Minimum Abutment Extension: The distance between the rail edge and the contact. The default is the minimum extension of the active layer over the contact for the technology.

Fill available space with ties: The tie layer is added to all the allowable space left in the compacted layout.



Tie Rail with Contact in Rail

Width: The width of the tie.

Offset: The amount the tie is vertically shifted from the boundary edge. A positive value indicates a shift to the inside of the cell while a negative value indicates a shift to the outside of the cell.

Overhang: The amount the tie extends past the sides of the cell. If contacts can be placed on edge of the boundary, this value is usually half the tie width. If they cannot, this value is usually 0.

Abutment:

With contact: The tie rail can touch MOSFET diffusion using a contact.

With no contact: The tie rail can touch MOSFET diffusion without using a contact.

With and without contact: The tie rail can touch MOSFET diffusion two ways: using a contact and using no contact.

No Abutment: The tie rail cannot touch MOSFET diffusion.

Minimum Abutment Dimension: The dimension of the diffusion shape used in the abutment. The default is the minimum dimension of the diffusion layer.

Minimum Abutment Length: The length of the common overlap between the tie and MOSFET diffusion shapes. The default is the minimum dimension of the diffusion layer.

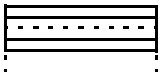
Minimum Abutment Extension: The distance between the abutment edge and the contact. The default is the minimum extension of the active over the contact for the technology.

Number of sides for abutment: The number of consecutive sides of the tie shape that can form an abutment.

Max Spacing: The maximum distance between ties (in microns).

Maximum Boundary Distance: The maximum distance between ties and the boundary edge (in microns). The default is half the maximum spacing.

Fill available space with ties: The tie layer is added to all the allowable space left in the compacted layout.



Width: The width of the tie.

Offset: The amount the tie is vertically shifted from the boundary edge. A positive value indicates a shift to the inside of the cell while a negative value indicates a shift to the outside of the cell.

Overhang: The amount the tie extends past the sides of the cell. If contacts can be placed on edge of the boundary, this value is usually half the tie width. If they cannot, this value is usually 0.

Abutment:

With contact: The tie rail can touch MOSFET diffusion using a contact.

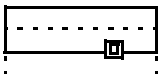
No Abutment: The tie rail cannot touch MOSFET diffusion.

Minimum Abutment Dimension: The dimension of the diffusion shape used in the abutment. The default is the minimum dimension of the diffusion layer.

Minimum Abutment Length: The length of the common overlap between the tie and MOSFET diffusion shapes. The default is the minimum dimension of the diffusion layer.

Minimum Abutment Extension: The distance between the rail edge and the contact. The default is the minimum extension of the active over the contact for the technology.

Fill available space with ties: The tie layer is added to all the allowable space left in the compacted layout.



Abutment (slider): The degree of preference between requiring and disallowing abutments.

Minimum Abutment Dimension: The dimension of the diffusion shape used in the abutment. The default is the minimum dimension of the diffusion layer.

Minimum Abutment Length: The length of the common overlap between the tie and MOSFET diffusion shapes. The default is the minimum dimension of the diffusion layer.

Minimum Abutment Extension: The distance between the rail edge and the contact. The default is the minimum extension of the active over the contact for the technology.

Number of sides for abutment: The number of consecutive sides of the tie shape that can form an abutment.

Tie Placement:

Require ties in all cells: Ties are used in all the cells.

Require ties in cells above grid size: The minimum cell width before ties must be used.

Do not require ties: Ties are used in the cells only if space is available after compaction. When this option is selected, abutments are disallowed and the Fill available space with ties option is locked on.

Max Spacing: The maximum distance between ties (in microns).

Max Distance Boundary: The maximum distance between ties and the boundary edge (in microns). The default is half the maximum spacing.

Fill available space with ties: The tie layer is added to all the allowable space left in the compacted layout.

Note: You can click Calculate to have Cadabra determine the default value for some of the options. All calculated values are displayed in black. Any values modified or input by a user are displayed in blue.

Required Rules for Tie Strategies

Certain design rules should be set between the MOSFET Active and opposing Tie diffusion layers in your technology to accommodate the tie strategy and its abutment option you select for your cell architecture. The following are guidelines to use:

- All tie strategies require a separation rule. The separation value is typically similar to that of Active to Active and Tie to Tie but may be different depending on the specific process rules being used.
- A connectivity rule is required when an abutment is made, which involves a tie rail that spans the cell width.

- An avoidance rule must be provided in all strategies that do not involve an abutment. Alternatively, in those strategies that do involve an abutment, a net avoidance rule should be used instead.
- A spanned edge separation rule must be used when implants are required in a layout. The value for this rule needs only to be as large at the implant extension, not the minimum separation value between the two layers. Typically this rule condition should be set as a “Manhattan” rule condition.
- If there is a net separation rule, it needs to be larger than zero but not larger than the default separation value.

The following table provides the rules that must be set:

Table 1 Required Rules for Tie Strategies

Tie Strategy	Abutment Option	Rules Between Active and Tie
Fully Strapped Tie Rail	With Contact	Connectivity Rule
		Net Avoidance Rule
		Separation Rule
		Vertical Spanned Edge Separation Rule (spanned edge condition on a separation rule - use the same value as the implant extension)
		Net Separation Rule > 0
		Separation Rule > Net Separation Rule
	With No Contact	Connectivity Rule
		Net Avoidance Rule
		Separation Rule
		Vertical Spanned Edge Separation Rule (spanned edge condition on a separation rule - use the same value as the implant extension)
		Net Separation Rule > 0
		Separation Rule > Net Separation Rule
	No Abutment	Avoidance Rule
		Separation Rule
		Net Separation Rule > 0
		Separation Rule > Net Separation Rule

Table 1 Required Rules for Tie Strategies

Tie Strategy	Abutment Option	Rules Between Active and Tie
Tie Rail With Contact In Rail	With Contact	Connectivity Rule
		Net Avoidance Rule
		Separation Rule
		Vertical Spanned Edge Separation Rule
		Horizontal Spanned Edge Separation Rule (spanned edge condition on a separation rule - use the same value as the implant extension)
		Net Separation Rule > 0
		Separation Rule > Net Separation Rule
	With No Contact	Connectivity Rule
		Net Avoidance Rule
		Separation Rule
		Vertical Spanned Edge Separation Rule
		Horizontal Spanned Edge Separation Rule (spanned edge condition on a separation rule - use the same value as the implant extension)
		Net Separation Rule > 0
		Separation Rule > Net Separation Rule
	No Abutment	Avoidance Rule
		Separation Rule
		Net Separation Rule > 0
		Separation Rule > Net Separation Rule

Table 1 Required Rules for Tie Strategies

Tie Strategy	Abutment Option	Rules Between Active and Tie
Tie Rail	With Contact	Connectivity Rule
		Net Avoidance Rule
		Separation Rule
		Vertical Spanned Edge Separation Rule
		Horizontal Spanned Edge Separation Rule (spanned edge condition on a separation rule - use the same value as the implant extension)
		Net Separation Rule > 0
		Separation Rule > Net Separation Rule
	No Abutment	Avoidance Rule
		Separation Rule
		Net Separation Rule > 0
		Separation Rule > Net Separation Rule

Table 1 Required Rules for Tie Strategies

Tie Strategy	Abutment Option	Rules Between Active and Tie
Discrete Tie	With Abutment	Net Avoidance Rule
		Separation Rule
		Net Separation Rule > 0
		Separation Rule > Net Separation Rule
	With Abutment on more than one side	Net Avoidance Rule
		Separation Rule
		Net Separation Rule > 0
		Separation Rule > Net Separation Rule
Discrete Tie (continued)	No Abutment	Avoidance Rule
		Separation Rule
		Net Separation Rule > 0
		Separation Rule > Net Separation Rule

Implants

This section covers the following topics:

- To add implants
- Implant Options

To add implants

To add implants, do the following:

1. In the Architecture Builder window, select Add > Implants from the Setup tab.
   The Property Editor dialog box appears.
2. Set the options (refer to Implant Options on page 121).
3. Click OK.
   The Property Editor dialog box closes. The implants are set and its name appears in the elements list.

Implant Options

This section covers the following topics:

P-Implant and N-Implant tabs

Implant Layer: The layer of the implant.

Avoidance Layers: The layers the implant should cut around.

Enclosing Layers: The layers the implant should enclose.

Filling Area: The distances between the edges of the implant and boundary edge.

MOSFET Implant tab

MOSFET Implants: A table of MOSFET elements and their implant layer and extensions. Only change these values if the implant is to be different than the one surrounding the diffusion region.

Diode Implant tab

Diode Implants: A table of diode elements and their implant layer and extensions. Only change these values if the implant is to be different than the one surrounding the diffusion region.

Note: You can click Calculate to have Cadabra determine the default value for some of the options. All calculated values are displayed in black. Any values modified or input by a user are displayed in blue.

Architecture Status

As you build your architecture, icons may appear beside any of the existing architectural elements in the Architecture Builder window. These icons indicate a status change in the element. The status of an element can be affected by either a change in the cell architecture or the technology that the architecture is based on. If an icon does appear beside an element, you must view the element message and from the message determine the appropriate course of action.

Following are the icons that may appear beside an element.

Note: An new icon appears beside cell elements that were added automatically by the Architecture Builder and need to be verified.

Caution: A modification warning message appears when a change in the element defaults has occurred, generally due to the addition or edit of another element or technology.

To view element messages

Viewing element messages allows you to review the conflict or modification warning for an architectural element. There are four types of messages that can be associated with each element:

- Synchronize Message (Green): The values in the Advanced tab conflict with the settings in the Setup tab. These messages can be resolved using the Resolve button.
- Default Message (Blue): The value of the element property should be set to the default value but does not match. These messages typically refer to numeric values that are associated with Calculate buttons. Resolving these messages changes the value of the element property to the default value.

- Resolvable Message (Black): A potential problem exists with the element settings or technology values. The problem is described in the message along with a recommended solution that the Architecture Builder can implement if you select to resolve the message.
- Warning Message (Orange): A potential problem exists but there is no recommended solution. Problems indicated by a Warning Message must be manually resolved, or you can click Ignore in the View Messages dialog box.

From the message, you can then determine the appropriate course of action. To view an element message:

1. In the Architecture Builder window, click on the architectural element that has an icon beside it.
   The architectural element menu appears.
2. Select View Messages.
   The View Messages dialog box appears.
3. Select the checkbox beside the message and click Resolve to accept the suggested changes or eliminate the conflict, or click Cancel to close the dialog box. For messages that cannot be resolved, you can click Ignore and the Architecture Builder ignores these messages. The text color of messages that are ignored is changed to burgundy and the warning icon beside the element is dimmed if all of the messages are ignored.
   The View Messages dialog box closes.

   Note: If a warning is not fixed while it is in the ignored status, Messages that have been ignored can be re-activated by selecting the ignored message and clicking Activate.

Working with Architectural Elements

This section covers the following topics:

To edit an architectural element

To edit an architectural element, do the following:

1. From the Setup tab in the Architecture Builder window, click on the architectural element you want to edit.
   The architectural element menu appears.
2. Select Edit.
   The Property Editor dialog box appears.
3. Edit the options. Refer to the specific options for the element that you are editing.
4. Click OK.
   The Property Editor dialog box closes and the architectural element properties are updated.

   Note: Editing an architectural element may affect the properties of another
   element. If this occurs, view the element message and edit accordingly.

To rename an architectural element

To rename an architectural element, do the following:

1. From the Setup tab in the Architecture Builder window, click on the architectural element that you want to rename.
   The architectural element menu appears.
2. Select Rename.
   The Element Name dialog box appears.
3. Enter the new name.

   Caution: The following characters cannot be used in the architecture name:
   {} [] `' `` " @ $; : \
4. Click OK.
   The Element Name dialog box closes and the name is updated in the element list.

To delete an architectural element

To delete an architectural element, do the following:

1. From the Setup tab in the Architecture Builder window, click on the architectural element that you want to remove.
   The architectural element menu appears.
2. Select Delete.
   The architectural element is removed from the elements list.

   Caution: You cannot delete the IO grid or boundary once they have been added.

Architecture Details

The Advanced tab displays the details of the architecture settings stored in the architecture *.al file. From this tab you can view and edit the various properties and functions directly in the Architecture Builder GUI without having to open and edit the *.al text file.

Caution: The features available in the Advanced tab are for advanced users only. Changing properties and adding functions can seriously compromise you setup. Changes you make are at your own risk. If you are uncertain about using these features, please contact your Cadabra Application Consultant for assistance.

The Advanced tab displays the details for the following settings:

Properties: The physical specification properties. The values for the displayed properties can be edited and new properties can be added.

Devices: The Device Templates registered in the physical specification. The properties can be added and edited and functions can be added to each of the displayed devices. Custom devices must be added using Add > Custom > Device when the Setup tab is active.

Device Mapping: The mapping of the SPICE netlist devices to the available Cadabra devices. This list cannot be edited or customized.

Callbacks: The Callback Templates registered in the physical specification. The properties can be added and edited and functions can be added to each of the

displayed callbacks. Custom callbacks must be added using Add > Custom > Callback when the Setup tab is active.

Design Steps: The Design Step Templates registered in the physical specification. The properties can be added and edited and functions can be added to each of the displayed design steps. Custom design steps must be added using Add > Custom > Design Step when the Setup tab is active.

Exporters: The Exporter Templates registered in the physical specification. The properties can be added and edited and functions can be added to each of the displayed exporters. Custom exporters must be added using Add > Custom > Exporter when the Setup tab is active.

Note: The way the callbacks and exporters work is that they cannot exist without a "@Classname" in the name. If you rename them and do not provide it will be added back on.

For the callbacks, "@Classname" refers to the type of design step the callback is used for. This means the value can be anything but is usually one of AutoPlacer, LayoutImporter, PlacementOptimizer, VerticalConditioner or SymbolicLayoutMigrator.

For the exporters, "@Classname" refers to what type of design point the exporter is designed to operate on. The choice can only be Layout or SymbolicLayout.

In both cases the type can be changed using the Rename feature or the Edit feature. In the Edit window there is a dropdown list that contains the appropriate choices. In the case of callbacks, if you want to use a design step not listed, you can specify it using the Rename feature.

Defaults: The properties and functions set in the DefaultsDB. The values for these properties and functions are used for ATL, Migrate GDS, Migrate-ATL, Placement, Routing, and Compaction. This section also displays other classes for which default values are typically set, based on the setup for the elements in the Setup tab. Under Defaults you can add new categories, add properties and functions to existing categories, and edit existing properties and functions.

Layout Style Rules: The rules that define how Cadabra uses the available resources when attempting to complete a cell layout. Resources include layers and devices. The rules are enforced under certain conditions that are based on expressions that consist of predefined keywords. Under Layout Style Rules you can add new rules and edit existing rules. Layout Style Rules that are added from the Advanced tab can be removed. Rules that have been added through AL cannot be removed.

This section covers the following topics:

Architecture Details: Properties

The properties for the settings in the Advanced tab are color coded:

- Initial (RED) properties: Indicates properties that have default values from the associated AL file that have not been customized or are not controlled by the Architecture Builder.
- Builder Controlled (BLACK) properties: Indicates properties that are specified in the Setup tab.
- Manually Controlled (BLUE) properties: Indicates properties that are manually controlled by changing the AL values associated with them in the Advanced tab. These can either be properties that are not specified in the Setup tab or property values that have been modified.

The value for a specific property can be changed by right-clicking the value, entering a new value, and then left-clicking anywhere in the Advanced tab to accept the new value. If you enter an invalid value, an error message is given and you must resolve the problem to continue.

If you have changed a property value in the Advanced tab and you want to reset the property to its default value, right-click on the property name and select Use Default. This changes the property value to its default value.

Note: In this instance, the term default does not refer to the actual default value for the property but the value that was set in the Setup tab.

Properties can be added for Physical Specification Properties, Callbacks, Devices, Design Steps, Exporters, and Default settings. To add a new property:

1. Select a callback, property, device, design step, exporter, or default category and select Add Property. For defaults, if the category you require isn't listed, you can add a new category by selecting Default > Add Category and then enter the name of the category.
   The Device (Callback, Design Step, Exporter, Default) Property Name dialog box appears.

2. Enter a name for the property and click OK.
   The Edit Property dialog box appears.
3. Enter a value for the property and click OK.
   The new property is added.

Architecture Details: Functions

Functions are displayed in a similar manner as properties, however, there are some differences. There can be more than one entry of any given function and all customized functions are placed at the bottom of the list in the order that they were added. As with properties, functions that are controlled by the Architecture Builder are displayed in black text. All functions added from the Advanced tab are displayed in blue text. Unlike properties, you cannot reset functions to a default value. Also, Architecture Builder controlled functions cannot be removed. Only those functions that are defined from the Advanced tab can be removed.

Functions can be added for Devices, Callbacks, Design Steps, Exporters, and Default categories. To add a new function:

1. Select an item that allows functions in the Advanced tab and select Add Function > Other.
   The Add New Function dialog box appears.
2. Enter the name of the function in the Arguments for option. The name of the function must be suffixed with “()”. For example, setLayers().
3. Enter up to five arguments in the remaining fields. Text strings must be surrounded by quotes. For example, “layer”.
4. Click OK.
   The function is added to the bottom of the list for the item.

   Note: You can also add additional existing functions by selecting Add Function and then the name of the existing function, if it available. A list of existing functions is provided if they exist for the item that you are adding a function to. You can then change the argument values in the Add New Function dialog box.

Architecture Details: Layout Style Rules

If a Layout Style Rule has been created by the Architecture Builder (from the Setup tab) only the comment, modified properties, dimension, and conditions for that rule can be changed. The name, resource and enforcement type cannot be changed. In the Advanced tab only the changed properties are displayed in blue. The unchanged properties are displayed in black.

If a Layout Style Rule is completely user-defined then any of the properties can be changed. In the display all of the fields are displayed in blue.

This section covers the following topics:

To add a new Layout Style Rule

To add a new Layout Style Rule:

1. In the Advanced tab select Layout Style Rule > Add.
   The Layout Style Rule Name dialog box appears.
2. Enter a name for the rule and click OK.
   The Rule Editor dialog box appears.
3. Set the options (refer to Layout Style Rules Options on page 130).
4. Click OK.
   The Rule Editor dialog box closes and the new rule appears in the Advanced tab under the Layout Style Rules setting.

To edit an existing Layout Style Rule

To edit an existing Layout Style Rule:

1. In the Advanced tab select the rule that you want to edit and select Edit.
   The Rule Editor dialog box appears.
2. Edit the options (refer to Layout Style Rules Options on page 130).
3. Click OK.
   The Rule Editor dialog box closes and the changed properties are displayed in the Advanced tab.

Layout Style Rules Options

Comments: A brief description or information about the rule. Comments are optional.

Enforcement: The rule applies to positive values, negative values, or both.

Resource: The list of devices and layers that can be used to create a rule.

Modified Properties: The properties available on the selected resource device. This option is only available when a device resource is selected. Click Add Property to select the properties to add from the pop-up list. Click Remove Property to remove any added properties.

Dimension: The minimum dimension for the selected resource layer. This option is only available when a layer resource is selected.

Conditions: The conditions on which the Layout Style Rule is based. A rule must have at least one condition. The conditions are based on a set of defined Reserved Keywords. To create a condition, select a keyword, data type and enter a value then click Add. The condition is added to the Conditions list. Use the Remove and Replace buttons to remove and modify existing conditions.

To integrate custom AL files

Custom AL files for devices, design steps, callbacks, and exporters can be integrated into your architecture from the Architecture Builder. A custom AL file is typically provided to you from your Synopsys Application Consultant. To integrate a custom AL file:

1. Create a new architecture or open an existing architecture.
2. From the Add menu, select Custom > Device (Design Step, Callback, or Exporter).
   The Add Custom Device (Design Step, Callback, or Exporter) and File dialog box appears.
3. Enter a name for the custom device (design step, callback, or exporter).
4. Enter the path and filename for the custom AL file or click Browse to open a file browser.
5. Click OK.
   The dialog box appears.
6. Enter the appropriate values for the options that appear in the dialog box.

Note: The options that appear in the dialog are specific to the custom file and they are specified within the file. Each custom file requires you to enter different options.

7. Click OK.
8. Manually resolve or ignore any warning messages that appear.

   Refer to To view element messages on page 122.

To manage design steps, callbacks, and exporters

If a custom design step AL file is added to the architecture, Cadabra must be told when (Post Import, Pre Route, Pre Compaction, Inter Compaction, or Post Compaction) to run the design step, or it is not be used.

If a custom callback AL file is added, it must be associated with a design step (Post AutoPlacer, Pre LayoutImporter, or Post LayoutImporter), otherwise, the it is not run. Both of these tasks can be accomplished using the Manage menu.

If a custom exporter AL file is added, Cadabra must be told to use the custom exporter.

Note: The Manage menu is only available when the Setup tab is active.

The Manage menu can also be used to manage the design steps, callbacks, and exporters that are already registered in the architecture. This allows you to change when a design step is run and edit, or create a new associations between a callback and a design step, or specify the use of specific exporters.

This section covers the following topics:

- To manage design steps:
- To manage callbacks:
- To manage exporters:

To manage design steps:

To manage design steps, do the following:

1. Select Manage > Design Steps > Post Import (Pre Route, Pre Compaction, Inter Compaction or Post Compaction).
   The manage dialog box appears.
2. Use the left and right arrows to move the available callbacks between the Unused and Used columns.
3. Use the up and down arrows to order the design steps in the Used column.
4. Click OK.

To manage callbacks:

To manage callbacks, do the following:

1. Select Manage > Callbacks > Post AutoPlacer (Pre LayoutImporter or Post LayoutImporter).
   The manage dialog box appears.
2. Use the left and right arrows to move the available callbacks between the Unused and Used columns.
3. Use the up and down arrows to order the callbacks in the Used column.
4. Click OK.

To manage exporters:

To manage exports, do the following:

1. Select Manage > Exporters.
   The Export dialog box appears.
2. Use the left and right arrows to move the available exporters between the Unused and Used columns.
3. Select an exporter in the Used column and click Configure Exporter if you have selected a built-in exporter. Configure Exporter is greyed-out if you have selected a custom exporter.
   The exporter specific dialog box appears.
4. Set the options accordingly (refer to Exporter Options on page 159).

5. Click OK.
   The Exporter dialog box closes and the exporter options are set.

Setting Layout Options

The layout options for the Migrate GDS, Automated Transistor Layout (ATL) and Migrate-ATL processes can be set up through the Architecture Builder. These styles are applied to any library created using the architecture.

You can set the layout options for placement, routing, compaction, and electromigration as well as specify the optimization goal. Measurement metrics can be specified for calculation each time the Automated Transistor Layout (ATL), Migrate-ATL, or Measure processes are run. You can also set importer and exporter options, including path layers and text annotations for exported layouts.

To set the optimization goal

The optimization goal drives the default values for the placement and routing layout styles. If the settings for a layout style are not consistent with the priority of the optimization goals, a warning icon will appear in the architecture list.

To set the optimization goal, do the following:

1. In the Architecture Builder window, select Layout Options > Optimization Goal.
   The Optimization Goal dialog box appears.
2. Select a goal and use the up and down arrows to change its priority in the list.
3. Click OK.
   The Optimization Goal dialog box closes and goals are set.

Working with Placement Styles

This section covers the following topics:

- To set placement style
- Placement Style Options

To set placement style

Placement style determines how transistors are placed during layout creation. Set this layout option if you are using the ATL or Migrate-ATL processes.

To set the placement style, do the following:

1. In the Architecture Builder window, select Layout Options > Placement Style.
   The Placement Style dialog box appears.
2. Set the options (refer to Placement Style Options on page 134).
3. Click OK.
   The Placement Style dialog box closes and the placement styles are set.

Placement Style Options

This section covers the following topics:

- General tab
- Vertical Conditioning tab

General tab

The options available in the General tab are explained in the following sections:

Note: Click Advanced to see additional available values for each of these options.

This section covers the following topics:

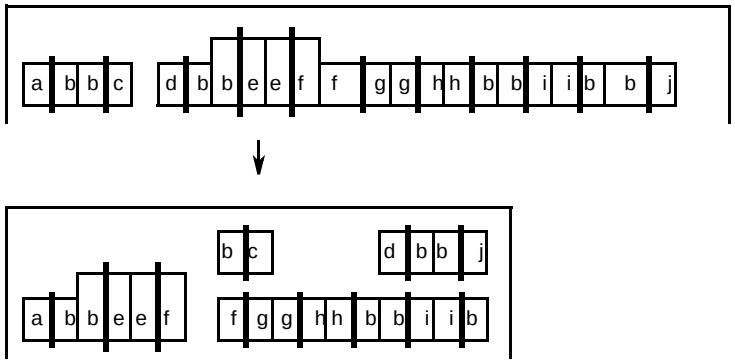
- Stack Transistors
- Modify Folding
- Virtual Shorts Policy

Stack Transistors

Transistors are stacked above or below each other where possible. Only two transistors of the same type can appear on the same x-coordinate and the x-coordinate must align the stacked pairs gates. Your architecture height must allow for stacked transistors or the cell can become infeasible in the vertical direction.

Why set this option?

Stacking transistors can help reduce cell size as shown in the figure below.



The possible values for the Stacked Transistors option are:

- *Not Allowed:* Stacking transistors is not allowed. The corresponding Place macro property `doStacking` is set to 0.
- *Simple:* Stacking is tried, but very conservative with regards to routability estimations. The Place macro properties related to stacking are set to the following values:

```
doStacking = 1
allowStackingOverCrossedGates = 0
aggressiveStacking = 0
```

- *Default:* Stacking is attempted with consideration to routability. More specifically, all three stacking styles are attempted and the `PlacementOptimizer` tries to emphasize routability over width (stacking) criteria. Therefore there will be fewer stacked MOSFETs than in the following two scenarios. The Place macro properties are set to the following values:

```
doStacking = 1
allowStackingOverCrossedGates = "Usual_Way"
aggressiveStacking = 0
```

- *Extra Over Crossed Gates:* This option is more aggressive than the *Default* option. Stacking over crossed gates is tried with little regard for routability. Simply, the tool tries to stack over crossed gates as hard as possible. The corresponding Place macro properties are set to:

```
doStacking = 1
allowStackingOverCrossedGates = 1
aggressiveStacking = 0
```

- *Aggressive:* This is the most aggressive stacking approach. Routability awareness is hardly considered and the `PlacementOptimizer` settings are towards getting as much stacking as possible (they emphasize the final width of the final solution). The corresponding Place macro properties are set to:

```
doStacking = 1
aggressiveStacking = 1
```

Note: When aggressive stacking is selected, the value of the `allowStackingOverCrossedGates` property is ignored and stacking over crossed gates is always tried.

Modify Folding

The settings in this group are related to the folding policy during placement and affect the following Place macro properties: `canRefold` and `foldingPolicy`.

The possible values are outlined below and display the corresponding settings for the Place macro properties:

- *Not Allowed*: Folding is not allowed. The Place macro property canRefold is set to 0.
- *For Minimum Area:* Folding is allowed, however both the `TileFolder` and `MosfetFolder` are used for folding and to set the folding style. The corresponding Place macro properties are set to:

```
canRefold = 1
foldingPolicy = "Default"
```

- *Intersperse Gates:* Folding is allowed, however, only the `TileFolder`is used for folding and sets the folding style. The Place macro produces placements using the *"IntersperseGates"* and *"FoldInPlace"* styles.The corresponding Place macro properties are set to:

```
canRefold = 1
```

```
foldingPolicy = "IntersperseGates"
```

- *Intersperse Gates for Series Only:* Folding is allowed, however, only the `TileFolder`is used for folding and sets the folding style. The Place macro produces placements using the `IntersperseGatesSeriesOnly` and `FoldInPlace` styles. The corresponding Place macro properties are set to:

```
canRefold = 1
foldingPolicy = "IntersperseGatesSeriesOnly"
```

- *Group Folded MOSFETs by Gates:* Folding is allowed, however, only the `TileFolder` is used for folding and sets the folding style. The Place macro produces placements using the `FoldInPlace` style. The corresponding Place macro properties are set to:

```
canRefold = 1
foldingPolicy = "KeepFoldedFingersTogether" or
"FoldInPlace"
```

Virtual Shorts Policy

The policy on whether or not a virtual short can be removed during transistor folding. The possible values are:

- *Keep All:* Always keeping virtual shorts ensures the stability of the circuits. However, the resulting layouts may be larger, or unroutable because of too many required METAL1 routes.
- *Remove All:* Always removing virtual shorts allows the circuits to usually be smaller. However, folded transistors with no virtual shorts cannot be resized.
- *No preference:* Cadabra determines the best virtual shorts policy based on the value of the foldingPolicy Place macro property.
- *Remove Inter Level:* The effect of this setting is the same as for `NoPreference`, but all of the virtual shorts that manifest between the cell levels after the cell is placed in double-height mode are removed. The Place macro stops with an error message if the cell layout is to be generated in single-height mode.
- *Keep All Except Inter Level:* The effect is that all virtual shorts which occur in each cell level are kept, and all those that manifest inter-level after placement in double-height mode are removed. The Place macro stops with an error message if the cell layout is to be generated in single-height mode.

Vertical Conditioning tab

Prefer Empty Space: Select one of:

- *Top:* Any space remaining after all the constraints have been satisfied is placed between the P-MOSFETs and the top boundary in a single-height cell. In a double-height cell, extra space is placed between the P-MOSFETs and what is interpreted as the top boundary of the MOSFET's subcell, which might be physically below a particular P-MOSFET.
- *Center:* Any space remaining after all the constraints have been satisfied is placed in the channel region between the P-MOSFETs and the N-MOSFETs.
- *Bottom:* Any space remaining after all the constraints have been satisfied is placed between the bottom row of MOSFETs and the bottom of the boundary in a single-height cell. In a double-height cell, extra space is placed between the N-MOSFETs and what is interpreted as the bottom boundary of the MOSFET's subcell, which may be physically above a particular N-MOSFET.
- *Constraints:* A table of vertical conditioning constraints and the priority for each constraint. A priority is a value from 0 to 10, where 0 indicates that the constraint is not to be used.

Working with Routing Styles

This section covers the following topics:

To set routing style

To set routing style, do the following:

1. In the Architecture Builder window, select Layout Options > Routing Style. The Routing Style dialog box appears.
2. Set the options (refer to Routing Style Options on page 139).
3. Click OK.
   The Routing Style dialog box closes and the routing styles are set.

Routing Style Options

This section covers the following topics:

Wire Costs tab

Cost: A group of scales that allow you to set the horizontal and vertical routing costs per wire. If you select infinity (•), the wire is never used for routing.

Important: Selecting the lock button  for a wire ensures that any adjustments to the horizontal and vertical routing costs for that wire are relative.

Power Costs tab

Cost: A group of scales that allow you to set the horizontal and vertical routing costs per power wire. The relativity of the cost determines the preference for which wires are used to connect to the rails. If you select infinity (•), the wire is never used for power routing.

Important: Selecting the lock button  for a wire ensures that any adjustments to the horizontal and vertical routing costs on power for that wire are relative.

Note: You can click Calculate to have Cadabra determine the default value for some of the options. All calculated values are displayed in black. Any values modified or input by a user are displayed in blue.

Contact/Port Costs tab

Cost: A scale that allows you to set the routing costs per contact or port. If you select infinity (•), the contact/port is never used for routing.

Note: You can click Calculate to have Cadabra determine the default value for some of the options. All calculated values are displayed in black. Any values modified or input by a user are displayed in blue.

Scenarios tab

Diffusion Jumpers: The policy on using diffusion jumpers for routing. Use the slider to set the cost for using diffusion jumpers. If you select infinity (•), diffusion jumpers are not allowed.

Poly Jumpers: The policy on using poly jumpers for routing. Use the slider to set the cost for using diffusion jumpers. If you select infinity (•), poly jumpers are not allowed.

Diodes: The policy on whether or not diodes are placed by the router or placed manually.

Output Net: The policy on which topology to use for the routing of output nets. The routing topologies that are supported are C-Shaped, I-Shaped, and H-Shaped. Set the following options:

Topology: The routing topology to use. The possible values are: `"none"`, `"cShaped"`, `"iShaped"`, or `"hShaped"`.

Topology Trigger: The values that trigger the use of the specified routing topology based on the output MOSFET width. The default value for both P-MOSFET width and N-MOSFET width is 0, which indicates that the specified routing topology is always used. The MOSFET output width is calculated as the sum of all P-MOSFET or N-MOSFET widths, which have diffusions on the output net.

Key Wire Type: The key wire can be any individual wire template or `@allTemplates`, which is the default value. The key wire is the vertical wire for I-Shaped and C-Shaped routing topologies and it is the horizontal wire for H-Shaped routing topologies.

Key Wire Trigger: The values that trigger the use of the specified key wire type based on the output MOSFET width. The default value for both P-MOSFET width and N-MOSFET width is 0, which indicates that the specified key wire type is always used. The MOSFET output width is calculated as the sum of all P-MOSFET or N-MOSFET widths, which have diffusions on the output net.

Internal Net: The policy on whether or not c-shapes can be used for the routing of internal nets.

This section covers the following topics:

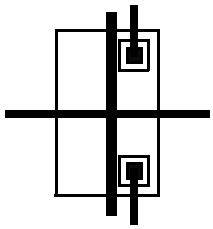
- Allow Diffusion Jumpers
- Allow Poly Jumpers

Allow Diffusion Jumpers

The policy on whether or not diffusion jumpers can be used for routing. A diffusion jumper occurs when a signal is provided from one part of the circuit, which is on a non-diffusion layer through a connection in diffusion, and back to a non-diffusion layer.

Why set this option?

If a device is blocking a wire from continuing routing in a non-diffusion layer, diffusion jumpers can be used to route through diffusion and avoid the device. However, as diffusion jumpers usually create a higher resistance path, you can select options to discourage the use of them or forbid them completely



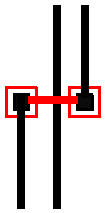
diffusion jumper

Allow Poly Jumpers

The policy on whether or not poly jumpers can be used for routing. A poly jumper occurs when a signal is provided from one part of the circuit, which is on a non-POLY layer through a connection in POLY, and back to a non-POLY layer.

Why set this option?

If a device is blocking a non-POLY wire from continuing routing in a non-POLY layer, poly jumpers can be used to route through POLY and avoid the device. However, as poly jumpers usually create a higher resistance path, you can select options to discourage the use of them or forbid them completely.



poly jumper

Gate Feedthroughs tab

Allow: The policy on using gate feedthroughs for routing. Use the slider to set the cost associated with gate feedthroughs. If you select infinity (•), gate feedthroughs are not allowed.

Max GF Fanout: This dialog allows you to set up rules for width- or finger-based gate feedthrough fanout. It includes a table to enter the rules based on the following options:

GF-MOSFET Width: The width of the gate feedthrough MOSFET. If you are setting up rules in this table, you must have at least one entry set to infinity, which will be enforced for any MOSFET larger than already specified.

Max Driven Width: The maximum driven MOSFET width. Set this value to infinity if you only want to consider fingers set to the maximum driven MOSFET width.

Max Driven # MOSFETs: The maximum number of driven MOSFET fingers. Set this value to infinity if you only want to consider the maximum driven width.

Note: When both Max Driven Width and Max Driven # MOSFETs are selected, the most restrictive rule is enforced based on the situation.

Use the Add and Delete buttons to add and remove rules from the table.

Max GF Depth: This dialog allows you to set a maximum depth for gate feedthroughs on the current path. A setting of 0 disallows gate feedthroughs.

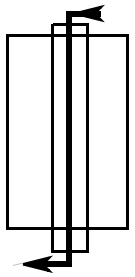
Allow Gate Feedthroughs

The policy on whether or not gate feedthroughs can be used for routing. A gate feedthrough occurs when the gate of one transistor is driven through the gate of another.

Why set this option?

In many cell architectures, a complex cell cannot be fully routed without the use of gate feedthroughs. However, as gate feedthroughs usually create a higher

resistance path, you can select options to discourage the use of them, but not to restrict them completely.



gate feedthrough

Penalties tab

Penalties: A table listing all of the routing penalties. Use the Add, Edit, and Delete button to add, edit, and remove penalties.

Name: The name of the penalty. Penalty names do not have to be unique.

Cost: The incremental cost incurred if the situation described in the penalty occurs. If the specified cost is INFINITY, it is not treated as an incremental cost; instead, the situation is treated as forbidden.

Template: The device template to which the penalty applies. Use control-click to select multiple templates from the drop-down list. The list is populated based on the wires, contacts, ports, and diodes already defined in the architecture. There are also common groupings of device templates, such as "@diffContacts", which translates to all of the defined contacts that connect to MOSFET diffusion.

Net: The net to which this penalty applies. Use control-click to select multiple nets from the drop-down list.

Direction: The direction of the device to which this penalty applies.

Region: The physical region in which the penalty applies. This is either a two-element list of real values of the form (*yMin, yMax*), or simply, "@allRegions".

Scenario: The scenario the penalty applies to.

MaxGFDepth: The maximum number of consecutive gate feedthroughs allowed on the specified nets. This option is only required if the scenario is set to "@gateFeedthroughs.

Use Preview to display the selected penalty in the Preview window. The penalty is highlighted in white on the preview canvas. If the specified region of the penalty falls outside the cell boundary, it will not appear on the canvas.

Working with Compaction Styles

This section covers the following topics:

To set compaction style

To set compaction style, do the following:

1. In the Architecture Builder window, select Layout Options > Compaction Style.
   The Compaction Style dialog box appears.
2. Set the options (refer to Compaction Style Options on page 144).
3. Click OK.
   The Compaction Style dialog box closes and the compaction styles are set.

Compaction Style Options

This section covers the following topics:

Layout Style tab

This section covers the following topics:

Diffusion Contact Cover

The preference for growing or minimizing the contact diffusion width when considering diffusion contact covers.

Which do I select?

Grow Contact Diffusion should be selected when less resistance is required or rectangular diffusions are preferred.

Minimize Contact Diffusion should be selected to reduce capacitance in your layouts.

Grow Contact Diffusion **Minimize Contact Diffusion**

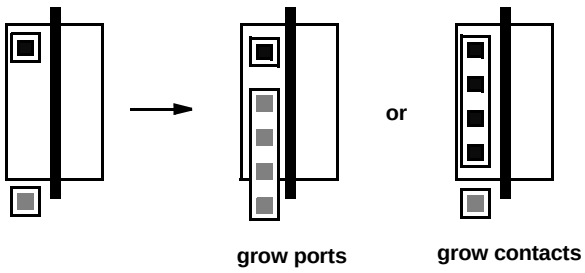
I/O Pin Hitpoint

The preference for growing ports or contacts when considering I/O pin hitpoints. I/O pin hitpoints are the connection points for your place and route tool.

Which do I select?

Grow ports should be selected to provide flexibility for your place and route tool since it generates more than one I/O pin hitpoint.

Grow contacts should be selected when diffusion resistance is a priority.



Note: Both choices are only available when you have a MOSFET and a contact as well as port with more than one cut defined in your cell architecture.

Diffusion Contact

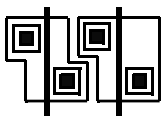
The preference for minimizing the diffusion width using gate bends or growing contacts when considering contacts in the diffusion.

Which do I select?

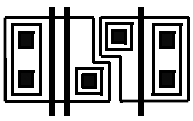
Minimize diffusion should be selected for low-power designs and higher density. The cell width and number of contact cuts are minimized.

Grow contacts should be selected for designs requiring low resistance.

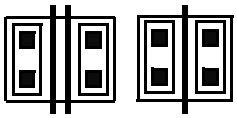
Maximize contact strapping should be selected for designs requiring low resistance and high reliability. This option will increase the width of the cell.



minimize diffusion



grow contacts



maximize contact strapping

Note: These choices are only available when you have a diffusion contact with more than one cut defined in your cell architecture.

Objectives tab

Unused: A list of constraint objectives that are not to be used during compaction.

Used: A list of constraint objectives that are to be used during compaction. The constraints are applied in the order in which they are listed.

Add: The Add/Edit Objective dialog box appears. This dialog allows you to set:

Name: The name for the objective.

Category: The type of objective. The objective can be set for performance of the circuit, or for aesthetic reasons.

Performance: The performance level for the objective. This can be High or Low. Saving an objective with high performance may lead to a better result, but will take longer to run.

Use the right and left arrows to move the objectives between the Used and Unused columns. Use the up and down arrows to change the objective order. Use Edit and Delete to update or remove objectives. Use Calculate to set the objectives back to the default order.

Layers tab

This section covers the following topics:

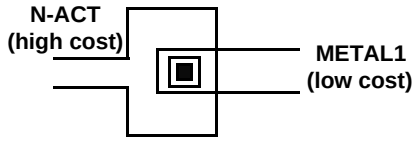
Layers

A table of compaction layers and their costs. Costs can be set to None, Low, Medium, or High by selecting an entry in the table and clicking the respective button.

Why set this option?

Assigning costs to layers allows the compactor to determine which shapes to preferably shorten during compaction. Layers with higher cost settings will be compacted before those with lower cost settings.

For example, if the compactor is faced with a situation as shown in the figure below and N-ACT has a higher cost setting than METAL1, then the compactor will shorten the N-ACT, pulling the contact to the left.



Preservation Options tab

Layer Based Preserve: A table listing all of the layers to be preserved. Use the Add, Edit, and Delete button to add, edit, and remove a layer based preserve.

Layer Name: The name of the layer to preserve. Select a layer from the drop-down list.

Relation: The manner in which layer edges are preserved. Select a relation type from the drop-down list. The possible values are:

absolute: The absolute positions of the edges are preserved.

relative exactly: The relative distances among a group of edges are preserved.

Note: If Relation is set to “relative exactly” only the relative positions within the same are preserved. The relative positions between different layers is not preserved.

Orientation: The type of orientation to preserve for the layer. Select an orientation from the drop-down list. The possible values are: manhattan, horizontal, and vertical.

Preserve Type: Two values are possible: hard or soft. For “hard” preserves, simple constraints are generated between the preserved edges and/or boundary constraints. These hard preserve constraints have a higher priority than other types of constraints and will overwrite or disable device, technology, or soft preserve constraints if necessary. For “soft” preserves, soft preserve constraints are generated. These constraints can not overwrite or disable other constraints.

Objective Type: The type of soft preserve objective to use. A value for this option is only required if Preserve Type is set to “soft”. Select an objective from the drop-down list. The possible values are:

edgeFirst: The number of edges moved during compaction is minimized.

evenDistribution: All of the edges moved during compaction are moved equally, by the same distance.

Soft Preserve Priority: The priority for the soft preserve. Select a value between 1 and 5. The soft preserves with the same specified priority are solved at the same time.

Template Based Preserve: A table listing all of the templates to be preserved. Use the Add, Edit, and Delete button to add, edit, and remove a template based preserve.

Template Name: The name of the template to preserve. Select a template from the drop-down list.

Relation: The manner in which edges are preserved. Select a relation type from the drop-down list. The possible values are:

absolute: The absolute positions of the edges are preserved.

relative exactly: The relative distances among a group of edges are preserved.

Note: If Relation is set to “relative exactly” only the relative positions within the same template are preserved. The relative positions between different templates is not preserved.

Orientation: The type of orientation to preserve for the layer. Select an orientation from the drop-down list. The possible values are: manhattan, horizontal, and vertical.

Preserve Type: Two values are possible: hard or soft. For “hard” preserves, simple constraints are generated between the preserved edges and/or boundary constraints. These hard preserve constraints have a higher priority than other types of constraints and will overwrite or disable device, technology, or soft preserve constraints if necessary. For “soft” preserves, soft preserve constraints are generated. These constraints can not overwrite or disable other constraints.

Objective Type: The type of soft preserve objective to use. A value for this option is only required if Preserve Type is set to “soft”. Select an objective from the drop-down list. The possible values are:

edgeFirst: The number of edges moved during compaction is minimized.

evenDistribution: All of the edges moved during compaction are moved equally, by the same distance.

Soft Preserve Priority: The priority for the soft preserve. Select a value between 1 and 5. The soft preserves with the same specified priority are solved at the same time.

Exclude: The layers and/or templates to exclude from preservation.

Layers: A list of layers to exclude from preservation. Click Add to open the Add Exclude Layers dialog box. This dialog allows you to select the layers to exclude.

Templates: A list of templates to exclude from preservation. Click Add to open the Add Exclude Templates dialog box. This dialog allows you to select the templates to exclude.

Layer Based Align Edges Tab

In this tab, you can set the priority for aligning edges of layers.

To set or change the priority of a layer, do the following:

1. Click on the layer name whose align edge priority you would like to set or change.
2. Depending on what priority you would like to set or change for the layer, click one of the following buttons from the lower portion of the interface:
    - None: No align edge priority is assigned to the selected layers. When compacting, layers with no align edge priority assigned to them are processed using the @alignedges objective.

- very Low (5): Very low align edge priority is assigned to the selected layer. When compacting, layers that are assigned this priority are processed using the @alignEdge5 objective.
- Low (4): Low align edge priority is assigned to the selected layer. When compacting, layers that are assigned this priority are processed using the @alignEdge4 objective.
- Medium (3): Medium align edge priority is assigned to the selected layer. When compacting, layers that are assigned this priority are processed using the @alignEdge3 objective.
- High (2): High align edge priority is assigned to the selected layer. When compacting, layers that are assigned this priority are processed using the @alignEdge2 objective.
- very High (1): Very high align edge priority is assigned to the selected layer. When compacting, layers that are assigned this priority are processed using the @alignEdge1 objective.

3. Repeat steps 1 and 2 for all the other layers whose align edge priorities you would like to set or change.
4. When you are done, confirm the changes made in steps in 1-3 by clicking OK or Apply.

Relaxation Styles Tab

In this tab, you can add, edit, delete, and order relaxation styles.

The following GUI items are available:

- Unused: This column displays the list of relaxation styles not used by the compactor.
- Used: This column displays the list of relaxation styles used by the compactor.

  Note: You can move relaxation styles between the Used and Unused columns by selecting the required relaxation style and clicking the left and right arrows that separate the two columns.

- Add a new style: Click this button in order to add a new relaxation style name.

- Edit or Show terms: To edit a relaxation style or to view details of a relaxation style, click the name of the required relaxation style from the Used or Unused columns, and then click the Edit or Show terms button.
- Delete a style: To delete a style, click the name of the required relaxation style from the Used or Unused columns, and then click the Delete a style button

Working with Electromigration Styles

This section covers the following topics:

To set electromigration style

Electromigration (EM) style determine how ports, contacts, and wires behave during layout creation. To set electromigration style, do the following:

1. In the Architecture Builder window, select Layout Options > Electromigration Style.
   The Electromigration Style dialog box appears.
2. Click Add.
   The Add Electromigration Style dialog box appears.
3. Set the options (refer to Electromigration Style Options on page 152).
4. Click OK.
   The Add Electromigration Style dialog box closes.
5. Click OK.
   The Electromigration Style dialog box closes and the EM styles are set.

   Important: You can remove a style by selecting it in the EM style table and clicking Delete.

Electromigration Style Options

MOSFET: The MOSFET element to use. Select either pMOS or nMOS from the drop-down list in the table. If the MOSFET width criteria is set to Independent of MOSFET Width, this option is greyed out.

Threshold: The threshold value the MOSFET width criteria must pass before the EM preference is applied to the specified Element. The width automatically defaults to the minimum MOSFET size, however, a different value can be manually entered. If the MOSFET width criteria is set to Independent of MOSFET Width, this option is greyed out.

Base on: The MOSFET width criteria to base the EM preferences on. The possible values are: Critical MOSFET width (unfolded width), MOSFET Finger Width (folded finger width), and Independent of MOSFET Width.

Apply To: The stage or net on which to apply the EM preferences.

Device: The port, wire, or contact element to which the EM preference applies. The element is selected from a drop-down list in the table. Each element is defined with its affected rule in brackets. For example, if a METAL1 wire is selected, the dimension rule associated with the wire layer is changed. For ports, it is the number of hit points that are affected, and for contacts, it is the number of contact cuts.

Port Location: The location of the port for a wire device can be considered or ignored when EM preference is applied to the device. This option is only available when a wire device is specified. If a wire device is not used, this field is displayed as “n/a” in the EM Style table. Unlike the other options, Port Location is not editable directly in the EM Style table. To edit this option, select it in the EM Style table and click Edit to open the Edit Electromigration Style dialog box.

Min: The minimum value for the selected element’s affected rule. The default value is populated automatically based on the value defined for that element in the Architecture Builder. A different value can be manually entered. An invalid value will not be accepted.

Max: The maximum value for the selected element’s affected rule. The default value is populated automatically based on the value defined for that element in the Architecture Builder. A different value can be manually entered. An invalid value will not be accepted. Click infinity (•) to set the maximum value to INFINITY.

Working with Text Annotation

This section covers the following topics:

To set text annotation

Setting the text annotation options allows you to specify how the exporter places port, cell, and cell name annotations used in the design. To set text annotation, do the following:

1. In the Architecture Builder window, select Layout Options > Text Annotation.
   The Text Annotation dialog box appears.
2. Set the options (refer to Text Annotation Options on page 153).
3. Click OK.
   The Text Annotation dialog box closes.

Text Annotation Options

This section covers the following topics:

Ports tab

Port Annotation: A table of the layer mappings for ports. The columns are:

Port Name: The name of the port.

Layer: The layer associated with the port.

Annotate only once per net: Only one port is annotated per net.

Text Alignment: The horizontal and vertical alignment of the port annotations.

Magnification: The magnification of the port annotations.

Width: The width of the port annotations.

Rails tab

Rail Annotation: A table of the layer mappings for power rails. The columns are:

Rail Name: The name of the power rail.

Layer: The layer associated with the power rail.

Horiz. Offset: The horizontal distance at which the annotations are offset from the ends of the power rail.

Vert. Offset: The vertical distance at which the annotations are offset from the ends of the power rail.

Annotate only once per net: Only one end of the power rail is annotated.

Text Alignment: The horizontal and vertical alignment of the power rail annotations.

Magnification: The magnification of power rail annotations.

Width: The width of the power rail annotations.

Origin: The end of the power rail to be annotated. This option has no effect if Annotate more than once per net is selected.

Cell Name tab

Cell Annotation: A table of the layer mappings for the cell. The columns are:

Cell Name: The name of the cell.

Layer: The layer associated with the cell.

Text Alignment: The horizontal and vertical alignment of the cell annotation.

Magnification: The magnification of the cell annotation.

Width: The width of the cell annotations.

Horizontal Origin: The horizontal side of the boundary to which the annotation refers.

Vertical Origin: The vertical side of the boundary to which the annotation refers.

Offset: The horizontal and vertical distances at which the annotation is offset from the cell.

To set path layers

Setting the path layers allows you to identify which layers the exporter includes in the cell layout. To set path layers, do the following:

1. In the Architecture Builder window, select Layout Options > Path Layers.

   Result: The Path Layers dialog box appears.

2. In the data column for each layer to be represented as a path, enter a "Y".

   Explanation: No entry or "N" indicates that no path data should be added for that layer.

   Note: You cannot leave this column blank for any of the layers; you must enter one of the two acceptable values: "Y" or "N". If you do not enter a value in this column for all layers, the following error message appears: `Expected value 'Y' or 'N' for layer <layer name>.`

3. Click OK.

   Result: The Path Layers dialog box closes.

Working with Measurement Metrics

This section covers the following topics:

To set measurement metrics

Setting the measurement metrics allows you to select a list of layout quality related cell properties that are calculated each time the Automated Transistor Layout (ATL), Migrate-ATL, or Measure processes are run.

To set measurement metrics, do the following:

1. In the Architecture Builder window, select Layout Options > Measurement Metrics.
   The Measurement Metrics dialog box appears.

2. Set the options (refer to Measurement Metrics Options on page 156).
3. Click OK.
   The Measurement Metrics dialog box closes.

Measurement Metrics Options

Average Diffusion Contact Growth: The average of the growth percentage of each diffusion contact.

Number of Poly Jumpers: The number of POLY jumpers.

Number of Diffusion Jumpers: The number of diffusion jumpers.

Maximum Number of GateFeedthroughs: The maximum number of gate feedthroughs on a net.

Maximum Number of Mosfets Affected by a GateFeedthrough: The number of MOSFETs affected by gate feedthroughs.

Longest Poly Route: The longest POLY route.

Worst Diffusion Contact Growth: The worst percentage of diffusion contact growth.

Number of Metal 1 Vertical FreeTracks: The number of METAL 1 vertical free tracks available.

Number of Metal 1 Horizontal FreeTracks: The number of METAL 1 horizontal free tracks available.

Number of Metal 2 Vertical FreeTracks: The number of METAL 2 vertical free tracks available.

Number of Metal 2 Horizontal FreeTracks: The number of METAL 2 horizontal free tracks available.

Number of Metal 3 Vertical FreeTracks: The number of METAL 3 vertical free tracks available.

Number of Metal 3 Horizontal FreeTracks: The number of METAL 3 horizontal free tracks available.

Working with Importers

This section covers the following topics:

To set the importer

Setting the importer allows you to map the layer numbers used in GDSII formatted files to the layer names used in Cadabra. Set the importer if you are using the Migrate GDS or Migrate-ATL processes.

To set the importer, do the following:

1. In the Architecture Builder window, select Layout Options > GDSII Importer. The GDSII Importer dialog box appears.
2. Set the options (refer to GDSII Importer Options).
3. Click OK.
   The GDSII Importer dialog box closes and the importer options are saved in the *GDSImportMap* file. This file is required for Initializing Libraries.

GDSII Importer Options

This section covers the following topics:

Layer Mapping tab

Layer Mapping: A table of the numbers and data types associated with each of the layers. These integers are used to map the layer numbers in GDSII formatted layouts to the layer names in the Cadabra formatted architecture.

Note: It is possible to specify two layer numbers for a given layer by entering the numbers in the Layer Number column separated by a comma. The import map file will have the following format for a layer that has two mappings:

```
N-WELL      3      0
N-WELL      9      0
```

Map File: The name of the file containing the mappings between the layer names in the technology and the layer numbers in the GDSII layouts. This map file can also be used to populate the Layer Mapping table. Enter the filename for the map file *or* click Browse to open a file browser. Once the map file name is entered, click Load to load the file into the layer mapping table.

Power Settings tab

Power Nets: The power nets to use. Enter the names of the power net in the appropriate fields:

VDD Net Names: The name pattern to match for the power net connected to the VDD power rail.

VSS Net Names: The name pattern to match for the ground net connected to the VSS power rail.

Preview tab

GDSII File: The file name of the GDSII layout you would like to preview using the GDSII importer options.

Note: The layer mappings from the table and the settings specified in the Architecture Builder are used to translate a GDSII file to the Preview canvas.

Working with Exporters

This section covers the following topics:

To set the exporter

Setting the exporter allows you to map the layer numbers used in GDSII formatted files to the layer names used in Cadabra. If you are using your own exporter, you can add it to the architecture by customizing the file in AL.

To set the exporter, do the following:

1. In the Architecture Builder window, select Layout Options > Exporter.
   The Exporter dialog box appears.
2. Select the exporters that you want to use and move them to the Used column using the left and right arrow buttons.
3. Select an exporter in the Used column and click Configure Exporter.
   The exporter specific dialog box appears.
4. Set the options (refer to Exporter Options).
5. Click OK.
   The Exporter dialog box closes and the exporter options are set.

Exporter Options

Custom exporter options are set from the Setup tab in the Architecture Builder.

This section covers the following topics:

- Export GDSII
- Export OpenAccess
- Export Milkyway
- Export Netlist
- Export Plib

Export GDSII

Layer Mapping: A table of the layer numbers and data types associated with each of the layers. These are used to export the layout in a GDSII file format.

Note: It is possible to specify two layer numbers for a given layer by entering the numbers in the Layer Number column separated by a comma. The GDSMap file will have the following format for a layer that has two mappings:

```
N-WELL       3       0
N-WELL       9       0
```

Map File: The name of the file containing the mappings between the layer names in the technology and the layer numbers in the GDSII layouts. This map file can be used to populate the Layer Mapping table. Enter the filename for the map file *or* click Browse to open a file browser. Once the map file name is entered, click Load to load the file into the layer mapping table.

Directory: The name of the default directory that the GDSII files are output to.

Naming Scheme: The default naming scheme for the GDSII files.

Extension: The default file extension used for each GDSII file created.

Use default extension: Whether or not the default GDSII file extension (*.gds) is used.

Export OpenAccess

Layer Preview: A table of layer numbers associated with each of the layers. These are used to export the layout in OpenAccess format.

Map File: The name of the file containing the mappings between the layer names in the technology and the layer numbers in the OpenAccess layouts. This map file can be used to populate the Layer Preview table. Enter the filename for the map file *or* click Browse to open a file browser. Once the map file name is entered, click Load to load the file into the layer mapping table.

Design: The location of the OpenAccess design. This is an optional field.

Export Milkyway

Layer Mapping: A table of layer numbers associated with each of the layers. These are used to export the layout in Milkyway format.

Map File: The name of the file containing the mappings between the layer names in the technology and the layer numbers in the Milkyway layouts. This map file can be used to populate the Layer Mapping table. Enter the filename for the map file *or* click Browse to open a file browser. Once the map file name is entered, click Load to load the file into the layer mapping table.

Note: If all of the layer names in the architecture are the same as the Milkyway layer name, a map file is not required.

Library: The default name of the library that the layers are exported to.

Export Netlist

Netlist Type: The type of netlist to export.

Directory: The name of the default directory that the Netlist files are output to.

Naming Scheme: The default naming scheme for the Netlist files.

Extension: The default file extension used for each Netlist file created.

Use default extension: Whether or not the default Netlist file extension is used. The default extension for SPICE is *.spi and the default extension for AL is *.al.

Export Plib

Directory: The name of the default directory that the Plib files are output to.

Naming Scheme: The default naming scheme for the Plib files.

Extension: The default file extension used for each Plib file created.

Use default extension: Whether or not the default Plib file extension (*.plib) is used.

Customizing an Architecture

Once you have finished working on your architecture in the Architecture Builder, you can add custom architectural elements by editing the AL file that was created when saving the architecture.

You can either generate a new.al file or merge to an existing one. If you merge to an existing .al file, the data from the architecture created in the Architecture Builder is inserted in the .al file without any alterations to the existing data.

The data in an output .al file is marked with comments to ease your reading and editing of the file. Following each registration section for an element type, are marked off areas for you to add your custom architectural elements.

Caution: Do not modify the comment lines in the .al file that begin with `/*` and end with `*/`. If you do, you may not be able to merge the file to an existing .al file.

Caution: Do not use the following reserved keywords when customizing the .al file: “`/*BEGIN`” and “`/*END`”.

Caution: You must verify and reconcile any compilation errors when you customize an architecture in AL.

To save an architecture

To save an architecture, do the following:

1. In the Architecture Builder window, select File > Save *or* Save As.
   If you select Save, the architecture is automatically saved. If you select Save As, the Save Architecture dialog box appears.
2. Enter the filename for the architecture *or* click Browse to open a file browser.
3. Set the following options:

   File: The filename for the architecture. The default extension is .pspec. Click Browse to open a file browser.

   AL File: The AL filename for the architecture. The default extension is .al. Click Browse to open a file browser.

   Merge with AL File: The architecture will be merged with an existing .al file. Cadabra inserts the data in the delimited areas and leaves the custom architectural elements unchanged. Click Browse to open a file browser.
4. Click OK.
   The Save Architecture dialog box closes and the architecture is compiled and saved as both a .pspec file and an .al file. The technology signature is verified and if not valid, a dialog box appears giving you the option of over-writing the technology file.

4

Initializing Libraries

Describes the various tasks involved in initializing libraries in Cadabra. Provides additional information to achieve better completion rates and cell layout results.

Before you can migrate or create a library, you need to initialize the library. If you are only running ATL, then initializing the library involves creating an empty library and adding cells. However, if you are running Migrate GDS or Migrate-ATL, then you also need to add source layouts and mappings between the cells and layouts.

Following is the workflow for initiating a library in Cadabra. For running ATL, you need to complete only the first two steps.

1. Create a library using an architecture. The architecture file is an AL (.al) file.

   Refer to To create a new library on page 164.

2. Add cells to the library using netlists as the input. The netlist files can be in AL or SPICE formatted files.

   Refer to To add cells on page 170.

3. Add source layouts to the library using GDS or Milkyway files as the input. You must also specify a GDS layer map file. The map file provides the mapping between layer numbers in GDSII formatted layouts to the layer names in the Cadabra formatted architecture.

   Refer to To add source layouts on page 184.

4. Map cells to source layouts by importing the mappings from a file, using the Auto-Map feature, or using the Edit Cell-to-Layout Mapping dialog box. A cell must be mapped to only one GDSII layout, however, multiple cells can be mapped to the same layout.

   Refer to To map cells to source layouts on page 187.

The following steps are optional and can be used to achieve better completion rates and cell layout results.

- **Apply cell modifiers:** Cell modifiers allow you to selectively apply placement, routing, or compaction layout styles at the cell level that override those set in the architecture for the library. A single cell modifier can be applied to several cells. Cell modifiers are saved in AL (*.al) format and can be customized and used in other libraries.

  Refer to Cell Modifiers on page 192.

- **Apply reference settings for sequential cells:** Reference settings allow you to selectively apply a reference cell or clone files to ensure a consistent layout for a family of cells, based on the symbolic layout of the reference cell or clones.

  Refer to Reference Settings on page 197.

To set the active path for the library

Setting the active path in the Cadabra window allows you to switch between Path Sets with differing libraries and input files (i.e. architectures, technologies, netlists, or GDS source layouts). Path Sets consist of a project and working directory. You must first have different Path Sets defined in your PathManager.al file.

To set the active path for the library, do the following:

- In the Cadabra window, select File > Set Active Path and the Path Set you would like to work with.
  The specified Path Set is made active.

  Note: Once an active path has been set, any File Browser opened from the Cadabra window will display the correct directory. For example, if you are opening a library, the File Browser displays the Libraries directory from the active path, or if you are adding cells, the Netlists directory, and so forth.

To create a new library

To create a new library, do the following:

1. In the Cadabra window, select Library > New.
   The New Library dialog box appears.

2. Enter a descriptive name for the library in Library Name.

   Caution: The following characters cannot be used in the library name:
   {} [] ‘’ “” @ $; : \

3. Enter the filename for the library in Library File *or* click Browse to open a file browser.
4. Enter the filename (*.al) of an architecture in Architecture File or click Browse to open a file browser.
5. In the Description section, select one of the following options with regard to cell description:
   - From Current Library: The cell description is read from the current library.

     Note: When you select this checkbox, the Library Name, Library File, and Architecture File fields are also populated with the current library’s information. You must modify the file name (the file name cannot be used as-is) because the library in memory is already written to that location.

   - From File: Type the name of the file from which you would like to extract the cell description. Alternatively, click Browse to open a file browser and navigate to the required file from which you would like to extract the file description.
   - None: Select this checkbox if you do not want a cell description when creating the library.
6. Click OK.

   Result: The new library appears in the Cadabra window in a new tab.

To open a library

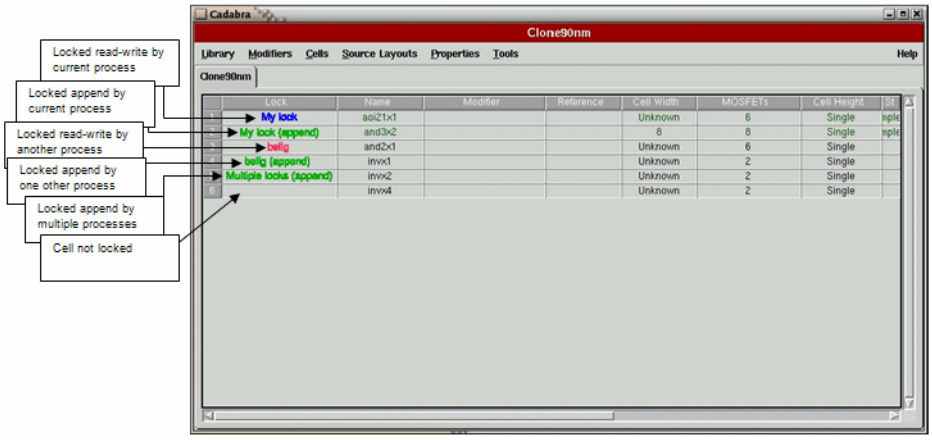
To open a library, do the following:

1. In the Cadabra window, select Library > Open.
   The Select a Library file browser appears.
2. Select a library.

Note: The abra tools allow you to open libraries created with an older version of a tool. However, the library will have to be upgraded, which in some cases may require renaming user cell properties that duplicate new built-in cell properties. Once a library is updated, it cannot be reopened in the older version of the tool.

3. Click OK.

Result: The file browser closes and the selected library appears in the Cadabra window as follows:



Important: You can have up to twelve libraries open in the Cadabra window. Each library is marked by a separate tab.

Note: Cadabra can open more than one library with the same name. If libraries with the same name are opened at the same time, the first library opened retains the original name and the subsequent library names are appended with a number. The names which contain a numerical suffix exist only while the library is open. The numerical suffix on the name is discarded when the library is closed.

Explanation: The Lock column of Cadabra window displays the My lock (append) status whenever the current process has an append lock on a cell; in this case, the My lock (append) status is displayed regardless of whether other processes also have an append lock on the same cell.

The Lock column of Cadabra window displays the Multiple locks (append) status only when the current process does not have an append lock on a cell and other processes have multiple append locks on the same cell.

To update a library

When there are multiple users working on a single library, you need to periodically update your library.

To update a library, do the following:

1. In the Cadabra window, select the tab of the library you would like to update.
2. Select Library > Update.
   All the cells in the selected library are updated.

To save a library

To save a library, do the following:

1. In the Cadabra window, select the tab of the library you would like to save, or, if you would like to create a new library based on a subset of cells in an existing library, select the cells you would like to save.
2. Select Library > Save *or* Save As.
   If you select Save, the selected library is automatically saved. If you select Save As, the Save Library dialog box appears.
3. Enter a descriptive name for the library in Library Name.

   Caution: The following characters cannot be used in the library name:
   {} [] ‘ “” @ $; : \
4. Enter the filename for the library in Library File *or* click Browse to open a file browser.
5. Select the Save selected cells as new library checkbox if you are saving a subset of cells to a new library, otherwise, proceed to step 6.
6. Click OK.
   The Save As dialog box closes and the library is saved under the specified filename.

Note: The library's cells are saved with the library. For information on these files, refer to Library File Structure on page 168.

Library File Structure

When a library is saved to disk, Cadabra creates a file structure similar to the following example:

```
LibName.lib
LibName.lib.cells/archName.psdata
                  cellName.cell
                  cellName.cell.data/1.dp
                                     1.nl
                                     3.dp
                                     3.ds
                  cellName.lock
                  cellprops.bdb
                  defaultsdb.data
                  sources.ldb
                  sources.ldb.lock
                  sources.ldb.lyts/sourceName.ldata
                  techName.tdata
```

From the example above:

LibName.lib	The library is saved in a .lib file.
LibName.lib.cells	The cells of the library are saved in a directory of the same name as the library but with a .cells extension.
archName.psdata	The relevant data from the architecture used to create the cell is saved in a .psdata file.
cellName.cell	The cells are saved in .cell files.
cellName.cell.data	The netlist, design points, and design steps of a cell are saved in a directory of the same name as the cell, but with a .data extension.
cellName.lock	The lock file for a cell is created when a cell is opened in the read-write access mode. The lock prevents multiple users from editing the same cell simultaneously. When the cell is saved or changed back to the read-only access mode, the lock file is removed.
cellprops.bdb	The cell properties are saved in a cellprops.bdb file.
defaultsdb.data	The particular defaults related to the library are saved in a defaultsdb.data file (i.e. defaults database). This includes the dialog defaults for the automated processes run from the main Cadabra window.
sources.ldb	The names of the source layouts being used are saved in a sources.ldb file (i.e. source layouts database).
sources.ldb.lock	The lock file for the source layouts database is created when the Source Layouts dialog is opened in the read-write access mode. The lock prevents multiple users from editing the source layout database simultaneously.
sources.ldb.lyts	The source layouts being used are saved in a sources.ldb.lyts directory under the cells directory.
sourceName.ldata	The source layouts are saved in .ldata files.
techName.tdata	The relevant data from the technology used to create the cell is saved in a .tdata file.

Caution: The name or content of these files cannot be directly modified. If they are, your library will be corrupted. You must use Library > Save As to rename a library and Cells > Rename to rename a cell.

To close a library

To close a library, do the following:

1. In the Cadabra window, select the tab of the library you would like to close.
2. Select Library > Close.
   The selected library closes.

   Important: Before closing the library, you can save the display settings by selecting Properties > Save Settings.

To add cells

You can add a single cell or multiple cells at a time. Cells can be based on the same netlist, however, these cells must be added one at a time.

To add cells, do the following:

1. In the Cadabra window, select the tab of the library you would like to add the new cell(s) to.
2. Select Cells > New.
   The New Cell dialog box appears.
3. Select the netlist file type.
4. Select Add one cell *or* Add multiple cells depending on the number of cells you would like to add.

If you selected Add one cell:

1. 1. Enter a unique name for the cell in Cell Name. If you do not specify a name, the netlist name is used.
2. 2. Enter the File Name of the cell netlist *or* click Browse to open a file browser.

If you selected Add multiple cells:

1. 1. Enter the Directory of the cell netlists *or* click Browse to open a file browser.
   All the files in the specified directory are listed with marked checkboxes beside them. You can filter the listed files using the Filter option.
2. 2. Select the netlists you would like to create cells from.
3. Click OK.
   A Confirm Write to Disk dialog box appears.
4. Click Yes.
   If you selected AL as the netlist type, the New Cell dialog box closes and the cell(s) are added to the selected library. If you selected SPICE, the SPICE to AL Conversion dialog box appears. Refer to To convert SPICE to AL on page 171.

To convert SPICE to AL

To convert SPICE to AL, do the following:

1. When creating a cell, select SPICE as the netlist file type in the New Cell dialog box.
2. Click OK.
   The SPICE To AL Conversion dialog box appears.
3. Set the options (refer to SPICE to AL Options on page 171).
4. Click OK.
   An .al file is created.

   Note: You can also convert SPICE to AL from a terminal window. This would allow you more options. For more information, refer to To convert SPICE to AL from a terminal window on page 175.

SPICE to AL Options

Netlist Name: The name of the netlist.

AL Filename: The directory and filename of the AL file.

Specify top level circuit: The top-level circuit of the netlist.

Read first line in file: The first line in the SPICE netlist is read.

Ignore case: The character case in the SPICE netlist is ignored.

Allow $. . .$ comments: This type of comment line is allowed in the SPICE netlist. If there are any $'s in the names on the netlist, you should not select this option.

Unfold MOSFETs: Parallel-connected transistors are unfolded into single, larger transistors. For more information, refer to Unfold MOSFETs on page 172.

Specify default MOSFET width: The default MOSFET widths for N and P MOSFETs if they are not specified in the SPICE netlist.

Specify default MOSFET length: The default MOSFET lengths for N and P MOSFETs if they are not specified in the SPICE netlist.

Models: The device mappings between the SPICE and AL netlists. For more information, refer to Models on page 173.

Nets: The net mappings between the SPICE and AL netlists. For more information, refer to Nets on page 174.

Manufacturing Grid Size: All the dimensions in the SPICE netlist are rounded to the closest multiple of the specified manufacturing grid size.

Scale MOSFET sizes: MOSFETs are scaled down by the specified value. For more information, refer to Scale MOSFET sizes on page 174.

Use Netlist filters: Parasitic elements are removed from the netlist using the specified filter file.

Disable warnings: The conversion process is silent, no warnings are issued.

Short resistors in the netlist: The polysilicon and diffusion resistors are automatically shorted as Cadabra can not use these parasitic resistors. If Save all devices is activated, only discarded resistors will be shorted.

Save all resistors: All resistors, capacitors and diodes are saved in the AL netlist.

Unfold MOSFETs

Parallel-connected transistors are unfolded into single, larger transistors.

Why set this option?

Unfolding MOSFETs can greatly improve transistor grouping.

You may also want to set this option if you are exploring different architectures. Netlists may previously have been folded to adhere to a specified cell height. However, if you are trying a new architecture with a greater cell height, you should unfold your netlists.

Also Set

The Lateral Diffusion Delta. This is the difference between the drawn and effective widths caused by encroachment of field oxide over the device well of a MOSFET. For more information, refer to Lateral Diffusion Option Details on page 20.

Models

The device mappings between the SPICE and AL netlists.

Why set this option?

Cadabra has its own internal names to represent N-type and P-type MOSFETs. You need to map the model names used in your SPICE netlist to the device types used in Cadabra.

To set a mapping:

To set a mapping, do the folloowing:

1. Select a Device Type from the list of Cadabra devices.
2. Specify the corresponding Model Name from your SPICE netlist.
3. Click Add.
   The device mapping is added to the table.

Also Set

The MOSFET model names in your architecture for the library in which you are using this cell netlist. If you do not list the model names used in your SPICE netlist in your architecture, an error will occur when you try to add a cell using the converted netlist.

Nets

The net mappings between the SPICE and AL netlists.

Why set this option?

Cadabra treats power, ground and signal nets differently when creating a layout. You need to map the net names used in your SPICE netlist to the ones in Cadabra, so the tool knows their net types. Cadabra uses VDD for power nets and VSS for ground nets.

To set a mapping:

To set a mapping, do the following:

1. Select a Net Type from the list of Cadabra nets.
2. Specify the corresponding Net Name from your SPICE netlist.
3. Click Add.
   The net mapping is added to the table.

   Note: Any ‘0’ characters at the beginning of a net name will be stripped in
   accordance with the SPICE standard.

Scale MOSFET sizes

MOSFETs are scaled down by the specified value. For example, if you enter a value of 2, MOSFETs sizes are divided in half.

Why set this option?

If you are using MOSFETs from an old library, where a different technology was used, you may need to scale down your MOSFETs.

You may also want to set this option, if you decide to change from a tall architecture to a shorter one. You could use the same netlist, but scale down the MOSFET widths. This could turn a high-speed library into a low-power one.

Also Set

The values to divide the MOSFET lengths and/or widths by in Divide MOSFET Length By and Divide MOSFET Width By.

To convert SPICE to AL from a terminal window

To convert SPICE to AL from a terminal window:

- In a terminal window, type:

```
spice2al [-debugparse]           [-debuglex]
         [-vdd <name>]           [-vss <name>]
         [-nmodel <name>]        [-pmodel <name>]
         [-nlname <name>]        [-width <value>]
         [-nwidth <value>]       [-pwidth <value>]
         [-length <value>]       [-nlength <value>]
         [-plength <value]       [-readfirst]
         [-scale <value>]        [-lscale <value>]
         [-wscale <value>]       [-short]
         [-top]                  [-unfold [delw]]
         [-nbulk]                [-pbulk]
         [-nobulkport]           [-global]
         [-discard]              [-param name <value>]
         [-manugrid <value>]     [-verbose]
         [-nocase]               [-dcomment]
         [-w]                    [-saveall]
         [-resmodel <name>]      [-capmodel <name>]
         [-diomodel]             [-filters <filename>]
         [-usegendev]            [-help]
```

```
<infile>                    <outfile>
```

An .al file is generated.

Command Options

The details of the various command options are as follows:

-debugparse	The debug parser is used.
-debuglex	The debug lexical analyzer is used.
-vdd <name>	The name of the power net.
-vss <name>	The name of the ground net.
-nmodel <name>	The name of the N-channel MOSFET model.
-pmodel <name>	The name of the P-channel MOSFET model.
-nlname <name>	The name of the converted netlist.
-width <value>	The default MOSFET channel width in microns.
-nwidth <value>	The default N-MOSFET channel width in microns.
-pwidth <value>	The default P-MOSFET channel width in microns.
-length <value>	The default MOSFET channel length in microns.
-nlength <value>	The default N-MOSFET channel length in microns.
-plength <value>	The default P-MOSFET channel length in microns.
-readfirst	The first line of the netlist is read.
-scale <value>	The MOSFET channel width and length are scaled by the specified value.
-lscale <value>	The MOSFET channel length is scaled by the specified value.

`-wscale <value>`	The MOSFET channel width is scaled by the specified value.
`-short`	All the resistors in the netlist are shorted. If you use this option with -saveall, only the discarded resistors will be shorted.
`-top`	The top-level circuit of the netlist.
`-unfold [delw]`	Parallel-connected MOSFETs are unfolded into single larger MOSFETs. The default delw is 0.
`-nbulk`	The ports for N-MOSFET bulk signals are output.
`-pbulk`	The ports for P-MOSFET bulk signals are output.
`-nobulkport`	Specifies that nets connected only to MOSFET bulk terminals should have no port.
`-global`	Nets are marked as global.
`-discard <string>`	Specifies the SPICE statement term(s) to ignore.
`-param name <value>`	The parameter's value.
`-manugrid <value>`	All the dimensions in the SPICE netlist are rounded to the closest multiple of the specified manufacturing grid size.
`-verbose`	The verbose mode is used, printing information as the SPICE file is processed. The default behavior is to be silent.
`-nocase`	The character case in the input file is ignored.
`-dcomment`	$. . .$ comment lines are allowed in the input file. If you select this option, there cannot be any $'s in the names on the netlist.
`-w`	The conversion process is silent, no warnings are issued.
`-saveall`	All resistors, capacitors and diodes are saved in the AL netlist.
`-resmodel <name>`	The name of the default resistor model.
`-capmodel <name>`	The name of the default capacitor model.

`-diomodel`	The name of the default diode model.
`-filters <filename>`	The name of the filter file to be used in removing parasitic elements from the netlist.
`-usegendev`	All the netlist devices (except MOSFETs) are stored as generic devices. Generally, you should use this option with -saveall.
`-help`	Help information is displayed.

About access modes

A cell can be accessed in the following modes:

- read-only: In this mode, you can only view cells; you cannot edit cells in read-only mode.
- read-write: In this mode, you have exclusive editing rights for a cell. If you open a cell in read-write mode, other users cannot open the cell in append mode.
- append: In this mode, multiple users can modify the cell at the deisgn-point level. If you open a cell in append mode, other users cannot open the cell in read-write mode.

When you open a cell in append mode, the access modes for design points (DPs) that already exist on disk become read-only. This means that you cannot delete or modify pre-existing design points; you can only add new design points to the tree.

Table 2 on page 179 shows the functionalities available for various access modes:

Table 2 Available Access Modes

Access Modes	Available Functionality					
	View DPs	**Add DPs**	**Edit New DPs**	**Delete DPs**	**Edit Saved DPs**	**Delete Saved DPs**
Read-Only	Yes	No	No	No	No	No
Append	Yes	Yes	Yes	Yes	No	No
Read-Write	Yes	Yes	Yes	Yes	Yes	Yes

These modes allow multiple users to simultaneously work on the same library.

Refer to Table 3 on page 179 for a summary of available access modes, given the current mode of a cell:

Table 3 Available access modes, given the current mode of a cell

Current Access Mode for Process A	Available Access Modes for Process X		
	read-only	**append**	**read-write**
Read-Only	Yes	Yes	Yes
Append	Yes	Yes	No
Read-Write	Yes	No	No

To change access modes

To change access modes, do the following:

To change access modes, do the following:

1. In the Cadabra window, select the cell or cells whose access mode you would like to change.
2. From the menu, do one of the following:
   - Cells→Access Mode→Read-Only

- Cells→Access Mode→Append
- Cells→Access Mode→Read-Write

Result: The cell's access mode is changed as specified and the Lock column in the Cadabra window is updated accordingly.

Note: If you are changing the access mode to Read-Only, but the cells have been edited and not saved, the Save Cells dialog box appears first.

Shortcut: You can also change the cell access mode from either the Cell Browser by selecting Access Mode from the background menu or from the Cell View window by selecting Design Point→Access Mode.

You can also change access modes from within a Cell Browser. To change access modes from within a Cell Browser, do the following:

- From within a Cell Browser of a cell, invoke the background menu and select one of the following:
  - Cells→Access Mode→Read-Only
  - Cells→Access Mode→Append
  - Cells→Access Mode→Read-Write

  Result: The cell's access mode is changed as specified

To copy a cell

You can create copies of existing cells in a library.

To copy a cell, do the following:

1. In the Cadabra window, select the cell(s) you would like to copy.
2. Choose Cells > Copy.
   The Copy Cell dialog box appears.

3. Specify the following details in the graphical user interface (GUI):

GUI Element	Description
Prefix	Specify a non-empty string to prepend to the name of the cell being copied, in order to create the new cell's name. **Note:** You must enter a value for either the Prefix or Suffix fields, or both. You cannot leave both the Prefix and Suffix text boxes blank.
Suffix	Specify a non-empty string to append to the name of the cell being copied, in order to create the new cell's name. **Note:** You must enter a value for either the Prefix or Suffix fields, or both. You cannot leave both the Prefix and Suffix text boxes blank.
Copy Design Trees	Select this checkbox to indicate if a cell's design tree should also be copied.
Select Newly Created Cells	Select this checkbox to indicate that newly created cells should be selected in the Library Browser at the end of the operation. This checkbox is selected by default.

4. Click OK.

   Result: The required cells are copied.

   Explanation: For more information on what cell properties are copied in the background during this operation, refer to the Library→copyCells() section in the *Cadabra AL Reference Guide*.

To rename a cell

To rename a cell, do the following:

1. In the Cadabra window, select the cell you would like to rename.
2. Select Cells > Rename.
   The Rename Cell dialog box appears.
3. Enter the new name for the cell in Cell Name.

Caution: Cell names must be unique within the same library.

4. Click OK.
   A Confirm Write to Disk dialog box appears.
5. Click Yes.
   The Rename Cell dialog box closes and the cell name is updated in the Cadabra window.

   Caution: Cell-to-layout mappings are not automatically updated when you rename a cell. You must update any mappings existing for cells that you rename.

To scale a cell

You can only scale cells that are not currently locked, do not have jobs submitted on them, and do not have design points other than the root point in the design tree.

To scale a cell, do the following:

1. In the Cadabra window, select the cells you would like to scale.
2. From the menu, do one of the following:
   - Choose Cells→Scale.
   - From the background menu of a cell browser, choose Scale.

   Result: The Scale Cell dialog box appears.
3. Type appropriate values in the Source and, if required, Target boxes of the following fields:
   - Minimum MOSFET Gate Length
   - Maximum N-MOSFET Gate Width
   - Maximum P-MOSFET Gate Width

   Note: By default, the Target fields are populated using information from the architecture of the library.
4. If required, you can select the Use Unit Cell checkbox to populate the Source fields using the dimensions of the unit cell.

Note: The unit cell is the smallest single inverter in the library where the P-MOSFETs and N-MOSFETs have been sized to fit in the N-Well in the architecture that they are used in.

5. Click OK.

   Result: The required cells are scaled.

To change cell height

Cadabra only supports single- and double-height cells in these orientations:

- Single-height cell: placement of an N-well region containing P-type MOSFETs in the top of the cell and a P-well region containing N-type MOSFETs in the bottom of the cell.
- Double-height cell: placement of a P-well region containing N-type MOSFETs in the top of the cell, an N-well region containing P-type MOSFETs in the middle of the cell, and a P-well region containing N-type MOSFETs in the bottom of the cell.

To change cell height, do the following:

1. In the Cadabra window, select the cell(s) you would like to change the height for.
2. Select Cells > Height > Single *or* Double.
   The cell's height is changed as specified and the Cell Height column in the Cadabra window is updated accordingly.

To save a cell

If you have modified a cell, you should save it so that others can view the results.

To save a cell, do the following:

- From the Cell Browser background menu, select Save.
  The cell is saved in the library.

To delete a cell

To delete a cell, do the following:

1. In the Cadabra window, select the cell(s) you would like to delete.
2. Select Cells > Delete.
   A Question dialog box appears to confirm the removal.
3. Click Yes *or* Yes To All.
   The selected cell(s) are permanently removed from disk.

   Caution: Cell-to-layout mappings are not automatically updated when you delete a cell. You must remove any mappings existing for cells that you delete.

To add source layouts

Adding source layouts allows you to read GDSII, OpenAccess, or Milkyway layouts into the layout database.

To add source layouts, do the following:

1. In the Cadabra window, select Source Layouts > Open.
   The Source Layouts dialog box appears.
2. Click Read-In.
   The Read-in Layouts dialog box appears.
3. Select the layout source.
4. Enter the location of the source files *or* click Browse to open a file browser.
   All the files in the specified location are listed with marked checkboxes beside them.
5. For GDSII, select a Filter extension.
6. Select the source layouts you would like to add to the library.
7. Set the options (refer to Read-in Layouts Options on page 185).
8. Click OK.
   The Read-in Layouts dialog box closes and the selected source layouts are read into the layout database.

9. Click OK.
   The Source Layouts dialog box closes.

Read-in Layouts Options

Layout Source: The source layout to read into the layout database. Choose from the following options:

- GDSII
- OpenAccess
- Milkyway

Location: The directory containing GDSII, OpenAccess, or Milkyway source layout.

Filter: (GDSII only) The file extension used to filter the files in the specified directory.

Structure Name: (GDSII only) The regular expression to be read from the source layout file to help determine which layout to read-in.

Overwrite existing layouts: Existing source layouts with the same name are overwritten. If this option is not selected, then any new layout that has the same name as an existing layout is added with the suffix #1.

Layer map file: (Optional for Milkyway) The file containing the mappings between the layer names in the technology and for GDSII, the layer numbers in the source layouts. The file must list the layer name first, then the layer numbers, as shown in the GDSII example below:

```
N-WELL       2     0
N-IMPLANT    8     0
P-IMPLANT    7     0
N-ACT        3     0
...
```

Microns per unit: (GDSII only) The ratio between GDS coordinates and the real coordinates (in microns). The default is 0.001.

To rename a source layout

To rename a source layout, do the following:

1. In the Cadabra window, select Source Layouts > Open.
   The Source Layouts dialog box appears.
2. Select the layout you would like to rename.
3. Click Rename.
   The Rename Source Layout dialog box appears.
4. Enter the new name for the layout in New Layout Name.
5. Click OK.
   The Rename Source Layout dialog box closes and the layout name is updated in the Source Layouts dialog box.

   Caution: Cell-to-layout mappings are not automatically updated when you rename a layout. You must update any mappings existing for layouts that you rename.

To remove a source layout

Removing a source layout allows you to remove a layout from the layout database.

To remove a source layout, do the following:

1. In the Cadabra window, select Source Layouts > Open.
   The Source Layouts dialog box appears.
2. Select the layout(s) you would like to remove.
3. Click Remove.
   A Question dialog box appears to confirm the removal.
4. Click Yes *or* Yes To All.
   The selected layout(s) are removed from the layout database.

   Caution: Cell-to-layout mappings are not automatically updated when you remove a layout. You must delete any mappings existing for layouts that you remove.

To map cells to source layouts

Mapping cells to source layouts enables automated migration. A cell must be mapped to only one GDSII layout, however, multiple cells can be mapped to the same layout. You can map cells to source layouts by importing the mappings from a file, using the Auto-Map feature, or using the Edit Cell-to-Layout Mapping dialog box.

Importing mappings

To import mappings, do the following:

1. In the Cadabra window, select Source Layouts > Edit Cell/Layout Mapping.
   The Edit Cell-to-Layout Mapping dialog box appears.
2. Click Read Mapping From File.
   The File Browse appears.
3. Select the file containing the mappings.

   Note: The file must list the cell name first, then the source layout name. The names should be separated with a space as this file cannot be delimited by a comma or anything else.

4. Click OK.
   The mappings are imported and the dialog is updated.
5. Click Dismiss.
   The Edit Cell-to-Layout Mapping dialog box closes.

Using Auto-Map

To use auto-map, do the following:

1. In the Cadabra window, select Source Layouts > Edit Cell/Layout Mapping.
   The Edit Cell-to-Layout Mapping dialog box appears.
2. Set the Auto-Map Criteria options (refer to Edit Cell-to-Layout Mapping Options on page 188).
3. Click Auto-Map.
   The mappings are automatically created based on similar cell and source layout names.

4. Click Save as Default Mapping.
   The mappings are saved.
5. Click Dismiss.
   The Edit Cell-to-Layout Mapping dialog box closes.

Mapping Cells to Source Layouts

To map cells to source layouts, do the following:

1. In the Cadabra window, select Source Layouts > Edit Cell/Layout Mapping.
   The Edit Cell-to-Layout Mapping dialog box appears.
2. Select the cell you would like to map from the Cell column.
3. Select the source layout you would like to map the cell to from the corresponding drop-down list in the Source Layouts column.
4. Repeat steps 2-3 until all the mappings have been added.
5. Click Dismiss.
   The Edit Cell-to-Layout Mapping dialog box closes.

Edit Cell-to-Layout Mapping Options

Cell/Layout Mapping: A table of cell-to-layout mappings.

Auto-Map: The cells are automatically mapped to the source layouts based on the Auto-Map Criteria.

Clear All: All the set mappings are cleared.

Ignore case: The letter-case is ignored during automated mapping.

Match: The naming criteria to be used to match cells to layouts with the auto-map feature. Possible values are:

<Cell> to <SourceLayout>: The cell and layout names must be identical.

Prefix<Cell>Postfix to <SourceLayout>: A prefix and/or postfix can be used to match cells with slightly differing names to layouts.

<Cell> to Prefix<SourceLayout>Postfix: A prefix and/or postfix can be used to match layouts with slightly differing names to cells.

Prefix/Postfix: The prefix and/or postfix to be applied to the cell or layout name as indicated by Match. A question mark (?) indicates a single differing character while an asterisk (*) indicates a differing string. For example, if you use the prefix?, Cadabra would match a cell named and2d1 to a layout named _and2d1.

Map all cells: All the cells are mapped during automated mapping and any existing mappings are overridden.

Map cells with no mapping: Only the cells with no mapping are mapped during automated mapping.

Read Mapping From File: A File Browser appears allowing you to select a file to import the mappings from.

Write Mapping To File: A File Browser appears allowing you to specify a file to export the mappings to.

To change a cell-to-layout mapping

Changing a cell-to-layout mapping allows you to map a cell to a different source layout.

To change a cell-to-layout mapping, do the following:

1. In the Cadabra window, select the cell you would like to change the mapping for.
2. Select Cells > Open.
   The Cell Browser appears.
3. Click and hold on the source layout design point or the netlist design point.
   The design point menu appears.
4. Select Change Cell/Layout Mapping.
   The Change Cell-to-Layout Mapping dialog box appears.
5. Select the new source layout you would like to map the cell to.
6. Click OK.
   The cell is mapped to the selected layout and the name of the layout appears below the source layout design point.

   Note: You can also change the cell-to-layout mapping by selecting Source Layouts > Edit Cell/Layout Mapping from the Cadabra window and using the Edit Cell-to-Layout Mapping dialog box.

To remove a cell-to-layout mapping

To remove a cell-to-layout mapping, do the following:

1. In the Cadabra window, select the cell you would like to remove the mapping for.
2. Select Cells > Open.
   The Cell Browser appears.
3. Click and hold on the source layout design point or the netlist design point.
   The design point menu appears.
4. Select Remove Cell/Layout Mapping.
   The cell-to-layout mapping is removed and the source layout design point is removed from the Cell Browser.

   Caution: A cell must be mapped to a source layout before running Migrate GDS or Migrate-ATL.

To get a netlist description

A netlist description provides a quick overview of the number of ports, nets, and MOSFETs in a netlist.

To get a netlist description, do the following:

1. In the Cadabra window, select the cell you would like to view the description for.
2. Select Cells > Open or Open (Read-Only).
   The Cell Browser appears.
3. Select Describe from the netlist design point menu.
   The Describe Netlist window appears, displaying the following:

- cell name,
- number of ports,
- number of MOSFETs,
- number of nets,
- maximum width of N-MOSFETs, and

- maximum width of N-MOSFETs.
- cumulative scaling history of the netlist, if applicable.

If a netlist has not been scaled, then this information is not displayed.

To export a description file

You can export a description file from a library using all or some of the cells in the library. The description file will, by default, contain all user-defined properties unless you exclude specific properties from the process.

To export a description file, do the following:

1. In the Cadabra window of the library you would like to export the description file from, choose Library→Export Description File.

   Result: The Export Description File dialog box appears.

2. Type a file name in the Export to File field or click Browse to open a file browser.
3. The Cell Properties listbox contains a list of all properties that you can export. To identify a cell property for export to a description file, select the required cell property in the Cell Properties listbox and click the arrow icon.

   Result: The Properties to Export listbox contains all the properties that you have selected to be exported.

4. You can manipulate the following Special Keyword Properties:
   - `netlist:` Indicates that the netlist from each cell should be used to create a new cell in the new library.
   - `gdsLayout:` Indicates that the layout associated with each cell should be included in the new library and mapped appropriately.
5. You can manipulate the following built-in cell properties:
   - `targetWidth:` Indicates that the target width for each cell should be included.
   - `modifierName:` Indicates that the cell modifier mappings should be included.
   - `cellHeightType:` Indicates that the type of cell height should be included.

- `reference:` Indicates that the reference cell mappings should be included.

Note: You can also manipulate all user-defined properties.

6. Click OK.

Result: The Export Description File dialog box closes and the properties are exported and saved to the specified file and directory. If a directory is not specified, the file is saved to the `CADABRAWORKING` directory.

Note: The description file is a TEXT file that can be modified using any text editor and is identified by a .descrip file extension.

Explanation: The exported properties can easily be used in any spreadsheet application.

Cell Modifiers

Cell modifiers allow you to apply default settings and layout styles at the cell level that override those set in the architecture that the library is based on. The Cell Modifier Builder uses the architecture settings that originated in the architecture file that the library was created with. However, a cell modifier needs to only contain the settings that are different from the ones set in the original architecture file.

The flow for setting up and using cell modifiers involves creating a new cell modifier or adding existing cell modifiers. Once the cell modifiers are added to a library, they can be associated to cells as required. A cell modifier can be associated with one cell, multiple cells, or no cell. Once a cell modifier has been created, it can be edited or removed from the library.

All cell modifiers are saved to disk in the AL (*.al) file format before they can be used. A cell modifier AL file can be customized and applied back to the library. When outputting a modifier to AL, there is an option that allows you to merge to an existing AL file. This option allows the customizations to be inserted in the file without any alterations to the existing data.

Because cell modifiers are associated with specific cell names, they can be transferred to other similar libraries by importing and exporting the cell modifier property.

To create a cell modifier

To create a new cell modifier, do the following:

1. In the Cadabra window select Modifier > Create.
   The Cell Modifier Builder dialog box appears.
2. Select the Setup tab.
3. Click on Placement Style > Edit in the side list or select Layout Options > Placement Style.
   The Placement Style dialog box appears.
4. Set the options (refer to Placement Style Options on page 134).
5. Click OK.
   The Placement Style dialog box closes and the placement styles are set.
6. Click on Routing Style > Edit in the side list or select Layout Options > Routing Style.
   The Routing Style dialog box appears.
7. Set the options (refer to Routing Style Options on page 139).
8. Click OK.
   The Routing Style dialog box closes and the routing styles are set.
9. Click on Compaction Style > Edit in the list or select Layout Options > Compaction Style.
   The Compaction Style dialog box appears.
10. Set the options (refer to Compaction Style Options on page 144).
11. Click OK.
    The Compaction Style dialog box closes and the compaction styles are set.
12. Select the Advanced tab. This step is optional and is only required if you want to modify the properties and functions set in the DefaultsDB.

    Caution: The features available in the Advanced tab are for advanced users only. Changing properties and adding functions can seriously compromise your setup. Changes you make are at your own risk. If you are uncertain about using these features, please contact your Cadabra Application Consultant for assistance.

13. Add properties and/or functions to the appropriate default categories.

For more information, refer to Architecture Details: Properties on page 127 and Architecture Details: Functions on page 128.

14. Select File > Save to save the modifier.
    The Save dialog box appears.
15. Enter the filename for the cell modifier file *or* click Browse to open a file browser.

    Note: The name that you specify for the filename is also the name used for the cell modifier. If you want to rename the cell modifier, select File > Rename Modifier.

16. Set the options:

    Output AL to File: The AL filename to output the cell modifier to.

    Merge with AL File: The cell modifier is merged with an existing .al file. Cadabra inserts the data in the delimited areas and ignores the custom architectural elements.

    Add to Library: The cell modifier is added to the library.

17. Click OK.
    The Save dialog box closes and the cell modifier is saved.

To add cell modifiers

You can add a single or multiple cell modifiers at one time. To add existing cell modifiers that were created in another library to the current library, do the following:

1. In the Cadabra window select Modifier > Add.
   The Add Modifier dialog box appears.
2. Select Add one modifier *or* Add multiple modifiers depending on the number of modifiers you want to add.
3. If you selected Add one modifier, enter the File Name of the cell modifier *or* click Browse to open a file browser. If you selected Add multiple modifiers:

   a. Enter the Directory of the cell modifiers *or* click Browse to open a file browser.
   All the files in the specified directory are listed with marked checkboxes beside them. You can filter the listed files using the Filter option.

b. Select the modifiers you would like to add to your library.

4. Click OK.
   The Add Cell Modifier dialog box closes and the cell modifiers are added to the library.

To associate cell modifiers

Cell modifiers can be associated to single or multiple cells. A cell modifier must first be created or added before it can be associated with a cell. To associate cell modifiers, do the following:

1. In the Cadabra window, select the cell(s) you would like to associate a modifier with.

   Important: Use Shift-click or Control-click to select multiple cells in the Cadabra window.

2. Select Cells > Modifier > Modifier Name.
   The modifier is associated with the cell as specified and the Modifier column in the Cadabra window is updated accordingly.

To edit a cell modifier

To edit an existing cell modifier, do the following:

1. In the Cadabra window select Modifier > Edit.
   The Cell Modifier Builder dialog box appears.
2. Select the Setup tab.
3. Click on Placement Style > Edit in the list or select Layout Options > Placement Style.
   The Placement Style dialog box appears.
4. Edit the options (refer to Placement Style Options on page 134).
5. Click OK.
   The Placement Style dialog box closes and the placement styles are set.
6. Click on Routing Style > Edit in the list or select Layout Options > Routing Style.
   The Routing Style dialog box appears.

7. Edit the options (refer to Routing Style Options on page 139).
8. Click OK.
   The Routing Style dialog box closes and the routing styles are set.
9. Click on Compaction Style > Edit in the list or select Layout Options > Compaction Style.
   The Compaction Style dialog box appears.
10. Edit the options (refer to Compaction Style Options on page 144).
11. Click OK.
    The Compaction Style dialog box closes and the compaction styles are set.
12. Select the Advanced tab. This step is optional and is only required if you want to modify the properties and functions set in the DefaultsDB.

    Caution: The features available in the Advanced tab are for advanced users only. Changing properties and adding functions can seriously compromise your setup. Changes you make are at your own risk. If you are uncertain about using these features, please contact your Cadabra Application Consultant for assistance.

13. Edit the properties and/or functions for the appropriate default categories.

    For more information, refer to Architecture Details: Properties on page 127 and Architecture Details: Functions on page 128.
14. Select File > Save.
    The Save dialog box appears.
15. Enter the filename for the cell modifier file *or* click Browse to open a file browser.
16. Set the options:

    Output AL to File: The AL filename to output the cell modifier to.

    Merge with AL File: The cell modifier is merged with an existing .al file. Cadabra inserts the data in the delimited areas and ignores the custom architectural elements.

    Add to Library: The cell modifier is added to the library.
17. Click OK.
    The Save dialog box closes and the changes to the cell modifier are saved.

Customizing a Cell Modifier

Once you have created or edited your cell modifier in the Cell Modifier Builder, you can further customize the placement, routing, and compaction layout styles by outputting the file to AL and editing that file.

You can either generate a new .al file or merge to an existing one. If you merge to an existing .al file, the data from the cell modifier created in the Cell Modifier Builder is inserted in the .al file without any alterations to the existing data.

The data in an output .al file is marked with comments to ease your reading and editing of the file. Following each registration section for each layout style, are marked off areas for you to add your customizations.

Caution: Do not modify the comment lines in the .al file that begin with */** and end with **/*. If you do, you may not be able to merge the file to an existing .al file.

Caution: Do not use the following reserved keywords when customizing the .al file: "/*BEGIN" and "/*END".

Caution: You must verify and reconcile any compilation errors when you customize a cell modifier in AL.

Reference Settings

Applying reference settings is recommended to obtain consistency between layouts and to reduce runtimes. Reference settings are applicable to sequential cell only. They can be applied to other types of cells, however, this may cause undesirable results. A reference setting can be either a reference cell or reference clone, which is associated with one or more cells, to ensure a consistent layout for a family of cells based on the symbolic layout of the reference cell or clone. A family of cells is defined as a group of cells that have the same unfolded netlist, regardless of MOSFET size.

The Reference Setting dialog box allows you to specify either clone files or reference cells as the point of reference for creating the layouts for the family of cells. The ability to specify references is useful for complicated cell architectures or cells that require significant hand editing to achieve a desired result. This approach allows you to take a finalized cell layout and apply it to other cells within the same family as a reference cell. You can export the cell

layout, or part of the cell layout, to a clone file for use in other libraries and you can also use clones files that have been created from other libraries as a reference in your current library. However, if you are using reference cells, they must exist in the same library as the target family of cells.

Because reference settings are associated with specific cell names, they can be transferred to other similar libraries by importing and exporting the reference cell property.

Reference Cells

The workflow for using reference cells is as follows:

1. Create the library and add the sequential cells. (Refer to To create a new library on page 164 and To add cells on page 170.)

   If you are going to run MigrateGDS, Migrate-ATL, or Import on the reference cells, you must also add source layouts and then map the cells to the layouts. (Refer to To add source layouts on page 184 and To map cells to source layouts on page 187.)

2. Identify the reference cells either automatically or manually. This step sets the Reference property for the child cells.

   Refer to To automatically set cell references on page 200 and To manually set clone or cell references on page 201.

3. Complete the reference cells using MigrateGDS, Migrate-ATL, ATL, or a combination of the individual process: Import, Place, Route, Compact, and Finalize.

4. Run ATL on the child cells - when the Reference property is set for the child cell, ATL automatically uses the reference when it is run.

   Refer to To run ATL on page 220.

   Note: When submitting jobs to scheduling software such as LSF, SGE, or even to your localhost, you can select the Create Job Dependencies option on the appropriate configuration dialog to create a dependency between the parent and child cells over the multiple job submissions. (For more information, refer to LSF Scheduler Configuration Options on page 306 and SGE Configuration Options on page 308.)

When a reference cell is specified for a cell, or a group of cells, a parent-child dependency between the cells is created. This means that all jobs can be submitted at the same time but the child cells are not started until the reference (parent) cells are completed.

Child cells can also be created based on partially completed parent cells (placed and routed). The child cell uses the same placement as the parent cell, and as much of the routing as possible. A warning is provided and ATL proceeds with routing and compaction that is not based on the parent cell.

If the parent cell is a completed cell, but the child cell cannot reuse any of the parent cell's routing due to refolding, the child cell is placed based on the parent cell and ATL proceeds with routing and compaction that is not based on the parent cell.

Reference Clones

The flow for using reference clone files involves specifying an existing clone file (*.cln), or files, to be applied to one or more cells in a library. Using reference clones allows you to reuse portions of a layout among different cells with common circuitry. A clone file, may be either a "whole cell" clone or a "partial cell" clone. If a "whole cell" clone is used, only one clone file needs to be specified for a family of cells. If "partial cell" clones are used, one or more clone files can be specified, along with the order of use for each file. A partial clone is a portion of a symbolic layout that has been exported to a clone file. Using partial clones allows you to select different portions from several symbolic layouts to be used as references for the placement and routing of the layouts for the specified family of cells.

The workflow for using reference clones is as follows:

1. Create clone files (*.cln) from existing symbolic layouts. You can also use a partial clones.

   Refer to To export a clone on page 370 and To clone part of a layout on page 371.

2. Create a `$ProjectPath/Clones` directory and put the clone files in this directory.

3. Create the library and add the sequential cells.

Refer to To create a new library on page 164 and To add cells on page 170.

4. In the Cadabra window, select the cells for which you want to specify clone references. Each cell or group of cells that requires a different reference clone must be selected individually.
5. Set the Reference Clones options in the Reference Settings dialog box. Once a clone reference is specified for cell, the Reference property is set to “External Clone”.

   Refer to To manually set clone or cell references on page 201 and Set Reference Options on page 201.
6. Run ATL or Place on the cells.

   Refer to To run ATL on page 220 and To place a cell on page 223.

To automatically set cell references

The automatic cell reference identification flow loads and runs an AL script, which identifies only sequential cell families and a reference cell for each family by netlist matching. From the user interface, you can set the criteria for the reference cell.

Note: You can change the default value for the reference flow from the largest driving strength to the smallest or average driving strength using the referenceCriteria default.

To run the automated script, do the following:

1. In the Cadabra window select the sequential cells that you want to set references for, or select Cells > Select All.
2. Select Cells > Reference > Auto Set.
   - `maxWidth:` The maximum width of the output transistors that corresponds to the highest drive strength.
   - `minWidth:` The minimum width of the output transistors that corresponds to the lowest drive strength.
   - `meanWidth:` The minimum width of the output transistors that corresponds to the lowest drive strength.

   Result: ÂThe identified reference cell name is displayed in the Reference cell property column for each of the selected cells.

Note: The reference appears in a format similar to: `[r]:<Cell_Name> or [R]:<Clone_Files>`. The "`R:`" or "`r:`" prefix indicates that matching clone folding is not used. To apply the match clone folding option, select the cells in the Cadabra window and select Cells > Reference > Set Manual. From the Reference Setting dialog select the Match Folding option under Set Reference Cells and click OK. The reference now appears in the format `[C]:<Cell_Name>`, or `[C]:<Clone_Name>` in the Reference property column.

To manually set clone or cell references

To manually set a clone file or cell reference, do the following:

1. In the Cadabra window select either a single cell, or a family of cells that you want to set a reference for.
2. Select Cells > Reference > Manual Set.
   The Reference Setting dialog box appears.
3. Set the options (refer to Set Reference Options on page 201).
4. Click OK.
   The Reference Setting dialog box closes and the specified reference is displayed in the Reference property column.

Set Reference Options

In the Reference Setting dialog box, the ability to specify clone files or a reference cell, for a single cell or a family of cells, is mutually exclusive.

Reference Clones

Set Clone Files: Clone files are used as the reference for producing identical placement and routing topologies.

Clone File: The directory path and file name of the clone to use. Use the Browse button to open a file browser. By default, all of the clone files in

`$ProjectPath/Clones` are displayed. After the clone file is specified, click Add to add the clone file to the Matching Order list.

Match Clone Folding: The folding in the target cell attempts to match as much of the folding in the reference clone file(s) as possible. If the clone folding leads to a too large or a too small MOSFET size, the MOSFET is refolded to an appropriate size so that it can be placed.

Matching Order: An ordered list of clone files to use. You must specify the order in which the clones are matched. Use the up and down arrows to define the matching order for the clones files.

Placement Order: The clone files in the Matching Order list are added to the Placement Order list. Use the up and down arrows to define the placement order for the clones files from left to right. Setting Placement Order is optional.

Reference Cells

Set Reference Cell: Cells are used as the reference for producing identical placement and routing topologies.

Match Folding: The folding in the target cell is identical to the folding in the reference cell.

Cell Name: The name of the cell in the current library to use as the reference cell. All of the cells in the library are listed in alphabetical order in the drop-down list. Type an upper-case character or string into the Cell Name field to retrieve only the cells with the names that begin with the characters entered.

Note: The cell property value appears in one of the following formats in the Reference cell property column in the main Cadabra window:

`[r]:<Cell_Name>`: The reference flow based on a given cell.

`[c]:<Cell_Name>`: The reference flow based on match folding.

`[R]:<Clone_Files>`: The reference flow based on clone files.

`[C]:<Clone_Files>`: The reference flow based on match clone folding.

To remove a clone or cell reference

To remove a clone or cell reference, do the following:

1. In the Cadabra window select either a single cell, or a family of cells that you want to remove a reference for.

   Note: Clone and cell references are mutually exclusive. You must remove clone and cell references individually.

2. Select Cells > Set Reference.
   The Reference Setting dialog box appears.
3. For a clone reference, select the clone files that you want to remove in the Matching Order list and click Delete, or click Delete All to remove all of the clone files.
4. For a cell reference, delete the cell name that appears in the Cell Name text field.
5. Click OK.
   The Reference Setting dialog box closes and Reference property column for the selected cells is empty.

Cell Properties

Cadabra provides some built-in cell properties for your library, but you can also define your own.

The cell properties are displayed in the Cadabra window. You can customize the display by showing or hiding certain properties. The property values for some of the built-in properties are automatically updated as you make changes to your library. However, for other properties, you have to enter the values directly into the table on the Cadabra window or import the values from a character delimited file (CDF).

Cadabra also allows you to export cell properties into a character delimited file for use in a spreadsheet application.

Built-in Cell Properties

The built-in properties provided in Cadabra are common to all the tools in the suite. However, only those applicable to Cadabra are shown by default in the Cadabra window.

ATL Time	The total time that the cell took for ATL. The time appears in the format: hh:mm:ss.
Average Diffusion Contact Growth (%)	The average of the growth percentage of each diffusion contact. This property is only calculated if it is set in the secondaryQualityMetrics property on the Measure macro.
Cell Area (um^2)	The current cell area in microns squared (i.e. the cell width multiplied by the cell height).
Cell Height (um)	The current cell height in microns.
Cell Height Type	The height of the cell based on type: single (pn) or double (pnp).
Cell Optimality	The optimality of the final layout based on cell width.
Cell Status	The completion status of the cell.
Cell Width	The current cell width in grids of the layout marked by the cell marker. “Unknown” indicates that the cell does not have a cell marker.
Cell Width (um)	The current cell width in microns of the layout marked by the cell marker. “Unknown” indicates that the cell does not have a cell marker.
Compaction Time	The time that the cell took to compact. The time appears in the format: hh:mm:ss.
Diffusion Jumpers	The number of diffusion jumpers. This property is only calculated if it is set in the secondaryQualityMetrics property on the Measure macro.
DPs	The number of design points in the cell's design tree.

Diffusion Quality	The diffusion quality of the cell based on the minimum amount of diffusion needed to route the cell.
Host	The name of the machine used to run the script on the cell.
Import Time	The time that the cell took to import. The time appears in the format: hh:mm:ss.
Job ID	The ID number of the job(s) submitted to the scheduling software.
Job Scheduler	The name of the job scheduler in use.
Job Status	The status of the cell if it has been submitted to the job scheduler.
Longest Poly Route	The length of the longest poly route. This property is only calculated if it is set in the secondaryQualityMetrics property on the Measure macro.
Max Gate Feedthroughs	The maximum number of gate feedthroughs on a net. This property is only calculated if it is set in the secondaryQualityMetrics property on the Measure macro.
METAL 1 Vertical Free Tracks	The number of METAL 1 vertical free tracks available. This property is only calculated if it is set in the secondaryQualityMetrics property on the Measure macro.
METAL 1 Horizontal Free Tracks	The number of METAL 1 horizontal free tracks available. This property is only calculated if it is set in the secondaryQualityMetrics property on the Measure macro.
METAL 2 Vertical Free Tracks	The number of METAL 2 vertical free tracks available. This property is only calculated if it is set in the secondaryQualityMetrics property on the Measure macro.

METAL 2 Horizontal Free Tracks	The number of METAL 2 horizontal free tracks available. This property is only calculated if it is set in the secondaryQualityMetrics property on the Measure macro.
METAL 3 Vertical Free Tracks	The number of METAL 3 vertical free tracks available. This property is only calculated if it is set in the secondaryQualityMetrics property on the Measure macro.
METAL 3 Horizontal Free Tracks	The number of METAL 3 horizontal free tracks available. This property is only calculated if it is set in the secondaryQualityMetrics property on the Measure macro.
Migration Time	The total time that the cell took to migrate. The time appears in the format: hh:mm:ss.
Modifier	The name of the modifier applied to the cell. The modifier is used to apply different placement, routing, or compaction layout styles than those set in the library's architecture.
MOSFETs	The number of MOSFETs in the cell's netlist.
MOSFET Folds	The number of MOSFETs in the marked design point after folding.
Num Gate Feedthrough Affected Mosfets	The number of MOSFETs in the cell which are affected by gate feedthroughs. This property is only calculated if it is set in the secondaryQualityMetrics property on the Measure macro.
Optimal Layout Placement	The placement used to produce the final layout. The placement values are based on the following design point tags: Placement1, Placement2, Placement3, Placement4, Placement5, Candidate Placement, and Alternate Alignment.
Owner	The name of the person responsible for working on the cell.
Placement Time	The time that the cell took to place. The time appears in the format: hh:mm:ss.

Poly Jumpers	The number of poly jumpers. This property is only calculated if it is set in the secondaryQualityMetrics property on the Measure macro.
Reference	The cell reference information. It appears in the following format: ■ `[r]:<Cell_Name>`: The reference flow based on a given cell. ■ `[c]:<Cell_Name>`: The reference flow based on match folding. ■ `[R]:<Clone_Files>`: The reference flow based on clone files. ■ `[C]:<Clone_Files>`: The reference flow based on match clone folding. ■ "`External Clone`": The reference flow based on an external clone file.
Routing Time	The time that the cell took to route. The time appears in the format: hh:mm:ss.
Scheduler Feedback	The job status of the cell defined by the scheduling software if it has been submitted to the job scheduler.
Script Type	The type of script that was run on the cell.
Start Time	The time (relative to Greenwich Mean Time - GMT) that the script was executed on the cell.
Target Width	The set target width for the cell. You can enter the target width for each cell directly into the table on the Cadabra window.
Width Delta	The cell width delta (i.e. the actual cell width minus the target cell width). A negative value indicates the target width has been met and passed.
Worst Diffusion Contact Growth	The worst percentage of diffusion contact growth. This property is only calculated if it is set in the secondaryQualityMetrics property on the Measure macro.

Cell Optimality

Cell optimality is the optimality of the final layout based on cell width. The optimality, which is determined during cell creation, can be:

Optimal	The cell width is at or below the target cell width. The cell row for an optimal cell is green.
Sub-Optimal	The cell width is above the target cell width. The cell row for a sub-optimal cell is blue.
Infeasible	There is no layout available due to an infeasible compaction. The cell row for an infeasible cell is red.

Important: You can sort cells according to optimality by clicking on the Cell Optimality column header in the Cadabra window. This allows you to quickly view any cells that require hand-editing.

Cell Status

The status of a cell is updated in the Cadabra window during cell creation. If a cell has not been worked on, the table entry for its status remains empty. The cell status can be:

Imported	The cell has been successfully imported.
Incomplete Import	The cell's original routing could not be preserved and requires hand-editing.
Unrouted	The structures in the netlist have been placed.
Placed	The cell has been successfully placed.
Routed	The cell has been fully routed.
Feasible	The cell has been successfully compacted.
Infeasible	The cell could not be compacted and requires hand-editing.

Completed	The cell has been completed and a final layout has been created.

Important: You can sort cells according to status by clicking on the Cell Status column header in the Cadabra window.

Job Status

When a cell is run using the scheduling software, the status of a job is updated automatically in the Cadabra window. It is the job status of the cell defined by Cadabra. A second status is provided in the Scheduler Feedback column. This column displays the job status of the cell as defined by the scheduling software. If a cell has not been submitted to the scheduler, the table entry remains empty. When a cell is run is distributed mode, the job status displayed in the user interface is the status of the last process to write to the library.

The job statuses in Cadabra can be:

Table 4 Job Statuses in Cadabra

Submitted	The initial status for submitted jobs. This status remains until the job starts.
Running	The job has been started on the remote machine. This status remains until the job completes or fails.
Finished	The job completed normally.
Failed	The job terminated abnormally.
Terminated	For an explanation of job status defined by the scheduling software, refer to the user documentation for the scheduler you are using.

Important: You can sort jobs according to status by clicking on the Job Status column header in the Cadabra window.

To add a cell property

Adding cell properties allows you to display the data available on your cells in the Cadabra window.

To add a cell property, do the following:

1. In the Cadabra window, select Properties > Add/Edit.
   The Add/Edit Properties dialog box appears.
2. Click New.
   The New Property dialog box appears.
3. Enter a descriptive name for the cell property in Name.

   Caution: The name must only be one word and it cannot be the same as the name of a built-in property.

4. Set the options (refer to Add/Edit Property Options on page 211).
5. Click OK.
   The New Property dialog box closes and the specified property is added to the library.
6. Click OK.
   The Add/Edit Properties dialog box closes.

   Note: The new property does not appear in the Cadabra window when you first create it. You must show the property (refer to To show or hide a cell property on page 211).

To edit a cell property

To edit a cell property, do the following:

1. In the Cadabra window, select Properties > Add/Edit.
   The Add/Edit Properties dialog box appears.
2. Select the property you would like to edit.
3. Click Edit.
   The Edit Property dialog box appears.
4. Set the options (refer to Add/Edit Property Options on page 211).

   Note: You cannot edit the Name of a property.

5. Click OK.
   The Edit Property dialog box closes and the selected property is updated.
6. Click OK.
   The Add/Edit Properties dialog box closes.

Add/Edit Property Options

Column Header: The title associated with the cell property to be displayed as the column header in the Cadabra window.

Default Value: The default value of a regular property. Each new cell created will initially have this value for this property.

To show or hide a cell property

Showing and hiding particular cell properties allows you to customize the table displayed in the Cadabra window.

To show or hide a cell property, do the following:

1. In the Cadabra window, select the tab of the library you would like to change the displayed properties for.
2. Select Properties > Show/Hide.
   The Show/Hide Properties dialog box appears.
3. Select a property from the Hide *or* Show listboxes.
4. Click > *or* < to move the selected property between the two listboxes.

   Important: You can also double-click on a property to move it from its current listbox to the other.

5. Click OK.
   The Show/Hide Properties dialog box closes and the properties listed in the Show listbox are displayed in the Cadabra window.

To save display settings

Saving the display settings allows you to save which properties are to be displayed in the main Cadabra window and their column widths.

To save display settings, do the following:

- In the Cadabra window, select Properties > Save Settings.
  The display settings are saved in the LibManagerPrefs.al file and are available the next time you open Cadabra.

To delete a cell property

You can only delete custom properties. However, you can hide built-in properties (refer to To show or hide a cell property on page 211).

To delete a cell property, do the following:

1. In the Cadabra window, select Properties > Add/Edit.
   The Add/Edit Properties dialog box appears.
2. Select the property you would like to delete.
3. Click Delete.
   A question dialog box appears to confirm the removal.
4. Click Yes.
   The specified cell property is removed.

To import cell properties

Importing properties updates the cell property values in the Cadabra window by reading a specified character delimited file (CDF). Only writable properties (such as target width or a custom writable property) can be imported.

To import cell properties, do the following:

1. In the Cadabra window, select Library > Import Cell Properties.
   The Import Cell Properties dialog box appears.
2. Enter a filename in Import from File *or* click Browse to open a file browser.

Note: The file must include the name of the cells and the properties to be imported. For an example, refer to Cell Properties Input File on page 213.

3. Set the options (refer to Import Cell Properties Options on page 213).
4. Click OK.
   The Import Cell Properties dialog box closes and the cell property values are imported and updated in the Cadabra window.

   Note: A lock is placed on the cells that you import properties for. If a lock already exists during import, then the properties for that cell are not imported.

Import Cell Properties Options

Delimiter: The character that is used to separate the property values in the file to be imported.

Read property names from file: All the properties named in the specified character delimited file (CDF) are imported.

Note: If you do not select Read property names from file, you can then specify exactly which cell properties you would like to import by moving property names between the two bottom listboxes. The cell properties listed in the right box are imported.

Cell Properties Input File

When importing cell properties, in addition to the property values, the input character delimited file (CDF) must include cell names.

The first line of the file should begin with Name (for the cell) followed by the name of each cell property. Each subsequent line should then start with the cell name and the property values for that cell.

Example

Name,targetWidth
and3x1,7

and2x1,8
ao21x1,9

To export cell properties

Exporting properties compiles the cell property values into a character delimited file (CDF). All the property values for all the cells are exported regardless of which properties are displayed in the Cadabra window.

To export cell properties, do the following:

1. In the Cadabra window, select Library > Export Cell Properties.
   The Export Cell Properties dialog box appears.
2. Enter a filename in Export to File *or* click Browse to open a file browser.
3. Set the option:

   Delimiter: The character to be used to separate the property values in the exported file.
4. Specify the cell properties you would like to export by moving property names between the two bottom listboxes. The cell properties listed in the right box are exported.
5. Click OK.
   The Export Cell Properties dialog box closes and the cell property values are exported and saved to the specified file and directory. If a directory is not specified, the file is saved to the CADABRAWORKING directory.

   Important: The exported properties can easily be used in any spreadsheet application.

5

Migrating Libraries and Creating Cells

Describes the various options available in Cadabra for migrating libraries and creating cells. Provides step-by-step instructions for migrating libraries and creating cells. Details the various tasks that you can perform with the Compaction Browser. Contains instructions on submitting jobs either to a local host or a scheduling software.

Cells can be automatically migrated and/or created in Cadabra by running one of the three processes: Migrate GDS, ATL (Automated Transistor Layout), or Migrate-ATL. *Migrate GDS* imports existing GDSII layouts, creating initial symbolic layouts, which are then compacted to meet the requirements of a new architecture. *ATL* places, routes and compacts cells, creating symbolic layouts, which meet the requirements of the set architecture. *Migrate-ATL* first runs Migrate GDS, then depending on your specifications, runs ATL. ATL can be set to run always or only on those cells that fail migration or are sub-optimal after migration.

Before migrating or creating cells, you must first initialize the library (refer to Initializing Libraries on page 163). Then, you can run Migrate GDS, ATL, or Migrate-ATL on the cells in the library. The entire processes can be run at once or their individual steps (i.e. Import, Place, Route, Compact, Finalize, and Export) can be run separately.

You must have read-write access to the cells you are running a process on. Cadabra will try to acquire read-write access to the cells you are running, but if a cell is in use by another user, it cannot be run.

Once a library has been created, you can view the results in the Cadabra window, Cell View window, or Cell Browser (refer to Viewing Results on page 311). Then, if necessary, you can hand-edit a cell in the Cell Edit window (refer to Hand-Editing Layouts on page 345).

Migration Prerequisites

Before a library can be migrated, certain conditions must first be met. Following are the prerequisites for migration in Cadabra.

Table 5 Migration Prerequisites

Migration Prerequisite	Description
Layer mapping file must be complete	The layer mapping file must be complete. If a GDSII layer, which is defined by two integers, is missing in the mapping file, all the objects (i.e. geometries and text labels) within the layer will be ignored. Consequently, the migration process will fail because either the netlists did not match or a fully routed symbolic layout could not be created.
Cells must be mapped to the correct source layouts	Each cell in the library must be mapped to the correct source layout. At the start of migration, the netlist of the source layout is extracted and compared to the netlist of the cell. If the two netlists do not match, the migration process fails. Refer to To map cells to source layouts on page 187.
Source layouts must have port annotations	The source layouts must have port annotations (i.e. text labels). Cadabra's migration process extract. s ports from the source layouts based on these annotations. Although Cadabra does allow customizations in which ports can be added in a different way, these other methods can be difficult.
Position of port annotations must indicate exact port positions	The position of port annotations must indicate the exact port positions, and not only which geometries are carrying ports. Otherwise, during migration, port extraction may fail or the ports may be created at incorrect positions. If ports are not positioned correctly, it will be difficult to snap the ports to the target IO grid without getting sub-optimal results.

Table 5 Migration Prerequisites

Migration Prerequisite	Description
Target MOSFET widths must be proportionate with target cell widths	The target MOSFET widths must be proportionate with the target cell widths. The migration process does not fold the geometries of MOSFETs provided by the source layouts. If the target MOSFET widths are too large with respect to the target cell width, the compaction component of migration will fail. If you open the Compaction Browser from the last compaction design point, you can view the critical path along the gates of the MOSFETs.
Target IO grid pitch must be consistent with the design rules	The target IO grid pitch must be consistent with the design rules (VIA dimension, METAL-OVER-VIA extension, METAL-TO-METAL separation, etc.). Refer to the IO grid pitch computing methods, Via-Via or Via-line (IO Grid Options).
Layer connectivity must be defined	For two intersecting layers to be considered connected, a layer connectivity rule must be set between the layers or the layers must have the same representative layer. If connectivity is not defined, there are disconnected shapes and the extracted netlist from the source layout displays more nets than there are in the target netlist. Consequently, the two netlists will not match and the migration process will fail.
Representative layers must be set for special layers	Representative layers must be set for special layers to ease device recognition during the import phase of the migration process. Otherwise, Cadabra may not be able to recognize certain devices. For example, if an architecture contains a POLYCOVER-TO-METAL1 contact and the layer mapping file associates POLY and POLYCOVER with the same GDSII layer, Cadabra will read the shapes on these layers as either POLY or POLYCOVER. In the case of POLY, if POLY is not set as a representative of POLYCOVER, then the importer will fail to recognize any POLYCOVER-TO-METAL1 contacts.

Table 5 Migration Prerequisites

Migration Prerequisite	Description
Ordered list of metal layers must be specified for pin layers	An ordered list of metal layers must be specified for each pin layer. If an annotation on the pin layer is contained by a shape on one of the specified metal layers, a port is created. The metal layers are considered in the specified order. In Cadabra, the list of metals can be set in AL using the data member, `textToPortLayerPolicy` on the LayoutImporter class.

To run Migrate-ATL

Running Migrate-ATL automatically runs Migrate GDS and ATL on the specified cells. Depending on the option specified, however, ATL may only be run on those cells that fail migration or are sub-optimal after migration. Before running Migrate-ATL, you must ensure the migration prerequisites have been met (refer to Migration Prerequisites on page 216).

To run Migrate-ATL, do the following:

1. In the Cadabra window, select the cell(s) to be migrated and created.
2. Select Cells > Run > Migrate-ATL.
   The Migrate-ATL dialog box appears.
3. Set the options (refer to Migrate-ATL Options on page 218).
4. Click OK.
   Migrate GDS, then ATL are run on the selected cell(s) and the Cell Browser and Cadabra window are updated with the results. The best layout is marked in the cell's design tree.

   Note: You can also run Migrate-ATL on a netlist design point by selecting Migrate-ATL from the netlist design point menu in the Cell Browser.

Migrate-ATL Options

Effort Level: The effort level, based on speed versus quality, in finding a solution.

Save feasible compaction data: The compaction data is saved.

Save between steps: The cell is saved after each phase.

Export: The best layout of the cell is exported in GDSII format. Layouts in PLib format and netlists can also be exported if the PLib and Netlist exporters are configured in the Export dialog box (refer to To export a cell, netlist, or clone on page 233). The GDSII formatted layouts are placed in the GDSOut path and the PLib formatted layouts are placed in the PLibOut path. The paths should be set during configuration. If the GDSOut or PLibOut paths are not set, the cells are exported to the directory from which Cadabra was started.

Enable constraint relaxation: Relaxation styles are respected.

Failed Migrate GDS: ATL is run on the cell if migration fails.

Sub-Optimal or Failed Migrate GDS: ATL is run on the cell if migration fails or results in a sub-optimal cell.

Always: ATL is always run on the cell.

Edit Cell/Layout Mapping: The Edit Cell-to-Layout Mapping dialog box appears. This dialog allows you to map cells to source layouts.

To run Migrate GDS

Running Migrate GDS automatically imports, compacts and finalizes existing GDSII layouts to meet the requirements of a new architecture. Before running Migrate GDS, you must ensure the migration prerequisites have been met (refer to Migration Prerequisites on page 216).

To run Migrate-GSDS, do the following:

1. In the Cadabra window, select the cell(s) to be migrated.
2. Select Cells > Run > Migrate GDS.
   The Migrate GDS dialog box appears.
3. Set the options (refer to Migrate GDS Options on page 220).
4. Click OK.
   Migration is run on the selected cell(s) and the Cell Browser and Cadabra window are updated with the results. The best layout is marked in the cell's design tree.

Note: You can also run Migrate GDS on a netlist design point by selecting Migrate GDS from the netlist design point menu in the Cell Browser.

Migrate GDS Options

Effort Level: The effort level for the compaction step, based on speed versus quality, in finding a solution.

Save feasible compaction data: The compaction data is saved.

Save between steps: The cell is saved after each step of the Migrate GDS process (i.e. import and compact).

Export: The best layout of the cell is exported in GDSII format. Layouts in PLib format and netlists can also be exported if the PLib and Netlist exporters are configured in the Export dialog box (refer to To export a cell, netlist, or clone on page 233). The GDSII formatted layouts are placed in the GDSOut path and the PLib formatted layouts are placed in the PLibOut path. The paths should be set during configuration. If the GDSOut or PLibOut paths are not set, the cells are exported to the directory from which Cadabra was started.

Use Preserve: The compaction style preservation options, specified in the Architecture Builder or Cell Modifier, are applied during compaction. (Refer to Preservation Options tab on page 147.)

Enable constraint relaxation: Relaxation styles are respected.

Edit Cell/Layout Map: The Edit Cell-to-Layout Mapping dialog box appears. This dialog allows you to map cells to source layouts.

To run ATL

Running ATL automatically creates cell layouts. The best layout is marked in the design tree and can be exported. A few of the generated cells may be sub-optimal and might require some hand-editing.

To run ATL, do the following:

1. In the Cadabra window, select the cell(s) to be created.

2. Select Cells > Run > ATL.
   The ATL dialog box appears.
3. Set the options (refer to ATL Options on page 221).
4. Click OK.
   ATL is run on the selected cell(s) and the Cell Browser and Cadabra window are updated with the results. The best layout is marked in the cell's design tree.

   Note: You can also run ATL on a netlist design point by selecting ATL from the netlist design point menu in the Cell Browser.

ATL Options

Effort Level: The effort level, based on speed versus quality, in finding a solution.

Use target width: The target width is considered when running ATL.

Save feasible compaction data: The compaction data is saved.

Save between steps: The cell is saved after each step in the ATL process (i.e. place, route, compact).

Export: The best layout of the cell is exported in GDSII format. Layouts in PLib format and netlists can also be exported if the PLib and Netlist exporters are configured in the Export dialog box (refer to To export a cell, netlist, or clone on page 233). The GDSII formatted layouts are placed in the GDSOut path and the PLib formatted layouts are placed in the PLibOut path. The paths should be set during configuration. If the `GDSOut` or `PLibOut` paths are not set, the cells are exported to the directory from which Cadabra was started.

Distribute: Select this checkbox to enable distributed processing.

Default: Select this checkbox to terminate jobs processing larger placements.

Complete All Branches: Select this checkbox to route and compact all tagged placements

Stop At First Result: Select this checkbox if you want the macro to terminate all jobs for the cell as soon as the number of layouts generated equals the maximum number of final layouts.

Number of Processed Placements: Specify the required number of processed placements.

Maximum Number of Final Layouts: Specify the maximum number of final layouts required.

Note: In the interface, the Distribute, Number of Processed Placements, and Maximum Number of Final Layouts options are only available when this dialog box is opened from the job scheduler.

To run Import

Importing a cell creates an initial symbolic layout from an existing GDSII layout using the cell's target netlist. Before importing a cell, you must ensure the migration prerequisites have been met (refer to Migration Prerequisites on page 216).

To run Import, do the following:

1. In the Cadabra window, select the cell(s) to be imported.
2. Select Cells > Run > Import.
   The Import dialog box appears.
3. Set the options (refer to Import Options on page 222).
4. Click OK.
   Import is run on the selected cell(s) and the Cell Browser and Cadabra window are updated with the results.

   Note: You can also run Import on a netlist design point by selecting Import from the netlist design point menu in the Cell Browser.

   Caution: If the output design point is marked with an Incomplete Import tag after import, this means the original routing could not be preserved and the cell requires hand-editing.

Import Options

Save after import: The cell is saved after import.

Edit Cell/Layout Mapping: The Edit Cell-to-Layout Mapping dialog box appears. This dialog allows you to map cells to source layouts.

To place a cell

Placing a cell fits netlist devices into the architecture. If placement selection customizations are required, they are specified in the customFilterDesignPoints.al File, customAddSizeBasedCost.al File, or customAddRoutingBasedCost.al File files which are located in the $CADABRAPROJECT/Macros/Placement directory. Cadabra automatically loads the file(s) when running Place. After placement, the cell is ready for routing.

To place a cell, do the following:

1. In the Cadabra window, select the cell(s) to be placed.
2. Select Cells > Run > Place.
   The Place dialog box appears.
3. Set the options (refer to Place Options on page 224).
4. Click OK.
   Placement is run on the selected cell(s) and the Cell Browser and Cadabra window are updated with the results.

   Note: You can also run Place on a netlist design point by selecting Place from the netlist design point menu in the Cell Browser.

Place Options

Place Option	Description	
Effort Level	Overview	The effort level, based on speed versus quality, in finding a solution.
Max Number of Results	Overview	The maximum number of different placements to find. By default, one solution is generated. The number of placements requested may not be met for the more simple cells, if that many placement solutions are not possible.
	Why set this option?	Generating several placement solutions allows you to compare different results. This can be valuable when exploring aggressive architectures that can have challenging routing.
	You must also set...	The Effort Level. Set this to the High Quality end of the scale to consider the most solutions possible.
Save after placement	Overview	The cell is saved after placement.

Customizing Options for Placing Cells

You can customize the placement of cells by configuring the following files:

customFilterDesignPoints.al File

The customFilterDesignPoints.al file allows you to filter design points for prospective placement selection when you run ATL or Place. This file is located in the $CADABRAPROJECT/Macros/Placement directory.

The function in the customFilterDesignPoints.al file must take a list of design point as its argument and return a filtered list of design points that can be applied to a design step.

For example, if you want to exclude placements with MOSFET islands larger than four, add the following code to the customization section of the file:

```
auto sdb = dp->symbolicDB;
if ( sdb->numMosfetIslands > 4 ) {
continue; //this code loops
}
```

customAddSizeBasedCost.al File

The customAddSizeBasedCost.al file allows you to calculate additional values for size-based placement costs when you run ATL or Place. This file is located in the $CADABRAPROJECT/Macros/Placement directory.

The function in the customAddSizeBasedCost.al file takes the following as arguments:

dp: a design point to estimate.

dpOriginalCost: the original cost of dp.

minCost: a minimal value of costs of design points.

maxCost: a maximal value of costs of design points.

The return value is the additional size-based cost that can be applied to a design step.

For example, to penalize the number of MOSFET islands, add the following code to the customization section of the file:

```
auto sdb = dp->symbolicDB;
auto numIslands = sdb->numMosfetIslands;
additionalCost = (numIslands/20.0)*minCost;
```

customAddRoutingBasedCost.al File

The customAddRoutingBasedCost.al file allows you to calculate additional values for routing-based placement costs when you run ATL or Place. This file is located in the $CADABRAPROJECT/Macros/Placement directory.

The function in the customAddRoutingBasedCost.al file takes the following as arguments:

dp: a design point to estimate.

dpOriginalCost: the original cost of dp.

minCost: a minimal value of costs of design points.

maxCost: a maximal value of costs of design points.

The return value is the additional routing-based cost that can be applied to a design step.

For example, to penalize the number of MOSFET islands, add the following code to the customization section of the file:

```
auto sdb = dp->symbolicDB;
auto numIslands = sdb->numMosfetIslands;
additionalCost = (numIslands/20.0)*minCost;
```

To route a cell

Routing a cell creates all the required electrical connections between the cell's devices and, if required, the ports and diodes are added. If routing penalties are required, they are specified in the cellRouterPenalties.al file which is located in the `$CADABRAPROJECT/Macros/Routing directory`. Cadabra automatically loads the file when running Route. After routing, the cell is ready for compaction.

To route a cell, do the following:

1. In the Cadabra window, select the cell(s) to be routed.
2. Select Cells > Run > Route.
   The Route dialog box appears.
3. Set the options (refer to Route Options on page 227).
4. Click OK.
   Routing is run on the selected cell(s) and the Cell Browser and Cadabra window are updated with the results.

   Note: You can also run Route on any unrouted or partially routed design point by selecting Route from the design point menu in the Cell Browser.

Route Options

Effort Level: The effort level, based on speed versus quality, in finding a solution.

Adjust MOSFET spacing before routing: The spacing between MOSFETs is adjusted to better reflect the availability of routing resources. MOSFET spacing is adjusted during automated placement, however, if you have manually edited the placement you are routing, you should select this option. This prevents the router from misusing any extra space.

Save between steps: The cell is saved after each step in the route process.

Enable route-compact feedback: Select this checkbox to enable route-compact feedback.

Complete cell: The cell automatically finishes the flow after route and compact is completed.

Use target width: The target width is considered when running route and compact.

Save feasible compaction data: The compaction data is saved.

Export: The best layout of the cell is exported in GDSII format. Layouts in PLib format and netlists can also be exported if the PLib and Netlist exporters are configured in the Export dialog box (refer to To export a cell, netlist, or clone on page 233). The GDSII formatted layouts are placed in the `GDSOut` path and the PLib formatted layouts are placed in the `PLibOut` path. The paths should be set during configuration. If the `GDSOut` or `PLibOut` paths are not set, the cells are exported to the directory from which Cadabra was started. This option can only be set if `completeATL` is set to on.

Distribute: Select this checkbox to enable distributed processing.

Default: Select this checkbox to terminate jobs processing larger placements.

Complete All Branches: Select this checkbox to route and compact all tagged placements

Stop At First Result: Select this checkbox if you want the macro to terminate all jobs for the cell as soon as the number of layouts generated equals the maximum number of final layouts.

Customizing Routing of Cells

You can configure routing of cells by configuring the following file:

cellRouterPenalties.al File

The `cellRouterPenalties.al` file allows you to turn on and off built-in routing penalties and define custom routing penalties, which are loaded when you run ATL or Route. This file is located in the `$CADABRAPROJECT/Macros/Routing` directory.

For built-in routing penalties, the `cellRouterPenalties.al` file contains flags that specify whether or not to use the penalties. If the flag is set to 1, the penalty is used. If it is set to 0, the penalty is ignored. The default value for all of the built-in routing penalties is 0.

For custom routing penalties, the function in the `cellRouterPenalties.al` file must take a design point as its argument and return a list of penalties in a format that can be applied to a design step.

Following is an example:

```
{
auto cellRouterPenalties = func( designPoint ) {
// Flags saying whether to use each of the built-in penalties.
// For each built-in penalty being used, the parameters should
be    // set in the corresponding section below:
    auto doTypeXPenalties = 0;
    auto doTypeYPenalties = 0;
    auto doTypeZPenalties = 0;

    // initialize the list of penalties
    auto penalties = list();

    // Built-in type X Penalties
    if (doTypeXPenalties) {
        auto typeXPenaltiesFunc = loadFromPath(
          ``Routing/Penalties/typeXPenalties'', 0, ``macros'' );
        auto metalWireName = ``Metal 1 Wire'';
        auto metalWirePenalty = 100;
        auto typeXPenalties = typeXPenaltiesFunc(
            designPoint,
            metalWireName,
            metalWirePenalty );
        penalties->merge( typeXPenalties );
    }

    // Built-in type Y Penalties
    ....etc...

    // Built-in type Z Penalties
    ....etc...

    // User Custom Penalties
    // Try to prevent the IO Port device from being placed near
    // the left and right edges of the cell

    // Get the symbolicDB.
    auto symbolicDB = designPoint->symbolicDB;

    // Get the physical spec and IO Grid.
    auto physicalSpec = symbolicDB->physicalSpec;
    auto ioGrid = physicalSpec->ioGrid;

    // Get the boundary shape.
    auto boundary = symbolicDB->boundary;

   // Create penalties that restrict the port devices from
    // being used along the left/right edges of the cell.

    // Define the cost.
```

```
    auto cost = 20;

    // Define the port template name.
    auto portTemplateName = "IO Port";

   // Define the offset from the left/right side of the cell.
   // The offset should be one horizontal IO Grid pitch.
    auto offset = ioGrid[0];

    // Define the left/right regions of the cell.
    auto leftRegion =
    list( boundary->minX, boundary->minY,
          boundary->minX + offset, boundary->maxY );
    auto rightRegion =
    list( boundary->maxX - offset, boundary->minY,
          boundary->maxX, boundary->maxY );
    // Add the penalties.
    penalties->append(
    list( cost, portTemplateName, leftRegion, "@port",
          "@allScenarios" ),
    list( cost, portTemplateName, rightRegion, "@port",
          "@allScenarios" ) );

    // return the list of penalties
    return penalties;
};
//Use this to make sure the function is returned
//when the file is loaded.

cellRouterPenalties;
}
```

To compact a cell

Compacting a cell removes all unnecessary space, reducing cell width to a minimum. The cell can then be finalized and exported.

To compact a cell, do the following:

1. In the Cadabra window, select the cell(s) to be compacted.
2. Select Cells > Run > Compact.
   The Compact dialog box appears.
3. Set the options (refer to Compact Options on page 231).

4. Click OK.
   Compaction is run on the selected cell(s) and the Cell Browser and Cadabra window are updated with the results.

   Note: You can also run Compact on a symbolic layout design point by selecting Compact from the symbolic layout design point menu in the Cell Browser.

   Caution: If the Cell Status is Infeasible after compaction, this means the cell could not be compacted properly and requires hand-editing.

Compact Options

Effort Level: The effort level, based on speed versus quality, in finding a solution.

Use target width: The target width is considered when running compact.

Use 1To1 migration: Use this option when there is a high degree of similarity in the design rules of the source and target layouts; cell migration in this situation involves minor changes. Turning on this option reduces the layout flexibility for the compactor (when using the migration macro).

Save after compaction: The cell is saved after compaction.

Save feasible compaction data: The compaction data is saved.

Enable constraint relaxation: Relaxation styles are respected.

Complete Cell: The cell automatically finishes the flow after compaction is completed.

Export: The best layout of the cell is exported in GDSII format. Layouts in PLib format and netlists can also be exported if the PLib and Netlist exporters are configured in the Export dialog box (refer to To export a cell, netlist, or clone on page 233). The GDSII formatted layouts are placed in the `GDSOut` path and the PLib formatted layouts are placed in the `PLibOut` path. The paths should be set during configuration. If the GDSOut or PLibOut paths are not set, the cells are exported to the directory from which Cadabra was started. This option can only be set if *Complete Cell* is selected.

Use Preserve: The compaction style preservation options, specified in the Architecture Builder or Cell Modifier, are applied during compaction. (Refer to Preservation Options tab on page 147.)

Initial layout tag: The initial layout design point to be preserved is marked by the specified tag in the Cell Browser. The default tag is “Completed Import”.

To finalize a layout

Finalizing a layout prepares the cell for export. You can only finalize cells that have generated a feasible compaction.

To finalize a layout, do the following:

1. In the Cadabra window, select the cell(s) to be finalized.
2. Select Cells > Run > Finalize Layout.
   The Finalize Layout dialog box appears.
3. Set the options (refer to Finalize Options on page 232).
4. Click OK.
   A final layout is added to the design tree.

   Note: You can also run Finalize on symbolic layout design points by selecting Finalize Layout from the design point menu of a symbolic layout design point in the Cell Browser.

Finalize Options

Save after finalization: The cell is saved after layout is finalized.

Export: The best layout of the cell is exported in GDSII format. Layouts in PLib format and netlists can also be exported if the PLib and Netlist exporters are configured in the Export dialog box (refer to To export a cell, netlist, or clone on page 233). The GDSII formatted layouts are placed in the `GDSOut` path and the PLib formatted layouts are placed in the `PLibOut` path. The paths should be set during configuration. If the `GDSOut` or `PLibOut` paths are not set, the cells are exported to the directory from which Cadabra was started.

To measure cell optimality

Measuring a cell's optimality checks its width. If the width is at or below the target cell width, the cell is optimal. Otherwise, the cell is sub-optimal. A cell can only be measured once its layout has been finalized.

To measure a cell's optimality, do the following:

1. In the Cadabra window, select the cell(s) to be measured.
2. Select Cells > Run > Measure.
   The Cell Optimality is updated in the Cadabra window.

   Note: Measure may be run from the Cell Browser by clicking and holding on a layout design point and selecting Measure. Measure may also be run from the Cell View window background menu.

To export a cell, netlist, or clone

Exporting a cell converts the cell's best layout (indicated by the cell marker) to the specified format. Cadabra supports GDSII, Milkyway, PLib, and Clone export file formats. Multiple cells can be exported to a single GDSII file (refer to To export multiple cells to a single GDSII file on page 235). A cell can also be exported from the Cell Browser window, in which case, you can export the layout of your choice (refer to To export from the Cell Browser on page 238).

The GDSOut and/or PLibOut path(s) must be defined during configuration when exporting in GDSII and/or PLib formats.

You can also export a netlist from a specified layout in either SPICE or Application Language (AL) format.

While exporting, each shape and text label has the ability to contain properties, similar to most other AL objects. These properties are restricted to strings and the associated values are restricted to those of simple AL types, as follows:

- `AlInt`
- `AlReal`
- `AlString`

- `AlList`
- `AlObject`

Any shape that is modified by any shape operations that result in creation a new shape loses the AL properties that were previously set on it.

Note: Currently, the only shape manipulation that does not create new shape objects is compaction.

Due to restrictions on GDSII data, properties and values can only exist in the format of:

- Property Name: `int16` (also known as `PROPATTR`)

  Therefore, during export, property names are converted to integer values. If the property name cannot be converted to an integer, then it is converted to 0.

- Property Value: `string` (also known as `PROPVALUE`)

  Only those property values that are strings are converted. If the property value is not a string, then it is converted to 1.

Note: Milkyway does not support shape properties. So, shape properties-related information is ignored in the final output. However, if shape properties exist, Cadabra issues warnings that the information is not transferred to the final output.

In the Cadabra window, select the cell(s) you would like to export, and do the following:

1. Select Cells > Run > Export Layout.

   Result: The Export dialog box appears.

2. Select the Exporters you would like to use and move them into the Used column using the “<“ “>” buttons.
3. Select the exporter to configure.

   Result: The Configure Exporter button is enabled.

4. Click Configure Exporter.

   Result: The Exporter Configuration dialog box appears for the exporter you have selected.

5. Set the options (refer to Export Options on page 236).
6. Click OK.

Result: The Exporter Configuration dialog box closes.

7. Click OK on the Export dialog box.

   Result: The Export dialog box closes and the layout(s) with the cell marker are exported in the selected format.

   Explanation: If you click Save As Defaults, the specified settings are saved as the default for this dialog as well as for when you run Migrate GDS, ATL, or Migrate-ATL.

To export multiple cells to a single GDSII file

If you select multiple cells in the Cadabra window for export, the Export dialog allows you to merge the resulting GDSII files into one single GDSII file.

To export multiple cells to a single GDSII file, do the following:

1. In the Cadabra window, select the cells you would like to export.
2. Select Cells > Run > Export Layout.
   The Export dialog box appears.
3. Select GDSII and move it into the Used column using the “<“ “>” buttons.
4. Select GDSII in the Used column.
   The Configure Exporter button is enabled.
5. Click Configure Exporter.
   The Exporter Configuration dialog box appears for the GDSII exporter.
6. Set the options (refer to Export Options on page 236).

   Note: Ensure that the Combine outputs option is selected and that an Output directory is defined.

7. Click OK.
   The Exporter Configuration dialog box closes.
8. Click OK on the Export dialog box.
   The selected layouts are exported to a single GDSII file.

   Note: This task can only be performed from the Cadabra window. You cannot merge multiple GDSII files to a single file when exporting from the Cell Browser or when submitting jobs to either a job scheduler or a localhost to run in the background.

Note: If you click Save As Defaults, the specified settings are saved as the default for this dialog as well as for when you run Migrate GDS, ATL, or Migrate-ATL.

Export Options

The following export options are available in the interface:

Clone

Directory: The directory in which to place the cloned layout(s). Click Browse to open a file browser.

Naming Scheme: The naming format for the cloned layout(s). The possible formats include cell name only or cell name and design point id.

Extension: The file extension to use.

Use default extension: This flag indicates whether or not to use the default file extension for the exported clone file(s).

GDSII

Layer map file: The layer map file name or click Browse to open a file browser. This file contains the mappings between the layer names in the technology and the layer numbers in the GDSII layouts.

Directory: The directory in which to place the exported layout(s). Click Browse to open a file browser.

Naming Scheme: The naming format for the exported layout(s). The possible formats include cell name only or cell name and design point id.

Extension: The file extension to use.

Use default extension: This flag indicates whether or not to use the default file extension for the exported GDSII file(s).

Combine outputs: The flag indicating whether or not to combine the GDSII files into a single GDSII file. This option is only available if multiple cells are selected in the Cadabra window.

Output: The directory in which to place the GDSII file. Click Browse to open a file browser. This option is only available if multiple cells are selected in the Cadabra window and *combine outputs* is selected.

OpenAccess

Layer map file: Type the layer map file name or click Browse to open a file browser. This file contains the mappings between the layer names in the technology and the layer numbers in the OpenAccess library. Layer matching is used if this file is not available at the time of export.

Export Design: Type the location of the OpenAccess design or click Browse to open a file browser and navigate to the OpenAccess design.

Export Cell Name: Type the name of the cell that you want to export.

Milkyway

Layer map file: The layer map file name or click Browse to open a file browser. This file contains the mappings between the layer names in the technology and the layer numbers in the Milkyway library. Layer matching is used if this file is not available at the time of export.

Cell Library: The directory in which to place the exported Milkyway library. Click Browse to open a file browser. You must provide a directory name.

Netlist

Netlist Type: The type of netlist to export, either Spice or AL (Application Language).

Directory: The directory in which to place the exported netlist(s). Click Browse to open a file browser.

Naming Scheme: The format for the exported netlist(s). The possible formats include cell name only or cell name and design point id.

Extension: The file extension to use.

Use default extension: This flag indicates whether or not to use the default file extension for the exported nelist file(s).

PLib

Directory: The directory in which to place the exported layout(s). Click Browse to open a file browser.

Naming Scheme: The naming format for the exported layout(s). The possible formats include cell name only or cell name and design point id.

Extension: The file extension to use.

Use default extension: This flag indicates whether or not to use the default file extension for the exported PLib file(s).

Note: Different options are available if you export from the Cell Browser or the Cell View window.

To export from the Cell Browser

Exporting a cell from the Cell Browser converts a selected layout design point to the specified format. Cadabra supports Clone, GDSII, Netlist, Milkyway and PLib export file formats. It is also possible to export a clone of a placed or routed design point from the cell browser.

The GDSOut and/or PLibOut path(s) must be defined during configuration when exporting in GDSII and/or PLib formats.

You can also export a netlist from a specified layout in either SPICE or AL (Application Language) format.

In the Cadabra window, select the cell you would like to export, and do the following:

1. Select Cells > Open.
   The Cell Browser for the selected cell appears with the best layout identified by the cell marker.
2. Click on the design point you would like to export.
   The design point menu appears.
3. Select Export.
   The Export dialog box appears.
4. Select the Exporters you would like to use and move them into the Used column using the “<“ “>” buttons.

5. Select the exporter to configure.
   The Configure Exporter button is enabled.
6. Click Configure Exporter.
   The Exporter Configuration dialog box appears for the exporter you have selected.
7. Set the available options (refer to Export from the Cell Browser Options on page 239).
8. Click OK.
   The Exporter Configuration dialog box closes.
9. Click OK on the Export dialog box.
   The Export dialog box closes and the layout is exported to the specified format.

   Note: You can also export the layout from the Cell View window by selecting Design Point > Export.

Export from the Cell Browser Options

The following options are available for exporting from the Cell Browser interface:

Clone

Export File: The directory path and file name for the cloned layout. Click Browse to open a file browser.

GDSII

Layer map file: The layer map file name or click Browse to open a file browser. This file contains the mappings between the layer names in the technology and the layer numbers in the GDSII layouts.

Export File: The directory path and file name for the exported layout. Click Browse to open a file browser.

OpenAccess

Layer map file: Type the layer map file name or click Browse to open a file browser. This file contains the mappings between the layer names in the technology and the layer numbers in the OpenAccess library. Layer matching is used if this file is not available at the time of export.

Export Design: Type the location of the OpenAccess design or click Browse to open a file browser and navigate to the OpenAccess design.

Export Cell Name: Type the name of the cell that you want to export.

Milkyway

Layer map file: The layer map file name or click Browse to open a file browser. This file contains the mappings between the layer names in the technology and the layer numbers in the Milkyway library. Layer matching is used if this file is not available at the time of export.

Export Library: The directory in which to place the exported Milkyway library. Click Browse to open a file browser. You must provide a directory name.

Export Cell Name: The cell name for the layout.

Netlist

Netlist Type: The type of netlist to export, either Spice or AL (Application Language).

Export File: The directory path and file name for the exported layout. Click Browse to open a file browser.

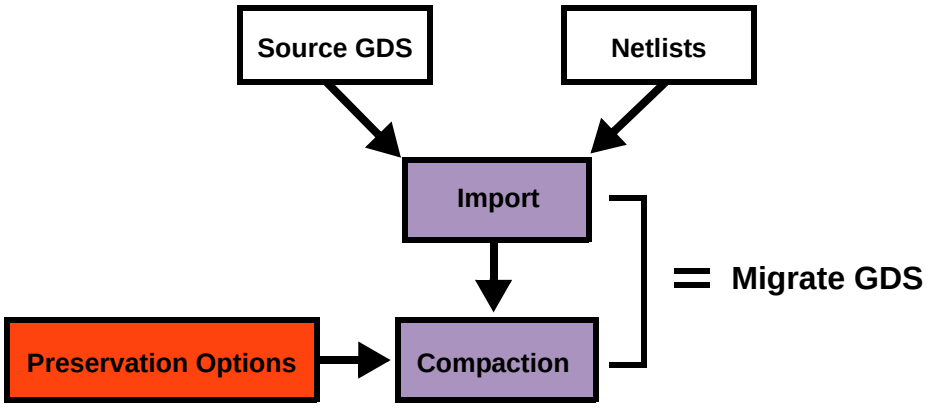
PLib

Export File: The directory path and file name for the exported layout. Click Browse to open a file browser.

ECO Migration

Engineering Change Order (ECO) migration is the ability to migrate an existing GDSII layout due to a minor design rule or architecture change while preserving specific aspects of the existing layout. For example, the ECO migration allows you to migrate a GDSII layout due to a design rule change in POLY while maintaining the existing horizontal METAL1 shapes of the original layout.

The ECO migration flow is as follows:



This flow incorporates the existing Migrate GDS flow with the ability to add preservation options on the compaction step.

Preservation options can be added to compaction from:

- The Compaction Style dialog box in the Architecture Builder. When using this approach, the preservation options are applied to all of the cells that are run.

  Refer to Compaction Style Options on page 144.

- The Compaction Style dialog box for Cell Modifiers. When using this approach, the preservation options are applied to only the cells that the modifier is applied to.

  Refer to To create a cell modifier on page 193.

- The Compaction dialog box when running Advanced > Cell Compact on an individual design point from the Cell Browser.

  Refer to Compaction Options on page 274.

Note: These approaches only allow for layer based and template based preservations only. It is possible to do area based, device based, shape based, edge based, and design rule based preservation from the `CellCompactor` class.

In order for the compactor to take advantage of the preservation options set in the Architecture Builder or Cell Modifiers you must tell the compactor to use preservation. This is done by selecting the Use Preserve option on either the Migrate GDS dialog box (refer to Migrate GDS Options on page 220) or the Compact dialog box (refer to Compact Options on page 231) before running Migrate GDS or Compaction on the cells in your library. When using the Compact dialog box, you must also specify the tag for the Initial Design Point to be preserved.

If you are running advanced compaction on an individual design point from the Cell Browser, the selected preservation options are run directly on the cell from the selected design point, which should be the initial design point that contains the layout aspects that you want to preserve.

Advanced Operations

Advanced operations are a collection of design steps which can be used by the more experienced users of Cadabra. Design steps allow you to do more in-depth and specific modifications to your libraries, but they require a deeper understanding of Cadabra. In addition, AL programming is sometimes necessary. For more information, refer to the AL Documentation.

Design Steps operate on a certain type of design point and create another design point (possibly a different type) on the design tree. Different types of design points have different design steps available. There are options on design steps that affect each other, so check for interactions between them.

The following design steps can be run on the appropriate design point in Cadabra:

Import Layout	Cell Edit
Fold MOSFETs	Align MOSFETs
Hierarchy Extraction	Generate Compaction Geometries
Select Configuration	Cell Compact
Edit Configuration	Generate Routing Geometries
Fold Tiles	Generate Layout
Merge Tiles	Migrate Design Tree
Place Tiles	
Optimize Placement	

There are also a number of custom design steps that may be run on design points in Cadabra. The availability of custom design steps is dependent on your architecture setup. However, you can also explicitly register custom design steps by customizing your architecture.al file (refer to Customizing an Architecture on page 161).

Post-Import Steps	**Final Layout Steps**
Connect Tie Rail	Add Layout Ties
	Add Implants
Edit Design Steps	Adjust Overlapping Tie Diffusions
Update Boundary	Fill Notches
	Merge Shapes
Pre-Compaction Steps	Path Shapes
Add Abutments	Reshape Gates
Add Multiple Gate Bends	Text Annotation
Jog At Gates	
Jog Wires Around Contacts	
Match MOSFET Sizes	
Optimize Horizontal Wires	
Selectively Pregrow Diffusion	

To import a layout

Importing a layout creates a symbolic layout from an existing GDSII file. The GDSII file is connected to a shape database which can be saved and imported in subsequent imports instead of a GDSII file. A mapping file which references the layer numbers in the GDSII file to the layer names in the technology of the Cadabra library is needed to connect the GDSII file to a shape database.

To import a layout, do the following:

1. In the Cell Browser, click and hold on the netlist design point.
   The design point menu appears.
2. Select Advanced > Import Layout.
   The Import Layout dialog box appears.
3. Select either GDSII or ShapeDB depending on the type of file being used to import the layout.
4. Enter the name of the GDSII layout or shape database file in Filename or click Browse to open a file browser.
5. Set the options (refer to Import Layout Options on page 244).
6. Click OK.
   The layout is imported and a symbolic layout design point is added to the design tree.

Import Layout Options

GDSII: This specifies that a GDSII layout and mapping file are to be used to import the layout.

ShapeDB: This specifies that a shape database file is to be used to import the layout.

Filename: The GDSII or shape database file to be used during import.

Mapping file: The file containing the mappings between the layer names in use in Cadabra and the layer numbers in the GDSII layouts. If there are multiple mappings for the same GDSII layer number in the file, then the last one provided is used. The file must list the layer name first, then the layer numbers, as shown in the example below:

```
N-WELL       2     0
N-IMPLANT    8     0
...
```

Units per micron: The number of GDSII file database units per micron. The default is 0.001.

Top level structure: The name of the top-level structure to be used if multiple structures are included in the GDSII file.

Cluster aligned contacts: Aligned contacts are merged in the resulting symbolic layout (providing no design rules are violated by the merge).

Virtual-Short Equality Tolerance: The tolerance for inserting a virtual short between the source-drain of two MOSFETs.

To fold MOSFETs

Folding MOSFETs converts a larger transistor into groups of smaller parallel-connected transistors. The smaller group of transistors has the same effective width and length of the larger transistor. This design step is useful for cells with height restrictions. It also allows some placement optimization techniques (such as stacking) to be more effective.

To fold MOSFETs, do the following:

1. In the Cell Browser, click and hold on the netlist design point.
   The design point menu appears.
2. Select Advanced > Fold MOSFETs.
   The Fold MOSFETs dialog box appears.
3. Set the Selector values to specify the MOSFETs this policy can act on. You can choose as many selectors as required. (Refer to Selectors on page 247.)

   Note: Using more than one selector defines multiple groups of MOSFETs, not an intersection of groups. For example, if one selector specifies all N-type MOSFETs and another selector specifies all MOSFETs whose width exceeds 5 microns, the selected MOSFETs will include all N-MOSFETs as well as those P-MOSFETs wider than 5 microns.

4. Set the Operator values to specify the actions in this policy. You can only choose one operator per policy. (Refer to Operators on page 248.)
5. Click Add.
   A folding policy is added.
6. Repeat steps 3-5 until all the required policies have been added.
7. Click OK.
   The netlist is folded. A modified netlist design point is added to the design tree.

   Note: Each policy describes a folding operation that will be performed. Policies are performed in the order in which they appear in the listbox. You can click Move Up and Move Down to reorder the policies.

Fold MOSFETs Options

The following options are available in the interface for folding MOSFETs:

Selectors

Option	Description	
MOSFET Type	Overview	MOSFETs are selected based on type.
MOSFET Width	Overview	MOSFETs are selected based on width.
MOSFET Length	Overview	MOSFETs are selected based on length.
MOSFET Name	Overview	MOSFETs are selected by name.
Select	Overview	The names of the MOSFETs to select.
Regular Expression	Overview	A regular expression used to select MOSFET names. Regular expressions can be used to collect all names that match a given rule. In a cell that has a large number of transistors, a regular expression quickly collects all the names that begin with, end with, or contain the given characters.

	Example	A cell contains these transistors:
		`mn0 mn1 mn2@1 mn2@2 mn2@3 mn3`
		`mp0 mp1 mp2 mp3@1 mp3@2`
		■ To collect all of the folded transistors, use: @*. This expression looks for the @ symbol (that designates folded transistors) anywhere in the name.
		■ To collect of the transistors that derive from the folding of mn2, use: mn2@*. This expression looks for the @ symbol preceded by an mn2.

MOSFET template	Overview	MOSFETs are selected based on templates.

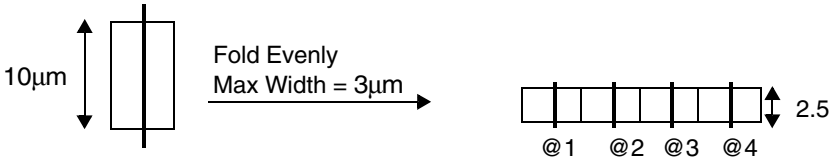
Operators

Option	Description	
Fold	Overview	MOSFETs are divided into smaller pieces. Folding reduces the size of MOSFETs to be no larger than the specified maximum width. MOSFETs can be folded evenly (to create MOSFETs of approximately the same size) or folded maximally (to create MOSFETs of a given size). Folding generates one principal and one or more secondary MOSFETs. When unfolding or resizing folded MOSFETs, only MOSFETs deriving from the same folding operation can be used. Refer to Principal vs. Secondary MOSFETs on page 253 for more details on these restrictions. Folded MOSFETs are automatically named using the original MOSFET name, followed by an asterisk (@) and a numeral.
Max Width	Overview	The maximum width for folded MOSFETs.

Option	Description	
Fold Evenly	Overview	MOSFETs of equal width are created. Their sizes do not exceed the maximum width.
	Why set this option?	Folding evenly allows you to have approximately equal sized MOSFETs.

Example

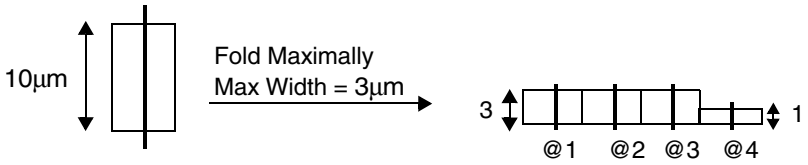
If a 10 micron MOSFET is folded evenly using a maximum width of 3 microns, four MOSFETs of 2.5 micron width will be generated.

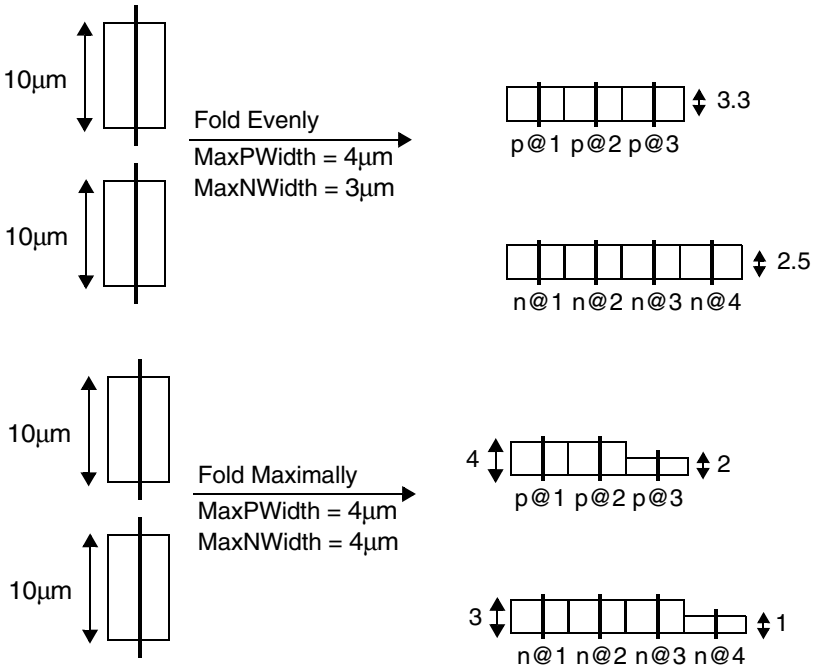


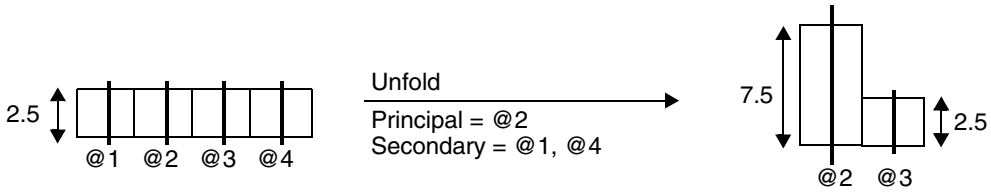
Folded MOSFETs are automatically named using the original MOSFET name, followed by

an asterisk (@) and a numeral.

Option	Description	
Fold Maximally	Overview	As many MOSFETs of the maximum width as possible are created. Any leftover width creates an extra MOSFET (like a remainder in division). The additional MOSFET may be smaller than the minimum allowable dimension for a MOSFET. If this occurs, the MOSFET will be increased to the minimum width. The other folded MOSFETs are resized accordingly.
	Why set this option?	Folding maximally generates extra space locally in the cell by creating an extra MOSFET. This space can be used for placing diodes, taps or for other specific routing purposes.
	Example	If a 10 micron MOSFET is folded maximally using a maximum width of 3 microns, three MOSFETs of 3 micron width will be generated, along with one MOSFET of 1 micron width. (Folded MOSFETs are annotated by a trailing @ and a numeral.)
Remove Virtual Shots	Overview	Balanced internal nets (that is, virtual shorts) are removed. Both the folding and paired folding operations allow the removal of virtual shorts. A virtual short cannot exist at an output node. Folded MOSFETs which have had their virtual shorts removed cannot be resized. In addition, to unfold these MOSFETs the entire group of MOSFETs generated by the original folding operation must be specified as the selector. They can then be unfolded into the original size.



Option	Description
Fold Paired	**Overview** N and P-MOSFETs are paired before folding. Paired folding reduces the size of MOSFETs to a specified maximum, similar to the folding operation. However, in paired folding, N-MOSFETs and P-MOSFETs are paired before folding. This is useful in fully complementary circuits. 
Max P Width	The maximum width for folded P-MOSFETs.
Max N Width	The maximum width for folded N-MOSFETs.

Option	Description
Unfold	**Overview**The MOSFETs in the specified list are unfolded. The selected MOSFET must be the principal MOSFET. MOSFETs chosen by the selector must be appropriate secondary MOSFETs (i.e. folded pieces of the same original MOSFET). Unfolding merges the widths of one or more secondary MOSFETs into a principal MOSFET. Principal and secondary MOSFETs must derive from the same original MOSFET. Only previously-folded MOSFETs can be unfolded. Folding generates one principal and one or more secondary MOSFETs. When unfolding or resizing folded MOSFETs, only MOSFETs deriving from the same folding operation can be used. Refer to Principal vs. Secondary MOSFETs on page 253 for more details on these restrictions. 

Option	Description	
Resize	Overview	The specified list of MOSFETs are resized. The selected MOSFET must be the principal MOSFET. MOSFETs chosen by the selector must be appropriate secondary MOSFETs. Resizing “adds” a specified amount of width to a principal MOSFET from one or more secondary MOSFETs. Principal and secondary MOSFETs must derive from the same original MOSFET. The principal MOSFET is resized by the specified delta width. A positive delta width increases the width of the principal MOSFET, while a negative delta width decreases the width of the principal MOSFET. This width is subtracted from or added to the secondary MOSFET(s) specified in the selector. Only previously-folded MOSFETs can be resized. Folding generates one principal and one or more secondary MOSFETs. When unfolding or resizing folded MOSFETs, only MOSFETs deriving from the same folding operation can be used. Refer to Principal vs. Secondary MOSFETs on page 253 for more details on these restrictions.
Resize Delta	Overview	The width to be added to the selected MOSFET.

Principal vs. Secondary MOSFETs

Folding and paired folding operations create one principal and one or more secondary MOSFETs.

The principal MOSFET must be identified by the operator when creating an unfolding or resizing operation. It is the principal MOSFET that will receive the additional width when unfolded or resized. This extra width is removed from the secondary MOSFETs, which must be identified by the selector of the policy.

The principal and secondary MOSFETs identified in a policy must have the same parent MOSFET and must derive from the same folding operation.

Example

A cell contains the following MOSFETs:

```
mn0   mn1@1   mn1@2   mn2@1   mn2@2   mn2@3
```

OK *Not*

```
Principal: mn1@1; Secondary: mn1@2Principal: mn1@1;
Secondary: mn0
```

```
Principal: mn2@3; Secondary: mn2@1, mn2@2Principal: mn1@1;
Secondary: mn2@3
```

To extract hierarchy

Hierarchy extraction identifies related transistors that form a recognized structure, such as an inverter or transmission gate and groups these transistors together as tiles.

To extract hierarchy, do the following:

1. In the Cell Browser, click and hold on a netlist design point.
   The design point menu appears.
2. Select Advanced > Extract Hierarchy.
   The Extract Netlist Hierarchy dialog box appears.
3. Set the options (refer to Extract Hierarchy Options on page 255).
4. Click OK.
   A configuration or configuration set design point is added to the design tree.

Extract Hierarchy Options

Option	Description	
Pruning Threshold	Overview	The maximum number of solutions used during extraction. This limits the number of possible solutions kept during each stage of the extraction.
	Why set this option?	A pruning threshold reduces the search space and the time required to perform the extraction.
Solution Cost Tolerance	Overview	Solutions whose cost is greater than the cost of the best solution times this value are pruned.
	What values should you use?	Set the tolerance to 1.00 to accept only the optimal solution. Set to a value of 2.00 to accept solutions that are twice as costly as the best solution. A value of 1.5 is reasonable for most cells.

Option	Description	
Do cloning	Overview	Clone files are used to generate a tile with the exact placement (and routing) information as in the cloned layouts. There are certain restrictions on using clones.
	Why set this option?	Cloning provides the same placement (and possibly routing) for the common circuitry in the netlists. For example, variations of a flip-flop can use the same placement for the common transistors. If there is a match between the cloned devices and the netlist devices, then a tile containing symbolic devices with identical geometry and internal states as that in the source layout is created and added as part in the configuration. A clone can be used to extract hierarchy from netlists if: ▪ netlists have similar devices and connectivity, (The target netlist can contain more transistors thanthe clone.) ▪ transistor widths in the target netlist are within the specified width tolerance of the cloned MOSFETs,and ▪ source and target cells have the same technology and architecture.

Option	Description	
	Also set	▪ The Clone File Names. These files are tried with this netlist. ▪ The Regenerate MOSFET geometry option. This regenerates the geometry of the cloned MOSFETs in the target cell. Any variation in the MOSFET width is reflected in the target cell. If this is not selected, the MOSFET geometry of the target cell is exactly the same as that of the source layout MOSFET geometry. ▪ The Preserve routing option. This determines the behaviour if all of the routing cannot be preserved. If selected, then none of the routing is added from the clone. If not selected, then the routing that caused the violation is not added, but the rest of the clone is used. ▪ The MOSFET Width Tolerance. The allowable difference in width between the source and target layouts. In the event that a design rule violation occurs or the MOSFET alignment in the source layout cannot be preserved in the target cell, clone instantiation is suspended and the next clone file (if any) is automatically used.
Do searching	Overview	Logical structures in the netlist are identified. This stage may be of limited value if many unknown structures exist.
Do chaining	Overview	Diffusion gaps are minimized by aligning gates wherever possible. The chaining phase can be lengthy for larger, more complex cells.
Allow gate crossing	Overview	The extractor can cross gates to reach solutions.
Allow partial chaining	Overview	A limited number of diffusion gaps are allowed to complete chaining.
Use alternative chaining	Overview	This is useful for highly folded cells. For best results, select Allow gate crossing.

Option	Description	
Do pairing	Overview	Available N and P-type transistors are matched.
Max Number of Configurations	Overview	The maximum number of configurations to be generated. This value sets the maximum possible number of solutions. If only one solution is found, one solution is generated.
	Why set this option?	Specifying a maximum number of configurations allows you to try alternative placements based on different groupings of transistors (tiles). If the scale is set to 1, a single configuration is generated. If the scale is set to a higher value, one or more configurations are generated (up to the specified maximum value).
Clone File Names	Overview	The cloned symbolic layout(s) to be used. Clones are applied in the order in which they appear in the list box.
Regenerate MOSFET geometry	Overview	The geometry of cloned MOSFETs is regenerated.
Preserve routing	Overview	If some of the routing cannot be preserved, then none of the routing is added from the clone.

Option	Description	
MOSFET Width Tolerance	Overview	The allowable MOSFET width tolerance of the target cell with respect to the MOSFETs in the source layout.
	What values should you set?	If you set the tolerance to 0%, then the MOSFET in the source layout and the target cell will have exactly the same width. If you set the tolerance to INFINITY, then the width tolerance restrictions are not applied for matching source layouts with target clones. The width of MOSFETs in the source and target cells can vary as much as needed. As the tolerance is increased, more variation in the width of MOSFETs is allowed. However, this can make reuse of the routing information more difficult.
	Also set	Do cloning. Otherwise, the MOSFET Width Tolerance option is not available.

To select a configuration

If a configuration set is generated, a single configuration must be selected before placing tiles.

To select a configuration, do the following:

1. In the Cell Browser, click and hold on a configuration set design point.

   Result: The design point menu appears.

2. Select Advanced > Select Configuration.

   Result: The Configuration Selection dialog box appears.

3. Set the slider to select a configuration *or* click Select all configurations to generate all possible configurations.

4. Click OK.

   Result: One or more configuration design points are added to the design tree.

To edit a configuration

Editing a configuration design point allows you to select an alternate MOSFET placement if there is one.

To edit a configuration, do the following:

1. In the Cell Browser, click and hold on a configuration set design point.

   Result: The design point menu appears.

2. Select Advanced > Cell Edit.

   Result: The Cell Edit dialog box appears.

3. Select View > Annotate Nets.

   Result: The annotations for all the nets appear.

4. Click-hold on the MOSFET group you would like to change the placement of.

   Result: The device menu appears.

   Explanation: If you click on a MOSFET group, and the device menu does not appear, then that MOSFET placement cannot be altered.

5. Select Next Placement or Previous Placement.

   Result: An alternate MOSFET placement appears.

6. Repeat steps 4-5 until you have the MOSFET placement you would like.

7. Select Design Point > Dismiss.

   Result: The Cell Edit dialog closes and a new configuration design point is created.

To fold tiles

Folding tiles folds transistors into multiple fingers with the same nets. This design step can be applied after hierarchy extraction. You can also fold transistors from the netlist using the fold MOSFETs design step.

To fold tiles, do the following:

1. In the Cell Browser, click and hold on a configuration design point. The design point menu appears.

2. Select Advanced > Fold Tiles.
   The Fold Tiles dialog box appears.
3. Set the options (refer to Fold Tiles Options on page 261).
4. Click OK.
   A configuration design point is added to the design tree.

   Important: Before folding, you can find the current maximum width of N and P-type transistors in the netlist by selecting Describe from the netlist design point menu.

Fold Tiles Options

P-type: The maximum width of P-MOSFETs after folding.

N-type: The maximum width of N-MOSFETs after folding.

Pair first: MOSFETs are paired before folding. This is useful for fully complementary circuits.

Individual: Transistors are individually folded without regard for matching N and P-types.

To merge tiles

Merging tiles associates some or all of the tiles in a configuration to reduce the total number of tiles. In large cells, this can improve the efficiency of the tile placement. Tile merging cannot be performed on configurations containing a single tile.

To merge tiles, do the following:

1. In the Cell Browser, click and hold on a configuration design point.
   The design point menu appears.
2. Select Advanced > Merge Tiles.
   The Merge Tiles dialog box appears.
3. Set the options (refer to Merge Tiles Options on page 262).
4. Click OK.
   A configuration design point is added to the design tree.

Merge Tiles Options

Net Weight Assignment: The relative importance of each net.

Target: The resulting number of tiles after merging.

Merging Coefficient: The importance of merging diffusion regions. A larger value tries to avoid diffusion gaps.

Interconnect Weight Coefficient: The importance of the total wire length. A larger value tries to reduce the wire length. This can improve routability in larger cells.

Size Balancing Coefficient: The importance of keeping balanced tile sizes. A larger value tries to merge smaller tiles together to achieve tiles of relatively the same size.

To place tiles

Hierarchy extraction creates tiles or associated groups of devices. Place Tiles places tiles in a symbolic layout.

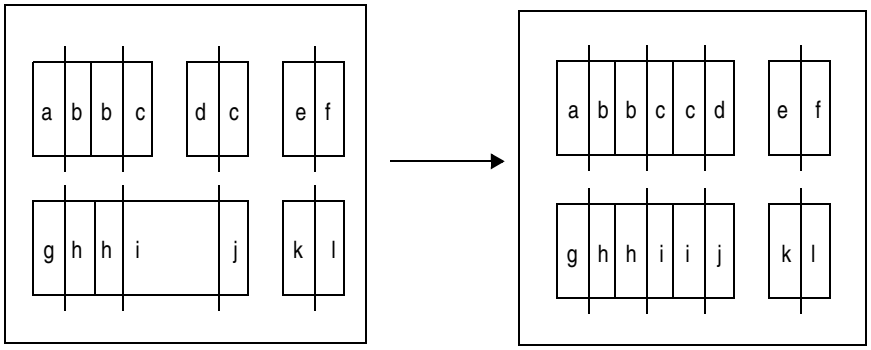
To place tiles, do the following:

1. In the Cell Browser, click and hold on a configuration design point.
   The design point menu appears.
2. Select Place Tiles.
   The Automatic Placement dialog box appears.
3. Set the options (refer to Place Tiles Options on page 263).
4. Click OK.
   A symbolic layout design point is added to the design tree.

   Note: You can view the symbolic layout after tiles are placed. Select Open from the design point menu of any symbolic layout design point.

Place Tiles Options

Options	Description	
Net Weight Assignment	Overview	The relative importance of each net.
Group tiles	Overview	Associated tiles are grouped and placed together. Grouping tiles allows more tiles to be placed in a shorter amount of time.
Ignore largest nets	Overview	During tile grouping, large nets that are connected to multiple tiles are ignored. The large nets are, however, still considered during tile placement.
Form isolated groups	Overview	Tiles that are connected to other tiles through only one net or one tile are grouped.
Minimize group connectivity	Overview	Tiles that have few nets between them are put in different groups.
Flip MOSFETs to minimize diffusion gaps	Overview	Where possible, MOSFETs are flipped to eliminate diffusion gaps.

Options	Description
	Why set this option? Flipping MOSFETs switches the side of a MOSFET's source and drain. This can reduce the number of diffusion gaps on a cell. For example, if a MOSFET's source is on the left and its drain on the right, the two will be switched if it allows for a diffusion merge to the right or left. The relative position of the MOSFET is maintained. That is, vertically aligned MOSFETs remain aligned and the order of MOSFETs in each row remain the same. 
Wire Length Coefficient	Overview	The importance of the total wire length. A larger value encourages the minimization of total wire length, which can improve routability.
Max Wire Length Coefficient	Overview	The importance of the wire with the longest possible length. A larger value encourages the minimization of very long wires, which can improve routability.
Diffusion Merging Coefficient	Overview	The importance of merging diffusion regions. A larger value tries to reduce the number of diffusion gaps.
Channel Density Coefficient	Overview	The importance of the channel density. A larger value can reduce channeldensity, which can improve routability.

Options	Description	
Maximum Density Coefficient	Overview	The maximum density importance. A large value stresses the contributionof the maximum channel density. A smaller value stresses the average channel density. Thus, if the average channel density is more important, this value should be small.
Optimality	Overview	Cadabra stops when a solution whose cost is less than this value times the cost of the best solution is found.
	Why set this option?	A set optimality restricts the number of solutions generated. If it is set to 1.0, only the optimal placement is accepted. If it is set to 1.2, placement stops once a solution which is a maximum of 1.2 times as expensive as the optimal solution is found. For large cells, try a higher value (e.g. 1.5) to have the placement finish in a reasonable time.
Time Limit	Overview	Cadabra stops after the specified time has passed.

To optimize a placement

The width of the symbolic layout created by Cadabra during tile placement can sometimes be reduced by stacking, flipping, or staggering MOSFETs. The stacking option only works for the cells that have enough space for stacking.

To optimize a placement, do the following:

1. In the Cell Browser, click and hold on a symbolic layout design point.
   The design point menu appears.
2. Select Advanced > Optimize Placement.
   The Optimize Placement dialog box appears.
3. Set the options (refer to Optimize Placement Options on page 267).
4. Click OK.
   A symbolic layout design point is added to the design tree.

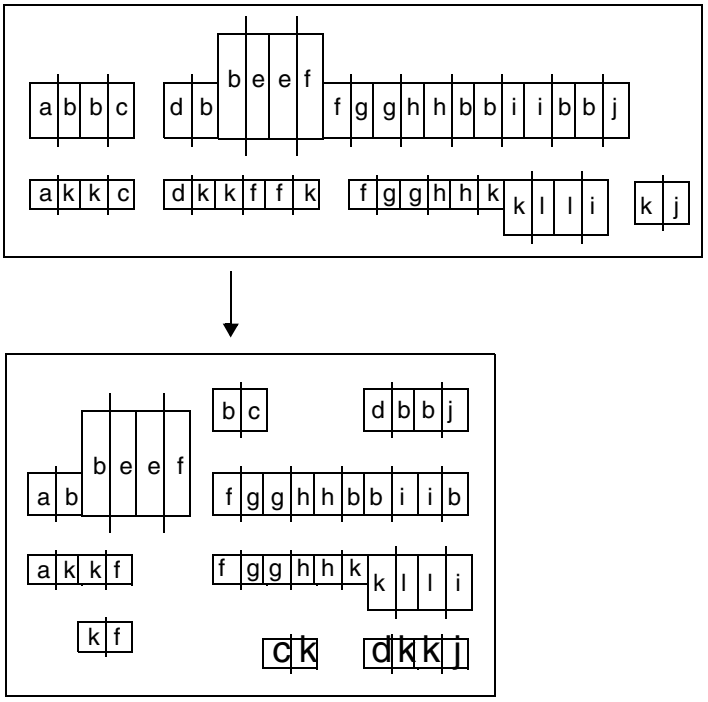
Note: This design step can only perform one of the two steps (stacking or flipping) at a time. To perform both stacking and flipping, run this design step twice. However, flipping must be performed before stacking.

Optimize Placement Options

Options	Description	
Perform MOSFET stacking	Overview	Where possible, MOSFETs are stacked above or below each other to reduce cell size. Only two transistors of the same type can appear on the same x-coordinate and the x-coordinate must align the stacked pairs gates. Your architecture height must allow for stacked transistors. Otherwise, if there is no space, MOSFETs are not stacked.

Why set this option?

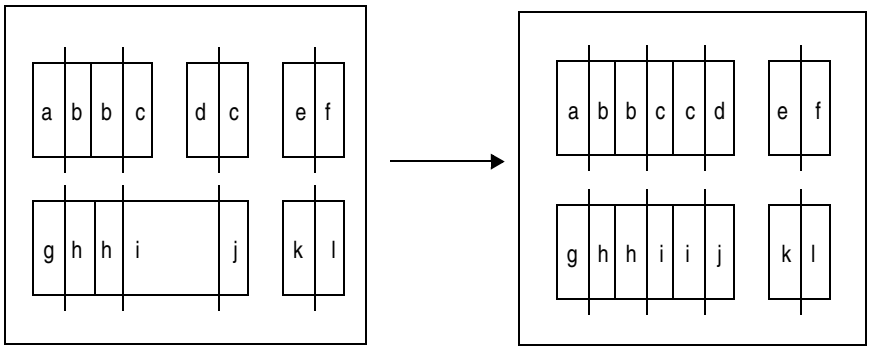
Stacking MOSFETs can help reduce cell size as shown in the figure below.



Aligned gate:	Overview	MOSFETs with the same gate nets are considered for stacking.

Options	Description	
Power net	Overview	Stacking is considered for MOSFETs with common diffusion nets where the stacked MOSFET (i.e. the MOSFET which is moved above or below the other) has a power net on its other diffusion.
Diffusion merge	Overview	Stacking is considered for MOSFETs where one side of aMOSFETs diffusion merges with the diffusion of the other, larger MOSFET beside it.
Wire Length Coefficient	Overview	The importance of the total wire length. A larger value encourages the minimizationof total wire length.
Stacked Routing Coefficient	Overview	The importance of the additional routing cost for stacked MOSFETs. A larger value encourages the minimization of routing.
Size Coefficient	Overview	The importance of maintaining the cell size. A larger value encourages the minimization of cell width.
Emphasize diffusion merging	Overview	Where possible, MOSFETs are flipped to merge diffusions during the search for stacked placements.
Use priority to limit search	Overview	Only the most useful placements are considered. This limitation reduces the search time.
Time limit	Overview	Cadabra stops optimization after the specified time has passed.

Options	Description	
Flip MOSFETs to minimize diffusion gaps	Overview	Where possible, MOSFETs are flipped to eliminate diffusion gaps.
	Why set this option?	
	Flipping MOSFETs switches the side of a MOSFET's source and drain. This can reduce the number of diffusion gaps on a cell. For example, if a MOSFET's source is on the left and its drain on the right, the two will be switched if it allows for a diffusion merge to the right or left. The relative position of the MOSFET is maintained. That is, vertically aligned MOSFETs remain aligned and the order of MOSFETs in each row remain the same.	



To align MOSFETs

MOSFET alignment policies are described by an operator and one or more selectors. The operator identifies the type of alignment operation, while the selector identifies the group of MOSFETs to be aligned. Any number of policies can be specified.

To align MOSFETs, do the following:

1. In the Cell Browser, click and hold on a symbolic layout design point.
   The design point menu appears.
2. Select Advanced > Align MOSFETs.
   The Align MOSFETs dialog box appears.

3. Set the Selector values to specify the MOSFETs this policy can act on. You can choose as many selectors as required. (Refer to Selectors on page 271.)

   Note: Using more than one selector defines a union of groups, not an intersection of groups. For example, if one selector specifies all N-type MOSFETs and another selector specifies all MOSFETs whose width exceeds 5 microns, the subset of MOSFETs will include all N-MOSFETs as well as those P-MOSFETs wider than 5 microns.

4. Set the Operator values to specify the actions in this policy. You can choose one operator per policy. (Refer to Operators on page 271.)
5. Click Add.
   The alignment policy is added.
6. Repeat steps 3-5 until all the required policies have been added.
7. Click OK.
   The alignment is performed. A symbolic layout design point is added to the design tree.

   Note: Policies are performed in the order in which they appear in the listbox. You can click Move Up and Move Down to reorder the policies.

Align MOSFETs Options

The following types of options are available for aligning MOSFETs:

Selectors

Options	Description	
MOSFET Type	Overview	MOSFETs are selected based on type.
MOSFET Width	Overview	MOSFETs are selected based on width.
MOSFET Length	Overview	MOSFETs are selected based on length.
MOSFET Name	Overview	MOSFETs are selected by name.
Select	Overview	The names of the MOSFETs to select.
Regular expression	Overview	A regular expression used to select MOSFET names. Regular expressions can be used to collect all names that match a given rule. In a cell that has a large number of transistors, a regular expression quickly collects all the names that begin with, end with, or contain the given characters.

	Example	A cell contains these transistors:
		`mn0 mn1 mn2@1 mn2@2 mn2@3 mn3`
		`mp0 mp1 mp2 mp3@1 mp3@2`
		■ To collect all of the aligned transistors, use: `@*` This expression looks for the `@` symbol (that designates aligned transistors) anywhere in the name.
		■ To collect of the transistors that derive from the aligning of `mn2`, use: `mn2@*` This expression looks for the `@` symbol preceded by an `mn2`.

Operators

Options	Description
Place at	MOSFETs are placed at a specified location.

Options	Description
Y Location	The y-coordinate where the MOSFETs should be placed.
Grid Snap Direction	Devices are snapped to the `nearest` y-grid, the next grid `up`, the next grid `down`, or `none` (do not snap to grid).
Alignment	MOSFETs are aligned with respect to the top, middle, or bottom of the group.
Grid Offset	MOSFETs are offset by the specified number of grids.
Absolute Offset	MOSFETs are offset by the specified number of microns.
Epsilon	MOSFETs are offset by + or - the epsilon value. (The epsilon value is set in the technology.) The epsilon value is used in preference to the absolute offset.
Offset by	MOSFETs are offset from the current location.
Freeze	MOSFETs are frozen to their current location and excluded from further alignments.
Exclude	MOSFETs are returned to their original locations and excluded from further alignments.

To generate compaction geometries

Compaction geometries can be generated from the Cell Browser. These geometries are pre-conditions that facilitate the compaction process. Each device controls how it is pre-conditioned.

To generate compaction geometries, do the following:

1. In the Cell Browser, click and hold on a symbolic layout design point. The design point menu appears.
2. Select Advanced > Generate Compaction Geometries.
   A symbolic layout design point is added to the design tree containing the appropriate geometries.

To use the Cell Compact design step

To use the Cell Compact design step, do the following:

1. In the Cell Browser, click and hold on a symbolic layout design point.
   The design point menu appears.
2. Select Advanced > Cell Compact.
   The Compaction dialog box appears.
3. Set the options (refer to Compaction Options on page 274).
4. Click OK.
   A symbolic layout or layout design point is added to the design tree.

Compaction Options

Option Type	Option	Description
Defaults	Use defaults from id	The id of a compacted design point for which you want to repeat the results for the currently selected design point. The defaults used in the specified design point id are propagated to the other tabs in the Compaction dialog box. You must click Update each time the Use defaults from id option is changed.
	Maximum Cell Width	The maximum cell width, in microns, allowed for the compation.
Controls	Solve objectives	Compaction objectives are solved and the cell is compacted.
	Relax infeasible constraints	Allows a specified set of constraints to be relaxed to continue compaction, but producing a feasible result. Click Configure to specify the order.
	Configure	The Constraint Relaxation Priority dialog box appears. This dialog allows you to specify a set of constraints to be relaxed in order.
	Generate Constraints and Objectives Only	A set of constraints and objectives are generated, but the cell is not compacted. Generating a set of constraints and objectives before compacting the cell allows you to verify the design rules with the Compaction Browser and understand the setup.

Option Type	Option	Description
Controls (*continued*)	Diagonal Relaxation Radius	A radius (in microns) defining the area in which shapes require more freedom to move relative to one another. **Why set this option?** A diagonal relaxation radius allows shapes within that radius to move around one another. The shapes outside the radius can only move in a single direction and must remain in the same relative orientation. The larger the radius you set, the greater the flexibility in movement, but also, the greater the compaction time. Whereas, a smaller radius results in lesser flexibility, but lesser compaction time as well.
	Snap horizontally	Constraints for snapping horizontally to the IO grid are enforced.
	Snap vertically	Constraints for snapping vertically to the IO grid are enforced.
	Relax height constraint	Boundary height constraints are relaxed.
	Relax width constraint	Boundary width constraints are relaxed.
Controls (*continued*)	Layer Based Relaxation Radius	A table listing all of the layers to which a relaxtion radius is applied. Use the Add and Delete buttons to add and remove a layer-based relaxation radius. The following are available: ▪ Layer1 Name: The name of the first layer to relax. Select a layer from the drop-down list. ▪ Layer2 Name: The name of the second layer to relax. Select a layer from the drop-down list. ▪ Relaxation Radius: A radius (in microns) defining the area in which the two specified layers can move relative to each other.

Option Type	Option	Description
Output Data	Save constraints and objectives	Generated constraints and objective terms are saved to disk. If saved, the compaction data can be browsed when the cell is re-opened. Otherwise, this data is not kept. This option can be selected individually for infeasible and feasible results.
	Output Geometry Type	The type of geometry to be generated.
Objectives	Unused	A list of constraint objectives that are not to be used during compaction.
Objectives (*continued*)	Used	A list of constraint objectives that are to be used during compaction. The constraints are applied in the order in which they are listed.
	Configure Objective	The Configure Objective dialog box appears. This dialog allows you to set conditions for the selected objective(s). Refer to Configure Objective Options on page 282.
	Create/Edit	The Create/Edit Combined Objective dialog box appears. This dialog allows you to create and weight combined objectives.
	Delete	The selected combined objective is removed.
Preservation Options	Use Preserve	The compaction style preservation options, specified in this dialog box, are applied during the Cell Compact design step.
	Initial layout	The initial layout design point to be preserved is marked by the specified tag in the Cell Browser. The default tag is “Completed Import”.

Option Type	Option	Description
Preservation Options (*continued*)	Layer Based Preserve	A table listing all of the layers to be preserved. Use the Add, Edit, and Delete buttons to add, edit, and remove a layer based preserve. The following option is available: ▪ *Layer Name*: The name of the layer to preserve. Select a layer from the drop-down list.
	Relation	The manner in which layer edges are preserved. Select a relation type from the drop-down list. The possible values are: ▪ `absolute`: The absolute positions of the edges are preserved. ▪ `relative exactly`: The relative distances among a group of edges are preserved. If Relation is set to `relative exactly` only the relative positions within the same are preserved. The relative positions between different layers is not preserved.
Preservation Options (*continued*)	Orientation	The type of orientation to preserve for the layer. Select an orientation from the dropdown list. The possible values are: `manhattan`, `horizontal`, and `vertical`.
	Preserve Type	Two values are possible: `hard` or `soft`. For "`hard`" preserves, simple constraints are generated between the preserved edges and/or boundary constraints. These hard preserve constraints have a higher priority than other types of constraints and will overwrite or disable device, technology, or soft preserve constraints if necessary. For "`soft`" preserves, soft preserve constraints are generated. These constraints can not overwrite or disable other constraints.

Option Type	Option	Description
Preservation Options (*continued*)	Objective Type	The type of soft preserve objective to use. A value for this option is only required if Preserve Type is set to “soft”. Select an objective from the drop-down list. The possible values are: ■ `edgeFirst`: The number of edges moved during compaction is minimized. ■ `evenDistribution`: All of the edges moved during compaction are moved equally, by the same distance.
	Soft Preserve Priority	The priority for the soft preserve. Select a value between 1 and 5. The soft preserves with the same specified priority are solved at the same time.
	Template Based Preserve	A table listing all of the templates to be preserved. Use the Add, Edit, and Delete button to add, edit, and remove a template based preserve.
	Template Name	The name of the template to preserve. Select a template from the drop-down list.
Preservation Options (*continued*)	Relation	The manner in which edges are preserved. Select a relation type from the drop-dowm list. The possible values are: ■ `absolute`: The absolute positions of the edges are preserved. ■ `relative exactly`: The relative distances among a group of edges are preserved. If Relation is set to “`relative exactly`” only the relative positions within the same template are preserved. The relative positions between different templates is not preserved.
	Orientation	The type of orientation to preserve for the layer. Select an orientation from the dropdown list. The possible values are: manhattan, horizontal, and vertical.

Option Type	Option	Description
Preservation Options (*continued*)	Preserve Type	Two values are possible: `hard` or `soft`. For "`hard`" preserves, simple constraints are generated between the preserved edges and/or boundary constraints. These hard preserve constraints have a higher priority than other types of constraints and will overwrite or disable device, technology, or soft preserve constraints if necessary. For "`soft`" preserves, soft preserve constraints are generated. These constraints can not overwrite or disable other constraints.
	Objective Type	The type of soft preserve objective to use. A value for this option is only required if Preserve Type is set to "soft". Select an objective from the drop-down list. The possible values are: ▪ `edgeFirst`: The number of edges moved during compaction is minimized. ▪ `evenDistribution`: All of the edges moved during compaction are moved equally, by the same distance.
	Soft Preserve Priority	The priority for the soft preserve. Select a value between 1 and 5. The soft preserves with the same specified priority are solved at the same time.
Relaxation Options	Unused	This column displays the list of relaxation styles not used by the compactor.
	Used	This column displays the list of relaxation styles used by the compactor. **Note:** You can move relaxation styles between the Used and Unused columns by selecting the required relaxation style and clicking the left and right arrows that separate the two columns.
	Add a new style	Click this button in order to add a new relaxation style name.

Option Type	Option	Description
	Edit or Show terms	To edit a relaxation style or to view details of a relaxation style, click the name of the required relaxation style from the Used or Unused columns, and then click the Edit or Show terms button.
	Delete a style	To delete a style, click the name of the required relaxation style from the Used or Unused columns, and then click the Delete a style button.

To set the constraints to be relaxed

The compactor produces an infeasible solution when conflicting constraints cannot be solved. Allowing certain constraints to be relaxed (or ignored) can solve this infeasibility.

To set the constraints to be relaxed, do the following:

1. In the Compaction dialog box, select Relax infeasible constraints on the Controls tab.
2. Click Configure.
   The Constraint Relaxation Priority dialog box appears.
3. Click on a + symbol to open that set of constraints.
   A list of individual constraints is displayed.
4. Select the constraints(s) to be relaxed.
5. Click Add to priority list.
   The constraint(s) are added to the Priority List. The constraints to be relaxed are indicated by a 4.

   Note: Constraints are relaxed in the order in which they appear in the Priority List. The order can be changed by dragging a constraint up or down in the list.

6. Click OK.
   The list of constraints are set.

To create a combined objective

Combined objectives are a collection of objectives applied concurrently. Each objective may be weighted and given more or less importance. A combined objective is indicated by a + sign.

To create a combined objective, do the following:

1. In the Compaction dialog box, click Create/Edit on the Objective tab.
   The Create/Edit Combined Objectives dialog box appears.
2. Enter a name for the new combined objective.
3. Select the objectives that are to form the combined objective.
4. Enter a weighting value beside each objective.

   Note: The value should be a non-negative integer. Cadabra tries harder to optimize the objectives that are weighted more highly.

5. Click OK.
   The Create/Edit Combined Objective dialog is closed and the new combined objective is added to the Used list on the Objectives tab.

   Note: You can edit an existing combined objective by selecting the combined objective and then clicking Create/Edit.

Configure Objective Options

Options	Description	
Resolve corner constraints	Overview	Shapes can be moved with more freedom while solving the associated objective. Corner (diagonal) constraints are initially solved when processing an objective. Re-solving these constraints can produce superior results, but may increase runtime.
Allow snapped shape movement	Overview	Permits snapped shapes to be moved during the compaction of the associate objective. Edges are snapped to either the IO grid or multiples of the manufacturing grid depending on the object type. **Why set this option?** Allowing snapped shapes unrestricted movement can produce better results. However, it also increases the run time of compaction. If snapped shapes are not allowed to move, they remain fixed at their position, which was determined by the previous objectives.
Resolve conditional constraints	Overview	The results of the conditional constraints objective are reconsidered. Re-solving these constraints can produce better results, however, the run time may be longer.
Optimality Tolerance	Overview	The acceptable quality of generated solutions. A value of 0% accepts only the optimal solution. A value of 10% accepts solutions that are, at most, within 10% of the optimal solution.
Time Limit	Overview	The time limit (in seconds) for the objective. Cadabra continues running the compactor until it reaches the specified time limit.
Iterations Limit	Overview	The maximum number of iterations used for the objective. The compactor stops work on the objective once the maximum number of iterations has been exceeded.

Options	Description	
Progress Threshold	Overview	The percentage by which the solution (objective value) must improve the current solution before the objective is considered to be showing progress. **Why set this option?** Setting a higher progress threshold allows you to avoid lengthy computations for certain objectives. If this threshold has not been passed within the time iteration limit set, no progress is assumed. Time and iteration limits can be set for the No Progress condition. For example, assume a progress threshold of 5% and a NoProgress iteration limit of 5000, if the solution does not decrease by at least 5% withing the 5000 iteration, then work on that objective is halted and the compactor moves on to the next objective. Setting the progress threshold to a higher value decreases the runtime of the compaction, but can reduce the quality of solutions generated.
Min. Target	Overview	The mininum target value for this objective. Once the minimum target is reached, the compactor moves to the next objective or, if this is the last objective, returns the current solution.
Max. Target	Overview	The maximum target value for this objective. If the compactor cannot reach the maximum target, then it will not process subsequent objective and will return an incomplete result.

To generate routing geometries

Routing geometries can be generated from the Cell Browser. These geometries are appropriate for adding routing devices, but the devices must be reshaped before compaction.

To generate routing geometries, do the following:

1. In the Cell Browser, click and hold on a symbolic layout design point.
   The design point menu appears.
2. Select Advanced > Generate Routing Geometries.
   A symbolic layout design point is added to the design tree containing the appropriate geometries.

To generate a layout

A layout design point displays final cell shapes and cannot be hand-edited. However, shape based post-processing can be performed on a layout (for example, adding implants or merging shapes). Layout geometry can be generated for export to downstream tools.

To generate a layout, do the following:

1. In the Cell Browser, click and hold on a symbolic layout design point.
   The design point menu appears.
2. Select Advanced > Generate Layout.
   A layout design point is added to the design tree.

   Note: A layout can only be generated from a feasible compacted design point.

To use the Connect Tie Rail design step

Connect Tie Rail is used during Migrate GDS and Import when there is a difference in tie strategies between the source and target architectures. This design step may be explicitly registered in the architecture .al file.

To use the Connect Tie Rail design step, do the following:

1. In the Cell Browser, click and hold on a symbolic layout design point.
   The design point menu appears.
2. Select Advanced > Post-Import Steps > Connect Tie Rail.
   The Connect Tie Rail design step is run on the design point and a symbolic layout design point is added to the design tree.

To use the Update Boundary design step

Update Boundary redraws the boundary and all related devices, to accommodate a modified transistor or new device placement. This design step may be explicitly registered in the architecture .al file.

To use the Update Boundary design step, do the following:

1. In the Cell Browser, click and hold on a symbolic layout design point.
   The design point menu appears.
2. Select Advanced > Edit Design Steps > Update Boundary.
   The Update Boundary design step is run on the design point and a symbolic layout design point is added to the design tree.

To use the Prepare Abutments design step

Prepare Abutments replaces the abutment of two layers with a specific device. This design step may be explicitly registered in the architecture .al file.

To use the Prepare Abutments design step, do the following:

1. In the Cell Browser, click and hold on a symbolic layout design point.
   The design point menu appears.
2. Select Advanced > Pre-Compaction Steps > Prepare Abutments.
   The Add Abutments design step is run on the design point and a symbolic layout design point is added to the design tree.

To use the Add Multiple Gate Bends design step

Add Multiple Gate Bends allows you to add 450 or 900 gate bends to transistors. This design step may be explicitly registered in the architecture .al file.

To use the Add Multiple Gate Bends design step, do the following:

1. In the Cell Browser, click and hold on a symbolic layout design point.
   The design point menu appears.

2. Select Advanced > Pre-Compaction Steps > Add Multiple Gate Bends.
   The Add Multiple Gate Bends design step is run on the design point and a symbolic layout design point is added to the design tree.

To use the Jog at Gates design step

Jog at Gates adds flexibility to the compactor for the final placement of MOSFET devices by inserting wire jogs where MOSFET gates are connected by a POLY wire. This design step may be explicitly registered in the architecture .al file.

To use the Jog at Gates design step, do the following:

1. In the Cell Browser, click and hold on a symbolic layout design point.
   The design point menu appears.
2. Select Advanced > Pre-Compaction Steps > Jog at Gates.
   The Jog at Gates design step is run on the design point and a symbolic layout design point is added to the design tree.

To use the Jog Wires Around Contacts design step

Jog Wires Around Contacts places wire jogs at specific locations where wires are close to contacts. This design step may be explicitly registered in the architecture .al file.

To use the Jog Wires Around Contacts design step, do the following:

1. In the Cell Browser, click and hold on a symbolic layout design point.
   The design point menu appears.
2. Select Advanced > Pre-Compaction Steps > Jog Wires Around Contacts.
   The Jog Wires Around Contacts design step is run on the design point and a symbolic layout design point is added to the design tree.

To use the Match MOSFET Sizes design step

Match MOSFET Sizes aligns the edges of MOSFETs with slightly different dimensions. This design step may be explicitly registered in the architecture .al file.

To use the Match MOSFET Sizes design step, do the following:

1. In the Cell Browser, click and hold on a symbolic layout design point. The design point menu appears.
2. Select Advanced > Pre-Compaction Steps > Match MOSFET Sizes. The Match MOSFET Sizes design step is run on the design point and a symbolic layout design point is added to the design tree.

To use the Optimize Horizontal Wires design step

Optimize Horizontal Wires attempts to remove constraints on the compactor caused by edge locking at the intersection of horizontal and vertical wires. This design step may be explicitly registered in the architecture .al file.

To use the Optimize Horizontal Wires design step, do the following:

1. In the Cell Browser, click and hold on a symbolic layout design point. The design point menu appears.
2. Select Advanced > Pre-Compaction Steps > Optimize Horizontal Wires. The Optimize Horizontal Wires design step is run on the design point and a symbolic layout design point is added to the design tree.

To use the Selectively Pregrow Diffusion design step

Selectively Pregrow Diffusion selectively pregrows the diffusion cover on contacts contained in a MOSFET diffusion. This design step may be explicitly registered in the architecture .al file.

To use the Selectively Pregrow Diffusion design step, do the following:

1. In the Cell Browser, click and hold on a symbolic layout design point. The design point menu appears.

2. Select Advanced > Pre-Compaction Steps > Selectively Pregrow Diffusion.
   The Selectively Pregrow Diffusion design step is run on the design point and a symbolic layout design point is added to the design tree.

To use the Add Layout Ties design step

Add Layout Ties adds well/substrate ties to a cell by searching for available space within a layout. This design step may be explicitly registered in the architecture .al file.

To use the Add Layout Ties design step, do the following:

1. In the Cell Browser, click and hold on a symbolic layout design point.
   The design point menu appears.
2. Select Advanced > Final Layout Steps > Add Layout Ties.
   The Add Layout Ties design step is run on the design point and a layout design point is added to the design tree.

To use the Add Implants design step

Add Implants derives implant shapes from diffusion and tie shapes. This design step may be explicitly registered in the architecture .al file.

To use the Add Implants design step, do the following:

1. In the Cell Browser, click and hold on a symbolic layout design point.
   The design point menu appears.
2. Select Advanced > Final Layout Steps > Add Implants.
   The Add Implants design step is run on the design point and a layout design point is added to the design tree.

To use the Fill Notches design step

Fill Notches removes notch errors resulting from compaction. It handles notches in both manhattan and 450 edge geometries. This design step may be explicitly registered in the architecture .al file.

To use the Fill Notches design step, do the following:

1. In the Cell Browser, click and hold on a symbolic layout design point.
   The design point menu appears.
2. Select Advanced > Final Layout Steps > Fill Notches.
   The Fill Notches design step is run on the design point and a layout design point is added to the design tree.

To use the Merge Shapes design step

Merge Shapes is designed to prepare layout export. It combines all touching shapes into polygons. This design step may be explicitly registered in the architecture .al file.

To use the Merge Shapes design step, do the following:

1. In the Cell Browser, click and hold on a symbolic layout design point.
   The design point menu appears.
2. Select Advanced > Final Layout Steps > Merge Shapes.
   The Merge Shapes design step is run on the design point and a layout design point is added to the design tree.

To use the Reshape Gates design step

Reshape Gates isolates those MOSFET gates that are distinct from POLY wires and must be exported in a specific context. This design step may be explicitly registered in the architecture .al file.

To use the Reshape Gates design step, do the following:

1. In the Cell Browser, click and hold on a symbolic layout design point.
   The design point menu appears.

2. Select Advanced > Final Layout Steps > Reshape Gates.
   The Reshape Gates design step is run on the design point and a layout design point is added to the design tree.

To use the Adjust Overlapping Tie Diffusions design step

Adjust Overlapping Tie Diffusions ensures that the MOSFET diffusion and tie diffusion shapes do not overlap in a selected layout design point. This design step may be explicitly registered in the architecture .al file.

To use the Adjust Overlapping Tie Diffusions design step, do the following:

1. In the Cell Browser, click and hold on a symbolic layout design point.
   The design point menu appears.
2. Select Advanced > Final Layout Steps > Adjust Overlapping Tie Diffusions.
   The Reshape Gates design step is run on the design point and a layout design point is added to the design tree.

To use the Path Shapes design step

Path Shapes replaces rectangles and polygons in the layout with path shapes. Path shapes are defined by their centerline and path widths while rectangles are defined by their bounding box and polygons are defined by their shape contours. This design step may be explicitly registered in the architecture .al file.

To use the Path Shapes design step, do the following:

1. In the Cell Browser, click and hold on a symbolic layout design point.
   The design point menu appears.
2. Select Advanced > Final Layout Steps > Path Shapes > Add (specific) Path Shapes.
   The Path Shapes design step is run on the design point and shapes meeting layer and width requirements are replaced with path shapes.

To use the Text Annotation design step

Text Annotation adds text labels to the layout design point. You can use text labels to annotate rails, hit point locations, internal nets, and cell names. This design step may be explicitly registered in the architecture .al file.

To use the Text Annotation design step, do the following:

1. In the Cell Browser, click and hold on a symbolic layout design point.
   The design point menu appears.
2. Select Advanced > Final Layout Steps > Text Annotation > Add (specific) Text item.
   The Text Annotation design step is run on the design point and one or more text labels are added to the layout design point.

Compaction Browser

After running the Automated Transistor Layout (ATL) and/or the Migrate GDS process, you may have some sub-optimal or infeasible cells in your library. That is, the cells did not meet the set target width or could not be compacted. You can analyze these cells in the Compaction Browser (and then hand-edit them in the Cell Edit window).

From the Compaction Browser, you can:

- browse through the constraints (refer to To browse compaction constraints on page 294)
- browse through the objectives (refer to To browse compaction objectives on page 296)
- analyze the critical path (refer to To view the critical path on page 297)
- analyze the infeasibilities (refer to To view infeasibilities on page 298)
- run advanced operations (refer to Advanced Operations on page 242)
- measure the distances on the layout (refer to To measure on the canvas on page 374)
- tag the layout (refer to To tag a design point on page 339)
- print the symbolic layout (refer to To print a layout on page 342)

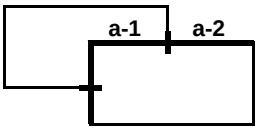
While you are browsing and analyzing the layout, you can set the following view options in the Compaction Browser: Zoom, Layer Filter, Device Filter, List of Hot Keys, List of Nets, Unrouted Nets, Net Annotations, and IO grid.

You can measure or zoom the layout using the toolbar. The bottom of the Compaction Browser displays information on the selected constraint or objective and the mouse button actions for the current cursor.

Some of the actions of the Compaction Browser can also be accessed from the background menu.

Browsing Compaction Constraints

Browsing compaction constraints in the Compaction Browser allows you to view the constraints generated by both the technology design rules and devices. You can view the constraints against an original edge or a constituent edge. Constituent edges are segments of original edges. They are created when the edge of a device overlaps another device or shape, as shown in the figure below. Edges a-1 and a-2 are constituent edges of the original edge a.



Device Edge Details

When a device edge is selected in the Compaction Browser, details of the edge are displayed in the status bar. The details include the following:

- the symbolic ID;
- the compaction ID;
- the layer;
- the net;
- the device ID;
- whether the edge is an internal (I) or external (X) edge;
- whether the edge is a left ([), right (]), top (^), bottom (_), or 45o (\) edge;
- whether the edge is an original (O) or constituent (C);

- the device ID; and
- the device name.

Example

```
Original Edge 1 {3683, METAL1, s0, 488, X, ^, O} --- 488
METAL1 Wire Constituent Edge 3682.2 {7958, METAL1, s0,
488, X, [, C} --- 488 METAL1 Wire
```

When an original edge that has constituents is selected, an X appears marking the edge as external edge regardless of any internal constituent edges.

Constraint Details

When a constraint is selected in the Compaction Browser, details of the constraint are displayed in the status bar or Relations dialog (depending on the type of constraint). The details displayed depend on the type of constraint as well. For example, the details for a simple constraint include the following:

- whether the constraint is vertical (|), horizontal (-), or diagonal (\);
- name of the constraint and the layers involved or the ID and name of the device which creates the constraint;
- the edges involved; and
- the minimum and maximum values involved.

Example 1 Simple Constraint

```
Simple: - Extension(nwellbar,ndiff) (E160,E26) [0.28,INFINITY]
```

If the selected constraint is a separation constraint with common run and/or width dependant conditions, the More button in the status bar is enabled. Although the constraint details are displayed in the status bar, you can click More to display the constraint details in the Constraints dialog box. If you do, the source and target shapes of the constraints are highlighted in the Compaction Browser. The source shape's contours are outlined in green and the target shape's contours are outlined in red. The constraint's source and target shape pairs are listed in the Constraints dialog box. If there is more than one pair, select the pair you would like to view.

The details for a separation constraint with common run and/or width dependant conditions include the following:

- whether the constraint is vertical (|), horizontal (-), or diagonal (\);
- the separation constraint and the layers involved or the ID and name of the device which creates the constraint;
- the edges involved;
- the minimum and maximum values involved; and
- the minimum common run value(s) (CR) and/or the minimum width value(s) (WD) with the layer the condition is dependant on, and the minimum separation value(s) (Sep).

Example 2 Separation Constraint

```
Simple: - Separation(METAL1,METAL1)(E1022,E988) [0.18,INFINITY]
(CR:0.52,WD:METAL1 0.18,Sep:0.17) (CR:0.60,WD:METAL1 0.23,
Sep:0.25)
```

To browse compaction constraints

To browse compaction constraints, do the following:

1. In the Cell Browser, click on a compacted cell design point   .
   The design point menu appears.
2. Select Open Compaction Browser.
   The Compaction Browser appears.

   Note: You can also open the Compaction Browser by double-clicking on a compacted cell design point.

3. Click  and  .
4. Select a device.
   The device is highlighted and all the edges that have constraints against them are marked in white.
5. Click  to browse constraints on original edges or  to browse constraints on constituent edges.

6. Select an edge.
   The constraints against the selected edge appear in pink and the edge details of the edge are displayed in the status bar.
7. Click  .
8. Select a constraint.
   The constraint turns yellow and its details are displayed in the status bar or Relations dialog (depending on the type of constraint). You can use the Relations dialog to select the components of conditional or compound constraints.

   Refer to Constraint Details on page 293.
9. Repeat the steps to continue browsing other constraints.

   Note: At any point in browsing the constraints, you can click  and filter which constraints are displayed and for which layers by using the Filter Constraints dialog that appears.

To filter constraints

Filtering constraints allows you to view constraints in the Compaction Browser based on layers or constraint types.

To filter constraints, do the following:

1. In the Compaction Browser, select Preferences > Filter *or* click  .
   The Filter Constraints dialog box appears.
2. Select the layers or constraint types you would like to view.
   The specified constraints are displayed in the Compaction Browser.

Browsing Compaction Objectives

Browsing compaction objectives in the Compaction Browser allows you to view the specific objectives the compactor is attempting to solve.

Objective Details

When an objective is selected in the Compaction Browser, details of the objective are displayed in the status bar. The details include the following:

- the name of the objective the terms are associated with,
- the device that generated the constraint and its ID number, and
- the directional force between the two edges represented in the format: edgeNumber x-weight y-weight.

In the example below, edge 1186 applies a force of 50 in the x-direction and 0 in the y-direction while edge 1184 applies a force of -50 in the x-direction and a 0 in the y-direction.

Example 3 Compaction Objectives

```
shrinkCovers, pdiff Contact(132) [E1186 50 0, E1184 -50 0]
```

To browse compaction objectives

To browse compaction objectives, do the following:

1. In the Cell Browser, click on a compacted cell design point   .
   The design point menu appears.
2. Select Open Compaction Browser.
   The Compaction Browser appears.

   Note: You can also open the Compaction Browser by double-clicking on a compacted cell design point.

3. Click  and  .
4. Select a device.
   The device is highlighted and its objectives appear in green.
5. Click  .
6. Select an objective.
   The objective turns yellow and its details are displayed.

For more information, refer to Browsing Compaction Objectives on page 295.

7. Repeat the steps to continue browsing other objectives.

   Note: At any point in browsing the objectives, you can filter which objectives are displayed using the drop-down list on the toolbar.

Viewing the Critical Path

If the compaction constraints are met during the Automated Transistor Layout (ATL) and/or Migrate GDS process, then a feasible layout is generated and you can view its critical path in the Compaction Browser.

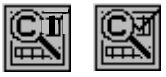
The critical path is based on the @minimizeWidth objective, which consists of a set of constraints from the left edge of the boundary to the right edge. Removing any of these constraints can help reduce the cell width.

You can change the objective the critical path is based on through AL (Application Language) using the annotateObjective data member from the CellCompactor class. However, if an objective other than @minimizeWidth is defined, the set of constraints that appear do not form an actual path. Removing any of these constraints could improve the objective, but to which degree is based on the individual constraint.

To view the critical path

Viewing the critical path allows you to analyze the constraints that form the path.

To view the critical path, do the following:

1. In the Cell Browser, click on a compacted cell design point  . The design point menu appears.
2. Select Open Compaction Browser.
   The Compaction Browser appears.

Note: You can also open the Compaction Browser by double-clicking on the compacted cell design point.

3. Select View > Show Critical Path.
   The critical path appears.

   Note: By default, the critical path is already displayed when you first open the Compaction Browser.

4. Click  .
5. Select a segment of the critical path.
   The segment turns yellow and the constraint details are displayed.

   For more information on constraint details, refer to Constraint Details on page 293.
6. Repeat step 5 to continue viewing the details of the critical path.

Viewing Infeasibilities

If the technology requirements and compaction constraints cannot be met during the Automated Transistor Layout (ATL) and/or Migrate GDS process by the compactor, then an infeasible layout is generated. You can view the infeasibilities in the Compaction Browser. The infeasibilities show the constraints that prevented a feasible layout from being generated.

For users that are running the advanced compact operation, you have the option of relaxing a set of constraints so that a feasible layout can be generated. When running the design step, select the Relax Infeasible Constraints option on the Cell Compact dialog and specify which constraints can be ignored.

To view infeasibilities

To view infeasibilities, do the following:

1. In the Cell Browser, click on an infeasible compaction design point  .

2. Select Open Compaction Browser.
   The Compaction Browser appears.

   Important: You can also open the Compaction Browser by double-clicking on the compacted cell design point.

3. Select View > Show Infeasible Path.
   The infeasibilities appear in red.

4. Click  .

5. Select an infeasibility.
   The infeasibility turns yellow and its details are displayed. If the details are long, they appear in a separate Description dialog box.

6. Repeat step 5 to continue viewing the details of the infeasibilities.

Submitting Jobs

Cadabra allows you to submit jobs to your localhost as a background process or to scheduling software for running cells and design points across a network of computers. If you are using job scheduling software, it must be built into Cadabra through the AL interface. (Refer to the Scheduler, SchedulerTemplate, and SchedulerDB class documentation in the *Cadabra AL Reference Guide*.) However, Cadabra does provide a built-in interface for LSF and SGE.

When jobs are submitted to the localhost, they are placed in a queue and are run in sequence in the background. If a job ends prematurely due to license unavailability, it is re-queued. Concurrent jobs can be run, but only based on the license availability and the specified *"Maximum number of jobs"* option. Jobs that have been submitted to the localhost will continue to execute in the background even if you exit Cadabra.

You can submit jobs on cells to scheduling software from the Cadabra window, the Cell View window and the Cell Edit window. You can submit jobs on design points from the Cell Browser. When jobs are submitted to job scheduling software, they are placed in a queue and, as machines become available, Cadabra is launched in a "no windows" mode and the jobs are processed.

Caution: If a Cadabra license is not available when a job is ready to be run, the job fails. The LSF scheduler option *"Wait for License Availability Before Running Jobs"* can be used to

avoid jobs failure in situations where computing resources are available but licenses are not. If you disable this option, or if you are using a different scheduling software, we recommend that you ensure that the number of computing resources for running a job does not exceed the number of Cadabra licenses you have.

The main Cadabra window displays and automatically updates the status of your job through the Job Status property (refer to Job Status on page 209).

To submit jobs

The following sections contain information on how:

To submit jobs from the Cadabra window

To submit jobs from the Cadabra window, do the following:

1. In the Cadabra window, select the cells to submit.

   Shortcut: You can select multiple cells by holding down the control key and clicking on each cell.

2. Select Cells > Jobs > Submit Jobs.
   The Submit Jobs dialog box appears.
3. Set the options (refer to Job Scheduler Options on page 303).
4. Click Submit.

   Result: The specified job is sent to run in the background of the localhost or to the queue. The status is displayed under Job Status in the main Cadabra window.

   Note: Jobs launched through the job scheduler always open cells in append mode. If you have a read-write lock on a cell, and you submit a job to the job scheduler, you will be prompted to save the cell and the access mode is switched to append. If you have an append lock on a cell and you submit a job to the job scheduler, you will be prompted to save the cell and the access mode remains as append.

Caution: Once a cell is run through the job scheduler, the library is automatically saved. If you want to run cells without automatically saving the resulting changes to the library, use Cells→Run instead.

To submit jobs from the Cell View or Cell Edit windows

To submit jobs from the Cell View or Cell Edit windows, do the following:

1. In either the Cell View window or the Cell Edit window click on the canvas and select Job > Submit Job from the background menu.
   The Submit Jobs dialog box appears.

   Note: When submitting jobs from the Cell Editor, a pop-up window appears and asks you if you want to save the library. This is because a new design point is created when the Cell Editor is invoked. After clicking Yes the Cell Editor window closes and the Submit Jobs dialog box appears.

2. Set the options (refer to Job Scheduler Options on page 303).
3. Click Submit.

   Result: The specified job is sent to run in the background of the localhost or to the queue. The status is displayed under Job Status in the main Cadabra window.

Note: Jobs launched through the job scheduler always open cells in append mode. If you have a read-write lock on a cell, and you submit a job to the job scheduler, you will be prompted to save the cell and the access mode is switched to append. If you have an append lock on a cell and you submit a job to the job scheduler, you will be prompted to save the cell and the access mode remains as append.

Caution: Once a cell is run through the job scheduler, the library is automatically saved. If you want to run cells without automatically saving the resulting changes to the library, use Cells→Run instead.

To submit a job on a design point

You can submit jobs to scheduling software on individual design points in the Cell Browser.

To submit a job on a design point, do the following:

1. In the Cell Browser, click on the design point that you want to run a job on and select Submit Job from the background menu.
   The Submit Jobs dialog box appears.
2. Set the options (refer to Job Scheduler Options on page 303).
3. Click Submit.
   The specified job is sent to run in the background of the localhost or to the queue. The status is displayed under Job Status in the main Cadabra window.

Job Scheduler Options

Option Type	Option	Description
General	Built-in Script	The specified built-in script is run on the cell(s).
	Name	The name of the built-in script that you would like to run on the cell(s). The available scripts depend on the licenses that have been installed. If you are submitting a job to the scheduler from a design point, ensure that you are using a script that is applicable to the selected design point.
	Configure	The dialog box for the specified script appears. You can set options for: ■ ATL (refer to ATL Options on page 221) ■ Migrate GDS (refer to Migrate GDS Options on page 220) ■ Migrate-ATL (refer to Migrate-ATL Options on page 218) ■ Import (refer to Import Options on page 222) ■ Place (refer to Place Options on page 224) ■ Route (refer to Route Options on page 227) ■ Compact (refer to Compact Options on page 231) ■ Finalize Layout (refer to Finalize Options on page 232) ■ Export (refer to Export Options on page 236) ■ Advanced Cell Compact (refer to Compaction Options on page 274) The Edit Cell/Layout Mapping option is disabled when setting the options for Migrate GDS, Migrate-ATL, and Import. The mappings must be set before submitting jobs to the scheduler. Mappings can be set by selecting Library°¨ Edit Cell/Layout Mapping. You must click Save as Defaults once your mappings are set. The options for the built-in scripts set at this point override any previously set defaults in Cadabra.

Option Type	Option	Description
	Effort Level	The effort level of the script, based on speed versus quality, in finding a solution.
General (*continued*)	Custom AL Script	The specified AL script is run on the cell(s). Specify the path and name of the AL script or click Browse to open a file browser. The script must return an AlObject that consists of two members: a tool name (i.e. Cadabra) and an AlFunction. The AlFunction must also contain two objects: a Cell Object and a Tool Area Parameter Object.
	Design Point	The design point(s) to run the specified script on. You can select the default or specify a design point by its ID or tag. The default depends on the specified script. For example, if you run ATL, the netlist design point is selected or if you run Route, the design point with the best placement is selected. You cannot specify a design point ID when you submit jobs from the Library Manager. This prevents any possible confusion that may arise when design point IDs change after a cell is saved. However, when you submit jobs from a Cell Browser, you can still specify a design point ID. **Note:** You cannot specify a design point ID when you submit jobs from the Library Manager. This prevents any possible confusion that may arise when design point IDs change after a cell is saved. However, when you submit jobs from a Cell Browser, you can still specify a design point ID.
Settings	Path Set	The current path. This path is set to default to the path of the current session.
	Job Output Directory	The directory in which to place the output files generated by Cadabra. The output directory automatically sets a default location based on the Path Set option. You can select a different output directory by clicking Browse.
	Overwrite Existing Outputs	Any existing output files are overwritten.

Option Type	Option	Description
Settings (*continued*)	Name	The name of the job scheduler to use. Select “localhost” to run the job in the background, or select a registered scheduling software to run the job across a network of computers. All the registered applications are available.
	Configure	The dialog for the specified scheduler appears. Cadabra provides basic interfaces to Platform Computing's LSFTM(Load Sharing Facility) and Sun microsystems® SGE (Sun Grid Engine) job scheduling software. Refer to LSF Scheduler Configuration Options on page 306 to configure LSF and SGE Configuration Options on page 308 to configure SGE. If you would like to use another scheduler, you must create a separate interface. If “localhost” is the specified job scheduler, a scheduler configuration dialog box appears with the following option: ▪ **Maximum number of jobs:** The maximum number of concurrent jobs that can be submitted to the “localhost”. The default value is 1. Synopsys recommends that this value not be set higher than the number of CPUs on your host, or the number of licenses available to you, whichever number is less. ▪ **Create Job Dependencies:** A dependency is created between parent cells and child cells among multiple job submissions.

LSF Scheduler Configuration Options

Option	Description
Resource Types	The type of operating system to run the jobs on. The list of available resources depends on the machines in the specified queue. If the operating system of the queue you would like to run a job on is different from the operating system you are running Cadabra on, you must select the appropriate resource type. Otherwise, the job will hang.
Queues	A list of the LSF queues that jobs may be submitted to. If no queues are selected, the jobs are sent to the default queue.
Begin Time [hh:mm]	The beginning time of the submitted job(s). If not set, the job will begin as soon as the queue is available.
Terminate Time [hh:mm]	The termination time of the submitted job(s). If not set, the job will run to completion.
CPU Time Limit [hh:mm]	The total CPU time the job(s) can use. This option is useful in preventing “runaway” jobs. If not set, the job will run to completion.
Send Dispatch E-mail	An e-mail is sent to the process owner when the job is submitted and begins execution.
Send Terminate E-mail	An e-mail is sent to the process owner when the job finishes.
Run in Exclusive Mode	The job is run alone on the queue host. Note that the selected queue must be configured to allow exclusive jobs.
Wait for License Availability Before Running Jobs	The license program ensures that required licenses are available before jobs are run. If this option is turned off, license availablity is not considered, which may cause jobs to fail if computing resources exceed the number of available licenses.
Create Job Dependencies	A dependency is created between parent cells and child cells among multiple job submissions.

Option	Description
Extra LSF Options	The additional LSF options you would like to place on the job. For example, the `- C <coreLimit>` sets a limit on core files. For other LSF options, refer to your LSF user documentation. LSF Documentation is also available on the web. The LSF scheduler configuration options can be customized in the lsf.al file located in: `$CADABRAHOME/al/schedulers`. In order to take advantage of the automatic requeuing for LSF, you must set the `CADABRA_LICENSE_UNAVAILABLE_EXIT_CODE` before launching the tool. Cadabra exits with the specified return code if a required license is unavailable. For more information, refer to the “Automatic Job Requeue” section in the *LSF Administrator’s Manual*.

SGE Configuration Options

Option	Description
Projects	A list of the available Sun grid system projects. Each project consists of a group of CPUs on which the jobs are run.
Begin Time [MMDDhhmm]	The beginning time of the submitted job(s). If not set, the job will begin as soon as the queue is available.
Send Dispatch E-mail	An e-mail is sent to the process owner when the job is submitted and begins execution.
Send Terminate E-mail	An e-mail is sent to the process owner when the job finishes.
Create Job Dependencies	A dependency is created between parent cells and child cells among multiple job submissions.
Extra SGE Options	The additional SGE options you would like to place on the job. For SGE options, refer to your *Grid Engine User's Guide*. SGE Documentation is also available on the web. The SGE scheduler configuration options can be customized in the sge.al file located in: `$CADABRAHOME/al/schedulers`. In order to take advantage of the automatic requeuing for SGE, you must set the `CADABRA_LICENSE_UNAVAILABLE_EXIT_CODE` before launching the tool. Cadabra exits with the specified return code if a required license is unavailable. For more information, refer to the *Grid Engine Administration Guide*.

To clear job status

Clearing the job status removes the values of any job-related properties for the specified cell(s). These properties include Job Status, Job Scheduler, and Job ID.

To clear job status, do the following:

1. In the Cadabra window, open the library you would like to clear the job status for by selecting Library > Open.

2. In the Cadabra window, select the cell(s) whose status is to be cleared.

   Important: You can select multiple cells by holding down the control key and clicking on each cell.

3. Select Cells > Jobs > Clear Job Status.
   The job status is cleared for the selected cell(s).

   Note: If you have previously submitted a job on a design point, you can clear the job status using the process above, or you can clear the job status from the Cell Browser by clicking the design point and selecting Clear Job from the background menu. This clears the job status for the cell in the Cadabra window.

   If you have previously submitted a job from the Cell View or Cell Edit window, you can clear the job status using the process above, or you can clear the job status from the the window by clicking on the canvas and selecting Job°¨ Clear Job from the background menu. This clears the job status for the cell in the Cadabra window.

To terminate jobs

To terminate jobs, do the following:

1. In the Cadabra window, open the library you would like to terminate jobs for by selecting Library > Open.
2. In the Cadabra window, select the cell(s) whose job is to be terminated.

   Important: You can select multiple cells by holding down the control key and clicking on each cell.

3. Select Cells > Jobs > Terminate Jobs.
   The jobs for the selected cell(s) are terminated.

   Note: If you have submitted a job on a design point, you can terminate the job status using the process above, or you can terminate the job from the Cell Browser by clicking the design point and selecting Terminate Job from the background menu. The job status for the cell is now displayed as Terminated in the Cadabra window.

If you have submitted a job from the Cell View or Cell Edit window, you can terminate the job using the process above, or you can terminate the job status from the Cell Browser by clicking the canvas and selecting Job°¨ Terminate Job from the background menu. The job status for the cell is now displayed as Terminated in the Cadabra window.

6

Viewing Results

Describes how results of layout creation can be viewed using the Cadabra, Cell Browser, Cell View, and View windows, and the various viewing options available in these interfaces. Provides information on viewing clone files using the Clone View window.

After running the GDS, Automated Transistor Layout (ATL), or Migrate-ATL processes, you can view the results of layout creation using the Cadabra, Cell Browser, Cell View and View windows.

If clone files were exported, you can also view the clone files using the Clone View window.

The following options are available for viewing results:

- The Cadabra window displays the properties (such as cell width or cell optimality) of each cell in the library. These cell properties are automatically updated during the Migrate GDS, ATL or Migrate-ATL processes.

  For more information, refer to Cadabra Window on page 312.

- The Cell Browser displays a cell's design tree. The design tree is a collection of partial layouts, which become more complete as you move down the tree. The best layout is highlighted by the cell marker. You can view a cell's design tree by opening the cell from the Cadabra window.

  For more information, refer to Cell Browser on page 315.

- The Cell View window displays a cell layout. You can view a cell layout by opening a cell's design point from its design tree.

  For more information, refer to Cell View Window on page 326.

- The View window displays multiple design points (that is, symbolic layouts or layouts) and source layouts. You can compare several design points, GDSII source layouts, or a design point to its corresponding source layout.

For more information, refer to View Window on page 328.

- The Clone View window displays the symbolic layout for a clone file. You can view a clone by loading a clone file and a physicalSpec object using the AL Window.

  For more information, refer to Clone View Window on page 336.

Cadabra Window

The main Cadabra window allows you to monitor and control the Migrate GDS, Automated Transistor Layout (ATL) and Migrate-ATL processing of a library.

From the Cadabra window, you can:

- access the Architecture and Technology Builders to set up a library;
- create and/or migrate libraries, and edit their cells;
- view and compare different layouts;
- change cell access modes;
- import or export cell properties;
- view library statistics; and
- access the AL Window and AL Debugger to run your own AL scripts.

The Cadabra window centralizes all the cell properties of a library in one location. As you make changes to a library, the Cadabra window is automatically updated. However, if there are multiple users working on a library, you should periodically update the library to view their changes as well. Update the library by choosing Update from the Library menu in the Cadabra window. If multiple libraries are open in the Cadabra window, you can update all open libraries by choosing Update All from the Library menu.

The access mode for the cell is displayed in the Lock column. If the cell is locked by another user, their user name appears in red. If you have a lock on the cell, the phrase “My lock” appears in blue.

As a layout designer or engineer, the Cadabra window is your primary location for migrating, creating, and editing cell libraries. Not only can you set up your architecture and migrate and create your libraries, but you can run basic layout operations provided by Cadabra and then hand-edit the cells if necessary. You can also run your own scripts in batch mode and monitor the progress and view

the generated layouts. You can add your own custom cell properties and have these displayed in the window.

As a manager, you might open Cadabra with a view license and use the Cadabra window to monitor the library development process. You could display only the cell properties that interest you and check the quality of each cell. You could also view a library's overall statistics and track the progress and rate of completion.

Library Statistics

Cadabra provides some basic library statistics that are described below. These can be viewed from the Cadabra window.

Library Statistic	Description
Number of Cells	The total number of cells in the library.
Average Number of MOSFETs	The average number of transistors per cell (that is, the total number of transistors in the library divided by the number of cells).
Maximum Number of MOSFETs	The number of transistors of the cell with the most transistors.
Library Density	The transistor density of the library (that is, the total number of transistors, including folded transistors, divided by the cell area in square millimeters divided by the number of transistors in a nand gate(4)).
Target Library Density	The target density of the library (that is, the total number of transistors divided by the target cell area in square millimeters divided by the number of transistors in a nand gate(4)).
Number of Cells Completed	The number of cells in the library that are completed.
Percentage of Cells Completed	The percentage of cells in the library that are completed (that is, the number of cells completed divided by the total number of cells in the library).

Library Statistic	Description
Total Run Time	The total time that the selected cells took to process. The time appears in the format: hh:mm:ss.
Average Run Time of Attempted Cells	The total run time of attempted cells divided by the number of attempted cells in the library. An attempted cell is a cell on which a script has been run and contains two or more design points. The time appears in the format: hh:mm:ss.

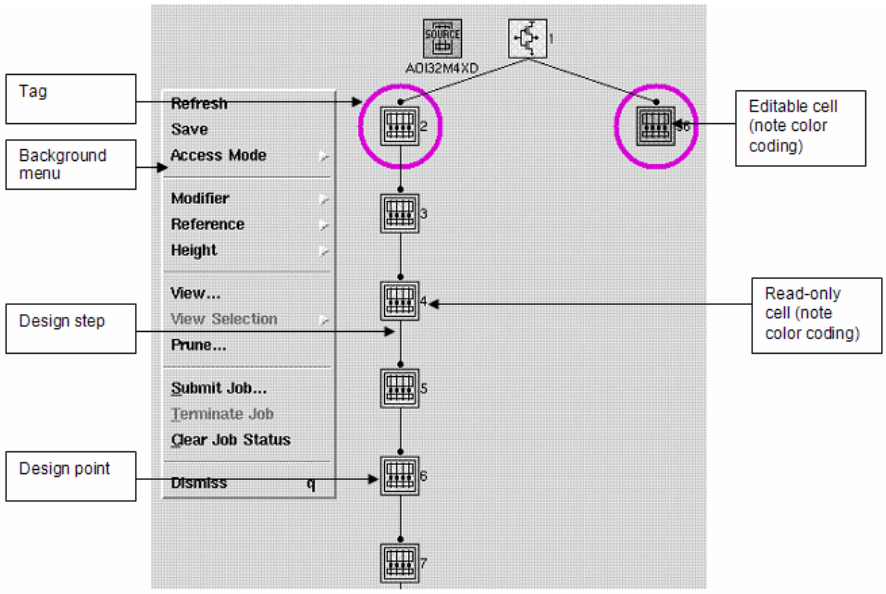
To view library statistics

To view library statistics, do the following:

1. In the Cadabra window, select the tab of the library you would like to view the statistics for.
2. Select Library > Statistics.
   The Library Statistics dialog box appears displaying the statistics for the selected library.

Cell Browser

The screenshot of a Cell Browser is as follows:



The Cell Browser window displays a cell's design tree. The details of the various items displayed in the Cell Browser are is follows:

- **Design tree:** Collection of design points that show the progress of the layout process.
- **Design points:** Partial designs that become more complete as you move down the tree. Applying an operation to a design point creates another, more finished design point.

  For more information, refer to Design Points on page 317.
- **Design steps:** Advanced operations that can be applied to design points.

  For more information, refer to Design Steps on page 317.
- **Design point tags:** Indicators that mark a design point as special in some way. The cell marker indicates the best layout generated. Only one marker can exist in the design tree.

For more information, refer to Design Point Tags on page 338 and Cell Marker on page 341

- **Background menu:** Offers a set of operations that work on the entire design tree, such as saving the cell, pruning the design tree, changing the cell's access mode, or comparing design points. You can display the background menu by clicking on a blank area of the window.

To open a cell

You can open a cell in the following modes:

- Read-Only: In this mode, you can view the cell's design tree regardless of whether or not the cell is being edited by another user.
- Read-Write: In this mode, you have read-write access and can modify the cell. If you open a cell in read-write mode, other users cannot open the cell in append mode.
- Append: In this mode, multiple users can modify the cell at the deisgn-point level. If you open a cell in append mode, other users cannot open the cell in read-write mode.

To open a cell, do the following:

1. In the Cadabra window, select the cell you would like to open.

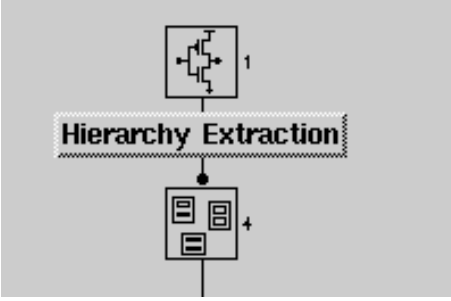
   Important: You can open multiple cells simultaneously by dragging the mouse over them, holding down the shift key and clicking on the first and last of a group, or holding down the control key and clicking on each cell.

2. Do one of the following:
   - Select Cells→Open→Read-Only
   - Select Cells→Open→Read-Write
   - Select Cells→Open→Append

   Result: The Cell Browser for the selected cell(s) appears.

   Important: You can close the cell by selecting Dismiss from the Cell Browser background menu.

Design Steps



Design steps are advanced operations that can be applied to a design point to create another more finished design point. In the Cell Browser, a design step is represented as a line between two design points.

You can click on a design step line to display the name of the design step or double-click on a design step line to display the values used in that design step.

Different design steps apply to different types of design points. For a list of design points and the operations available, refer to Design Points on page 317.

Design Points

Design points represent partial designs in a cell's design tree. The different types of design points represent the cell in its varying stages of completion. Most design points can be opened so you can view the layout at that point.

Certain design points can be singled out by tagging them with colored rings or design point tags.

You can perform operations on individual design points by clicking on the design point and selecting from the menu that appears. Each type of design point has different menu options.

Source Layout	Netlist	Configuration	Placed Cell
			
Routed Cell	**Compacted Cell**	**Layout**	
			

Source Layout Design Point

The source layout design point appears beside the netlist design point in the cell's design tree, if the cell is mapped to a source layout. The name of the layout appears below the source layout design point.

If the source layout is removed from the LayoutDB, the source layout design point will have an X on it, which indicates that the mapping is invalid.

From the source layout design point menu, you can:

- View with Source Layout (refer to To compare a design point to a source layout on page 331)
- Change Cell/Layout Mapping (refer to To change a cell-to-layout mapping on page 189)
- Remove Cell/Layout Mapping (refer to To remove a cell-to-layout mapping on page 190)

Netlist Design Point

The netlist design point is the first design point in the cell's design tree. It describes the cell's netlist (characteristics). If Cadabra, performs a folding operation, a folded netlist icon is shown.

From the netlist design point menu, you can:

Describe	Tag
Change Cell/Layout Mapping	Remove Tags
Remove Cell/Layout Mapping	Remove Tags Recursively
Migrate GDS	Advanced > Fold MOSFETs
ATL	Extract Hierarchy
Migrate-ATL	Import Layout
Import	Delete All Below
Place	
Export	
Submit Job	
Terminate Job	
Clear Job	

Configuration Design Point

The configuration design point is a partially-placed layout. A configuration is a collection of tiles generated during hierarchy extraction. The configuration set design point consists of multiple configurations. It can be generated by running Advanced > Extract Hierarchy on the netlist design point and setting the Max Number of Configurations option to greater than 1.

From the configuration design point menu, you can:

Open	Advanced > Fold Tiles
View with Source Layout	Merge Tiles
View with Reference Layout	Place Tiles
View with Optimal Layout	CellEdit
Submit Job	Delete
Terminate Job	Delete All Below
Clear Job	Prune Other Branches
Tag	
Remove Tags	
Remove Tags Recursively	

Placed Cell Design Point

The placed cell design point represents a cell once all the devices in the cell have been placed and is ready for routing. The devices can be viewed by opening the design point.

From a placed cell design point menu, you can:

- Open
- View with Source Layout
- View with Reference Layout
- View with Optimal Layout
- Route
- Compact
- Finalize Layout
- CellEdit
- Export
- Submit Job
- Terminate Job
- Clear Job
- Tag
- Remove Tags
- Remove Tags Recursively
- Delete
- Delete All Below
- Prune Other Branches
- Advanced > Optimize Placement
  - Generate Compaction Geometries
  - Align MOSFETs
- Pre-Routing Steps > Update Boundary
- Pre-Compaction Steps > Prepare Abutments
  - Add Multiple Gate Bends
  - Jog at Gates
  - Jog Wires Around Contacts
  - Match MOSFET Sizes
  - Optimize Horizontal Wires

Routed Cell Design Point


The routed cell design points represent a cell that has been routed. It can also represent a routed cell with ports (second icon).

From the routed cell design point menu, you can:

Open	Delete
View with Source Layout	Delete All Below
View with Reference Layout	Prune Other Branches
View with Optimal Layout	Advanced > Generate Compaction Geometries
Route	Cell Compact
Compact	Align MOSFETs
Finalize Layout	Pre-Routing Steps > Update Boundary
CellEdit	Pre-Compaction Steps > Prepare Abutments
Export	Add Multiple Gate Bends
Submit Job	Jog at Gates
Terminate Job	Jog Wires Around Contacts
Clear Job	Match MOSFET Sizes
Tag	Optimize Horizontal Wires
Remove Tags	
Remove Tags Recursively	

Compacted Cell Design Point

The compacted cell design point represents a cell that contains all of the required devices and has been compacted to reduce any extra space. All of the spacing rules are enforced. A 4 on the icon indicates that the compaction is DRC correct. A *C* on the icon indicates compaction shapes. You must convert them to routing geometries (icon without the *C*) before the design point can be routed or converted to a layout. A magnifying glass indicates that the compaction data has been saved and you can inspect the data, such as the critical path, constraints, edges, using the Compaction Browser. A slash through the icon indicates that the compaction, although feasible, has some DRC errors.

From the compacted cell design point menu, you can:

Open	Tag
View with Source Layout	Remove Tags
View with Reference Layout	Remove Tags Recursively
View with Optimal Layout	Advanced > Open Compaction Browser
Route	Cell Compact
Compact	Generate Routing Geometries
Finalize Layout	Generate Layout
Submit Job	Delete
Terminate Job	Delete All Below
Clear Job	Prune Other Branches
Cell Edit	

Layout Design Point

The layout design point is the final layout. You can export the cell using any exporter defined during the planning phase (refer to To set the exporter on page 158).

From the layout design point menu, you can:

Open	Advanced > Final Layout Steps > Add Layout Ties
View with Source Layout	Add Implants
View with Reference Layout	Fill Notches
View with Optimal Layout	Merge Shapes
Measure	Path Shapes
Export	Reshape Gates
Submit Job	Text Annotation
Terminate Job	Adjust Overlapping Tie Diffusions
Clear Job	Delete
Tag	Delete All Below
Remove Tags	Prune Other Branches
Remove Tags Recursively	
Mark/Unmak Layout	

To open a design point

Opening a design point allows you to view the layout. You cannot view a cell before it is imported or placed.

To open a design point, do the following:

1. In the Cell Browser, click and hold on the design point you would like to open.
   The design point menu appears.
2. Select Open.
   A Cell View window appears displaying the cell layout.

   Note: You can close the Cell View window by selecting Design Point > Dismiss.

To view multiple design points

Multiple design points can be selected from the Cell Browser for viewing in the View window. This allows you to view and/or compare any design point layout with other design point layouts from a specified cell.

To view multiple design points, do the following:

1. In the Cell Browser, select the design points you would like to view by holding down the Shift key while clicking on multiple design points.
   The selected design points are highlighted in yellow.

   Important: Multiple design points can also be selected by drawing a box around them. To do this, hold down the shift key while dragging the cursor around a group of design points

2. Click anywhere on the Cell Browser canvas background.
   The Cell Browser background menu appears
3. Select View Selection > Selected Design Points.
   The View window opens displaying the design point layouts.

   It is also possible to view the selected design points with the source layout, if one exists, or with the optimal layout. Select either View Selection > With Source Layout or View Selection > With Optimal Layout.

   Important: To de-select an individual design point, click on it again while holding down the Shift key. To de-select all of the design points, right-click anywhere on the Cell Browser canvas.

To delete a design point

Deleting unnecessary design points allows you to explore the design tree better.

To delete a design point, do the following:

1. In the Cell Browser, click and hold on the design point you would like to delete.
   The design point menu appears.

2. Select Delete *or* Delete All Below.
   A Question dialog box appears to confirm the removal.
3. Click Yes.
   The selected design point or all the design points below it are permanently deleted.

To prune the design tree

Pruning the design tree allows you to remove unused branches of the tree. Design points are pruned based on design point tags.You must tag a design point in each branch you would like to keep.

To prune the design tree, do the following:

1. From the Cell Browser background menu, select Prune.
   The Keep Design Points dialog box appears.
2. Select a design point type from the Design Point list box.
3. Select one or more tags.

   Important: You can select multiple tags by dragging over them or holding down the shift key and clicking on the first and last of the group. You can also hold down the control key and click on each tag.

4. Click OK.
   Any design points with the selected tag(s) will be kept. Other branches are permanently removed.

   Shortcut: Select Prune Other Branches from the menu of a design point in the branch to be kept. All other branches are removed.

Cell View Window

The Cell View window allows you to view a layout (or design point) selected from the cell's design tree.

From the Cell View window, you can:

- measure the distances on the layout;
- print the layout; and
- tag the layout.
- export a clone of a symbolic layout.

If you have an editing license and have the cell open in read-write mode, you can also:

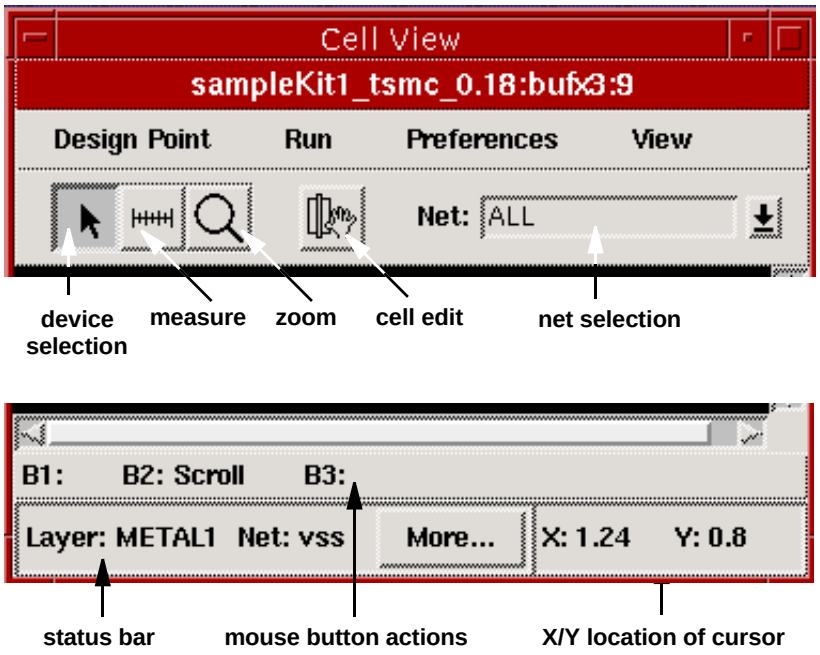
- run cell creation (that is, route, compact, finalize layout, measure, or migrate design tree);
- submit jobs to scheduling software;
- run advanced operations; and
- access the Cell Editor and Compaction Browser.

If the cell is open in read-only mode, you can change the access mode to read-write by selecting Design Point > Access Mode > Read-Write.

When you run an advanced edit from the Cell View window, a new design point is created on the cell's design tree.

While you are viewing your layout, you can set the following view options in your Cell View window: Zoom, Layer Filter, Device Filter, Unrouted Nets, Net Annotations, IO Grid, List of Hot Keys, and List of Nets.

You can select, measure or zoom all parts of the layout using the toolbar. The bottom of the Cell View window displays information on the selected device and mouse button actions for the current cursor.



View Window

The View window allows you to compare design points, source layouts, and a design point to its corresponding source layout, reference layout, or optimal layout. The design points, source layouts, reference layouts, and optimal layouts are displayed in individual frames.

Although you can load an infinite number of layouts in the View window, you can only display a maximum of sixteen frames at a time. The Frames menu lists all of the loaded layouts.

The actions available in the View window are only applicable to the active frame. From the View window you can:

- measure the distances on the layout;
- export a layout; and
- print the layout(s).

You can also set the following view options in your View window: Zoom, Layer Filter, Device Filter, Net Annotations, IO Grid, List of Hot Keys, Nets, Unrouted Nets, and Text Labels.

Note: If you are viewing a source layout, the Net Annotations, IO Grid, and Unrouted Nets view options are disabled.

As in the Cell View window you can select, measure, or zoom all parts of the layout using the toolbar. The bottom of the View window displays information on the selected device and mouse button actions for the current cursor.

Managing Frames

The frames in the View window can be split, viewed in full, or removed from display. You can also re-order the frame tiling format.

Splitting frames in the View window allows you to view multiple design points or source layouts or multiple frames of the same design point or source layout in one window. You can split the frame by selecting Layout > Split Frame Left/Right *or* Split Frame Top/Bottom. You can return to the previous frame split by selecting Layout > Last Frame Split.

Note: Since only sixteen frames can be displayed at a time in the View Window, the Split Frame menu items are disabled once you reach this maximum.

Viewing a full frame layout allows you to view a single design point or source layout in one window. You can view a full frame by selecting Layout > Full Frame. The active frame fills the full window and any other frames are removed from display.

Removing frames allows you to reduce the number of displayed frames and, if necessary, make room for displaying other frames. You can remove a frame by selecting Layout > Remove Frame. Removed frames are still available from the Frames menu. To display a frame, select Frames and the required layout.

The format of the frame tiling can be changed by selecting Frames > Change Tiling. This opens the View Window Tiling dialog and allows you to select either Smart size tiling, which displays the design point layouts according to the size of the cell(s), or Fixed size tiling, which displays the design point layouts based on the specified number of rows and columns for tiling, in equal sized frames.

You may also open design points from the View window by selecting Layout > Open in Cell Viewer. The design points are opened in the Cell View window.

Important: You can also manage frames using the pop-up menu and hot keys.

Important: You can display multiple frames by splitting a frame, then selecting a layout from the Frames menu.

To view or compare design points

Comparing design points allows you to view multiple symbolic layouts and layouts based on design point tags from one or more cells.

To view or compare design points, do the following:

1. In the Cadabra window, select the cell(s) containing design points you would like to view.
2. Select Cells > View.
   The View Design Points dialog box appears.
3. Select a design point tag from the Design Point Type listbox.

   Important: You can select several design point tags by holding down the control key and clicking on each tag.

4. Select a Tiling option:
   Smart size tiling which displays the design point layouts according to the size of the cell(s) in the View window.
   Fixed size tiling which displays the design point layouts based on the specified number of rows and columns for tiling in the View window.
5. Select View with Source Layout if you would like to view the source layout(s) with the design point layout(s) for the specified cell(s).
6. Click OK.
   The View window appears displaying the selected design point(s).

To view or compare source layouts

To view or compare source layouts, do the following:

1. In the Cadabra window, select Source Layouts > Open.
   The Source Layouts dialog box appears.
2. Select the source layout(s) you wish to view.

   Important: You can select several layouts by dragging the mouse over them, holding down the shift key and clicking on the first and last of a group, or holding down the control key and clicking on each layout.

3. Click View.
   The View window appears displaying the selected source layout(s).

   Note: You can have up to sixteen layouts displayed in the View window.

   Important: You can also view a source layout from the Cell Browser by selecting View Source Layout from the source layout design point menu or double-clicking on the source layout design point.

To compare a design point to a source layout

Comparing design points to source layouts allows you to view design points with their corresponding source layouts.

To compare a design point to a source layout, do the following:

1. In the Cadabra window, select the cell containing design points you would like to view.
2. Select Cells > Open.
   The Cell Browser for the selected cell appears.
3. Click and hold a design point.
   The design point menu appears.
4. Select View with Source Layout.
   The View window appears, displaying the design point and its source layout in individual frames.

You can also compare design points and source layouts directly from the Cadabra window. This method allows you to compare several design points to a source layout.

1. In the Cadabra window, select the cell containing design points you would like to view.
2. Select Cells > View.
   The View Design Points dialog box appears.
3. Select a design point tag from the Design Point Type listbox.

   Important: You can select several design point tags by holding down the control key and clicking on each tag.

4. Select a Tiling option:
   Smart size tiling which displays the design point layouts according to the size of the cell(s) in the View window.
   Fixed size tiling which displays the design point layouts based on the specified number of rows and columns for tiling in the View window.
5. Click the View with Source Layout checkbox.
6. Click OK.
   The View window appears, displaying the design point(s) and its source layout in individual frames.

To compare a design point to an optimal layout

Comparing design points to source layouts allows you to view design points with their corresponding optimal layouts.

To compare a design point to an optimal layout, do the following:

1. In the Cadabra window, select the cell containing design points you would like to view.
2. Select Cells > Open.
   The Cell Browser for the selected cell appears.
3. Click and hold a design point.
   The design point menu appears.
4. Select View with Optimal Layout.
   The View window appears, displaying the design point and its optimal layout in individual frames.

You can also compare design points with the corresponding optimal layout from the Cell Browser. This method allows you to compare several design points to an optimal layout.

1. In the Cell Browser, select the design points you would like to view by holding down the Shift key while clicking on multiple design points. The selected design points are highlighted in yellow.

   Important: Multiple design points can also be selected by drawing a box around them. To do this, hold down the shift key while dragging the cursor around a group of design points

2. Click anywhere on the Cell Browser canvas background. The Cell Browser background menu appears
3. Select View Selection > With Optimal Layout. The View window opens displaying the design point layouts with the optimal layout.

To compare a design point to a reference layout

Comparing design points to reference layouts allows you to view design points with their corresponding reference (parent) layouts.

To compare a design point to a reference layout, do the following:

1. In the Cadabra window, select the cell containing design points you would like to view. The cell must have an associated completed reference cell or reference clone(s).
2. Select Cells > Open. The Cell Browser for the selected cell appears.
3. Click and hold a design point. The design point menu appears.
4. Select View with Reference Layout. The View window appears, displaying the design point and its reference layout in individual frames.

You can also compare design points with the corresponding reference layout from the Cell Browser. This method allows you to compare several design points to a reference layout.

1. In the Cell Browser, select the design points you would like to view by holding down the Shift key while clicking on multiple design points. The selected design points are highlighted in yellow.

   Important: Multiple design points can also be selected by drawing a box around them. To do this, hold down the shift key while dragging the cursor around a group of design points

2. Click anywhere on the Cell Browser canvas background. The Cell Browser background menu appears
3. Select View Selection > With Reference Layout. The View window opens displaying the design point layouts with the reference layout.

To export a clone from the Cell View window

Cloning captures the placement and routing information of a symbolic layout design point so that the same placement and routing can be re-used for another cell. The cell information is saved in a clone file *(.cln)*. Refer to Do cloning for restrictions on use of cloned symbolic layouts.

To export a clone from the Cell View window, do the following:

1. In the Cell View window, select Design Point > Export. The Export dialog box appears.
2. Select Clone and move it to the Used column using the “<“ “>” buttons.
3. Select Clone in the Used column. The Configure Exporter button is enabled.
4. Click Configure Exporter. The Exporter Configuration dialog box appears for the exporter you have selected.
5. Set the options (refer to Export Clone Options on page 336).

6. Click OK.
   A clone file *(*.cln)* is saved to disk. This clone file can be used during hierarchy extraction of similar netlists to re-use placement and routing information.

   Note: You can also clone a portion of a symbolic layout. For more information on cloning specific devices, refer to To clone part of a layout.

Export Clone Options

Option	Description	
Clone Name	Overview	The descriptive name of the clone. By default, this is the cell name.
MOSFET Placement Priority	Overview	The order in which MOSFETs are placed. This placement order is important for placing other MOSFETs that are aligned to the first (primary) MOSFET. Primary MOSFETs are listed first and placed before secondary MOSFETs.
	Why set this option?	When the MOSFETs in the target cell have a different width, the alignments are used to maintain the correct placement of MOSFETs. Secondary MOSFETs are placed after their primary MOSFET and are either top or bottom-aligned to their primary. This change in width can affect the alignments. The placement priority allows you to identify which MOSFETs have alignments that are more crucial and should therefore be placed first. In the event that a design rule violation occurs or the MOSFET alignment in the source layout cannot be preserved in the target cell, clone instantiation is suspended and the next clone file (if any) is automatically used.
Export File	Overview	The clone is saved in this file. By default, the filename ends in .cln.

Clone View Window

The Clone View window allows you to view an exported clone file instantiated in a given architecture.

From the Clone View window, you can:

- measure the distances on the layout; and
- print the layout.

While you are viewing your clone, you can set the following view options in your Clone View window: Zoom, Layer Filter, Device Filter, Unrouted Nets, Net Annotations, IO Grid, List of Hot Keys, List of Nets. You can also set the option “Show background devices”, which toggles to display or hide background devices such as rails, well, and boundary on the canvas.

You can select, measure or zoom all parts of the clone using the toolbar. The bottom of the Clone View window displays information on the selected device and mouse button actions for the current cursor.

To view a clone

Opening a clone file in the Clone View window allows you to view the symbolic layout for the clone in relation to a physical specification object.

To view a clone, do the following:

1. Open the AL Window by selecting Tools > AL Window from the Cadabra window.
   The AL Window appears.
2. Enter the following commands in the lower-half of the AL Window:

```
physicalSpec = getLibrary( “LibraryName” )->physicalSpec;
c = loadClone( “Clones/cloneName.cln” );
c->openView( physicalSpec );
```

   Note: Press Shift-Enter after each line.

   Note: You can close the Clone View window by selecting Clone > Dismiss.

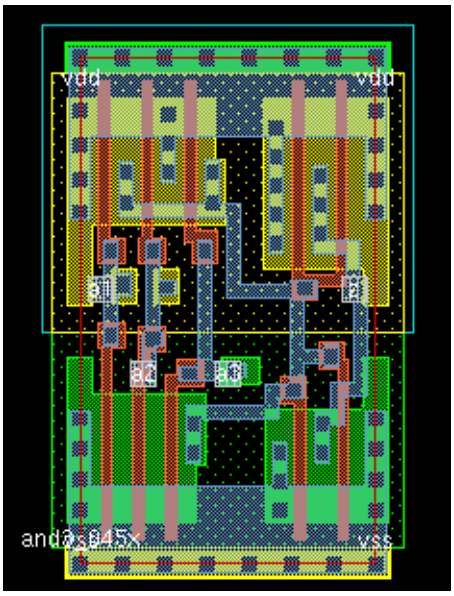
To view text labels

Viewing text labels allows you to view the labels for source layouts. This feature is useful for viewing port locations on source layouts migrated from a GDSII file.

Note: This view option is not relevant to viewing design point layouts.

To view text labels, do the following:

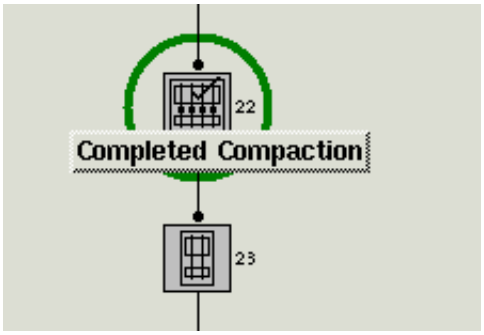
- In the View window, select View > Show text labels. The text labels appear on the selected frame.



Design Point Tags

Design point tags mark a design point as special in some way. For example a design point can be marked as the best layout, a layout to be compared with another one, a layout to be preserved during pruning of the design tree.

Tagging places a colored circle around the design point. You can click on the tag to show the text of the tag. If multiple tags are applied to a design point, the circle shows the colors of the different tags.



Standard Design Point Tags

Cadabra provides the following standard design point tags:

- Placement 1, Placement 2, Placement 3, Placement 4, Placement 5, are the the first, second, third, fourth, and fifth placements selected.
- Candidate Placement, indicates all of the symbolic layout design points selected after Place is run.
- Alternate Alignment, placement is attempted with an alternative MOSFET alignment.
- Incomplete Route, some hand routing is required.
- Completed Route, a completely routed cell. You can compact this layout.
- Incomplete Compaction, the layout could not be compacted.
- Completed Compaction, a compacted cell. You can finalize this layout.
- Incomplete Import, the layout could not be imported.
- Completed Import, an imported cell. You can compact this layout.
- Reference Clone, a completely compacted cell chosen for reference.
- Finalize Layout, the final layout.

Using Design Point Tags

Design point tags are used to select design points for some common operations, such as pruning or comparing design points.

When pruning design trees, you can indicate which branches should be kept by tagging a design point on that branch. Then, during pruning, you can select those tags. Tagged design points are not removed.

When comparing design points, you can tag the design points to be compared. Then, you can select those tags in the View dialog box.

To tag a design point

Tagging a design point allows you to mark it for further work, for example, as a branch for pruning, or comparison with other design points.

To tag a design point, do the following:

1. In the Cell Browser, click and hold on the design point you would like to tag. The design point menu appears.

2. Select Tag.
   A cascaded menu of the tags available for this type of design point appears.
3. Select the tag you would like to apply.
   The tag appears on that design point.

   Note: If a tag has already been applied to a design point, the checkbox next to the tag entry in the menu will be colored. You can remove a design point tag by reselecting the tag from the cascading menu.

   Important: You can also add a design point from the Compaction Browser, Cell View or Cell Edit windows by selecting Design Point > Tag and the appropriate tag.

To remove design point tags

To remove all tags on a design point, do the following:

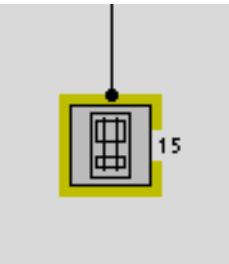
1. In the Cell Browser, click and hold on the target design point.
   The design point menu appears.
2. Select Remove Tags from the design point menu.
   All tags on the current design point are removed.

To remove all tags on a branch:

1. In the Cell Browser, click-hold on the target design point.
   The design point menu appears.
2. Select Remove Tags Recursively from the design point menu.
   All tags from the current design point to the leaves are removed.

   Caution: Some tags are automatically applied during Migrate GDS, ATL and Migrate-ATL. You should not remove these unless their design points will not be processed further.

Cell Marker



Running Migrate GDS, ATL or Migrate-ATL adds a yellow cell marker, which indicates the best layout generated. Only one marker can be present in a design tree and it can only be applied to a layout design point. Cell information, such as status and width, are based on this design point. If you create a better layout (for example, while hand-editing a cell), you can move the marker to another design point.

To mark a layout

The cell marker indicates the best layout available in a design tree. If you have hand-edited a cell and created a better layout, you may want to mark that layout. The marker can only be used on a layout design point.

To mark a layout, do the following:

1. In the Cell Browser, click and hold on the design point of the layout you would like to mark.
   The design point menu appears.
2. Select Mark Cell from the design point menu of the layout you would like to mark.
   The design point icon is outlined in yellow.

   Note: The cell status and width displayed in the Cadabra window are based on the marked design point.

   Important: You can remove the marker from a design point by selecting Unmark Cell from the design point menu.

To print a layout

To print a layout, do the following:

1. In the Cell View or Cell Edit window, select Design Point > Print *or* in the View window, select Layout > Print or Layout > Print all Frames *or* in the Compaction Browser, select Print from the background menu.
   The Print dialog box appears.
2. Set the options.
3. Click OK.
   The page is printed or saved to disk.

   Note: You can print the entire design tree by selecting Print from the Cell Browser background menu.

   Note: If you select Layout > Print all Frames in the View window, all of the design point layouts are printed as they are tiled, but without the scroll bars.

Print Options

Printer: The image is sent directly to the printer indicated.

File: The image is saved to the postscript file indicated.

Print in: The color tone to print the file in.

Orientation: The orientation for the printed file. Select Portrait for a tall page or Landscape for a wide page.

Print Size: The size of the image. The default size fits a standard 8.5 x 11 inch page.

To zoom in the Compaction Browser

Zooming allows you to view the full area or focus on specific areas of the canvas in the Compaction Browser.

To zoom in the Compaction Browser, do the following:

1. In the Compaction Browser, click on the canvas.
   The background menu appears.
2. Select Zoom In, Zoom Out or Full View.
   The focus changes to the zoom selected.

7

Hand-Editing Layouts

Provides step-by-step instructions for hand-editing sub-optimal cells using the Cell Edit window.

After running any of the automated processes (that is, Migrate GDS, ATL, or Migrate-ATL), you may have some sub-optimal cells in your library. That is, the cells were not completed or did not meet the set target width. You can hand-edit these cells in the Cell Edit window.

From the Cell Edit window, you can:

- Edit individual or grouped devices in the layout.

  Refer to Editing Devices on page 347.
- Run route, compact, or finalize layout
- Submit jobs to scheduling software.

  Refer to Submitting Jobs on page 299.
- Run advanced operations.

  Refer to Advanced Operations on page 242.
- Measure the distances on the layout.

  Refer to To measure on the canvas on page 374.
- Tag the layout.

  Refer to To tag a design point on page 339.
- Export a clone of a symbolic layout design point.

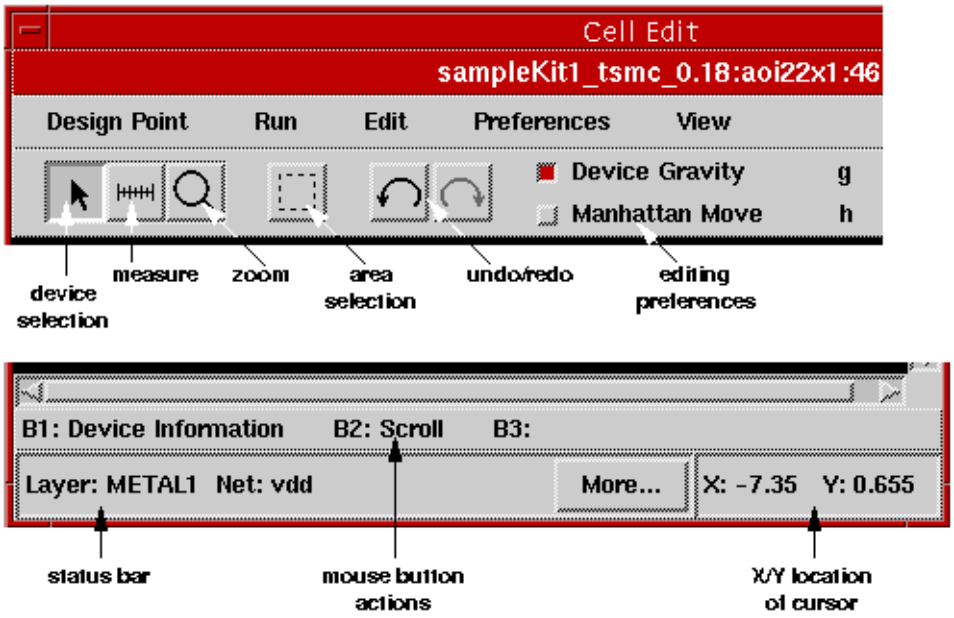
  Refer to To export a clone on page 370.
- Print the layout.

  Refer to To print a layout on page 342.

When you run an advanced edit from the Cell Edit window, a new design point is created on the cell's design tree. However, you can run some of the advanced edits in place by selecting them from under the Run > In Place menu.

While you are hand-editing your layout, you can set the following view options in your Cell Edit window: Zoom, Layer Filter, Device Filter, Unrouted Nets, Net Annotations, IO Grid, List of Hot Keys, List of Devices, List of Nets, and Routing Conflicts.

You can select, measure or zoom the devices of the layout using the toolbar. The bottom of the Cell Edit window displays information on the selected device and mouse button actions for the current cursor.



Some of the actions of the Cell Edit window can also be accessed from the background menu.

To hand-edit a layout

To hand-edit a layout, do the following:

1. In the Cadabra window, select the cell you would like to hand-edit.
2. Select Cells > Open.
   The Cell Browser for the selected cell appears and the cell's access-mode is changed to read-write.

3. Click on the design point you would like to hand-edit.
   The design point menu appears.
4. Select Cell Edit from the design point menu.
   The Cell Edit window with the layout of the selected design point appears and a copy of the selected design point is created in the Cell Browser.
5. Perform the necessary edits.
6. Select Design Point > Dismiss.
   The Cell Edit dialog box closes and the Cell Browser is updated.

   Important: You can also access the Cell Edit window for hand-editing a layout from any Cell View window by selecting  .

Editing Devices

Hand-editing a layout generally requires adding and/or editing devices. All devices, except for wires, are added by defining a single-point. Wire devices are added by defining multiple-points.

Following are the actions you can perform on the devices in the Cell Edit window:

Add Devices

Add Wire Devices

Change Layers

Update Routing Geometries

Reshape Devices

Flip Devices

Rotate Devices

Resize MOSFETs

Fold MOSFETs

Unfold MOSFETs

Rip Devices

Make Devices Unrippable

Merge MOSFETs

Modify Device Properties

Resize Wires, Contact Covers, and Port Covers

Add Gate Bends

Move Gate Bends

Add Wire Jogs

Delete Devices

If an editing action violates any design rules, an error message appears in the status bar of the Cell Edit window and the action is not performed.

If you add a device that has modified routing geometries due to routing style preferences or electromigration constraints, the routing geometries displayed in the Cell Editor may not accurately reflect the routing geometries that will appear in the final layout. For more information, refer to Modified Routing Geometries on page 351.

While you are editing the devices of your layout, you can also set the following editing preferences:

- Allowing 45^0 wires
- Snapping Devices to a Grid
- Device Gravity
- Manhattan Move
- Show Detailed Routing Geometries

To add a device

Most devices, except for wires, are added by defining a single-point. You can add wire devices by defining multiple-points.

To add a device, do the following:

1. In the Cell Edit window, select a Net.
2. Select Edit > Add Device and the device you would like to add.

   Result: The device appears on the screen.

   Important: You can display a list of the available devices by selecting View > Show Devices. From this list, you can select and drag the device you would like to add onto the canvas.

Shortcut: You can also add a device by using the “y” hot key. Cadabra displays only those devices that do not cause short-circuit or avoidance violations under your mouse. If there are no valid devices to be displayed, an information message appears indicating the same.

3. Click in the location where you would like to add the device. The device is added to the layout and another one appears.

   Caution: The device will not be added if placing it in the spot indicated violates any avoidance design rules.

4. Continue to click and add the device as necessary *or* right-click to cancel the operation.

   If you add a device that has modified routing geometries due to routing style preferences or electromigration constraints, the routing geometries displayed in the Cell Editor may not accurately reflect the routing geometries that will appear in the final layout. For more information, refer to the Modified Routing Geometries on page 351.

To add a wire device

When hand-editing a layout in the Cell Editor, most devices are added by defining a single-point. However, wire devices are placed by specifying two or more points.

To add a wire device, do the following:

1. In the Cell Edit window, select a Net.
2. Select Edit > Add Device and the wire device you would like to add.

   Note: You can also add a wire device by using the “y” hot key. Cadabra displays only those wire devices that do not cause short-circuit or avoidance violations under your mouse. If there are no valid wire devices to be displayed, an information message appears indicating the same.

3. Click at the first endpoint.
4. Do one of the following:
   - Click at the next point.

- Double-click if it is the final endpoint.

Result: The device appears and is drawn to the next point.

Explanation: At any point while adding the wire, you can:

- press C on your keyboard and change layers (for more information, refer to To change layers on page 350;
- right-click to cancel the last wire segment added; or
- double-right-click to cancel the entire operation.

Caution: The device will not be added if placing it in the spot indicated violates any design rules.

To change layers

You can change layers when you add a wire in the Cell Edit window. This feature gives you flexibility in creating efficient and scalable cell layouts.

To change layers, do the following:

1. When you add a wire, do one of the following:
   - Press the “c” key on the keyboard
   - Double-click the center mouse key or wheel.

   Result: A list of layers appears.

   Explanation: Cadabra displays only those layers that do not cause short-circuit or avoidance violations. If there are no valid wire layers to be displayed, an information message appears indicating the same.

   Note: The option to change layers is only available when you manually route. When you choose to change layers by pressing the “c” hotkey, Cadabra goes either up one layer or down one layer and adds a contact device. You can then continue to route in another layer.

   If only one layer can be changed, a contact is automatically added and the layer is automatically changed.

2. Select the layer that you would like to change to.

   Result: A contact is added. If required, you can continue adding wires.

Modified Routing Geometries

When a device is manually placed in the Cell Editor, the device's routing geometries may not accurately reflect the routing geometries that will appear in the final layout. This occurs in situations when the device has modified routing geometries, such as the requirement for multiple contacts due to electromigration constraints, or the requirement to widen wires due to routing style preferences or electromigration constraints.

Under these circumstances, you can do the following:

- Leave the devices as they are in the Cell Editor. The routing geometries will be updated when compaction is run.
- Show the detailed routing geometries in the Cell Editor, but do not correct them until compaction is run.
- Update the routing geometries prior to compaction in the Cell Editor.

Any potential routing conflicts caused by updating the routing geometries can viewed prior to updating.

The details of the modified routing geometries for a device can be viewed by selecting the new device and clicking the More button at the bottom of the Cell Edit and Cell View windows. The More button is only available when a device with modified routing geometries or a MOSFET is selected.

To update routing geometries

Updating routing geometries reshapes the applicable devices in the symbolic layout. If reshaping a device causes violations, the device is left as is in the layout and any required reshaping will be done during compaction.

To update routing geometries, do the following:

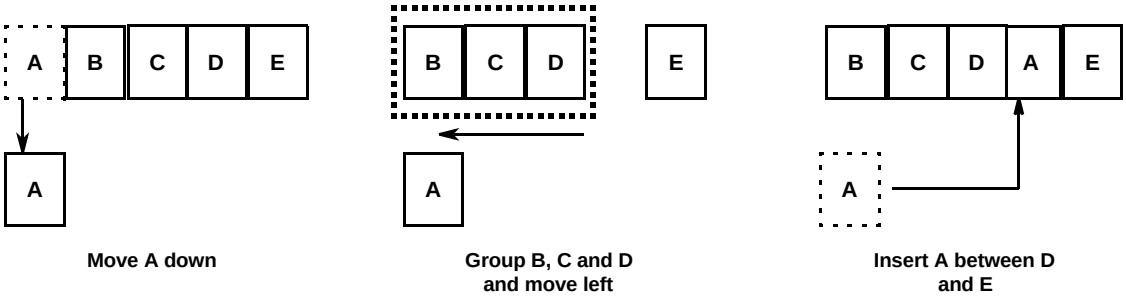
To apply the modified routing geometries:

- In the Cell Edit window, select Edit > Update Routing Geometries.
  The routing geometries are updated in the layout.

Group Editing

When hand-editing a layout in the Cell Editor, you can group a set of devices and then move, flip, or delete the group as a whole. You can also set Cadabra to automatically reshape the devices in a group upon move by selecting Group > Auto Reshape > On from the device menu.

Grouping devices before editing them allows you to maintain certain orientations and/or distances between the devices. For example, since transistors usually occur in clumps, you might use group move while hand-editing a placement to maintain the chain of transistors as shown in the figure below.



To group devices

Grouping devices in the Cell Editor allows you to then move or flip a set of devices as a whole. You can group all the devices in a layout by selecting Edit > Select All or you can add devices individually to a group.

To group devices, do the following:

1. In the Cell Edit window, click on the device you would like to have in the group.
   The device menu appears.
2. Select Add to Group.
   A box appears around the device making it a part of the group.

   Important: You can group MOSFETs of the same source by selecting Auto-Group MOSFETs from a MOSFET's device menu.

3. Repeat steps 1-2 until you have added the necessary devices to the group.

Important: You can remove a device from the group by selecting Remove From Group on the device menu.

Shortcut: Click  and select an area on the canvas in which you would like to group all the devices.

To modify device properties

Properties on individual devices can be modified from the Cell Editor if the properties have been specified by `DeviceTemplate > instanceProperties`.

Note: Modifications to the properties are not automatically reflected in the shape or position of the device unless the Auto Reshape option is enabled. Otherwise, you must manually Reshape the device or run Compact on the cell layout.

To modify device properties, do the following:

1. In the Cell Edit window, click on the device for which you would like to modify individual properties.
   The device menu appears.
2. Select Modify Properties.
   A list of the properties that can be modified for the selected device appears.
3. Select a property from the list to modify.
   The Edit Property dialog for the selected property appears.
4. Edit the property value.
5. Click OK.
   The dialog box closes and the device property is updated.

To move a device

Devices can be moved individually or by groups in the Cell Editor. To move devices by group, you must first group them. Typically, MOSFET devices should be moved in groups as they often occur in clumps.

To move a device, do the following:

1. In the Cell Edit window, click on the device or device group you would like to move.
   The device menu appears.
2. Select Move *or* Group > Move Group.
   The device(s) become “attached” to the cursor.
3. Move and click to place the device(s) in the new spot.

   Note: If placing the device(s) in the indicated spot violates any design rules, the device(s) are not placed and warning messages appear at the bottom of the Cell Editor.

To reshape a device

Reshaping a device in the Cell Editor generates its original geometry. You can also have Cadabra automatically reshape a device upon move by setting the Auto Reshape option on the device menu. For a group of devices, you would select Group > Auto Reshape > On.

To reshape a device, do the following:

1. In the Cell Edit window, click on the device you would like to reshape.
   The device menu appears.
2. Select Reshape.
   The original geometry of the device is generated.

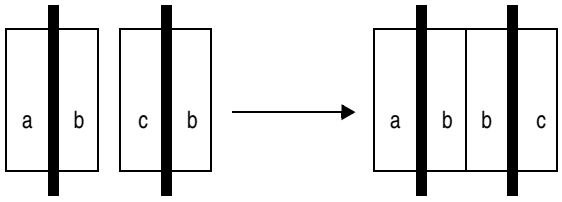
To flip a device

When hand-editing a layout in the Cell Editor, devices can be flipped individually or by groups. To flip devices by group, you must first group them.

To flip a device, do the following:

1. In the Cell Edit window, click on the device or device group you would like to flip.
   The device menu appears.
2. Select Flip *or* Flip X *or* Flip Y *or* Group > Flip X *or* Flip Y.
   The device(s) are flipped in the direction indicated.

Note: Flipping a MOSFET device switches the side of its source and drain, as shown in the figure below.



Flipping MOSFET

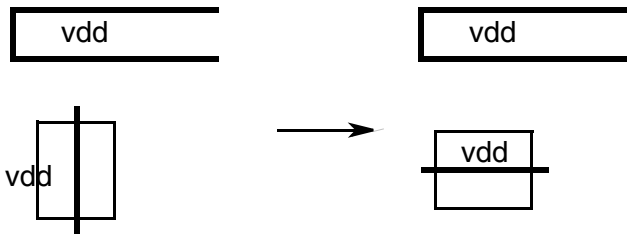
To rotate a device

When hand-editing a layout in the Cell Editor, rotating devices in the channel region allows you to reduce the space in that area. However, rotated devices may make the cell harder to route.

To rotate a device, do the following:

1. In the Cell Edit window, click on the device you would like to rotate. The device menu appears.
2. Select Rotate CW *or* Rotate CCW.
   The device is rotated 900 in the direction indicated (that is, clock-wise or counter clock-wise).

   Important: You might rotate a MOSFET device to make an easier connection to a rail device as shown in the figure below.



Rotating MOSFET

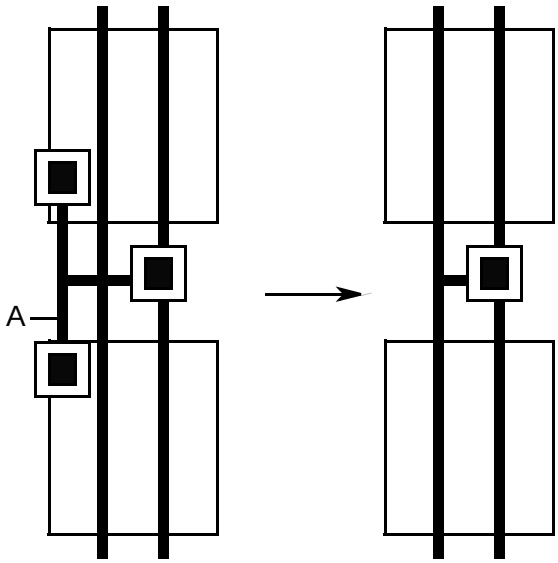
To rip up a device

Ripping up a device in the Cell Editor removes the device *and* its attachments. To remove only a device, use delete. Since MOSFET devices cannot be removed, you can only remove its attachments.

To rip up a device, do the following:

1. In the Cell Edit window, click on the device you would like to rip-up. The device menu appears.
2. Select Rip-Up *or* Rip-Up Attachments for a MOSFET device. The device and/or its attachments are removed.

   Note: Rip up of attachments continues in both directions until the point of a junction. For example, as shown in the figure below, ripping up wire A, removes the wire and its attachments up to the junction connecting the MOSFET gates.



To make a device unrippable

Making a device unrippable prevents you from being able to rip up the device.

To make a device unrippable, do the following:

1. In the Cell Edit window, click on the device you would like to make unrippable.
   The device menu appears.
2. Select Make Unrippable.
   The device is made unrippable.

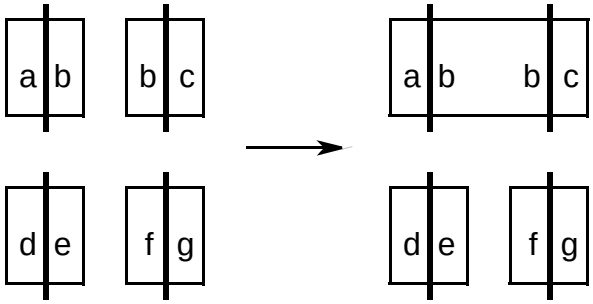
   Note: You can make a device rippable again by selecting Make rippable from its device menu.

To merge MOSFETs

Merging in the Cell Editor connects a MOSFET to another MOSFET or a rail. The two connecting sides must have the same net.

To merge MOSFETs, do the following:

1. In the Cell Edit window, click on the MOSFET you would like to merge.
   The device menu appears.
2. Select Merge > Left *or* Right *or* Up *or* Down.
   The MOSFET merges to the neighboring device in the specified direction.



Merging MOSFETs

Important: You can reverse your merging operation by selecting Unmerge from the device menu.

To fold MOSFETs

Folding MOSFETs in the Cell Editor converts a larger transistor into a group of smaller parallel-connected transistors, while maintaining the overall size of the original MOSFET.

To fold MOSFETs, do the following:

1. In the Cell Edit window, click on the MOSFET you would like to fold.
   The device menu appears.
2. Select Fold/Unfold.
   The Fold/Unfold MOSFETs dialog box appears.

   Note: The dialog displays the current width of the target MOSFET, the total (aggregate) width of all the MOSFETs generated from the parent of the target, and the original width of the parent.

3. Select Fold.
4. Set the options.
5. Click OK.
   The MOSFET is folded.

To unfold MOSFETs

Unfolding MOSFETs in the Cell Editor merges one or more transistors that were generated by an original folding operation.

To unfold MOSFETs, do the following:

1. In the Cell Edit window, click on the MOSFET you would like to unfold.
   The device menu appears.
2. Select Fold/Unfold.
   The Fold/Unfold MOSFETs dialog box appears.

   Note: The dialog displays the current width of the target MOSFET, the total (aggregate) width of all the MOSFETs generated from the parent of the target, and the original width of the parent.

3. Select Unfold.
4. Set the options.
5. Click OK.
   The MOSFET is unfolded.

Fold/Unfold MOSFETs Options

Target MOSFET: The MOSFET to be folded or unfolded.

Fold: The MOSFET is folded.

Direction: The direction for placing the generated MOSFETs. Horizontal MOSFETs can be folded left or right, while vertical MOSFETs can be folded up or down.

Evenly: Even folding is used and MOSFETs of equal width are generated.

Tolerance: The maximum allowable deviation in total width from the netlist MOSFET width. For example, if a value of 5% is specified, the total width of the folded MOSFET must be within 5% of the original width.

Maximum Finger Width: MOSFETs at the specified maximum width are generated.

Minimum Number of Fingers: MOSFETs with at least the specified minimum number of fingers are generated. If this option is selected with Maximum Finger Width, then the minimum number of fingers is executed first, according to the specified maximum finger width.

Maximally: Maximal folding is used and as many MOSFETs as possible at the specified maximum width are generated. If necessary, a smaller MOSFET is generated to account for any remaining width.

Maximum Finger Width: The maximum finger width (in microns) for maximal folding.

Unfold: The MOSFET is unfolded.

Unused: A list of the MOSFETs that are not used for MOSFET folding operations, but are a part of the symbolic layout and are related to the target MOSFET.

Source MOSFETs: A list of the MOSFET(s) to be unfolded into the target MOSFET.

Reset drawn width to netlist width: The drawn MOSFET width is reset to the netlist width.

Direction: The direction of alignment. For example, “bottom” indicates that the generated MOSFETs are bottom-aligned.

Align Folded/Unfolded MOSFETs To: The MOSFET to which all folded MOSFETs will be aligned. The default MOSFET is the target MOSFET. The default alignment for P and N-type MOSFETs are the defaults set for the symbolic database.

To resize MOSFETs

Resizing MOSFETs grows or shrinks the size of a MOSFET. MOSFETs can be resized based on the target MOSFET, using a source MOSFET within the cell, or based on the netlist MOSFET.

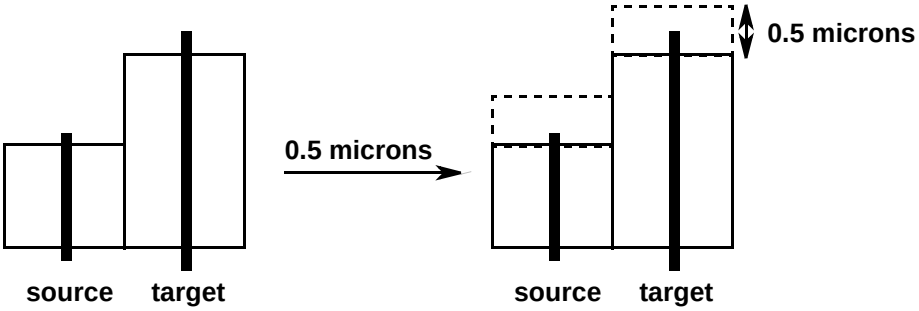
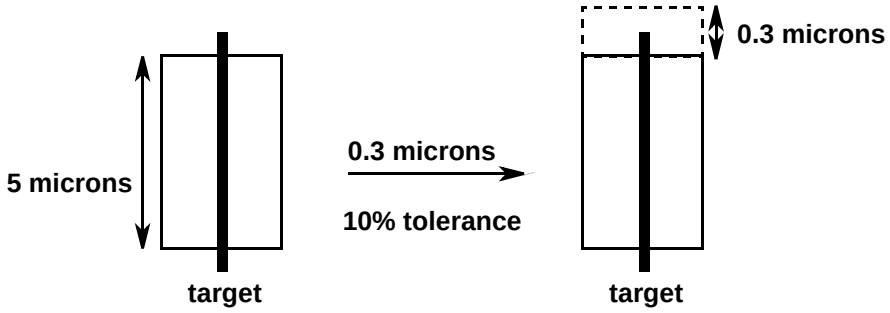
To resize MOSFETs, do the following:

1. In the Cell Edit window, click on the MOSFET(s) you would like to resize.
   The device menu appears.
2. Select Resize.
   The Resize MOSFETs dialog box appears.

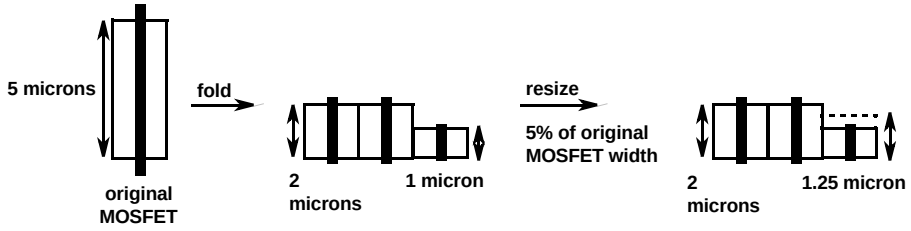
   Note: The dialog displays the current width of the MOSFET, the total (aggregate) current width of all the MOSFETs generated from the parent of the MOSFET, and the original width of the parent MOSFET.

3. Set the options.
4. Click OK.
   The MOSFET(s) are resized.

Resize MOSFETs Options

Option	Description
Adjust fold ratio from source to target	MOSFETs are resized from sources. When resizing with sources, the change in width is removed from the source MOSFET(s) and applied to the target MOSFET, as shown in the figure below.  Resizing with source MOSFETs can only be performed on a folded MOSFET.
Resize MOSFETs in netlist	Overview — MOSFETs are resized without sources. Resizing without sources adjusts the width of the netlist MOSFET without affecting other transistors in the layout. *Also Set* The Tolerance Setting. This tolerance is the percentage width by which netlist MOSFETs are adjusted. The change in MOSFET width cannot exceed this tolerance. For example, if the target MOSFET is 5 microns in width, a tolerance of 10% would allow a maximum change in width of 0.5 microns. Therefore, a resize of 0.3 microns is allowed as shown in the figure below. 

Option	Description	
Tolerance Setting	Overview	The percentage width by which netlist MOSFETs can be adjusted when sources are not used.
Unused	Overview	A list of all the MOSFETs in the cell that are not used for the resizing operation.
Source MOSFETs	Overview	A list of the MOSFETs to be used as a source of width for the resizing operation. Source MOSFETs must have been generated by a previous folding operation that created the target MOSFET.
Target MOSFETs	Overview	A list of the target MOSFETs that are to be resized.
Change in target MOSFETs	Overview	The amount by which the target(s) should be resized (in microns).
Percent change of target MOSFETs	Overview	The amount (positive or negative) by which the target(s) should be resized (as a percentage of the target MOSFET width).

Option	Description
Percent change of original MOSFETs	*Overview* The amount (positive or negative) by which the target(s) should be resized (as a percentage of the original MOSFET width). The amount of resizing can be specified in one of three ways: ▪ As a value specified in microns. The value must be greater than the manufacturing grid. ▪ As a percentage of the target MOSFET width. For example, if a value of 1% is specified, the target would increase in size by 1% of the target MOSFET width. ▪ As a percentage of the original (parent, if the target has been previously folded) MOSFET width. For example, a 5% change in width indicates 5% of the original MOSFET width rather than 5% of the target MOSFET width. This amount can vary if the target MOSFET has been folded, as shown in the figure below.  The original MOSFET is 5 microns wide. After folding, 2 MOSFETs of 2 microns in width and 1 MOSFET of 1 micron in width are created. The target (third) MOSFET is 1 micron wide, but the original MOSFET is 5 microns wide. In this example, 5% of the target MOSFET width would give a resize delta of 0.05 microns. Five percent of the original MOSFET width would give a resize delta of 0.25 microns.
Reset drawn width to netlist width	Overview — The drawn width is reset to the netlist width. If this option is not used, the drawn width to netlist width ration is preserved during resizing.
Direction	Overview — The direction in which to align the resized MOSFET(s). The MOSFETs are aligned to the MOSFET specified in Align Resized MOSFET To.

Option	Description	
Align Resized MOSFET To	Overview	The MOSFET to which all the resized MOSFETs should be aligned. The default is the MOSFET from which the Resize step was selected.

To resize wires, contact covers, and port covers

Resizing wires, contact covers, and port covers stretches or shrinks their sizes.

To resize wires, contact covers, and port covers, do the following:

1. In the Cell Edit window, click on the side of the wire, contact cover, or port cover that you would like to resize.
2. Choose Stretch/Shrink from the background menu that appears or press the hot key “s” on the keyboard.

   Note: The Stretch/Shrink option is enabled in the background menu only only if you click the side of a wire, contact cover, or port cover. This option is disabled if you click anywhere else.

   To cancel the operation, right-click in the interface.

3. Move the mouse in the direction in which you would like to resize the wire, contact cover, or port cover.

   Result: The wire, contact cover, or port cover stretches or shrinks, depending on the direction of the mouse movement.

   Note: Due to overlaps, if you are forced to select the sides of multiple wires, contact covers, and port covers, pressing the hot key “s” on the keyboard displays a drop-down menu containing the list of devices that can be resized. Select the required device that you want to resize.

   Due to overlaps, if you are forced to select multiple sides of the same device, pressing the hot key “s” on the keyboard displays a drop-down menu containing the list of layers for the device. Select the required layer of the device that you want to resize.

Due to overlaps, if you are forced to select multiple sides of the same device in the same layer, the resize operation is performed on the first shape in the symbolic shape DB.

Cadabra supports the resizing of wires only on the direction of the wire's length. Also, a wire's length cannot shrink to less than 1 manufacturing grid.

Cadabra supports the resizing of contact covers and port covers in four directions. the minimum supported size for shrinking is 1x1 manufacturing grid.

Note: When resizing, Cadabra checks for possible occurrences of short-circuit or avoidance violations. If such violations exist, the resizing operation is aborted and an error message is displayed indicating the violation occurences.

4. Double-click at the end point to finish the resizing operation.

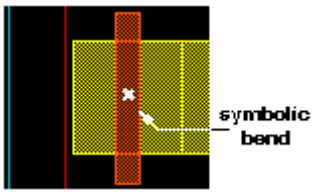
   Result: The required wires, contact covers, and port covers are resized.

To add a gate bend

When adding a gate bend in the Cell Edit window, you can specify the direction of the bend or you can allow Cadabra to determine the direction for you. You can only add bends to MOSFET gates.

To add a gate bend, do the following:

1. Click on the gate you would like to add a bend to.
   The device menu appears.
2. Select Add Bend *or* Add / Bend *or* Add \ Bend.
   A symbolic gate bend is added, which will be committed during compaction.



Important: You can change the direction of the bend by selecting Change Bend Direction and the new direction from the MOSFET's device menu.

Important: You can delete a gate bend by selecting Delete Bend from the MOSFET's device menu.

To move a gate bend

Moving a gate bend in the Cell Edit window allows you to change the location of the bend on the MOSFET gate.

To move a gate bend, do the following:

1. In the Cell Edit window, click on the gate bend you would like to move.
   The device menu appears.
2. Select Move Bend.
   A copy of the bend is attached to the cursor.

3. Click at the spot you would like to move the bend to.
   The gate bend is moved to the new location.

   Important: You can delete a gate bend by selecting Delete Bend from the MOSFET's device menu.

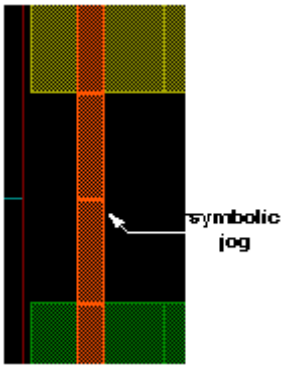
To add a wire jog

Wire Jogs provide the compactor with more flexibility when arranging wires.

To add a wire jog, do the following:

1. In the Cell Edit window, click on the wire you would like to add a jog to.
   The device menu appears.

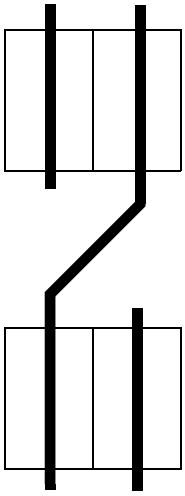
2. Select Jog.
   A symbolic jog is added, which will be committed during compaction.



Allowing 45^0 wires

When hand-editing a layout in the Cell Editor, you can allow 450 wires by selecting the option under the Preferences menu. However, 450 wires must first have been set on the wire template in the architecture.

You might use 450 wires to connect cross gates as shown in the figure below.



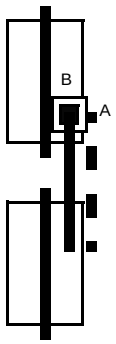
Snapping Devices to a Grid

When hand-editing a layout in the Cell Editor, your devices automatically snap to either the manufacturing or the epsilon grid. You can set the grid by selecting it under the Preferences > Snap X or Snap Y menus.

Device Gravity

When hand-editing a layout in the Cell Editor, you can have your devices automatically gravitate to the nearest device. You can set device gravity by selecting the option on the toolbar of the Cell Edit window.

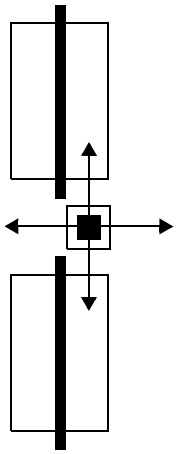
Enabling Device Gravity while adding devices, such as contacts for routing, eases the placement of devices. For example, as shown in the figure below, if you set the first endpoint for a wire at point A, the endpoint will gravitate to point B (the contact) when Device Gravity is enabled. You do not have to be too precise in placing your devices.



Also, Enabling Device Gravity allows you to merge MOSFETs by moving a MOSFET so it comes into physical contact with another MOSFET and when they touch, the MOSFET being moved automatically snaps to the top or bottom edge of the other MOSFET.

Manhattan Move

When hand-editing a layout in the Cell Editor, you can restrict device movement to the manhattan axis (that is, the vertical and horizontal axes). You can set the manhattan move by selecting the option on the toolbar of the Cell Edit window.



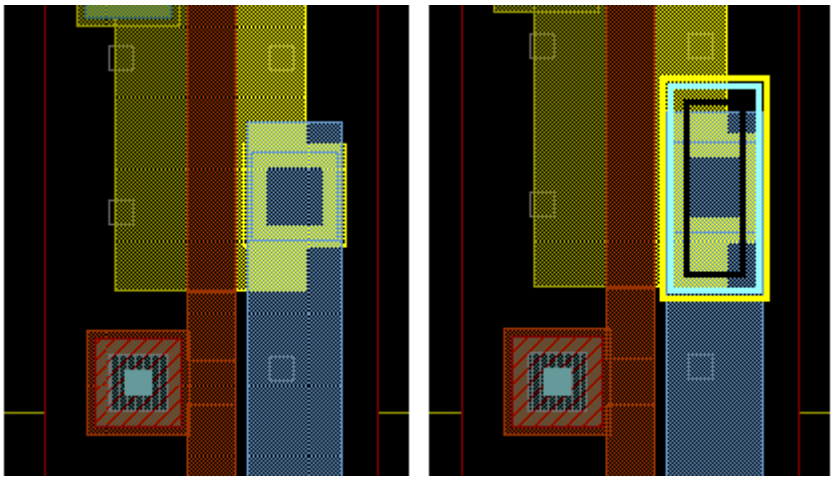
Important: Enable Manhattan Move while adding devices such as contacts for routing, to retain alignments.

Show Detailed Routing Geometries

Detailed routing geometries can be viewed for contacts, diodes, and wires in the Cell Edit window before the modified routing geometries are updated in the symbolic layout by selecting Preferences > Show Routing Geometries.

The modified routing geometries are highlighted, as shown in the following figure.

Typically, modified routing geometries are not displayed for ports in the Cell Editor unless the port direction has been defined in the Architecture Builder. However, modified routing geometries are applied to ports during compaction. A port's modified routing geometries can be viewed by selecting the port and clicking on the More button at the bottom of the Cell Edit and Cell View windows.



To delete a device

Deleting a device in the Cell Editor removes *only* the device. To remove a device and its attachments, use rip up. Devices can be deleted individually or by groups. MOSFET devices cannot be deleted.

To delete a device, do the following:

1. Click on the device you would like to delete.
   The device menu appears.
2. Select Delete *or* Group > Delete Group.
   The device(s) are removed.

To export a clone

Cloning captures the placement and routing information of a symbolic layout design point so that the same placement and routing can be re-used for another cell. The cell information is saved in a clone file *(.cln)*. Refer to Do cloning for restrictions on use of cloned symbolic layouts.

To export a clone, do the following:

1. In the Cell Edit window, select Design Point > Export.
   The Export dialog box appears.
2. Select the Clone and move it to the Used column using the “<“ “>” buttons.

3. Select the Clone in the Used column.
   The Configure Exporter button is enabled.
4. Click Configure Exporter.
   The Exporter Configuration dialog box appears for the exporter you have selected.
5. Set the options.
6. Click OK.
   A clone file *(*.cln)* is saved to disk. This clone file can be used during hierarchy extraction of similar netlists to re-use placement and routing information.

   Note: You can also clone a portion of a symbolic layout. For more information on cloning specific devices, refer to To clone part of a layout.

To clone part of a layout

You can clone a portion of a symbolic layout for re-use during hierarchy extraction of a similar netlist. Refer to Do cloning for restrictions on use of cloned symbolic layouts.

To clone part of a layout, do the following:

1. In the Cell Browser, click and hold on a symbolic layout design point.
   The design point menu appears.
2. Select Cell Edit.
   The Cell Editor window appears showing the layout of this design point.
3. Click on a device to be cloned and select Add to Group.
4. Repeat step 3 until all the devices to be cloned have been grouped.

   Shortcut: Click  and select an area on the canvas in which you would like to group all the devices.
5. Select Design Point > Export.
   The Export dialog box appears.
6. Select Clone and move it to the Used column using the “<“ “>” buttons.
7. Select Clone in the Used column.
   The Configure Exporter button is enabled.

8. Click Configure Exporter.
   The Exporter Configuration dialog box appears for the exporter you have selected.
9. Set the options.
10. Click OK.
    A clone file (*.cln) is saved to disk. This clone file can be used during hierarchy extraction of similar netlists to re-use placement and routing information.

Export Clone Options

Option	Description	
Clone Name	Overview	The descriptive name of the clone. By default, this is the cell name.
Trim Wires	Overview	The horizontal wires to the left and right boundary of the clone are trimmed back to the bounding box of the MOSFET shapes if this option is selected. Also, any devices to the left or right boundary of the clone, which lie completely outside of the MOSFET shapes bounding box, are removed.
Devices To Be Cloned	Overview	This option sets whether the selected devices or all the devices in the layout are exported. (This option is only available if you select Export Clone from a Cell Edit window.)
Export File	Overview	The clone is saved in this file. By default, the filename ends in .cln.
MOSFET Placement Priority	Overview	The order in which MOSFETs are placed. This placement order is important for placing other MOSFETs that are aligned to the first (primary) MOSFET. Primary MOSFETs are listed first and placed before secondary MOSFETs.
	Why set this option?	When the MOSFETs in the target cell have a different width, the alignments are used to maintain the correct placement of MOSFETs. Secondary MOSFETs are placed after their primary MOSFET and are either top or bottom-aligned to their primary. This change in width can affect the alignments. The placement priority allows you to identify which MOSFETs have alignments that are more crucial and should therefore be placed first. In the event that a design rule violation occurs or the MOSFET alignment in the source layout cannot be preserved in the target cell, clone instantiation is suspended and the next clone file (if any) is automatically used.

Option	Description	
Export File	Overview	The clone is saved in this file. By default, the filename ends in .cln.

To zoom

Zooming allows you to view the cell layout's full area or focus on specific areas of the canvas in the Architecture Builder, Compaction Browser, Cell Edit, Cell View and View windows. You can zoom using either the zoom button or the options under the View menu.

Using the Zoom Button

To zoom using the Zoom button, do the following:

1. Click  .
2. Select the area you would like to zoom in on *or* right-click to switch to full view.
   The focus changes to the area selected.

Using the View menu

To zoom using the View menu, do the following:

- Select View > Full View *or* Zoom In *or* Zoom Out.
  The focus changes to the zoom selected.

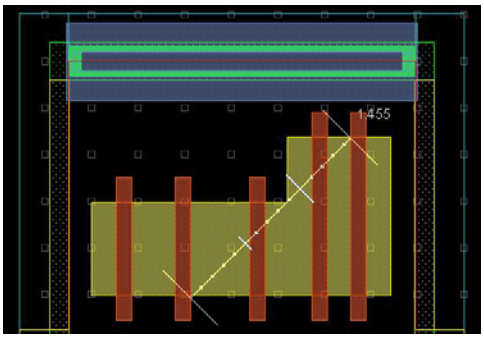
To measure on the canvas

Measuring allows you to check the width of and distances between shapes on the canvas in the Architecture Builder, Compaction Browser, Cell Edit, Cell View, and View windows.

To measure on the canvas, do the following:

1. Click  .
2. Click and drag the mouse between the points of measurement on the canvas.

   Result: A ruler appears marking the measured distance and the delta X and Y values appear in the status bar.



Note: You can make multiple measurements by repeatedly clicking and dragging the mouse on the canvas.

Important: You can customize the ruler scale size. In the GUI, go to Preferences→Measuring→Set Ruler Scale Size. In the dialog box that appears, you can set values in the range of 0.1 to 1 micron per unit. The default value is 1 micron.

When you set the value of the ruler scale size to below 1 micron, and perform step 2 in the previous procedure, notice the marks on the ruler which indicate 1/10th and 0.5 calibrations.

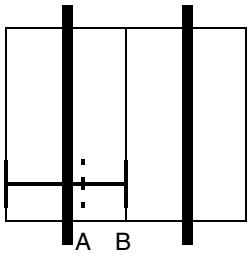
Important: You can remove all of the measurements by right-clicking or selecting Preferences > Clear Ruler or you can remove the last measurement by selecting Preferences > Clear Last Ruler.

Measuring to the Nearest Edge

When measuring areas on the canvas in the Architecture Builder, Compaction Browser, Cell Edit, Cell View, or View windows, you can have the ruler

automatically gravitate to the nearest edge. You can set gravity to the nearest edge by selecting the option under the Preferences > Measure menu.

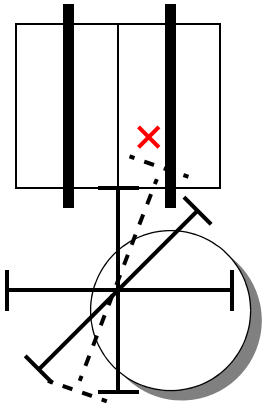
If, as shown in the figure below, you try to stop the ruler at point A, the ruler automatically gravitate to point B when Gravity to Nearest Edge is enabled.



Measuring 45^0 Angles

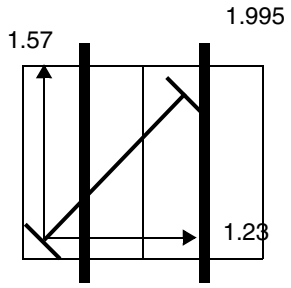
When measuring areas on the canvas in the Architecture Builder, Compaction Browser, Cell Edit, Cell View, or View windows, you can restrict diagonal measurements to 450 angles by selecting Preferences > Measure > Only Allow 45 Degree Rulers.

You can still measure in the horizontal and vertical directions.



Measuring Delta X/Y

When measuring areas on the canvas in the Architecture Builder, Compaction Browser, Cell Edit, Cell View, or View windows, the Delta X and Y values always appear in the status bar. However, you can have these values appear directly on the canvas by selecting Preferences > Measuring > Show Delta X or Show Delta Y.



Snapping Ruler to a Grid

When measuring areas on the canvas in the Architecture Builder, Compaction Browser, Cell Edit, Cell View, or View windows, your ruler automatically snaps to either the manufacturing or epsilon grid. You can set the grid by selecting it under Preferences > Measuring > Snap menu.

To show/hide layers

Showing and hiding particular layers in the Architecture Builder, Compaction Browser, Cell Edit, Cell View and View windows allows you to better analyze layouts with multi-layer contacts or interconnecting layers.

To show/hide layers, do the following:

1. Select View > Show Layer Filter.

Result: The list of layers appears to the right of the window.

2. Select the layers you would like to show.

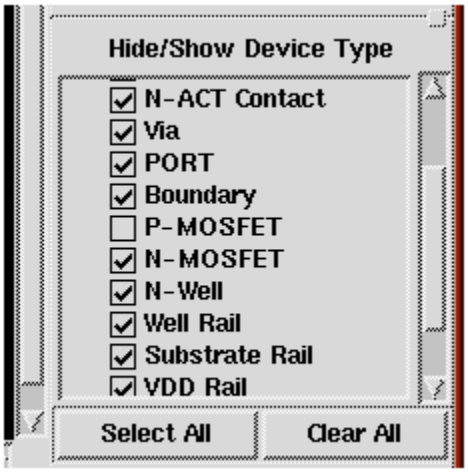
To show/hide device types

Showing and hiding particular device types in the Compaction Browser, Cell Edit, Cell View and View windows allows you to better analyze the ports and contacts of a layout.

To show/hide device types, do the following:

1. Select View > Show Device Type Filter.

Result: The list of device types appears to the right of the window.



2. Select the device types you would like to show.

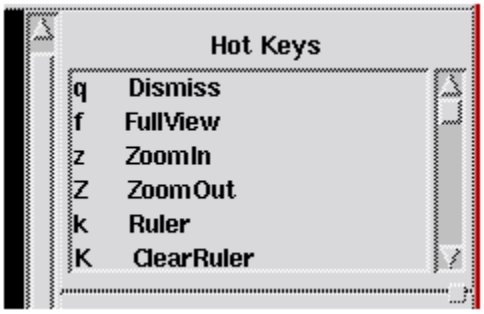
To view a list of hot keys

Hot keys provide keyboard short-cuts for actions performed in the Architecture Builder, Compaction Browser, Cell Edit, Cell View, and View windows. You can edit your hot key bindings in the EditorDefaults.al file found in your .cadabra directory.

To view a list of hot keys, do the following:

- Select View > Show Hot Keys.

  Result: The list of hot keys appears to the right of the window.



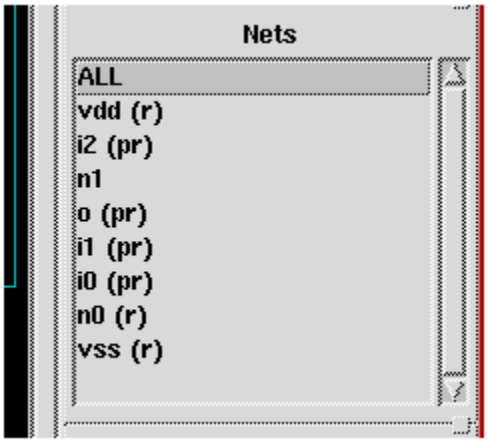
To view a list of nets

A list of nets can be viewed in the Compaction Browser, Cell Edit, Cell View, or View windows.

To view a list of nets, do the following:

- Select View > Show Nets.

  Result: The list of available nets appears to the right of the window. A *p* appears beside the nets that ports have not been placed on and an *r* appears beside the nets that have not been routed.



To view a list of devices

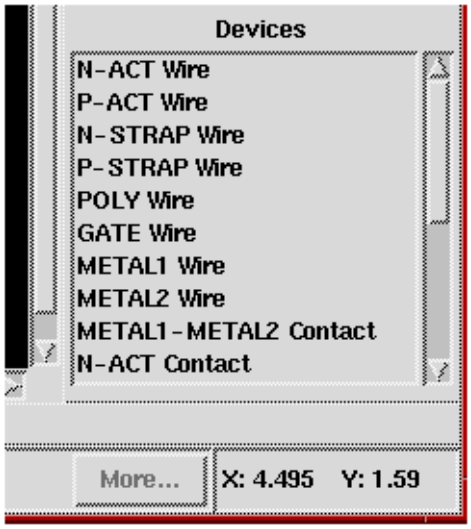
To view a list of devices, do the following:

- In the Cell Edit window, select View > Show Devices.

  Result: The list of available devices appears to the right of the window.

To view unrouted nets

Viewing unrouted nets not only allows you to see which nets need to be routed, but you can also analyze the placement of nets in regards to routing. Unrouted

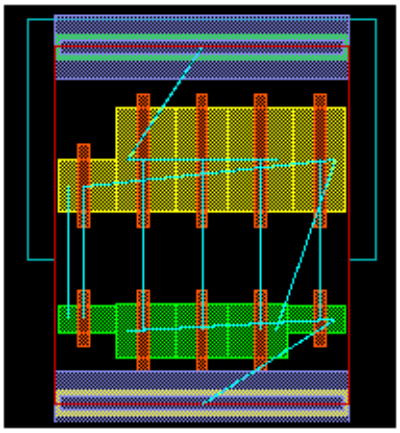


nets can be viewed in the Compaction Browser, Cell Edit, Cell View, or View windows.

To view unrouted nets, do the following:

- Select View > Show unrouted nets.

  Result: The unrouted nets are marked with connecting blue lines.



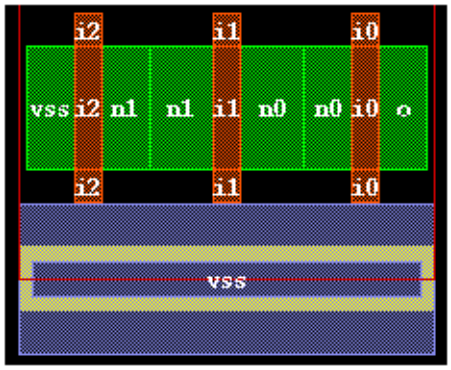
To annotate nets

Annotating nets allows you to view and analyze the placement of nets in the Compaction Browser, Cell Edit, Cell View, or View windows.

To annotate nets, do the following:

- Select View > Annotate nets.

  Result: The annotations for all the nets appear.



To view the I/O Grid

To view the I/O grid, do the following:

- In the Compaction Browser, Cell Edit, Cell View, or View window, select View > Show IO grid.

  Result: The I/O grid appears on the canvas.

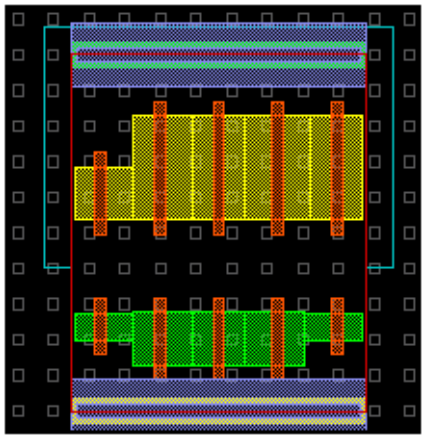
  Note: In the View window, the IO grid cannot be viewed for frames displaying source layouts.

To view device information

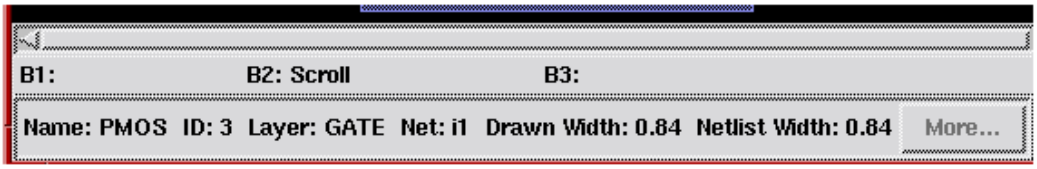
Device information can be viewed in the Cell Edit or Cell View window.

To view device information, do the following:

- Click on the device you would like to view the information for.



Result: The device information appears in the status bar at the bottom of the window.



Important: You can view more detailed information for MOSFET devices and for port, contact and wire devices with EM requirements by clicking on the More button.

To show routing conflicts

Routing conflicts for devices manually added to the symbolic layout can be viewed in the Cell Edit window.

To show routing conflicts, do the following:

- Select View > Show Routing Conflicts.
  The devices with routing conflicts are highlighted in the symbolic layout. Red highlights indicate that the geometries do not fit the layout and have caused short circuits and/or avoidance violations. Yellow highlights indicate that the use of a particular device is prohibited by the electromigration requirements set in the Architecture Builder.

To show routing conflicts

abutment
Refer to *diffusion abutment*.

AL (Application Language)
Cadabra's proprietary Application Language used for scripts, netlists, and data files.

AL file
An AL file is composed of Cadabra's Application Language and must first be interpreted before it can be understood by Cadabra. Also refer to *compiled AL file*.

annotation
An annotation is a form of labeling. For example, a layout can be annotated with the net names that each device carries.

architecture
An architecture defines the behavior of devices in a library and the size, location and boundary conditions of the different regions that make up a standard cell. For example, an architecture defines the size of the cell boundary, the location of the N-well and power rails, and the properties of the transistors.

asymmetrical extension rule
An asymmetrical extension rule indicates that an extension is not the same distance on all sides. For example, an asymmetrical extension rule can be applied to a contact cover whose cover extension is different on the opposite sides of the contact.

ATL (Automated Transistor Layout)
ATL is the process which automatically places, routes, compacts and finalizes a cell in Cadabra.

background devices
A background device is generally a boundary relative device that must be placed in the layout, but would not be placed during routing. This device enforces the boundary condition rules (i.e. N-well, power rails, well/substrate tie rails) and could possibly enforce some special layout rules as well. A background device is generally added during the initial placement and cannot be modified by any hand-editing.

balanced gate bends
Balanced gate bends are two gate bends of equal length on adjacent MOSFETs with the same width. Cadabra implements balanced gate bends using the Gate Bend Balancer device.

bash
Bash (Bourne Again SHell) is a shell or command language interpreter which is “sh” compatible.

blocking layer
A blocking layer is a pseudo mask layer (that does not represent a physical layer) used to indicate areas of a cell that are reserved according to set design rules. The blocking layer is typically used to provide a free routing channel.

boundary
A boundary enforces bounding dimensions on the cell layout. The dimensions of the boundary are generally calculated based on integer multiples of the IO grid and can maintain a fixed height or be flexible. Generally, the boundary is defined with a fixed height and a variable width.

breakpoint
A breakpoint is used by Cadabra's AL Debugger. A breakpoint causes the AL Debugger to pause on a specific line of AL code during execution. A breakpoint can be temporary or permanent.

callback
A callback is an AL function used in Cadabra to augment default behaviors. For example, a callback can influence the way certain design steps are performed.

canvas
A canvas is used to display a cell architecture or partially completed or completed layout of a cell. Examples of canvases are the Architecture Builder, Cell Edit, and Cell View windows.

category
A category is a string used as a key to obtain the correct defaults from a defaults database or the correct search paths for file loading.

caution
A caution is a sign that may appear when you add or edit the various elements of the cell architecture. The caution sign indicates a change in the defaults of an element.

cell
A cell is a logic block made of two or more transistors. Examples of cell types are an inverter, a 2-input AND gate, and a D flip-flop.

cell browser
A cell browser is a window that displays the progress of the layout process. The window contains the design tree which is made up the executed design steps and resulting design points of a cell. Also refer to *design tree*.

chaining
Chaining is a part of the hierarchy extraction process, which allows the hierarchy extractor to link together long strings of MOSFETs that have electrically-like diffusions. Chaining makes maximum use of cell space and makes MOSFETs easier to route. The hierarchy extractor considers gate alignment when chaining MOSFETs, but it also allows for some flexibility.

channel
A channel is the region between the source and drain diffusions, which is typically created on the polysilicon layer. The channel does not include the gate endcaps that extend beyond the MOSFET diffusion.

channel density
Channel density measures the number of horizontal routes at any vertical slice in a symbolic layout.

circuit
A circuit is a collection of MOSFET devices that are connected to implement a function.

cloning
Cloning is a method of capturing existing patterns of MOSFET placement and routed circuitry. Cloned patterns can be exported and then reused during hierarchy extraction to duplicate the placement and routing information in a new cell.

compaction
Compaction is a design step that minimizes a cell's area and/or width. Compaction also optimizes secondary objectives such as minimizing diffusion and minimizing wire length.

compiled AL file
A compiled AL (Application Language) file is a file composed of Cadabra's Application Language that has already been interpreted and can be understood by Cadabra. Also refer to *AL file*.

configuration
A configuration is the resulting design point after a collection of tiles has been generated during hierarchy extraction.

conflict
A conflict is a sign that may appear when you add or edit the various elements of the cell architecture. The conflict sign indicates a violation within the cell architecture.

constraint
A constraint defines limits for the compactor on the relative spacing between two edges in a symbolic layout. A constraint always applies to two edges. The two edges can be on the same shape, different shapes of the same device, or different devices. A constraint is typically generated to enforce a technology's design rules, but it can also be generated by the devices themselves to enforce specific rules.

contact
A contact is a device that allows one cell layer to connect to another cell layer through a contact layer. All three layers constitute the contact.

critical path
The critical path is the set of constraints (typically running from left to right) in a cell that prevents further minimization of a cell's area and/or width. The critical path is a layout measure, not a method of circuit timing performance.

C-Shape
A C-Shape is a type of routing that connects diffusions in the form of a “C” pattern. The C-Shape for a given net is the result of horizontal routing along the contacts on the P-type MOSFETs and N-type MOSFETs as well as a vertical routing over the gate of the same net. The C-Shape of the wire leaves the middle section of the layout free providing more room to connect other nets within the cell as well as the placement of ports.

custom design step
A custom design step (also known as a custom operation) automates specific operations that should be applied to different design points of the cell during the design flow. These operations are predefined during the definition of the architecture.

dead zone
A dead zone is the area between two spacing intervals. Two spacing intervals can be defined between two device edges. If the two intervals do not overlap, then a dead zone is created. For more information, refer to Dead Zone Interval on page 65.

defaults database
A defaults database is a storage of defaults. The defaults are listed as an AL list and indexed by category. The category is the key linked to the default for storage or retrieval.

design points
Design points are partial designs of a cell. New design points are created when performing an operation on the cell.

design point tag
A design point tag is used to flag a significant design point in a cell design tree. Design point tags can be used as reminders or can be used to “collect” design points for viewing or for further exploration.

design rule
A design rule represents a physical or electrical requirement for a layer or between any two layers. A physical rule usually pertains to spacing or dimensions and an electrical rule usually pertains to connectivity or avoidance. Design rules are set in the technology.

design rule check (DRC)
A design rule check is a program or operation that verifies whether a physical layout conforms to a set of layout design rules for a specific technology.

design rule condition
A design rule condition modifies the requirements of an existing design rule if certain conditions are met. Design rule conditions are set in the technology.

design steps
Design steps are layout operation performed on a cell. Design steps take design points as their input, perform operations on it, and output other resulting design points.

design tree
A design tree is a collection of design points and design steps, which provides a graphical representation of the cell design process. Each design point in the tree represents a cell layout that becomes more complete as you move down the tree. Each design step is represented by a line leading from one design point to another.

design tree migration
Design tree migration is a process which re-uses complete cell designs in a different setup. Design tree branches, cells, or entire libraries can be migrated. Design tree migration only applies to Cadabra formatted libraries. Also refer to *migration*.

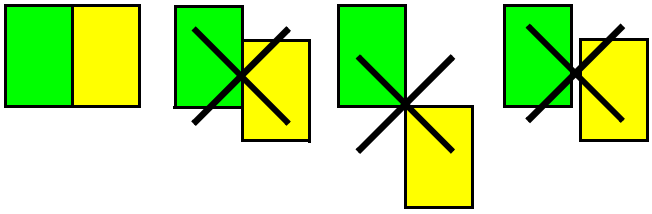
device
A device is an atomic element of a circuit or cell. Examples of devices are MOSFETs, diodes, wires, contacts, or customized user devices.

device mapping
A device mapping is a link between a symbolic device and a particular template. All the symbolic devices in a cell need to be mapped to a template so that the device can receive information on its type, its maximum size and other requested data.

diffusion
Diffusion is a charged layer of material that constitutes the MOSFET source/drain.

diffusion abutment
A diffusion abutment occurs when a shape on the MOSFET active diffusion layer and a shape on the tie diffusion layer meet the following conditions:

Diffusion Abutment Definition



diffusion gap
A diffusion gap is the space that must be left between two diffusions that cannot be connected electronically because they carry different nets.

diffusion jumper
A diffusion jumper occurs when a signal is provided from one part of the circuit to another through a connection in diffusion. Also refer to *jumper* and *poly jumper*.

diffusion merging
Diffusion merging is when two MOSFETs are placed side by side and one MOSFET's diffusion extends into an adjacent MOSFET's diffusion.

diode
A diode is the junction between P-type and N-type diffusion. A diode only permits uni-directional current.

double-height cell
A standard cell consisting of three well regions: a P-well region containing N-type MOSFETS positioned at the top portion of the cell, an N-well region containing the P-type MOSFETS positioned in the middle portion of the cell,

and a P-well region containing the N-type MOSFETS positioned in the bottom portion of the cell. This is the equivalent of abutting two single-height cells along their top boundary edge.

drain
A drain is a region on a MOSFET and is always paired with a source region. The two regions are separated by a gate. A drain is usually implemented with a diffusion layer mask.

drawn width
The drawn width is the width of a MOSFET displayed in a symbolic layout before compaction. Since transistors are initially created with straight gates, the drawn width is sometimes set to slightly less than the netlist width to approximate the dimensions the MOSFET will assume after gate bends are used. After compaction, the MOSFET will match the netlist width.

effective width
The effective width is the width of a MOSFET that takes into account the effect of 45º or 90º gate bends. This is calculated by measuring the length of the centerline of the gate.

electrical design rule
An electrical design rule defines the electrical connectivity between design layers.

environment variable
An environment variable is a placeholder for information. For example, an environment variable is often set for path information that is commonly required by the tool. Creating environment variables prevents the need to constantly re-enter information.

epsilon
The epsilon is the smallest non-zero value that can be represented by the technology. The value of epsilon must be specified as a fraction of the manufacturing grid. By default, epsilon is 1/4 of the manufacturing grid.

exception
An exception is a result that is returned when a run-time error occurs or when a throw is issued while you are running a script.

exporter
An exporter converts files from one format to another.

field oxide
Field oxide is an insulating layer within an integrated circuit.

flip/flop circuit
A flip/flop circuit is a logic memory element used for storing bit values. For example, D-flip-flops and JK flip-flops have differing control structures and usually contain a latch element. Also refer to *latch circuit*.

floating height
A floating height is a height that can vary. Cells can have floating heights.

folding
Folding is a method of splitting a transistor that is too wide for a cell into several smaller transistors with the same resulting drive strength.

gate
A gate is the POLY shape on a MOSFET which lies between the two diffusion shapes.

gate bend
A gate bend is an enhancement used in a MOSFET layout in which the gate geometry is staggered through the introduction of a 45º (sometimes 90º) segment. Gate bends can be used to accommodate contacts or large device widths. Also refer to *balanced gate bends*.

gate crossing
A gate crossing is when a MOSFET is located above and beside two other MOSFETs with a different net from its own but whose nets are the same as each others, while being located diagonally across from a MOSFET with its own net.

gate endcap
Refer to *gate extension*.

gate extension
A gate extension is a shape that is attached to the gate but extends outside the diffusion. This shape is part of the MOSFET device. For example, hammer head shapes attached to the gate ends would be considered gate extensions.

gate feedthrough
A gate feedthrough is when the gate of one transistor is driven through the gate of another. Gate feedthrough can be measured by two factors: how deep they are, or how many gate feedthroughs are connected in series, and the number of MOSFETs that are affected by them.

gate separator device
The gate separator is a background device that enforces more than minimum spacing between two gates. This device is used when the diffusion between two gates contains a contact and/or is connected to another diffusion and additional spacing is required between the gates on either side.

GDSII
GDSII is a standard file format for transferring two-dimensional design data.

GDSII exporter
The GDSII exporter is an exporter used to convert Cadabra layouts to GDSII layouts. The exported GDSII layouts contain complete layout shape and text information of the finished cells. The GDSII layouts are used for input to other down-stream layout and ASIC design tools.

ghost layer
A ghost layer is a layer that does not represent a physical layer and as such does not appear in the final layout. A ghost layer usually serves as a marker layer or a blocking layer, which keeps certain physical layers out of a particular region of the layout during routing and/or compaction.

hammer head
A hammer head is a shape attached to the gate endcap. A hammer head ensures that any gates that are not connected extend past the transistor.

hierarchy extraction
Hierarchy extraction is a design step which groups transistors into locally-optimal groups called tiles. This process takes place in three stages: *searching*, *chaining*, and *pairing*.

implant
An implant determines which type of impurities must be inserted into diffusion sections, thereby adjusting the threshold voltage of a MOSFET. Adding implants is a necessary masking step used in forming MOSFET diffusions. Implants are also visible around ties.

import
Import is a process which creates a symbolic layout from the information in a GDSII file. The symbolic layout contains symbolic devices, which can be manipulated in Cadabra.

infeasibility
An infeasibility marks an area in a layout that contains compaction constraints the compactor could not satisfy to achieve a successful result.

in-place design steps
An in-place design step is an operation performed from the Cell Edit window that changes the current design point instead of creating a new design point and performing an operation on that new design point.

IO grid
The IO grid is a representation of the global P&R (placement and routing) grid in Cadabra. Standard cell ports are typically placed on this grid and the boundary dimensions are typically integer multiples of the IO grid pitch.

IO grid offset
The IO grid offset is the distance between the IO grid lines and the origin of the coordinate system (0,0).

IO pin hitpoints
IO pin hitpoints are connection points to the circuit terminal. Also refer to *port*.

jumper
A jumper occurs when a signal is provided from one part of the circuit to another on a single layer. Also refer to *diffusion jumper* and *poly jumper*.

latch-up
A latch-up is any unwanted side effect that may result from a voltage applied across a circuit.

latch circuit
A latch circuit is a one bit storage element used by itself or within a flip/flop element. Also refer to *flip/flop circuit*.

lateral diffusion
Lateral diffusion is the delta between the drawn and effective widths caused by the encroachment of field oxide over the device well. Sometimes known as the “Bird's Beak” effect. For more information, refer to Lateral Diffusion.

layer
A layer is a component of a cell layout. Layers contain rules and can be annotated with names, colors, and patterns. A collection of layers form a technology. Also refer to *blocking layer*, *ghost layer*, *marker layer*, *predefined layer*, and *representative layer*.

layer mapping file
A layer mapping file is the file used to map GDSII layer/type pairs into the layer names in the technology.

layout
A layout is a geometrical representation of a netlist subcircuit.

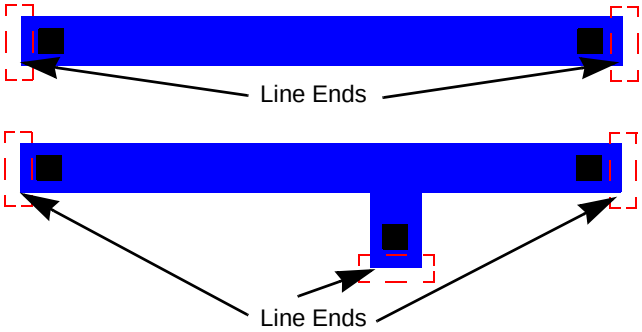
layout mapping
A layout mapping is a link between a cell and source layout.

leaf
A leaf is a design point at the end of a design tree branch. It has no outgoing design points.

library
A library is a collection of cells that share the same technology and architecture.

license daemon
The license daemon controls user access to Cadabra software. The daemon runs without being attached to any specific terminal, ensuring that you can access the software you have been issued.

line end
A line end is recognized as as two consecutive convex corners on the small edge of a shape. A line end is only signficant on specific routing layers and it is usually found at the end of a contact.



log
A log is a file that captures information from each Cadabra session. This information can be reused to create simple scripts. Log files are named to reflect the session or PID number and the machine name where the process is running (e.g. cadabra.mymachine.13885.log).

manufacturing grid
The manufacturing grid represents the finest granularity of the layout on which devices can be placed. All design rule intervals must be a multiple of the manufacturing grid.

marker layer
A marker layer is a layer that does not represent a physical layer. A marker layer is used to provide special shapes in the layout so that annotations can be made and/or so that devices can be extracted properly (e.g. diodes).

microns
A micron is a metric unit valued at one millionth of a meter. Microns are used to measure linear distances within a physical cell layout in design rules or other geometric rules.

migration
Migration is a process which converts existing GDSII layouts to new GDSII layouts by mapping the original layout to new technology process rules or architectures. Migration only applies to GDSII formatted libraries. Also refer to *design tree migration*.

Milkyway exporter
The Milkyway exporter is an exporter used to convert Cadabra layouts to Milkyway .CEL views. The exported Milkyway layouts contain complete set of layout shapes and text labels from the finished cells. The Milkyway layouts are intended for input to other down-stream layout and ASIC design tools.

minimum area hitpoint
A minimum area hitpoint is a device that implements a gridded hitpoint to connect to the cell's primary input/output ports.

model
A model is an abstraction of a function's behavior. Just as a subway map is an abstraction of a subway system, a circuit model is an abstraction of the behavior of a physical electric circuit layout. There are behavioral, static timing, and dynamic timing models.

modular device
A modular device is a custom device that you can implement to represent various layout features. By using a modular device, you can assemble a wide variety of complex devices, with a relatively small number of simple shape components.

MOSFET
A MOSFET is an atomic element of a circuit that is comprised of metal, oxide, and silicon, which forms a field effect transistor (FET). The MOSFET is an active element that provides a switch function in the digital circuit. MOSFETs have either a N-MOS or P-MOS type composition. A MOSFET is comprised of a source, drain, and gate region.

MOSFET region
The MOSFET region is the region where MOSFETs can be placed in a layout. There is generally a separate region for N-type and P-type MOSFETs.

net
A net is a connection between elements within a physical layout. Nets are usually defined in a netlist.

netlist
A netlist defines a cell's characteristics: name, number of I/O ports, number of MOSFETs, number of nets, number of other devices, the circuit I/O nodes, the P and N-MOSFET widths, and signal connectivity.

notch
A notch is created when two external edges on the perimeter of a shape ‘face’ each other and have a
common edge.

n-type
An n-type is a physical device that consists of a semiconductor material doped to have an excess of n-type electrical carriers (electrons).

objective
An objective forces the compactor to minimize a dimension (e.g. minimize width) or other measurable objective. Once constraints have been met, the compactor tries to enforce any specified objectives.

operators
An operator is a named operation that performs functions on selected subsets.

optimal layout
An optimal layout is the final layout for a cell, which is at, or below, the target cell width.

overhang
An overhang is the amount that a region extends past the dimensions of a boundary.

pairing
Pairing is a part of the hierarchy extraction process, which allows the hierarchy extractor to pair
MOSFETs that are not included in existing circuitry patterns.

parallel component
A parallel component is a part of a script which represents an array of design steps that adds breadth to the tree.

physical design rule
A physical design rule defines layer geometrical requirements that must be enforced to ensure layout designs are functional and manufacturable with an appropriate yield. These rules are usually provided in foundry design rule documents.

pitch
Pitch is the space between IO grid lines.

placement
Placement is a design step that arranges all devices of a netlist in a symbolic representation.

poly jumper
A poly jumper occurs when a signal is provided from one part of the circuit to another through a connection in POLY. Also refer to *diffusion jumper* and *jumper*.

port
A port is a device which implements a gridded hitpoint for connecting to the cell's primary input/output ports. The device has similar shapes to a contact, since the chip level router usually connects standard cells with layers other than those used within the cell.

power diffusion
Power diffusion is diffusion on a power net. Also refer to *diffusion*.

power net
A power net is a named net within a circuit netlist that represents a physical connection to a power supply rail such as VDD, or VSS (Ground).

power rail
A power rail is a background device that passes a signal over the width of a cell. Power rails are usually created for a VDD or VSS net, but can also be created for other signals such as a clock or reset signal. Power rails correspond with boundary dimensions.

power routing
Power routing refers to the wires and contacts needed to fully connect all VSS and VDD nodes to the power rails.

predefined layer
A predefined layer is a layer that sets the color and stipple patterns for system graphics.

preferred rule
A preferred rule applies a greater value for a specific design rule in the final layout when possible. For more information, refer to Preferred Rule on page 64.

principal MOSFET
A principal MOSFET is the MOSFET that receives the width contributed by the secondary MOSFETs during unfolding or resizing. Principal MOSFETs must be identified by an operator and secondary MOSFETs must be identified by a selector. Also refer to *secondary MOSFET*.

process ID
A process ID number is the current number of your Cadabra, session. The number is shown in the titlebars of the Interrupt button and AL Window and helps you to differentiate between multiple concurrent sessions.

pruning
Pruning is the process of removing branches from a design tree.

p-type
A p-type is a physical device that consists of a semiconductor material doped to have an excess of p-type electrical carriers (holes).

rail
A rail is a device that provides a boundary relative shape used for providing a signal of a given net to cross the width of the cell. The most common usage is a power rail, but can also be used for other signals (such as clock, quiet, or reset).

range
A range is a set of values that a variable can have.

relative offset
A relative offset is the placement of devices relative to other devices.

representative layer
A representative layer is a layer that defines the physical mask layer which consists of a set of logical layers. Representative layers are typically used to differentiate a variety of design rules against a physical mask layer. For more information, refer to Representative Layers.

resistor
A resistor is a passive circuit element formed in a C-MOS circuit using chemical treatment and/or geometric mask patterns.

root
A root is the first design point at the top of the design tree. This design point cannot be removed.

routing
Routing is a design step that adds wires, contacts, ports, and diodes to a symbolic layout so that it completely implements the input netlist.

routing geometry
The routing geometry refers to the shapes that are present in the symbolic layout during the routing phase of ATL (Automated Transistor Layout). Devices may present a slightly different set of shapes during compaction or after layout generation.

searching
Searching is part of the hierarchy extraction process, which allows the hierarchy extractor to match parts of the netlist circuitry with known patterns.

secondary
A secondary MOSFET is a MOSFET that contributes with its given width to the principal MOSFET during unfolding or resizing. Secondary MOSFETs must be identified by a selector and principal MOSFETs must be identified by an operator. Also refer to *principal MOSFET*.

series components
A series component is a part of a script which represents a single chain of design steps that adds depth to the tree.

shape database
The shape database (shapeDB) contains geometry, placement, and possibly routing information on the shapes in the GDSII layout.

single-height cell
A standard cell consisting of two well regions: an N-well region containing the P-type MOSFETS positioned in the top portion of the cell and a P-well region containing the N-type MOSFETS positioned in the bottom portion of the cell.

snapping
Snapping is the process of moving cell objects to an IO grid coordinate. Typically, a snapped item moves to the grid point closest to it.

source
A source is a region on a MOSFET and is always paired with a drain region. The two regions are separated by a gate. A source is usually implemented with a diffusion layer mask.

source layout
A source layout is the GDSII layout used as input for the migration process. The netlist of the source layout is extracted and compared to the netlist of the cell. If the two netlists do not match, the migration process fails.

SPICE
SPICE (Simulated Program with Integrated Circuit Emphasis) is a circuit and simulator analyzer software.

spice2al
spice2al is a program separate from Cadabra, that is run from the command line. The program converts cell netlists in SPICE format to AL format. AL formatted netlists are required as input to Cadabra.

stipple pattern
A stipple pattern is the textural representation of a layer.

strap
Strap is a layer that is typically used for a tie connection.

substrate
Substrate is the doped silicon material which forms the foundation for MOS transistors.

symbolic boundary
The symbolic boundary is a device that acts as a bounding box for the entire cell.

symbolic device
A symbolic device is a representation of a layout feature, which defines how the device is drawn, how it interacts with other devices, and how it behaves during compaction. Symbolic devices include MOSFETs, ports, wires, contacts, and the boundary, as well as special user-defined devices.

symbolic layout
A symbolic layout is a representation of a cell layout in which transistors, wires, contacts, and other cell features are represented by symbolic devices. Symbolic layouts capture the topology of a cell layout, but not the exact dimensions.

tap
A tap is a connection made in the layout to avoid latch-up of the circuit. The layer typically used for a tap connection is called strap. Taps are also referred to as ties.

technology
A technology defines the layers used in the manufacturing process and the process design rules governing the behavior of shapes on those layers.

tie
A tie is a connection made in the layout to avoid latch-up of the circuit. The layer typically used for a tie connection is called strap. Ties can be placed as horizontal rails of contacts or they can be generated to fill in the gaps after a cell layout has been compacted. Ties can also be referred to as taps.

tie rail
A tie rail is a horizontal rail of tie material placed along the width of the cell. Tie rails implement a well or substrate tie. Depending on the tie strategy, contacts may or may not be needed for the length of the rail shape.

tile
A tile consists of logically-related transistors that are grouped together through a process of searching, chaining, and pairing, called hierarchy extraction.

tile merging
Tile merging is a method of minimizing the number of tiles in a cell, which speeds up the auto placement process.

transistor
A transistor is an active switching element in a circuit.

VDD
VDD is the positive power supply net.

verification
A verification is a consistency check that you can run on the technology that verifies that all the basic requirements of the technology are being met.

via
A via is an electrical connection between overlapping routing layers that is created with cuts in the insulating silicon dioxide. For example, METAL1 is connected to METAL2 through a via.

virtual short
A virtual short occurs when you do not connect MOSFETs that were folded in a series.

VSS
VSS is the negative (or ground) power supply net.

well
A well is a diffusion layer used to create an effective substrate within an actual substrate of an opposite carrier.

wire
A wire is a device which represents a single straight strip of material, used to form a connection between two points.

wire jog
A wire jog is a very short horizontal or vertical wire segment inserted into a larger orthogonal wire segment to facilitate bending.

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