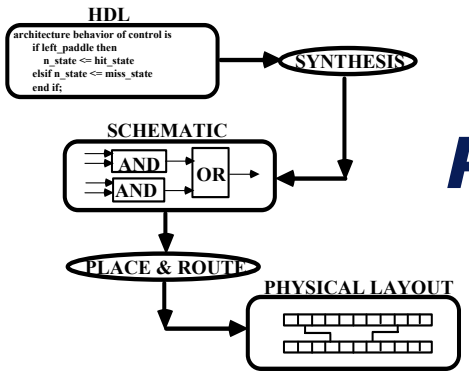
DESIGNING FPGAS & ASICS



Component Reuse

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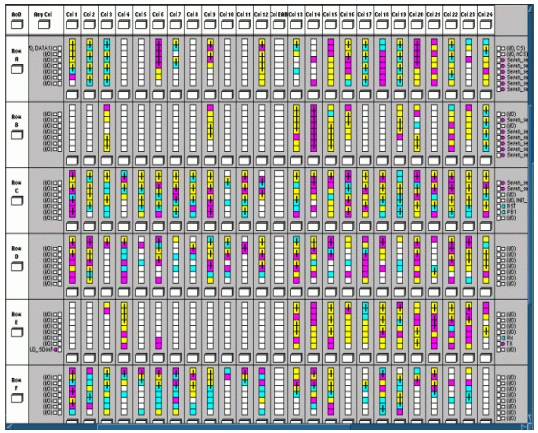
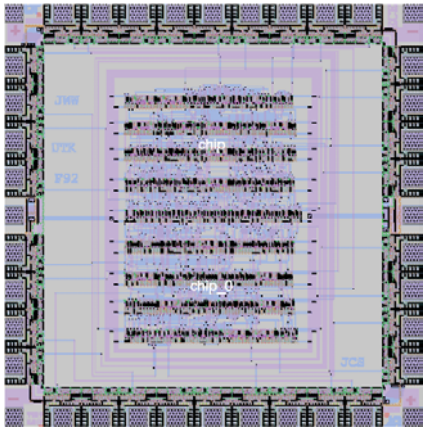


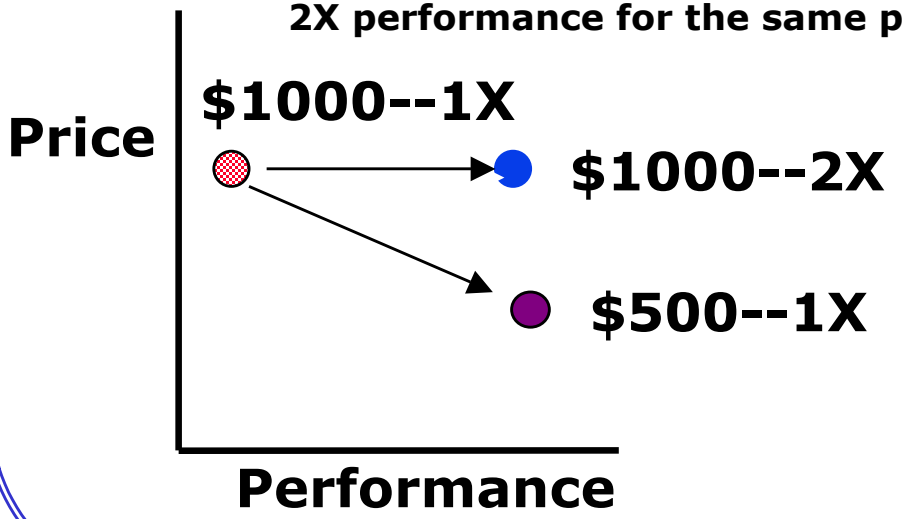


COURSE OUTLINE

- Overview of FPGAs and ASICs
- Using Synthesis
- HDL Examples
- Simulation and Testing
- Physical Place and Route
- Testing ASICs
- Component Reuse

ELECTRONIC PRODUCTS ARE PERVASIVE AND ALWAYS IMPROVING

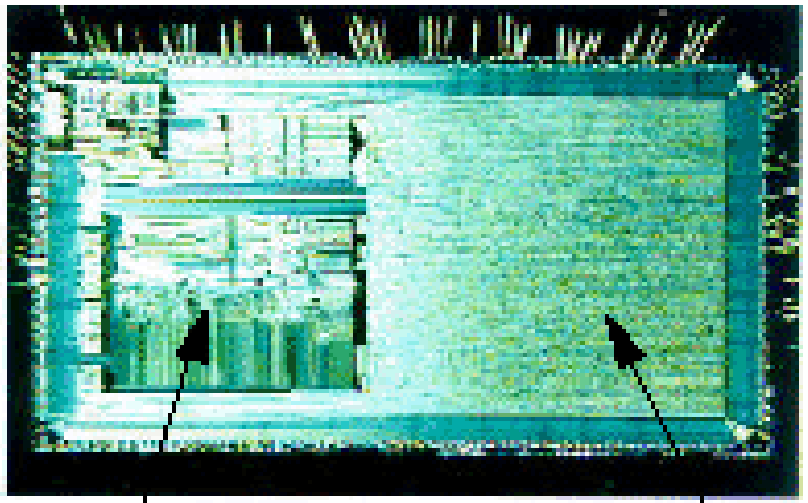
Moore's Law: Every 18 months integrated circuit manufacturing can produce 2X performance for the same price or the same performance for half the price.



Design Example

Nokia 9000 wireless phone/PDA

Nokia 9000



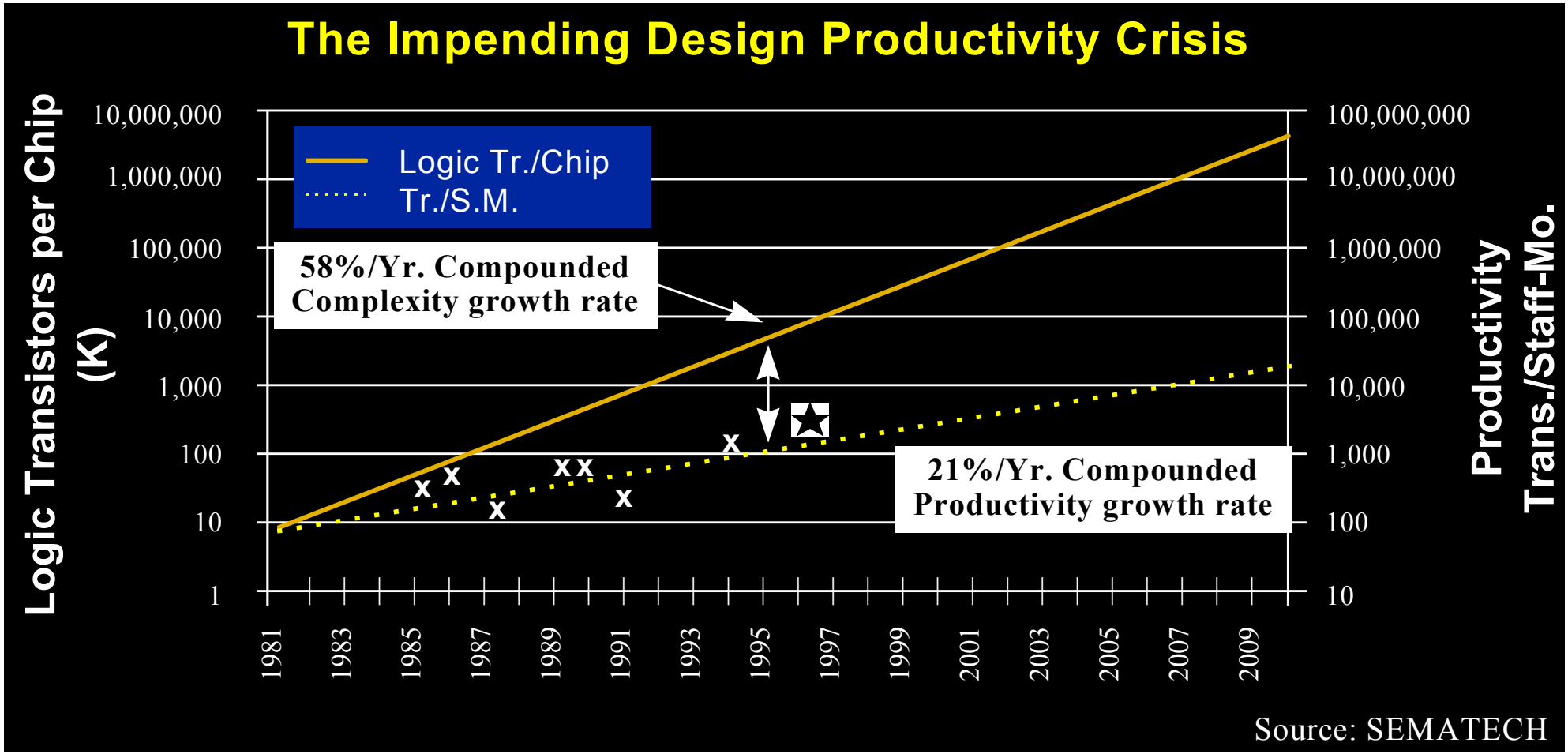
Embedded μP Core

90K CBA gates

- Personal digital assistant (PDA) and GSM cellular phone
- Embedded block imported into a CBA foundation
- "Required 2 Mask Designers instead of 20"

SYNOPSYS®

DESIGN PRODUCTIVITY LAGS MANUFACTURING CAPABILITY



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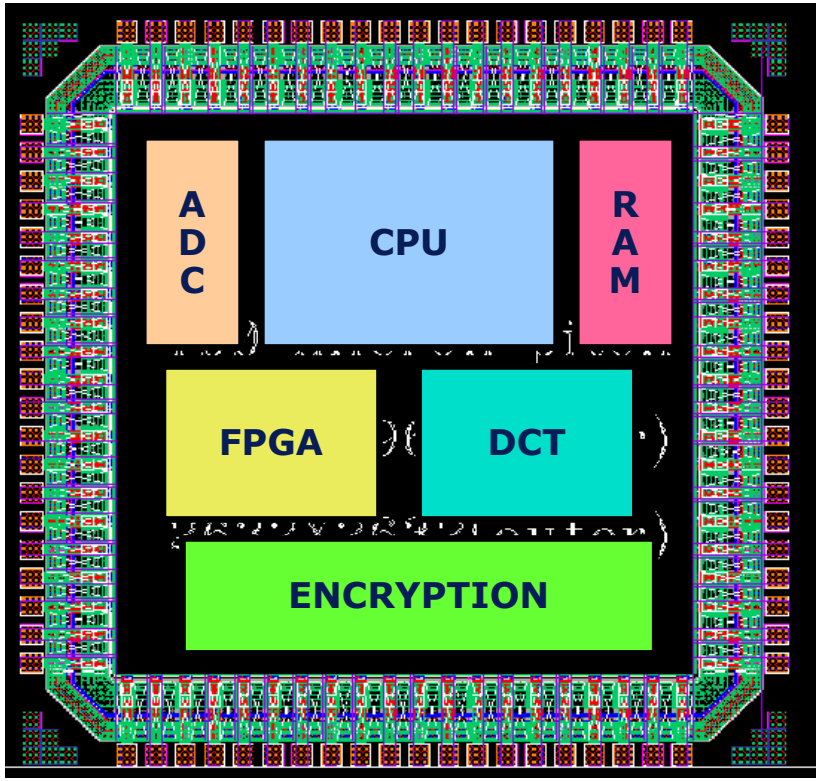
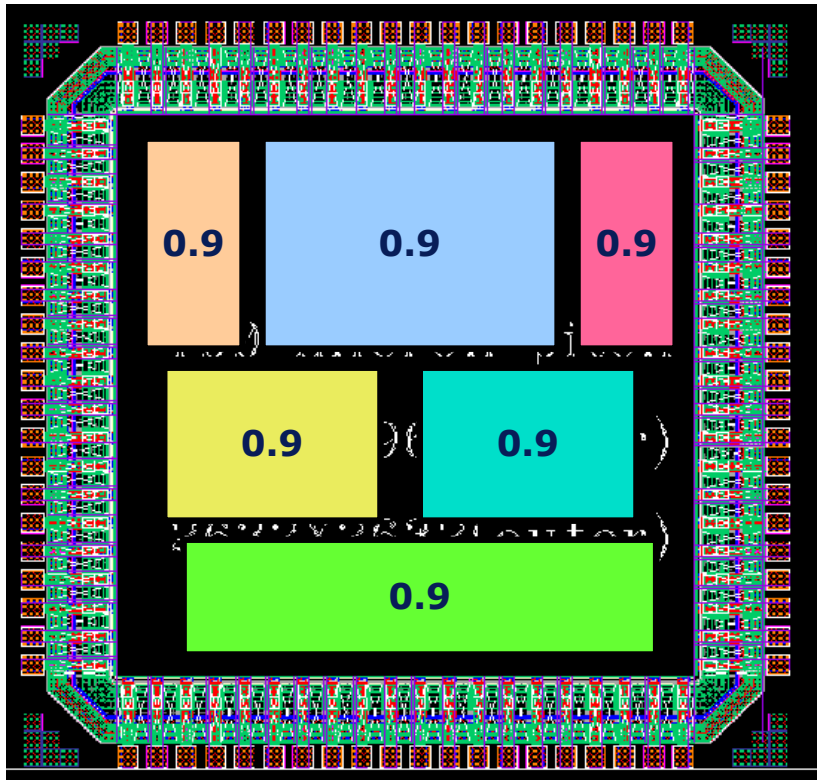
A SYSTEM-ON-CHIP CAN REUSE COMPONENTS

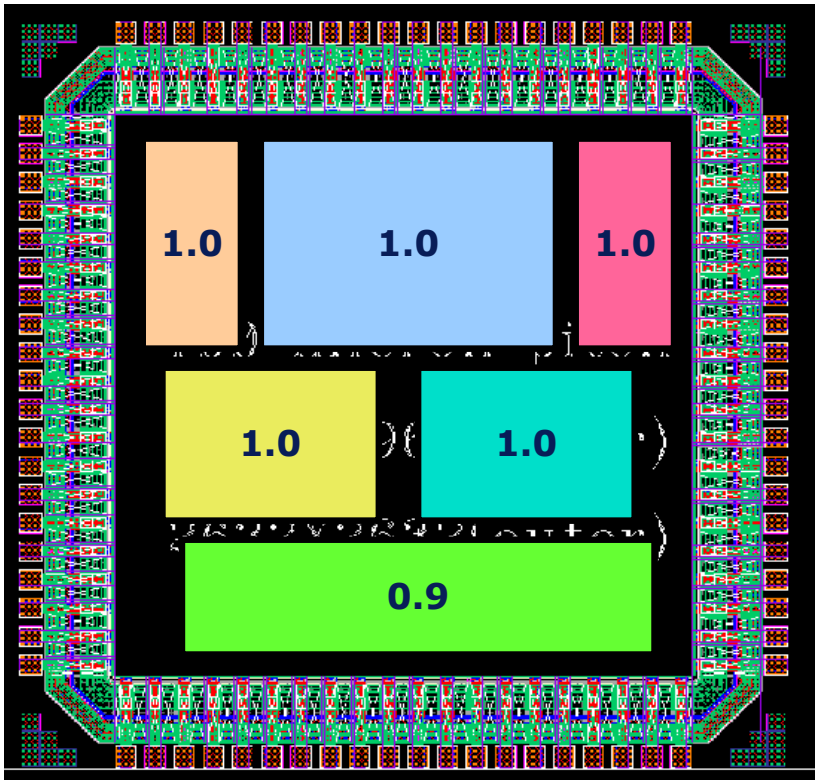
- EACH COMPONENT MUST BE "KNOWN GOOD"
- DETAILED INFORMATION IS REQUIRED FOR SUCCESS
- BEST WHEN COMPONENTS ARE DESIGNED FOR REUSE



UNPROVEN COMPONENTS AND INTERCONNECT ARE RISKIER AND MORE TIME-CONSUMING TO VERIFY

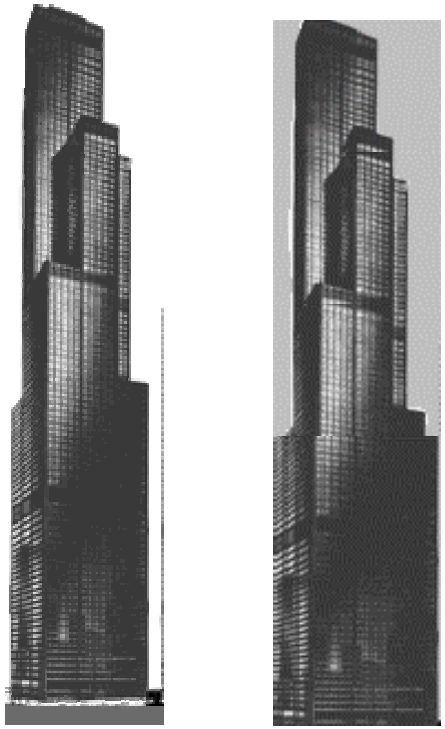


Interconnect 0.9 so
0.9x0.9x0.9x0.9x0.9x0.9x0.9
= 0.5

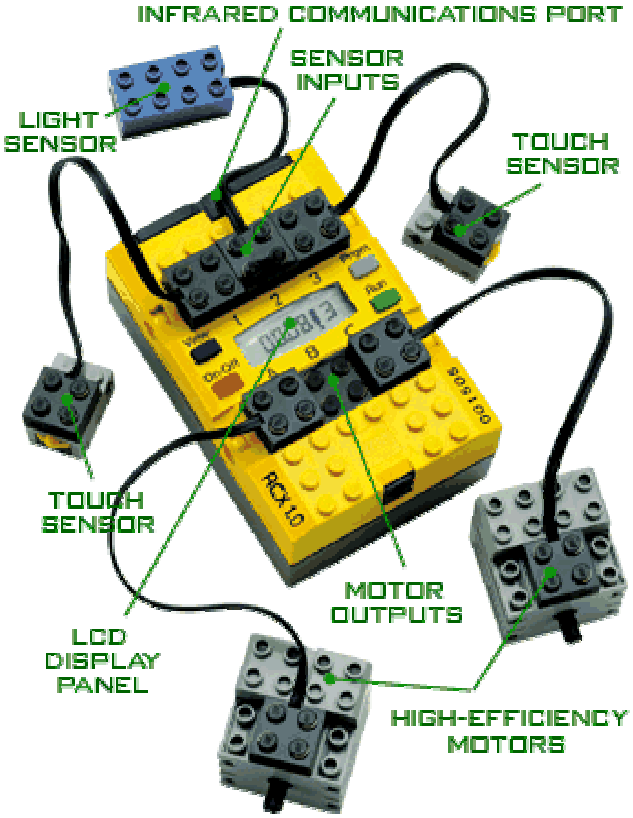


Interconnect 0.9 so
1.0x1.0x1.0x1.0x1.0x0.9x0.9
= 0.8

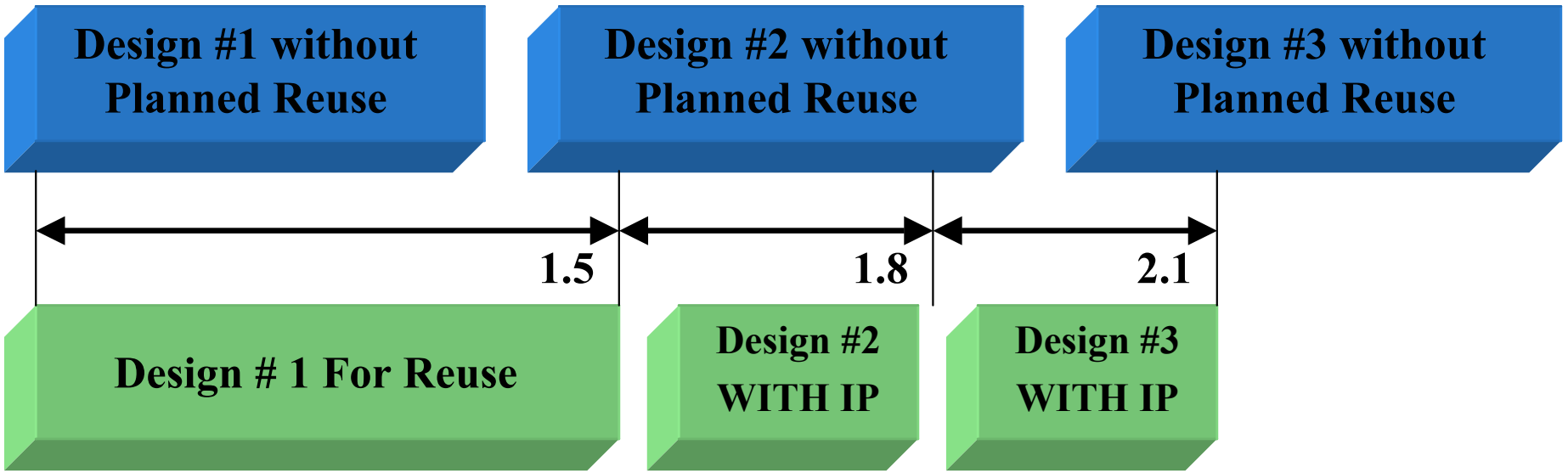
WE BUILD SKYSCRAPERS USING STANDARDIZED BLOCKS



So, let's use standardized blocks to build systems



DESIGN WITH REUSE CAN HAVE A SIGNIFICANT IMPACT



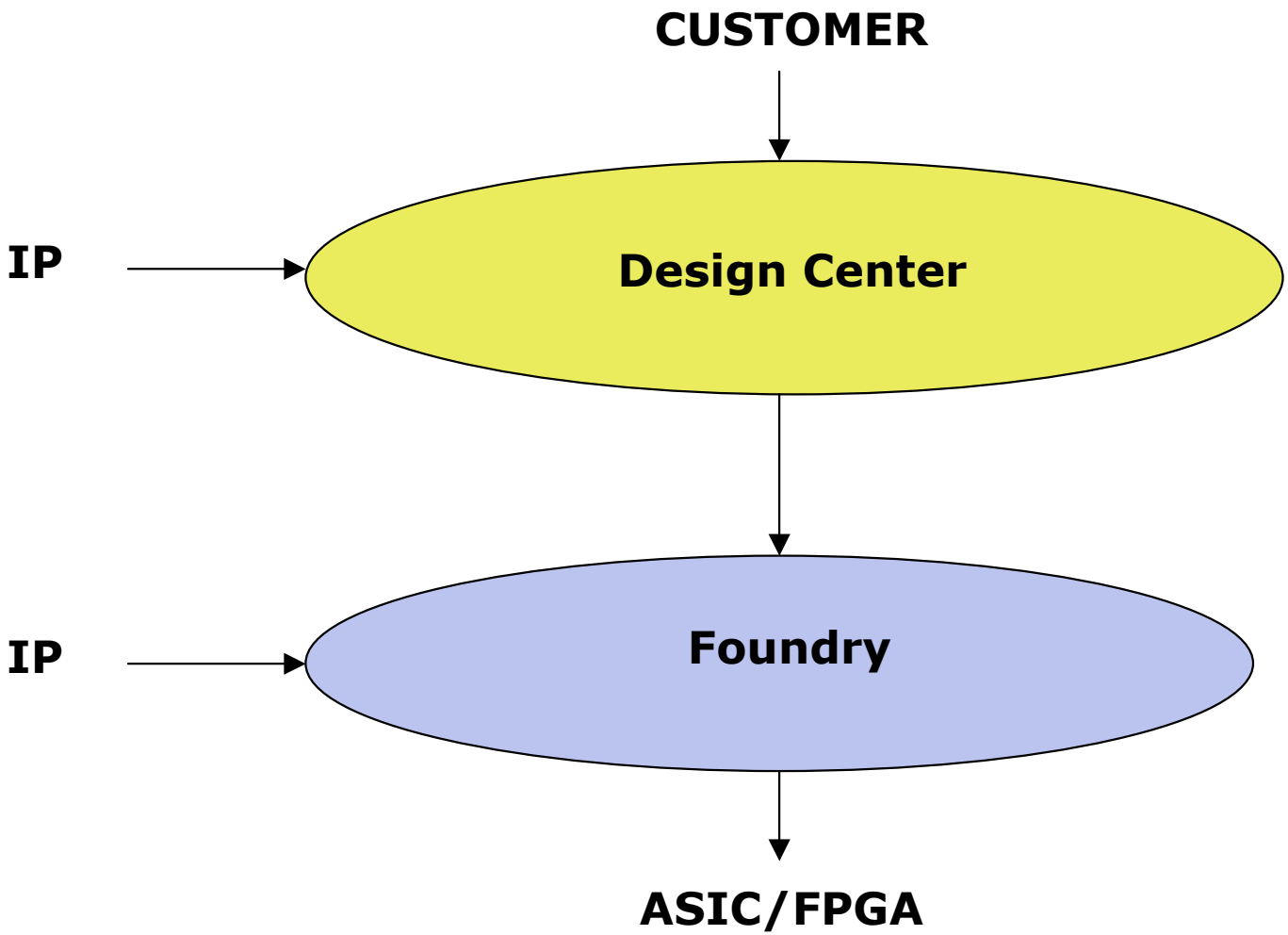
IP blocks should have well-defined interfaces

Often, IP are more like patches that must be stitched together like a quilt

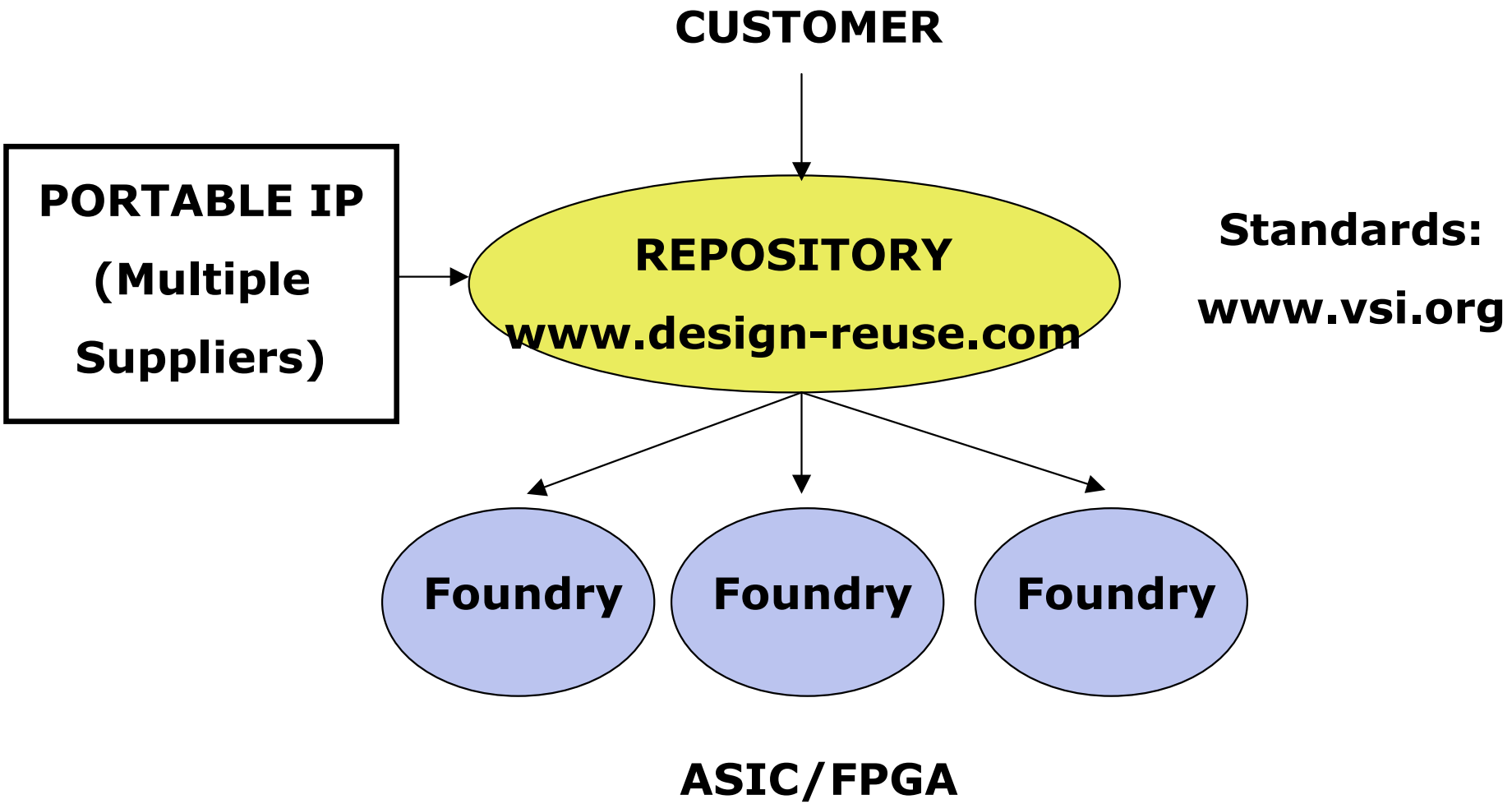
REQUIREMENTS FOR REUSABLE IP

- **BASICS:**
  - **HDL Models**
  - **Functional Description**
  - **Application Intent**
  - **Interface Specifications**
  - **Authors and Owners**
  - **Size, Delay, Power Estimates**
  - **Packaging Info**
- **ALSO NEED:**
  - **Test Bench (Input Stimuli/Output Responses**
  - **Tools and Versions Used/Needed**
  - **Foundry Used For Fab**
  - **Size, Delay, Power Measurements**
  - **Testability Features (BIST, JTAG, SCAN)**

LOW-RISK IP CAN ATTRACT BUSINESS BUT PRICES MAY NOT BE COMPETITIVE



AN OPEN COMPETITIVE MARKET HAS BEEN INITIATED



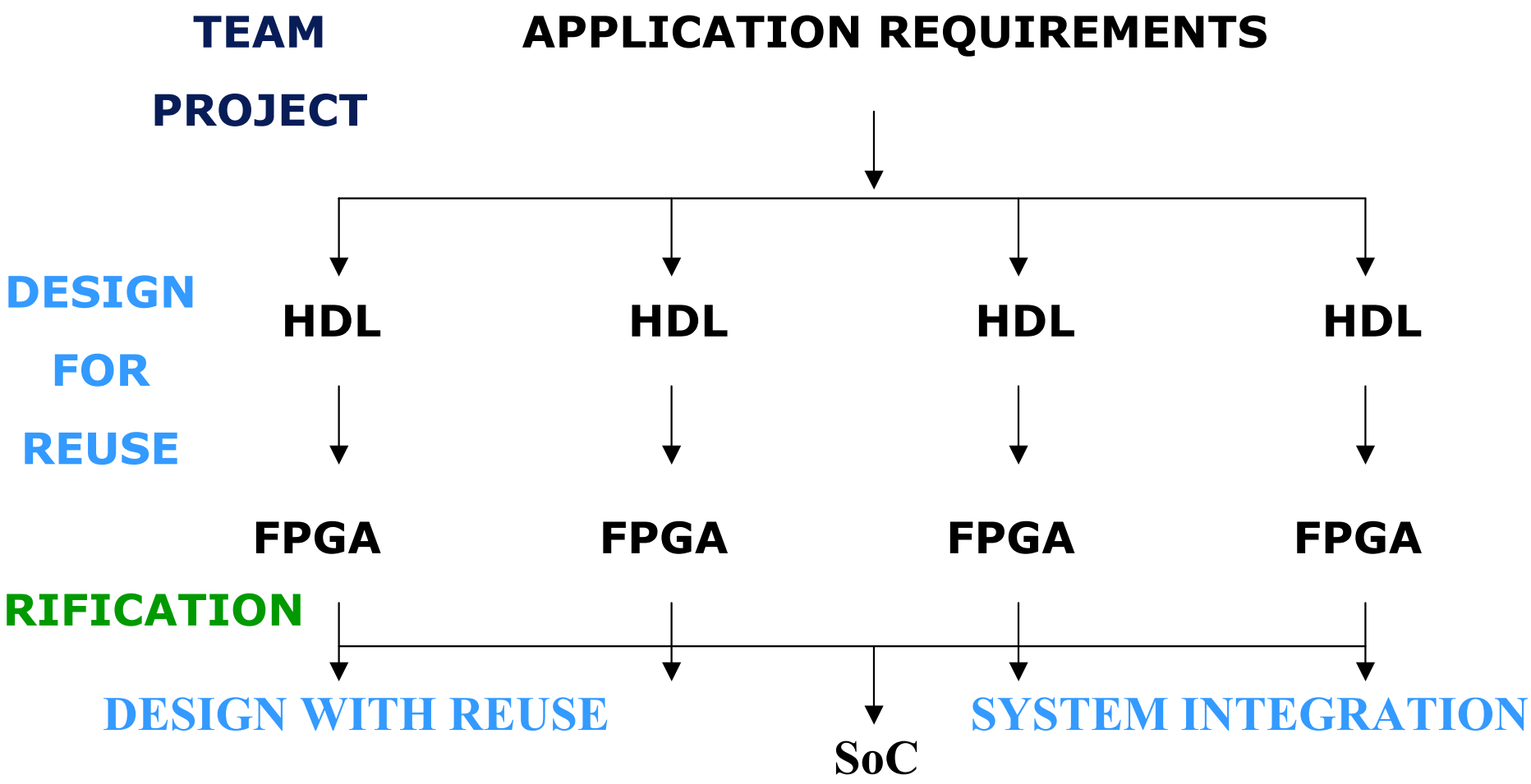
MARKETPLACE EXPERIENCES

- **STAR IP:**
  Blocks requiring 100+ staff years to design (like ARM, MIPS) have become bestsellers and come with lots of support.
- **Small IP:**
  Blocks requiring 1-2 staff years to design are priced at 1/3 of the development cost.
  Buyers are skeptical about the value and often prefer to do these in-house.
- **Medium IP:**
  Blocks requiring 5-10 staff years are profitable for both seller and buyer. However, some suppliers have been bought by foundries to add to the foundries' captive portfolios.

RECONFIGURABLE FPGA-BASED BOARDS CAN PROTOTYPE DIGITAL DESIGNS

- **FPGAs can contain soft or hard IP (including CPUs).**
- **www.atmel.com**
- **www.altera.com**
- **www.triscend.com**
- **www.xilinx.com**

DESIGN-FOR-REUSE and DESIGN-WITH-REUSE



SUMMARY

- We must reuse previous designs to exploit IC manufacturing.
- Designs must be well-documented and well-understood.
- Design-for-reuse and design-with-reuse take time and effort.
- Verification can be done using simulation and prototyping.
- Proven components can be verified in less time.
- Platform design can reduce risk and attract business.
- Digital and analog designs can be prototyped using reconfigurable systems.
- FPGA chips can contain soft or hard CPU cores.
- Multi-project brokers provide inexpensive state-of-the-art fabrication.