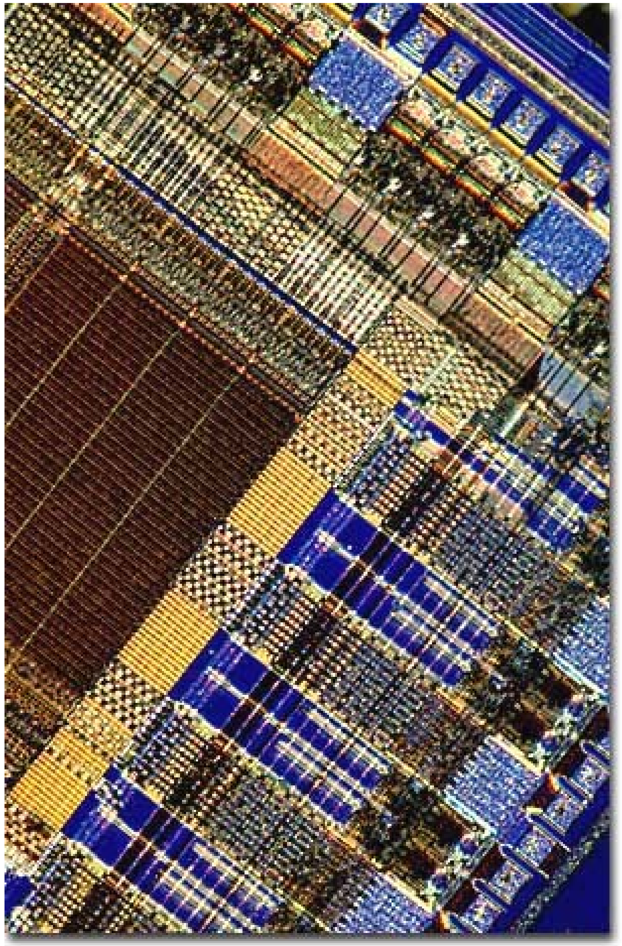
The McGraw-Hill Companies

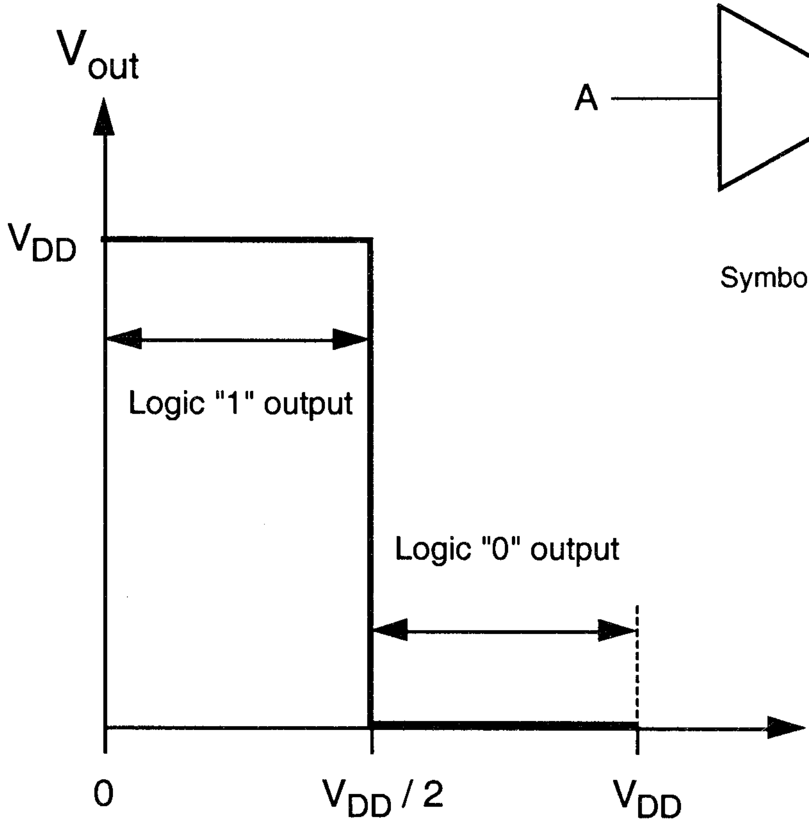
CMOS Digital Integrated Circuits

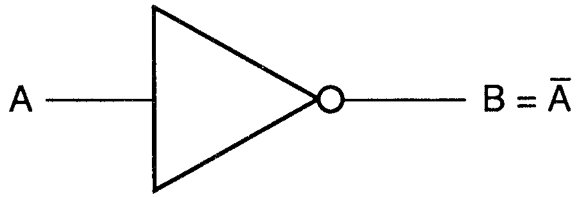


Chapter 5
MOS Inverters: Static Characteristics

S.M. Kang and Y. Leblebici

Ideal Inverter





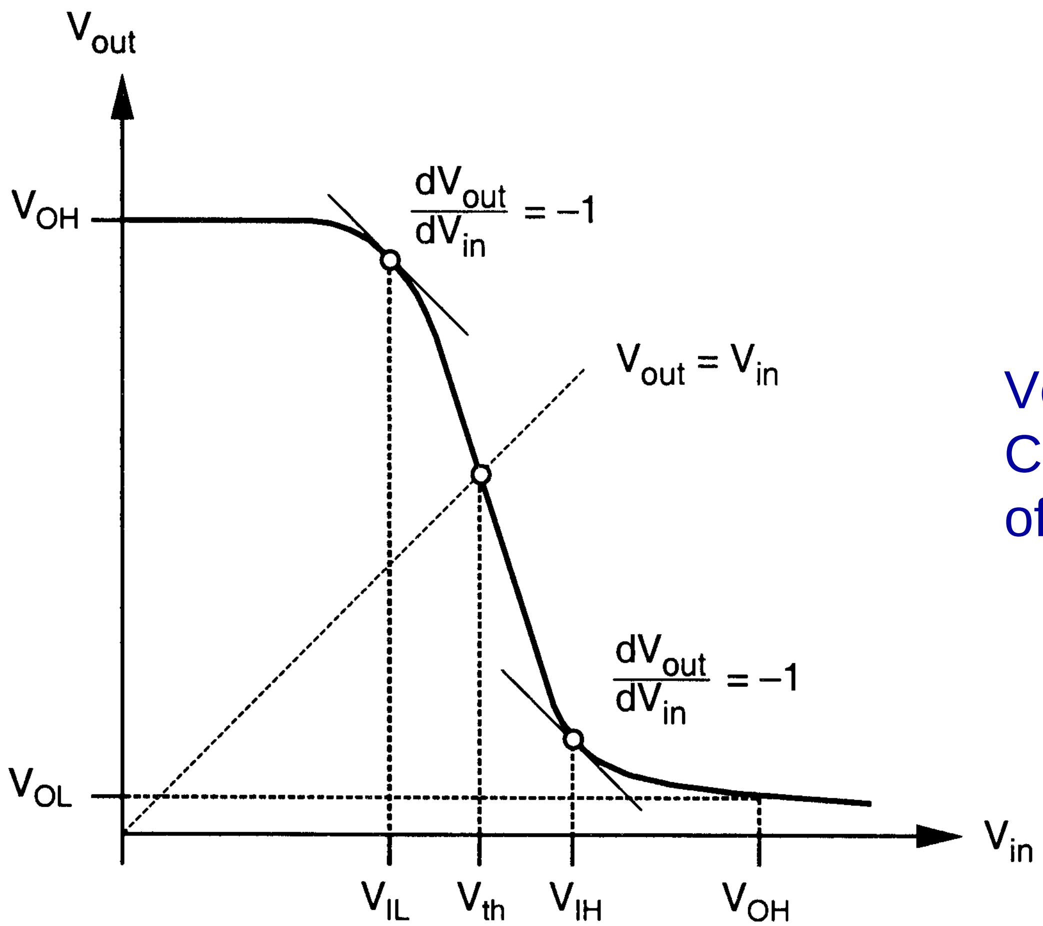
Symbol

A	B
0	1
1	0

Truth Table

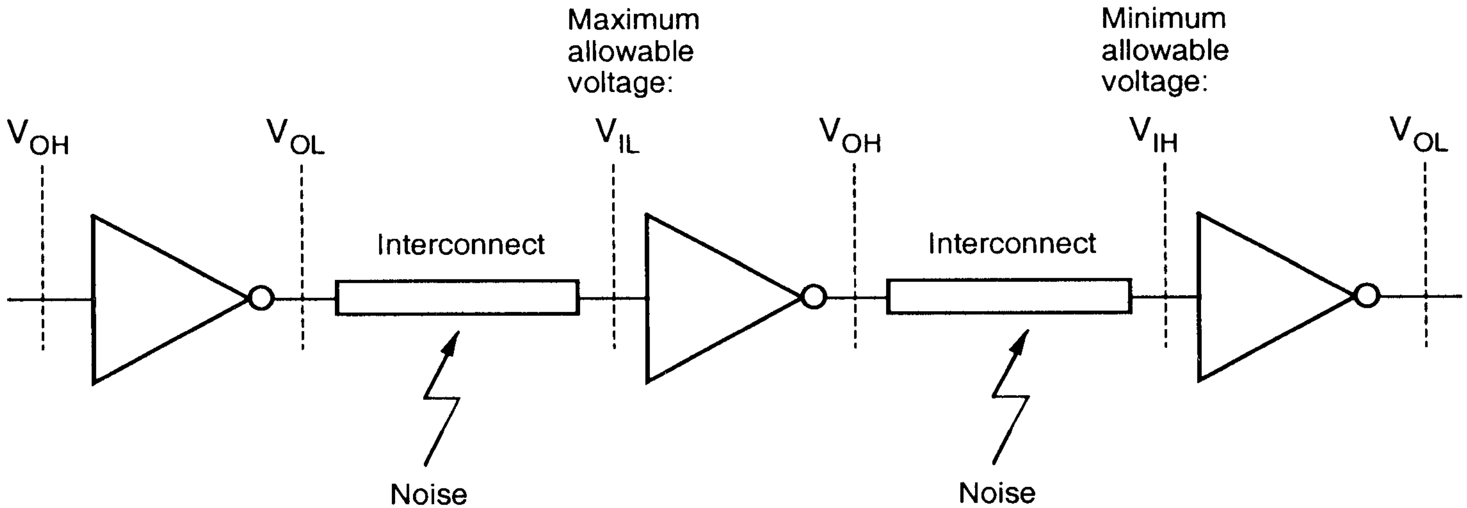
Voltage Transfer Characteristic (VTC) of the ideal inverter

Generic Inverter VTC



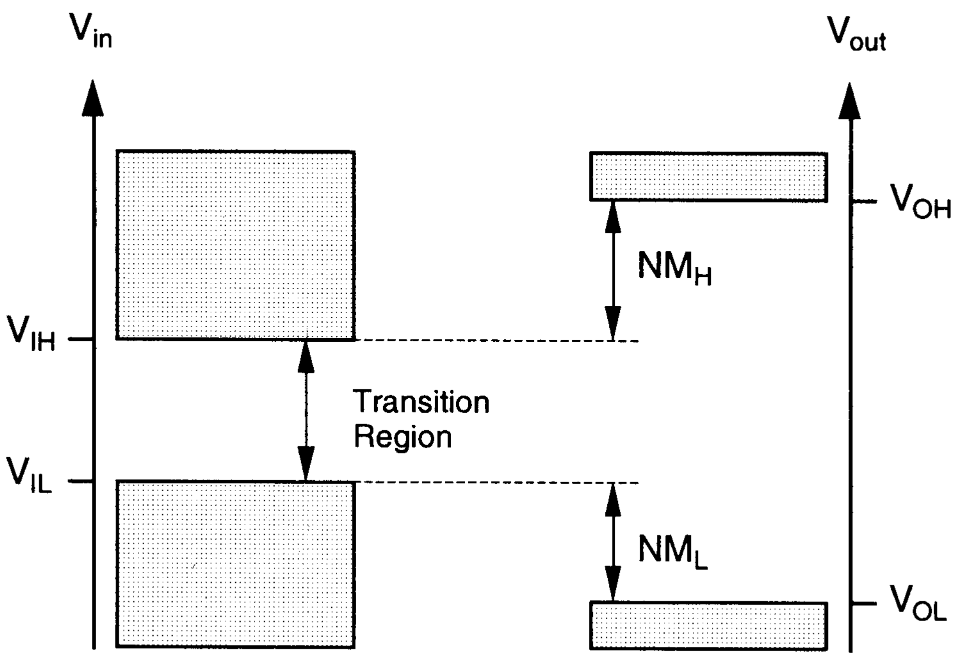
Voltage Transfer Characteristic (VTC) of a typical inverter

Noise Margins



Propagation of digital signals under the influence of noise

Noise Margins



Definition of
noise margins

$$NM_L = V_{IL} - V_{OL}$$

$$NM_H = V_{OH} - V_{IH}$$

Noise Margins

Nominal output

$$V_{out} = f(V_{in}) \tag{5.5}$$

Output under noise

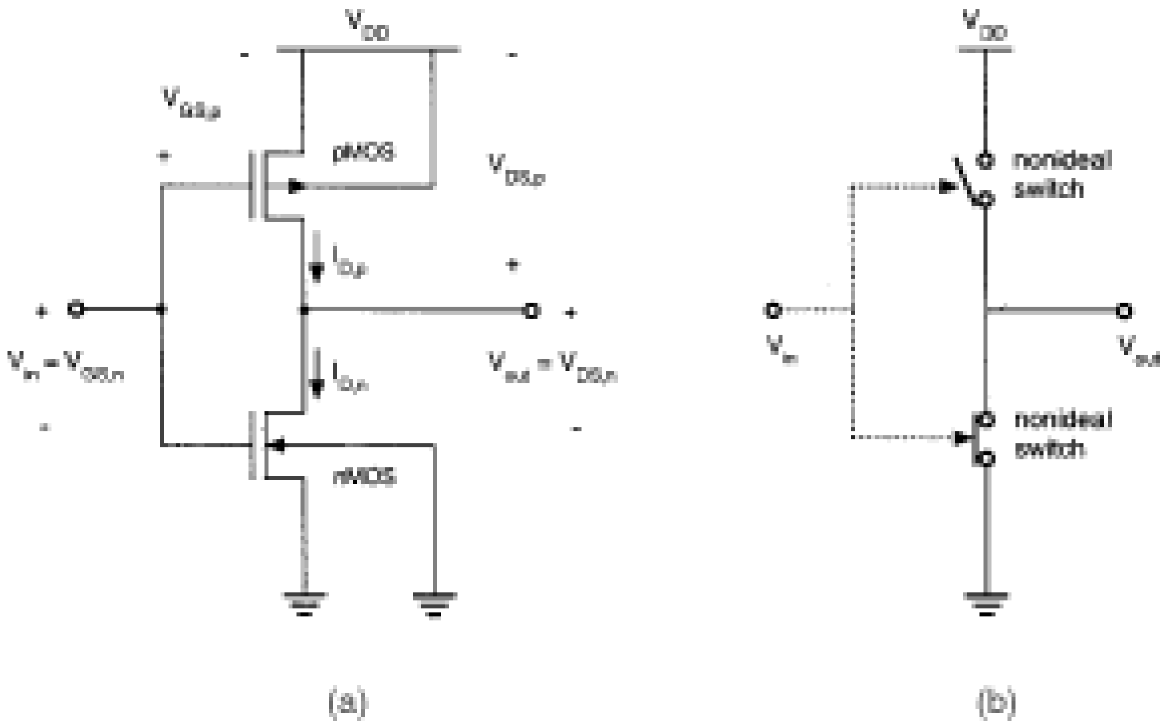
$$V'_{out} = f(V_{in} + \Delta V_{noise}) \tag{5.6}$$

$$V'_{out} = f(V_{in}) + \frac{dV_{out}}{dV_{in}} \cdot \Delta V_{noise} + \textit{higher order terms (neglected)} \tag{5.7}$$

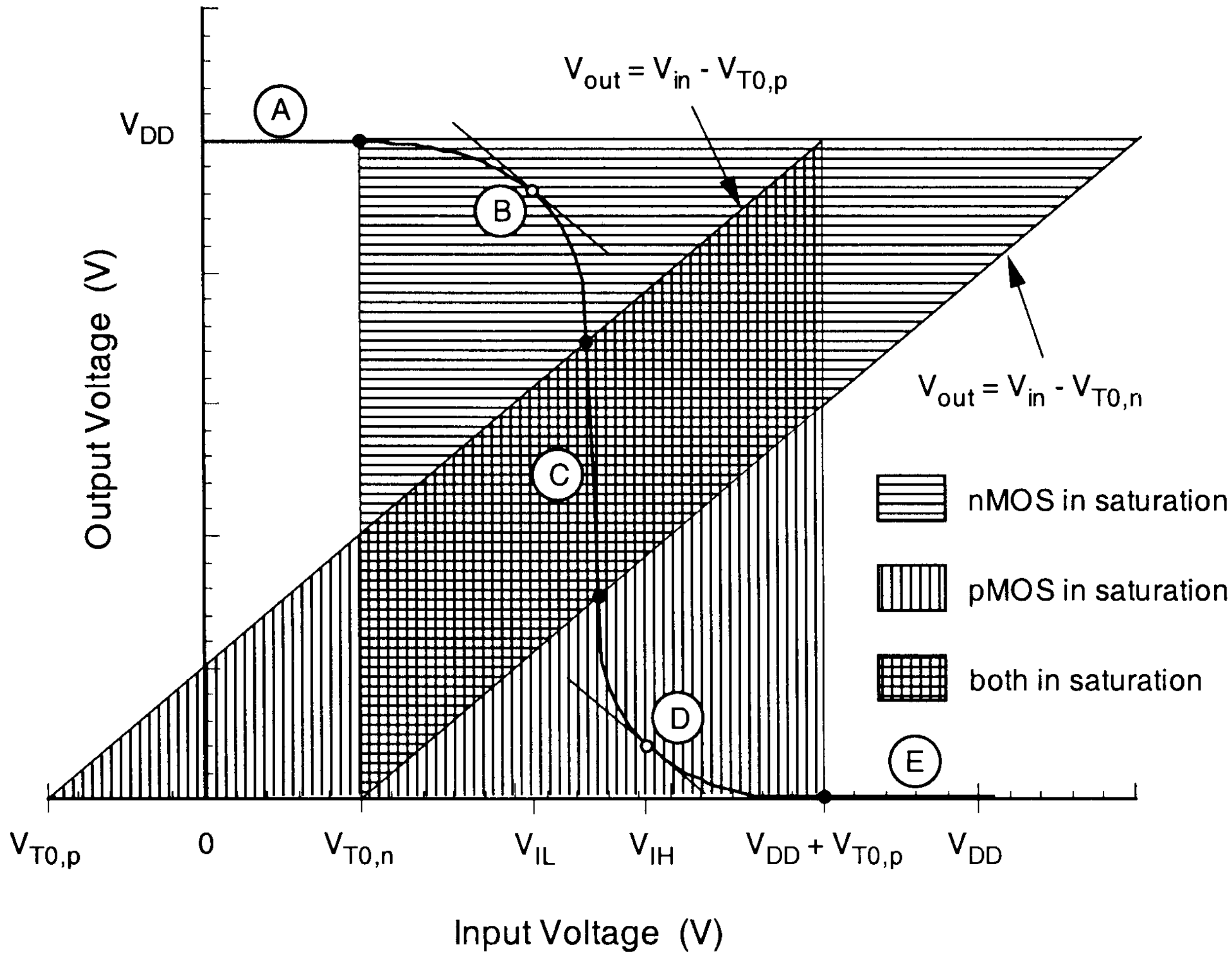
The nominal operating region is defined as the region where the gain is less than unity !

$$\textit{Perturbed Output} = \textit{Nominal Output} + \textit{Gain} \times \textit{External Perturbation} \tag{5.8}$$

CMOS Inverter Circuit



CMOS Inverter Circuit



CMOS Inverter Circuit

determine
noise
margins

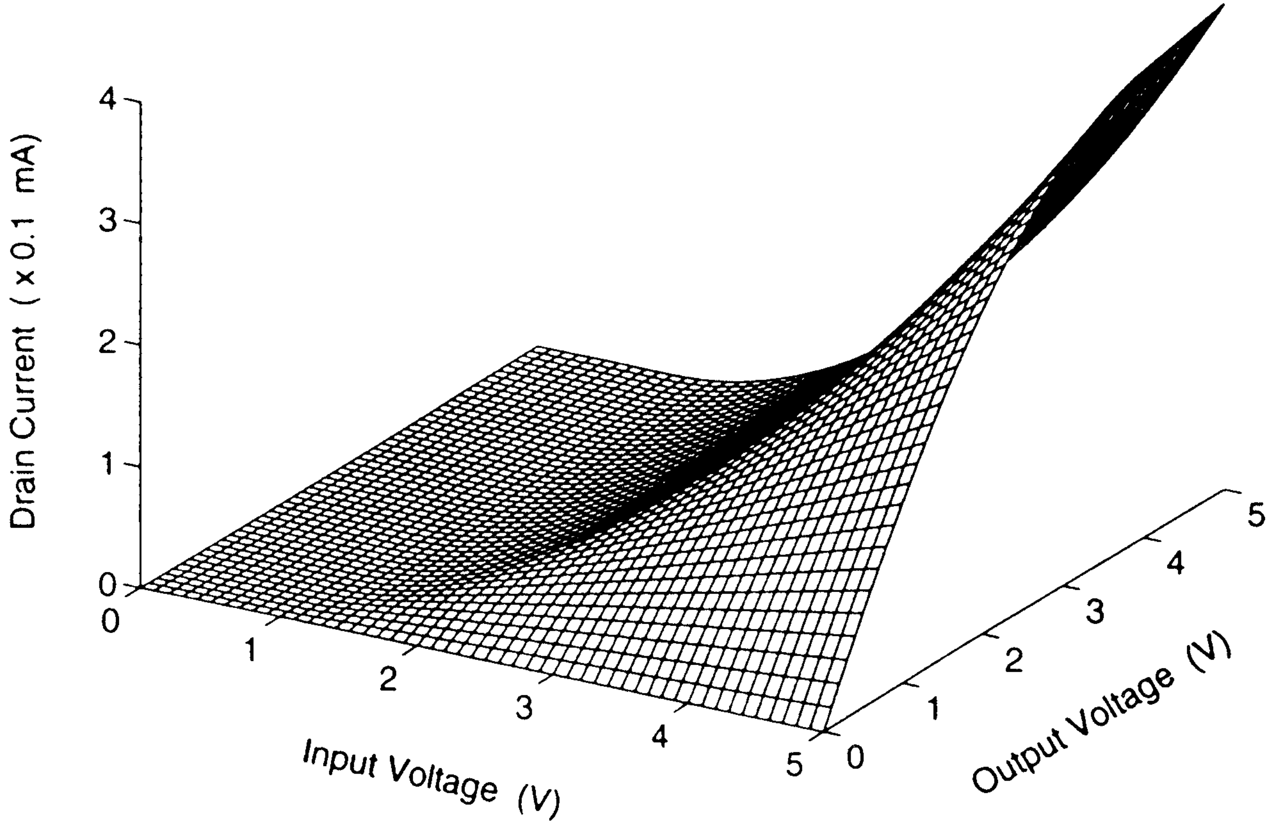
$$V_{IL} = \frac{2V_{out} + V_{T0,p} - V_{DD} + k_R V_{T0,n}}{1 + k_R} \quad (5.62)$$

$$V_{IH} = \frac{V_{DD} + V_{T0,p} + k_R \cdot (2V_{out} + V_{T0,n})}{1 + k_R} \quad (5.67)$$

inversion (switching)
threshold voltage

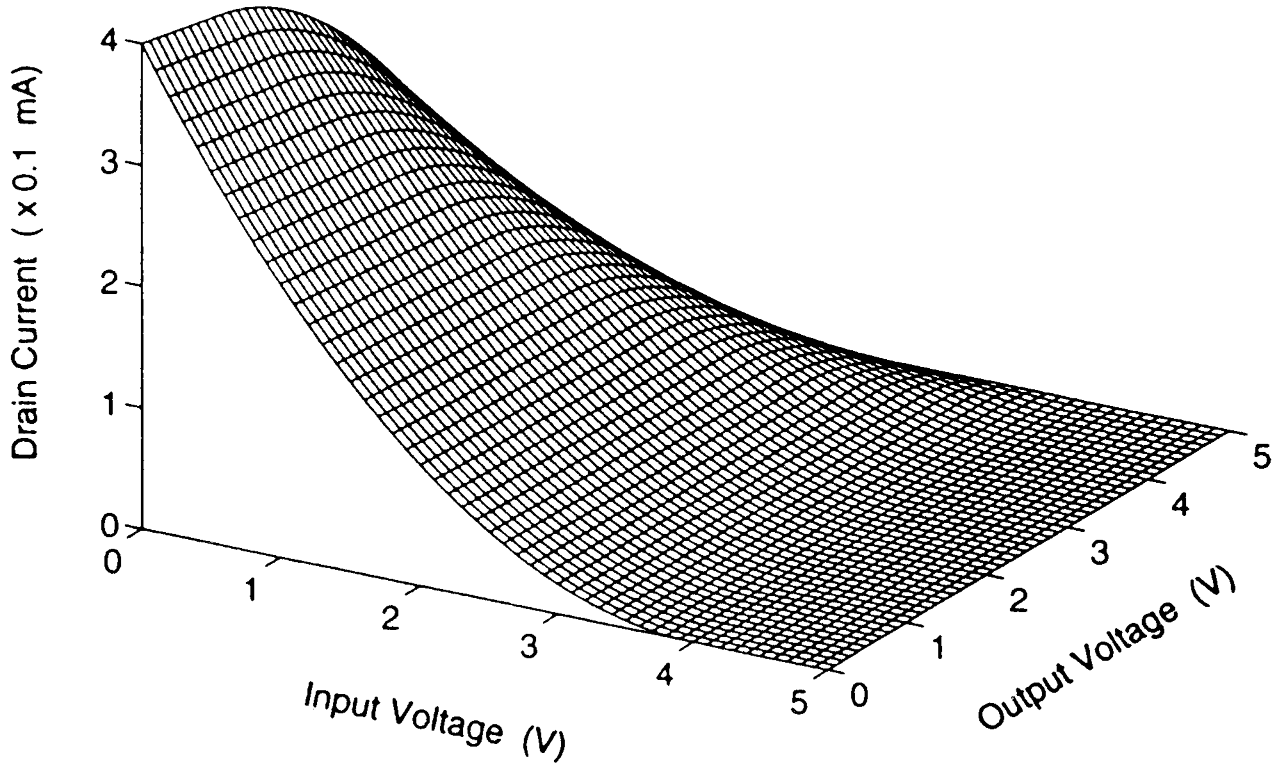
$$V_{th} = \frac{V_{T0,n} + \sqrt{\frac{1}{k_R}} \cdot (V_{DD} + V_{T0,p})}{\left(1 + \sqrt{\frac{1}{k_R}}\right)} \quad (5.71)$$

CMOS Inverter Circuit



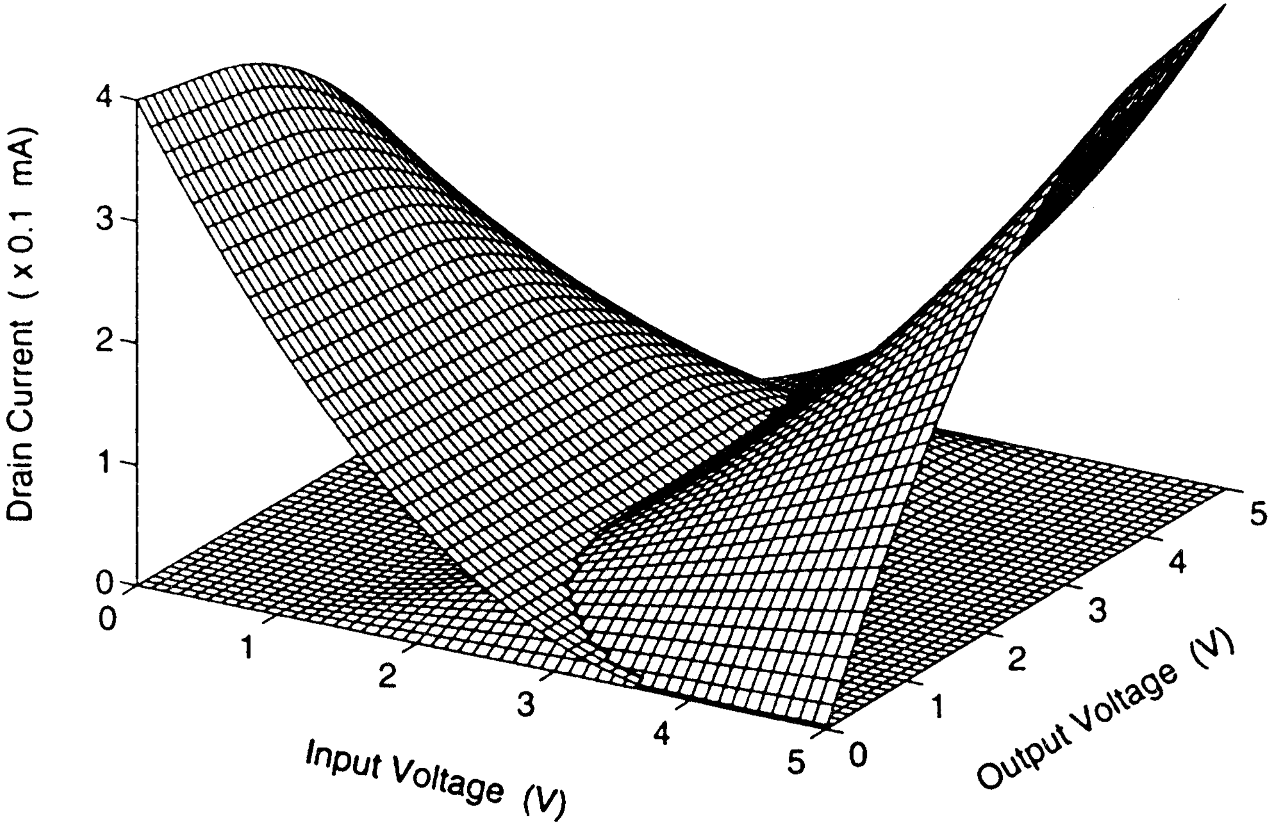
nMOS transistor current-voltage characteristics

CMOS Inverter Circuit



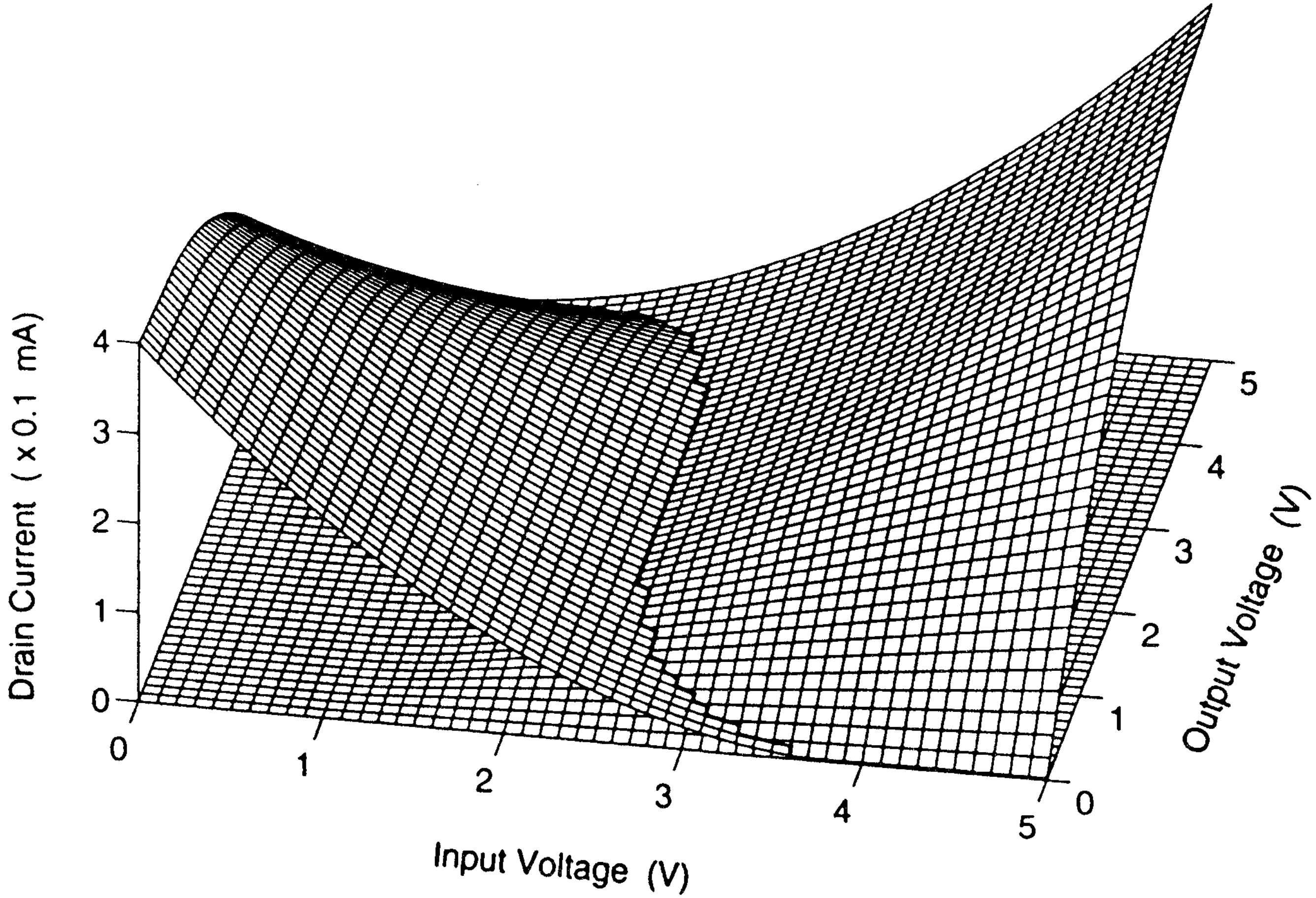
pMOS transistor current-voltage characteristics

CMOS Inverter Circuit



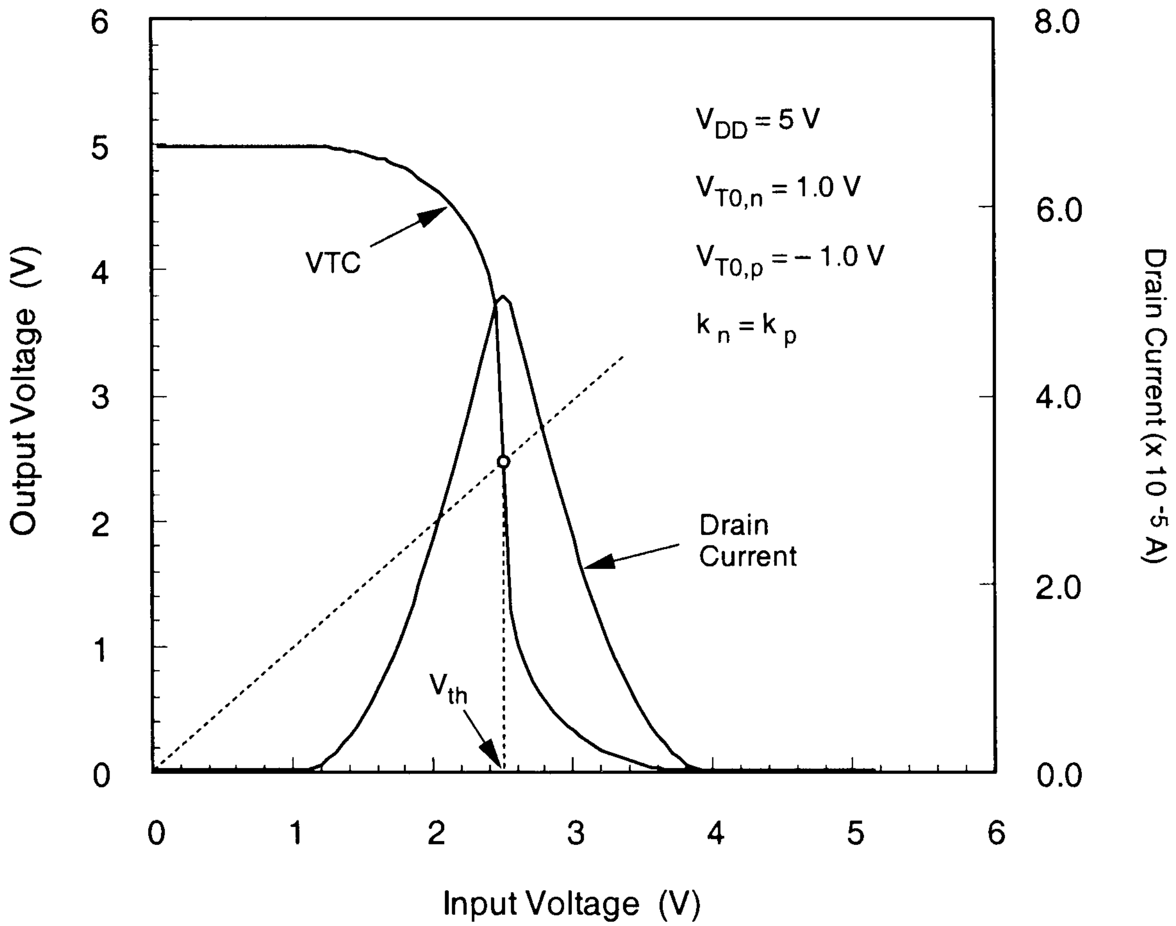
Intersection of current-voltage surfaces of nMOS and pMOS transistors

CMOS Inverter Circuit



Intersection of current-voltage surfaces gives the VTC in the voltage plane

CMOS Inverter Circuit



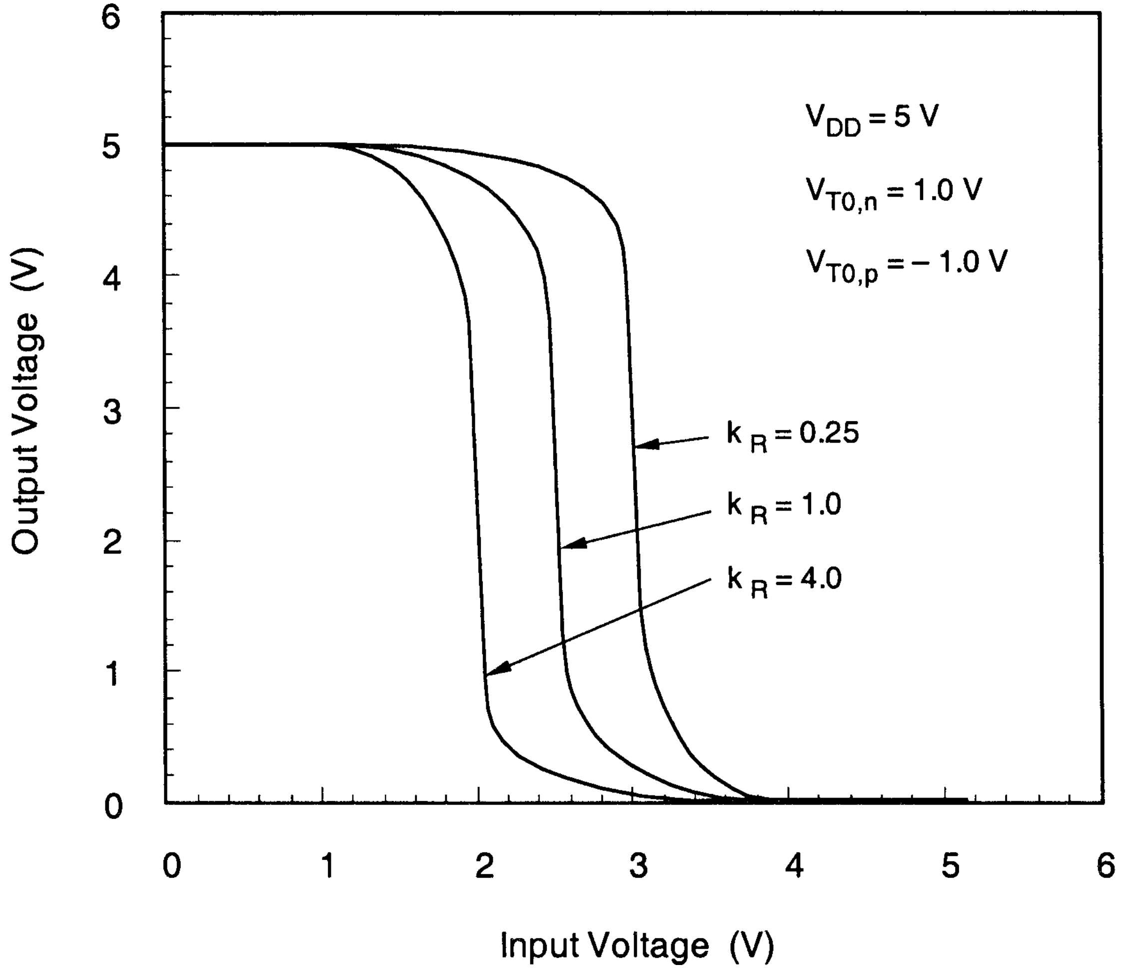
CMOS Inverter Circuit

How to choose the k_R ratio to achieve a desired inversion threshold voltage:

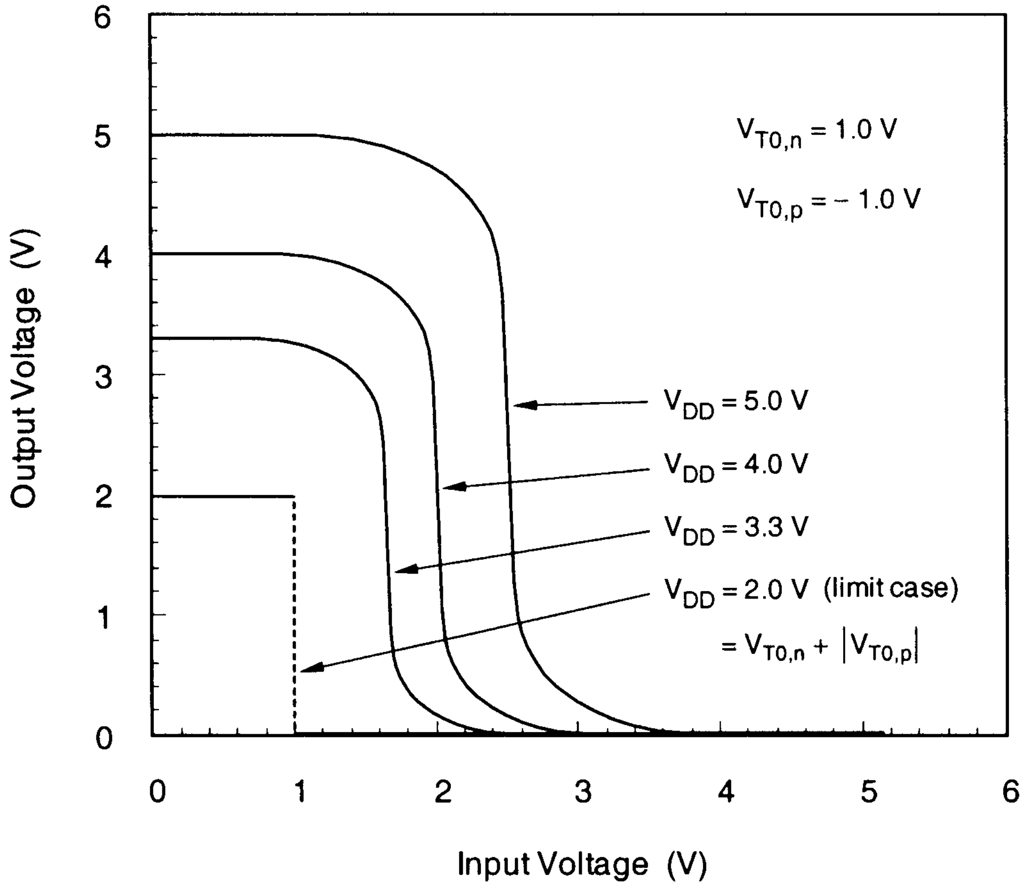
$$k_R = \frac{k_n}{k_p} = \left(\frac{V_{DD} + V_{T0,p} - V_{th}}{V_{th} - V_{T0,n}} \right)^2 \qquad (5.73)$$

$$\frac{k_n}{k_p} = \frac{\mu_n C_{ox} \cdot \left(\frac{W}{L} \right)_n}{\mu_p C_{ox} \cdot \left(\frac{W}{L} \right)_p} = \frac{\mu_n \cdot \left(\frac{W}{L} \right)_n}{\mu_p \cdot \left(\frac{W}{L} \right)_p} \qquad (5.77)$$

CMOS Inverter Circuit

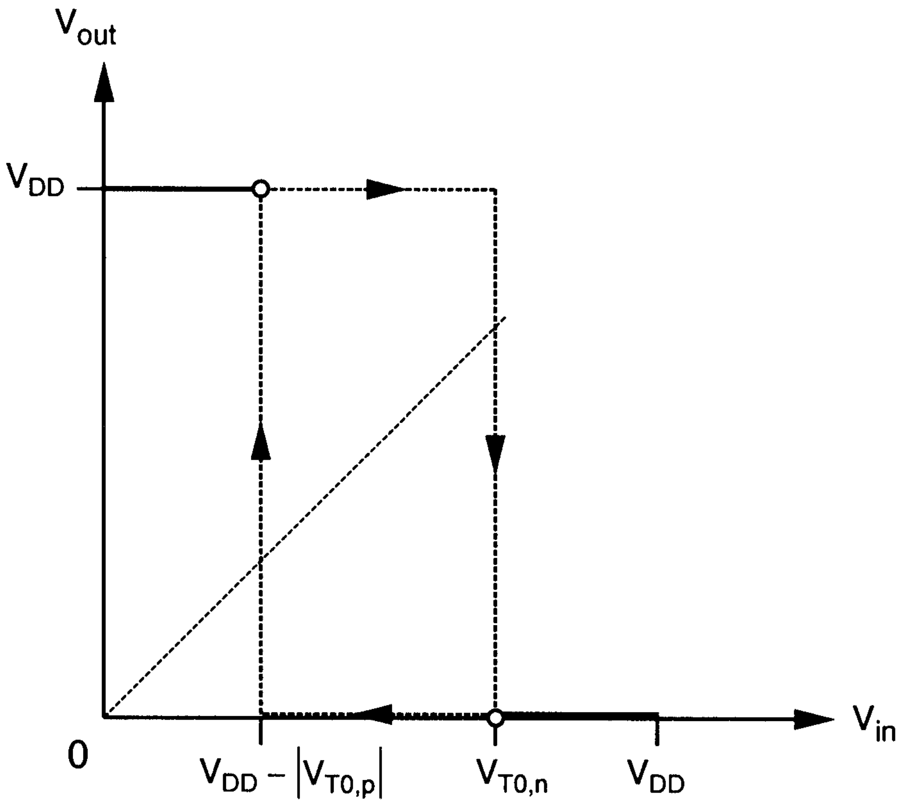


Supply Voltage Scaling



VTC of a CMOS inverter for different power supply voltage values.

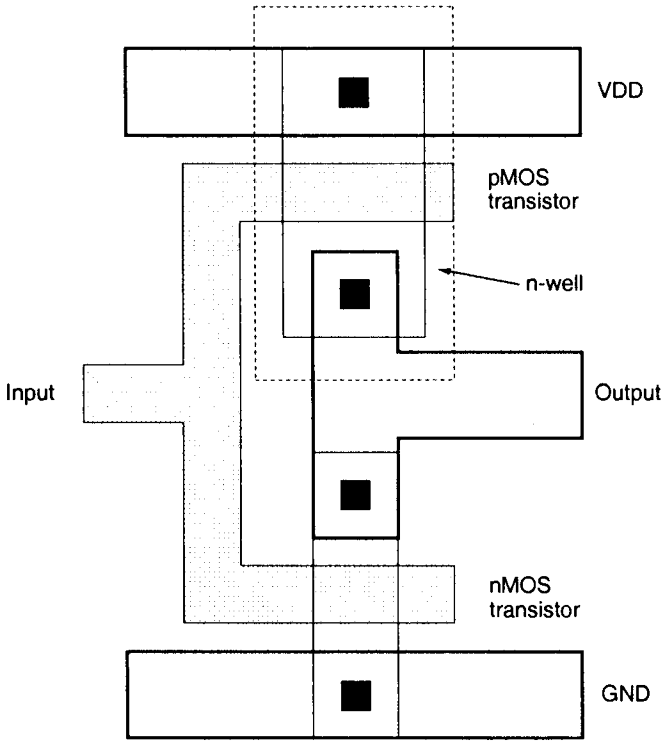
Supply Voltage Scaling

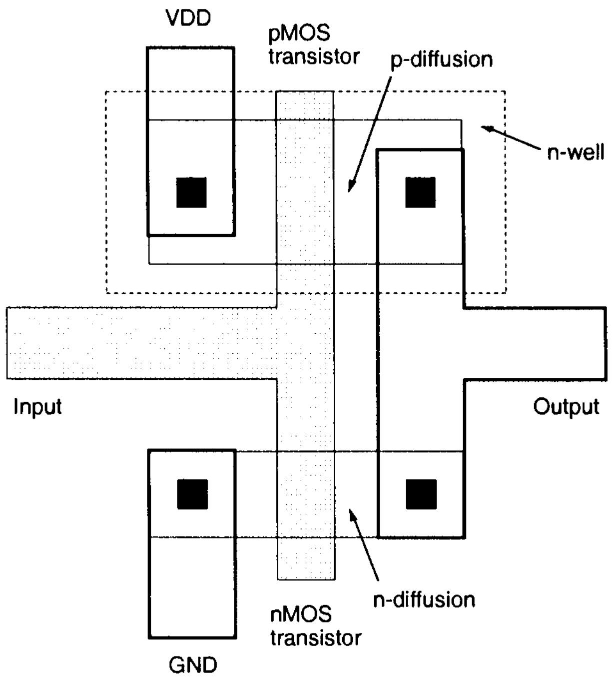


VTC of a CMOS inverter, when operated with a supply voltage that is smaller than $(V_{Tn} + |V_{Tp}|)$.

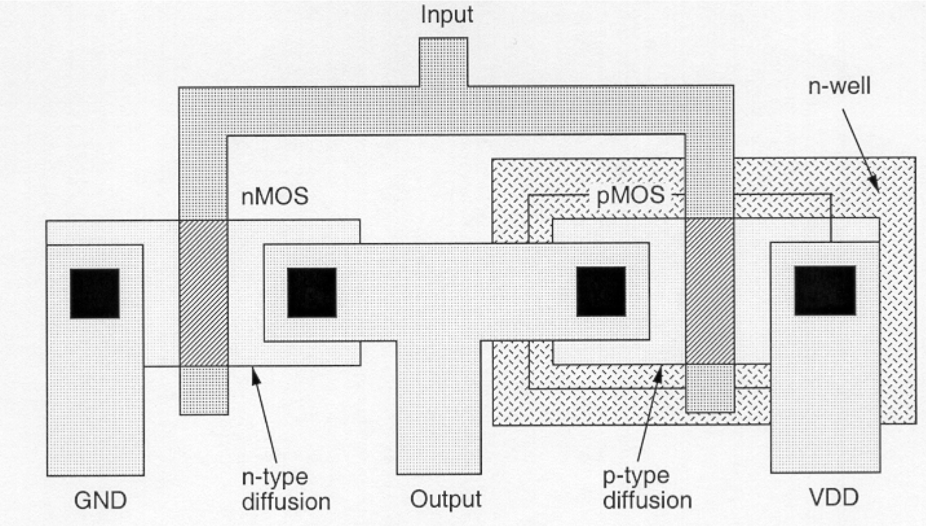
→ Hysteresis behavior !

CMOS Inverter Layout

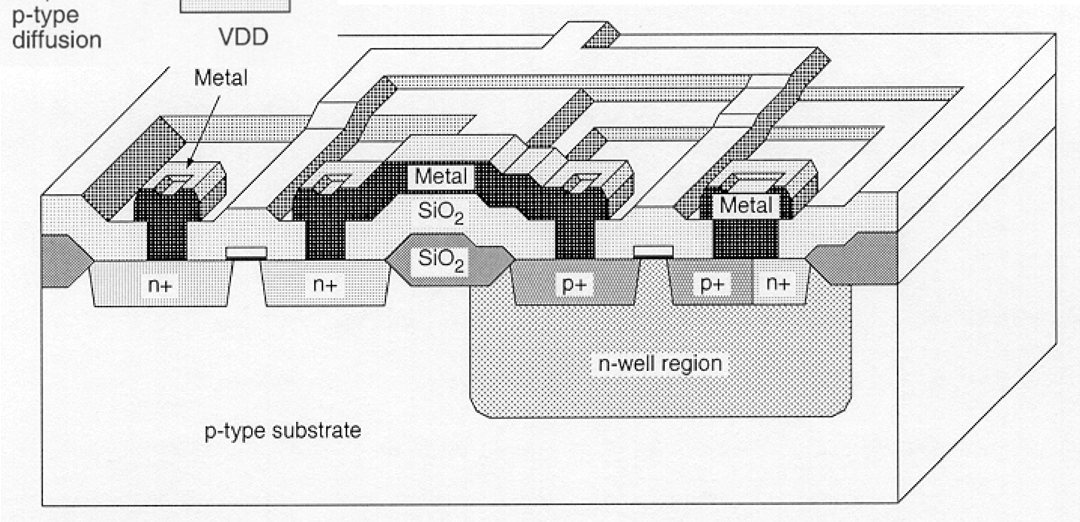




CMOS Inverter Layout



Mask layout
of the inverter



Simplified
cross-section