News: In Play in EDA:

In Play in EDA, Vol 1 No 8, April 30, 2004

FPGAs are from Venus, ASICs from Mars

By Peggy Aycinena

Think about this: FPGAs are sensitive souls in touch with their inner child. They're ready at a moment's notice to re-invent themselves in response to the whim or whimsy of their masters, or at least to be very forgiving if a mistake is made. Theirs is a kind of unconditional love; a little too much so, in some folks' eyes.

ASICs, on the other hand, are set in their ways from the moment they're conceived. They demand a lot of up-front tools and expenditure, lots of harrumphing NREs, and insist on being in charge from the beginning all the way through to the very end. They probably sit around and guzzle beer on the weekends, probably don't pick up after themselves, and certainly don't do laundry. Really, who needs them?

Let's turn away from Venus and Mars, and turn instead to that happy blue planet residing in-between. Who lives there?

Structured ASICs, of course; the guys who aren't too sensitive and aren't too harsh. In fact, maybe they're just right because suddenly they're the most popular guys in the solar system. Everybody wants to know them, or to know somebody who knows them. Who could ask for more?

Maybe you know somebody who knows somebody who knows a structured ASIC, but have you every actually met one? Is that happy blue planet really just a mythical place, a kind of Middle Earth, or is it solid ground where structured ASICs roam free and proud?

Two voices -- one from eASICS and one from Leopard Logic -- would like to answer those questions for you. Their comments constitute Part IV of my topical review and Run Up to DAC 2004. (To read Parts I and II, see **In Play in EDA, Vol 1 No 7, April 23, 2004**.)

But first, read Part III of my topical review where LogicVision CEO and President Jim Healy talks about morphing the company's message from Design for Test to Design for Yield. Along with structured ASICs, yield's going to be the other big celebrity at DAC this year.

DAC Run-up III - "DFT" now spelled "DFY"

Jim Healy is the brand new CEO at **LogicVision** and he's definitely a man on a mission. Everybody knows that LogicVision, founded in 1992 by Chairman Vinod Agarwal, has long been an industry leader in embedded test technology. The company provides tools for inserting test structures and is practically synonymous with the term "DFT."

But Healy's mission, as he sees it, is to widen the bin within which the LogicVision technology is pigeonholed. The bin he's looking to get the company into is bigger than DFT; it's labeled "DFY -- Design for Yield."

Healy's fully aware of the history of the company and believes that test structures are important. But he's also arguing that the significance of DFT structures resides in more than their nifty ability to examine a chip's innards after the die come off the line. He says the real impact of test structures can only be understood in light of their ability to increase yield, a very hot topic today. In light of the buzz swirling around yield at this moment, should Healy's new messaging strategy prove viable, he may very well end up showing the way for other players in the test industry to move out of the shadows and into the mainstream conversation in EDA.

Happily then, since my own mission right now is to try and touch on the major themes in EDA in advance of DAC 2004, Jim Healy's comments, which touch on both test and yield, let me basically kill two birds with one stone. Test is important. Yield is important. And they're both in play in this discussion.

Healy told me, "I've been in the industry for quite some time. In fact, I've been around test since 1967. Prior to coming to LogicVision last summer, I'd spent time at a number of companies including

Spirox in Taiwan and Credence."

"When Vinod asked me to join LogicVision in July, I was flattered and happy to join the organization. The LogicVision technology has been ahead of its time for quite a while, but when I got here and examined the company's history I saw that perhaps up until recently the market hasn't been ready for the LogicVision message."

"What I was seeing was that until everybody got to 130 nanometers and below, they weren't really accepting the fact that LogicVision's essentially invasive approach was the right way to go about achieving testability. Now that everybody's dealing with smaller line widths and smaller geometeries, however, LogicVision's historical stance is proving to be accurate and on the mark. In fact, both Mentor and Cadence are trying to affect a position in the market that mimics our own at this point."

"Clearly, we've got the technology and we've had it for a long time. What I'm seeing as my mission here at LogicVision is to provide a means of executing that technology for the customers who can really use it. I'm moving to put the proper internal processes in place and to get the message out to the industry that we've got excellent products, they're easy to use, and top-notch engineers want to have access to the technology. But at the same time, I'm enhancing that message in a significant way."

"I want people to know that LogicVision's tools are not just about embedded test. They're about responding to the number one problem facing the industry today, and that's Design for Yield. I'm positive this argument is a cogent one and I expect it to produce results in very short order."

"I believe that our historical positioning as a test company has run its course. I had VLSI Research do a study of 18 different customers, and all 18 said that intuitively they knew they could save money on test by using embedded structures, but not one of those companies had bothered to find out what kind of savings might be realized by investing in the technology. As LogicVision has historically been associated with classical design for test, this has not proved an adequate positioning for us from a business point of view."

"As it turns out, when we told those same 18 companies that we could improve their yield -- something that's very important in the digital consumer age -- they suddenly became very interested in our message. And it's a message that plays well with both engineers and upper management. We discovered that we needed to be addressing both of those audiences with a revised message, and quite literally that was the start of my mission to reposition LogicVision. So we're moving from the 'test' bin, if you will, to the 'yield' bin."

"We're aware that most guys today who position themselves in the 'yield' bin are in the pre-silicon end of the business. They're providing tools to pre-empt post production problems with strategies implemented in the early stages of design. What we're saying, however, is that embedding the appropriate type and quantity of test structures into the chip itself, will allow people to do quick and timely post-production evaluations. The resulting information can be fed back upstream to improve the thinking on the design or, just as importantly, to discern which products coming off the line are viable and should move on into packaging."

"This second diagnostic ability is what distinguishes us from the other guys in the 'yield' bin. We can provide the information needed to head off the costs associated with the packaging of essentially damaged goods. Chips fail; that's a reality in manufacturing, particularly at 130 nanometers and below. But determining which chips are flawed in a quick and inexpensive manner should also be a reality in manufacturing."

"Not surprisingly, my message is playing very well. Although, not all of the ATE [automatic test equipment] vendors are choosing to understand because our message also says that if you use our technology, you can start to move away from the need for high-end ATE equipment. The real beneficiaries of our technology are the end users and we know they're starting to understand, but it's the designers who will ultimately benefit the most. They'll be able to predict with good accuracy that the results of their efforts will see the light of day with less cost and frustration at the end of the pipeline"

"Yield's a very big topic right now and the end-game for many people

these days. As the industry moved from 0.18 technology to 0.13 technology, expectations were that yields would remain unchanged. But those expectations proved false. At 130 nanometers, the yields were terrible. In fact, I'm hearing that they're actually better at 90 nanometers than they've been at 130. Meanwhile, the cost of designing and producing chips has gone way up. People today are even less able to absorb losses due to yield failures than they were in the past."

"It's not surprising then that so many people are jumping into the yield business. In fact, there are so many companies involved today, we're trying to set up a consortium of the companies who are in the 'yield' bin - everybody who wants to play in that market. There's a lot of interest out there among those players and we think the time for a coordinated effort is now."

"Of course, all of this also plays into the current interest in SIPs, system-in-packages, which are just multi-chip modules from the past renamed. Today you've got two choices - build a monolithic chip, an SoC, with all your functionality on a single chip, or build a system of multiple chips in a package. SIPs today tend to be a lot less costly to develop and manufacture, however, and you can do them fairly fast."

"And although SoCs give you better performance, the longer lead time for development is a big problem for people. The lower yield on these complex devices is also a problem. If you can meet your product specs with a slightly larger form factor solution, and can deal with a product that's slightly less power efficient than an SoC, then an SIP is probably the way to go. Our tools are playing well in the SIP market, especially since we can verify known-good-die (KGD) through non-contact, at-speed embedded test. Consequently, we're expecting growth in the SIP market as well."

"The last couple of years have not been kind to our stock valuation. However, I believe our new message will turn things around and we expect to be cash flow positive once again by the fourth quarter [of this year]. Although stock prices are not always that important, they do have a psychological impact on how people view a company. We're fully aware of that and are convinced that we're on the right

tack to address that."

"Additionally, we intend to move forward to acquire other companies in our market niche to add to our technology portfolio. We would rather do that to jump start our forward progress, rather than only bootstrap advancements with in-house R&D."

"LogicVsion was and is focused on test. The benefits are still there: namely, lower cost and more accurate measurements of on-chip performance. But I feel that now we've identified and clarified for the industry our true value proposition. All the time that we've been focused on test we've actually been all about yield. And since there's clearly a yield bandwagon out there today, we think it's time to climb on board. We have the data to prove we can provide higher quality yield. The technology hasn't changed. We're just using different words to describe it."

DAC Run-up IV: Structured ASICs come down to Earth

Structured ASICs

Zvi Or-Bach is the Founder, President, CEO and Chairman of **eASIC**. It was very interesting to speak with Zvi on Wednesday, April 28th, about structured ASICs. According to many, Zvi is viewed as the "father" of structured ASICs. Not only does he fully endorse the concept, he's very specific about what the term means. He told me, "The best definition of a structured ASIC is on the **Structured ASIC Association (SAA)** website."

He read from the website: "A structured ASIC is an integrated circuit architecture and methodology that delivers reduced entry cost and faster time to silicon using a predefined arrangement of late-stage mask-customizable logic and pre-diffused macros and IP."

Zvi said that's the most accurate technical definition in use today and reflects the reality of a device where at least one metal layer is generic; the remaining metal layers -- however many that may be -- are customized. Zvi was adamant that a structured ASIC is not a gate array, because the metal layers in a gate array are custom all the way to the top.

But Zvi also acknowledged that there's a more "popular" definition for the term that's floating around. That definition is simple: A structured ASIC is something, which is neither an FPGA, nor a standard cell. Based on this definition, he told me, "There are lots of people jumping onto the 'structured ASIC' bandwagon, and all want to use this increasingly popular term. But many of their activities and solutions are not at all close to the accurate definition, but those people claim they're involved in the technology nonetheless."

"In either case, the real move towards structured ASICs began when people realized that mask costs were quickly growing beyond the reach of most designers. In DAC 2001, there was a panel called: 'When (will) FPGAs kill ASICs?' The FPGA panelists including Xilinx and Altera, were saying that FPGAs would soon overtake and replace ASICs. At the same time, LSI Logic was saying that ASICs would be alive forever. I was also a panelist and suggested that it doesn't have to be one or the other. In fact a new approach, now called structured ASIC, could fill the growing gap between FPGAs and traditional ASICs, and become a powerful alternative. I said that as the industry moves to 90 nanometers and below, this solution would become a preferred choice for over 90 percent of the design community."

"At a technical level, the mask problems began in earnest at 0.65 micron. Below that, the mask costs have increased by 2x per process generation, for two reasons. First, each generation has more metal layers, which increases the number of masks required in manufacturing. Second, the individual masks themselves have become more expensive because of the complex lithography issues. So people need more masks and each mask costs more. It's created a crisis in the ASIC world."

"FPGAs, however, have never offered a good solution in terms of cost, performance, or power. Not surprisingly, there has been a collective move to structured ASICs. With this technology, a significant portion of the masks can be generic -- at least the first 3 metal layers these days; customization of the masks starts after metal layer 3. It's beyond that layer that we define as 'late-stage masks,' per the SAA definition, for the manufacturing process. It's obvious that the more 'structured' the ASIC, the less customer-

specific masks involved in the manufacturing. Reducing the number of customized masks doesn't affect the customers' ability to achieve their full required functionality and subsequent product differentiation."

"The structured ASIC solution is quite clearly a move away from the original, primitive building blocks involved in early design, which were simply layers of transistors in a gate array. Unfortunately, even then we were misusing terms."

"The term 'ASIC,' for example, implies that it's specific to an application. But an 'application-specific' device is actually an ASSP. Andy Rappaport used to say that an ASIC is, in fact, a 'user-specific' IC. I agree with him, but also admit we've had a long history in the industry of misusing our terminology. For our discussion here, a structured ASIC is a much more complex device than a gate array; that's why we came up with a new term for that technology."

"So eASIC offers structured ASICs, but the very unique thing about our structured ASIC is that we offer it with no NRE, like an FPGA. No other ASIC company does that. We're arguing that even beyond consideration of how many metal layers are customized -- 1,2, 3, or more -- we can implement any design by customizing just a single via layer. Furthermore, we customize the logic by initializing Look-Up-Tables (LUTs), similar to an FPGA, which gives our customers' products the flexibility to debug, post silicon.

"I founded Chip Express in 1989. In 1996, we were the first company to offer what today is called a structured ASIC. This was the CX6000, a 0.65-micron MUX-based architecture that employed at least one generic metal layer. Then when I started eASIC in 1999, we developed a new technology, which blends the very best of FPGA and ASIC architectures. Our solution today takes FPGA concepts for defining the logic without masks, and only uses a single via-mask to customize the interconnect in an 'ASIC' manner."

An alternative to structured ASICs

Stefan Tamme is Vice President of Sales and Marketing at **Leopard Logic**. If you're looking for the technical middle ground between a

powerful ASIC and a flexible FPGA, Tamme's the guy you want to talk to. He's offering the best of both possible worlds, or so he says.

During a phone conversation on April 27th, Tamme told me that Leopard Logic's Gladiator CLD is the first commercially available device that combines ASIC and FPGA technology on the same chip. Tamme says the resulting product offers significant improvements in performance, power, and price over an FPGA; and significant improvements in NRE over a traditional ASIC, especially for those mid-market customers whose volume demands reside somewhere between 1000 and 100,000 units.

The "elevator" pitch on Gladiator CLD says the chip has two parts -- the mask programmable (MP) portion and the field programmable (FP) portion -- and the two portions can be handled with equivalent ease by knowledgeable designers, be they ASICguys or FPGA guys. Per Tamme, those designers can append the Leopard Logic back-end tools to their existing toolset and start producing designs quicker than you can say, "Best of both possible worlds."

Sounds pretty good and, if nothing else, the technology might help abort the awkward arguments at cocktail parties and panel discussions nowadays between the ASIC bigots and the FPGA bigots. Tamme says Leopard Logic is offering a way to establish a compromise between the two. In effect, he's saying that both sides are right and the real solution is a mix of the technologies.

Meanwhile, not surprisingly, Tamme is less enthused about the 'other' technology; the structured ASIC. He says, "Customers have been telling us for a couple of years now that they're looking for an alternative to the overall investment risk and time to market that traditional ASICs are associated with, but structured ASICs don't solve this problem."

"The FPGA guys want to make everyone believe that they can deliver the alternative. They say an FPGA can be everything to everyone, and that ASICs are going to go away. FPGA vendors have done a great job confusing the market; we meet people who believe they can buy a multi-million-gate FPGA with 500MHz performance for just $20. But if you really look at those products, the features quoted are

not found in one and the same FPGA, but rather represent features of two different devices. High-end FPGAs are not costing just tens of dollars, they're actually costing hundreds or thousands of dollars per unit."

"Meanwhile, the term 'structured ASIC' showed up on the horizon just before DAC last year and people looking for an alternative started listening to the vendors selling that technology. We think a structured ASIC is really just a down-graded ASIC, however, and neither a new nor particularly attractive solution."

"In fact, the structured ASIC design flow looks just like a gate-array design flow, where the netlist is shot over the fence to an ASIC vendor for timing closure, back-end design, etc. There's almost as much risk and delay there as with a traditional ASIC, but you won't see the risk until you see the timing problems at the other end."

"The structured ASIC guys talk about how much it's like an FPGA, but what they're offering is just as hard-wired as a gate array. The technology is not new, even if the name is. It's mostly based on 10 or 15-year-old gate array technology, with some bells and whistles attached and a new name. It's still a multi metal-layer process, plus via layers."

"You still have to use a traditional ASIC router to make the interconnects, plus you have to deal with all of the crosstalk problems, and so forth, at 130 and 90 nanometers. The only reason that structured ASICs are a fad today is because nobody wants to admit that they're actually in the gate-array market. It's that simple."

"We don't view our Gladiator CLD as a structured ASIC, although it does address similar market needs. It's more like an upgraded FPGA; an FPGA++, if you will. Clearly, it's structured, but if you drill down into the technology, we're really coming at our solution from an FPGA perspective. Our secret sauce is in the interconnect because the interconnect drives the density, performance and power consumption on an FPGA."

"At the same time, our architecture is fundamentally different from

legacy FPGAs, because it's very scalable -- even down to 65 nanometers -- since it doesn't include any pass gates. Hundreds of thousands of designers who are seasoned FPGA designers understand our architecture in minutes. If they're ASIC designers, it only takes a half a day of training for them to catch on and be up and running."

"We've got two distinct fabrics on the Gladiator CLD. The performance and power advantages are in the MP fabric, and the programmability advantages reside in the FP fabric. But we only use one via layer fabric to configure the device. Our logic cells are configured so that it's easy for a designer to shift blocks around, even at the netlist level. And you use the same design flow and gate libraries between the two fabrics, so the technology's easy to use for any FPGA designer on the planet. What we're offering is a true FPGA fabric with the performance and power advantages of an ASIC, but with orders of magnitude of improvement over anything like a structured ASIC."

EDA Players: programs, people, partnerings, and a little bit of pain

DAC 2004 organizers announced that on-line early registration will end on Monday, May 17th, but there's an ACM/IEEE discount in affect until May 10th. You can register in person at the conference - it's running June 7th to 11th in San Diego - but it will cost more. So best to do it now.

Actel announced the appointment of **Dan McCranie** to its Board of Directors. Currently, McCranie currently serves as Chairman of the Board for ON Semiconductor, Xicor, and Virage Logic. Previously, McCranie was Vice President of Sales and Marketing at Cypress Semiconductor and Chairman, CEO and President of SEEQ Technology. He has also held positions at Harris Corp., AMD, American Microsystems, and Philips. McCranie has a BSEE from Virginia Polytechnic University.

Tensilica announced that **Grant Martin** has joined the company as Chief Scientist. He will be responsible for leading Tensilica's long-term SoC methodology roadmap. Most recently, Martin was a fellow

in the office of the CTO of Cadence Design Systems at the Cadence Berkeley Labs. Previously, he held other positions at Cadence and was the company's chief representative on several EDA and IP design standards initiatives. Prior to Cadence, Martin was at Bell-Northern Research/Northern Telecom and Burroughs Machines Ltd. He is widely published and has edited or co-edited several important technical texts. Martin has a B.S. and M.S. in mathematics from the University of Waterloo in Canada.

Altium announced it has appointed **Embedded Systems Solutions** as the company's sole reseller in India, replacing Altium's network of six separate resellers. **Kayvan Oboudiyat**, CEO at Altium, is quoted: "India is shaping up to become a world powerhouse for the design and development of a wide range of high-tech products. To enable this rapid growth and keep up with demand, electronics design engineers in India need access to powerful and professional design tools at affordable prices that enable them to take advantage of the latest design technologies."

Aptix filed for Chapter 11 protection this week. That's never great news for a company, but it's particularly painful in this case because their CEO just was arrested a few weeks ago. Not surprisingly, everybody's abuzz about it all and I was advised to call **Jeff Dorsch** to get his take on the story. Dorsch, the former Editor in Chief of Electronic News, is now tracking EDA companies for the on-line business information provider, **Hoovers**.

Dorsch said, "This is a pretty spectacular case. I can't remember the last time that the CEO of an EDA company was arrested by the FBI, and it's pretty clear that Moshen's arrest helped precipitate the bankruptcy. I know that Aptix has been putting out a spin saying that Moshen's legal woes are not affecting them -- and I'm not saying that the arrest caused the bankruptcy directly -- but his problems are definitely affecting things at the company. It's been a tremendous burden for Aptix to deal with."

"Do I have sympathy for the company? Yes, because few people are going to extend them credit or anything else while they're in Chapter 11. But if I were a customer, I wouldn't necessarily flee. I'd sit down with my Aptix rep and see how their situation is affecting my

relationship as a customer. And I realize the good news that this is Chapter 11, and not Chapter 7, which means Aptix is trying very hard to get out from under their troubles."

The Play Book: tools & technology

Arithmatica announced its new **CellMath** product line for standard cell and custom IC design flows. The company says this new IP will help companies improve silicon efficiency without changing current design practices, and that by applying it to math-critical blocks in graphics chips the products can reduce overall chip area by upwards of 10 percent. CellMath is appropriate for math-intensive 3D graphics acceleration and high-performance processors that need on generation-to-generation improvements in performance, power and area

Dave Burow, CEO of Arithmatica, is quoted: "The explosive growth in consumer electronic products that require 3D graphics, high-quality audio and video, and high-bandwidth data transmission is driving the demand for powerful, easily implemented, cost-effective silicon math. We are pleased that technology leaders like NVIDIA, Xilinx, Layer N and others have successfully deployed our technology to improve the speed, area and power consumption of their math-intensive chips for their next-generation products."

Giga Scale Integration Corp. (Giga Scale IC) announced the **InCyte** design specification product family for optimizing between design goals including die size, power, leakage, speed, yield and cost. The company says the InCyte products (**InCyte-Specify** and **InCyte-Create**) are for design teams who want to optimize logic and analog IP, embedded memory and repair, I/Os, power leakage and switching activity at the start of a project; managers and architects should use the tools to compare and visualize various tradeoffs in library characteristics, semiconductor process nodes, memory configurations and IP. The InCyte products include a specification cockpit, estimation engine, floorplan generator, performance calculator and compare display, and are bundled with a portfolio of libraries and various hard and soft IP macros.

InCyte-Specify displays tradeoffs between conflicting requirements of

die size, memory yield, total power, leakage and cost. Users can find specific architectural problems while determining if their IP and library choices will meet design goals. InCyte-Create allows users to add details to the design model and blocks, and vary assumptions without backend design. Teams can evaluate tradeoffs in switching activity, memory performance, yield and IP alternatives. InCyte-Create is meant for design teams who have already selected a foundry or ASIC vendor; it comes with the ability to "seed" initial chip estimation into commercial floorplanners through LEF/DEF or custom interfaces.

Meanwhile, **VCX Software** announced an agreement with Giga Scale IC to link VCX's IP access and management technology into Giga Scale IC's new InCyte planning suite. The two organization say the integration of their capabilities will facilitate faster and easier interaction between users and suppliers of semiconductor IP.

Hier Design announced that the company has added NVIDIA Corp. as a customer.

Optimal announced the release of the O-Wave product series for 3D, full-wave signal integrity simulation, analysis and verification for high-speed IC, packaging and PCB. The company says the O-Wave algorithms accelerate cycle times for high-speed electromagnetic simulation, such as S-parameter extraction of RF IC designs, by upwards of 10x over the speed of other commercially available products with just one third the memory capacity requirements. According to the company, "The full-wave parasitic extraction capabilities of the O-Wave series work best on high-speed, high-complexity designs, where on-chip and I/O speeds exceed 2Ghz. Quasi-static signal integrity tools do not provide enough accuracy for high-speed designs and other full-wave tools cannot efficiently handle complex structures due to speed and computer capacity limitations."

Synopsys announced that Toshiba has taped out several 90-nanometer SoC designs targeted at audiovisual and office equipment products using Synopsys' **Galaxy Design Platform**. The companies report the designs were created using Design Compiler, DesignWare Library, Power Compiler, Physical Compiler, Astro, PrimeTime, Star-

RCXT, and DFT Compiler.

Magma Design Automation announced an expanded licensing agreement with NEC Electronics whereby NEC design teams and centers will deploy Magma's tools including **Blast Create**, **Blast Plan**, **Blast Fusion APX**, **Blast Rail**, and **Blast Noise**. NEC says it has implemented numerous designs using the Magma software.

Magma also announced the **Quartz Formal** verification tool, which the company says is based on Boolean equivalence technology licensed from **IBM**. Magma CEO **Rajeev Madhavan** is quoted: "This logic equivalence checking technology is truly battle tested. It is based on technology that has been proven on some of the most demanding custom and standard IC designs IBM has produced. Quartz Formal is a complete equivalence checking environment that encompasses the design implementation spectrum from RTL to gates and transistors. With this transaction we will be providing our customers with formal verification technology that supports RTL-to-gate equivalence checking, gate-to-gate equivalence checking and unique transistor-to-gate equivalence checking."

Meanwhile, **Magma** and **Virage Logic** announced they have collaborated to produce a design flow for both structured ASIC and standard cell libraries. Magma's Blast Fusion support for Virage Logic's Area, Speed and Power (ASAP) Logic Metal Programmable Libraries has been validated by both companies and will be added to existing support for the ASAP Logic Standard Cell Libraries. In addition, customers will be able to use Magma's standard ASIC design flow and Virage Logic's libraries that include all the necessary requirements and constraints for their structured ASIC designs.

Brani Buric, Senior Director of Product Marketing at **Virage Logic**, is quoted: "Working closely with Magma to support our ASAP Logic Metal Programmable Libraries provides our mutual customers with the added benefit of cutting costs and reducing turnaround time with mask generation in their structured-ASIC design flow. Magma users now have the flexibility of mixing and matching our metal programmable and standard cell libraries on the same design to achieve maximum savings in overall chip costs."

Mentor Graphics and **X-FAB Semiconductor Foundries** announced the availability of the first three in a series of technology design kits (TDKs) supporting X-FAB's CMOS process technologies. The three kits, the **XC06**, **XC035** and **XC035 LV**, have been validated and are now available with the Mentor Graphics analog/mixed-signal (AMS) IC design flow.

Novas Software announced that **Ricoh** is expanding its licensing of Novas debug tools over the next three years. Ricoh's Electronic Devices Co. says the new contract will double the number of Novas licenses as Ricoh integrates the tools into the engineering environments of its overseas Imaging System LSI Development Centers.

TriCN announced availability of its **Base I/O** library in the 130-nanometer process at **Chartered Semiconductor**. TriCN's Base I/O library is a set of cells containing all elements necessary for pad ring assembly.

The Halftime Program

FGPAs may be from Venus, but the guys who design them are definitely warriors. Ask Clive "Max" Maxfield; he's just published "The Design Warrior's Guide to FPGAs" and for my money it's your very best bet if you've got a lot of "willing," but very little "way" to prepare for the technical issues facing you at DAC. Max's book is delightful, light-hearted, wonderful to look at, and easy to read -- all 500 pages! It's also chock-a-full of discussion and discourse on so many of the themes that pervade DAC, EDA, and design.

Not only does the book discuss the fundamentals of the physics behind an FPGA, what distinguishes an FPGA from an ASIC, and the contrasting design styles between the two categories of devices, it also touches on embedded processors, DSPs, partitioning for hierarchical design, silicon virtual prototyping, IP, language wars, signal integrity, and deep-submicron effects.

Look, you've only got a month til DAC. Surely you're too busy to sit down and plow through 10 dry, pedantic textbooks before you arrive in San Diego. So, if you're really committed to sounding

knowledgeable at DAC, and even more importantly to understanding what everybody else is talking about once you're there, I suggest that you get Max's book. You can order a copy from Barnes & Noble using the link below. Simply select Title, enter "Design Warrior's Guide" and then click on Search using the form below.

But don't take my word for it. The back of the book carries side-by-side endorsements from Richard Goering and Gary Smith. These guys are definitely warriors, and if they don't know of what they speak, who does?

With apologies to Don Maclean -- and anybody named Pi -- I want to thank to Gary Smith for the following: www.vvc.edu/ph/TonerS/mathpi.html. Please note, the opinions expressed herein do not necessarily reflect those of the management or staff.

Peggy Aycinena is a Contributing Editor at SOCcentral and can be reached at peggy@soccentral.com