IP Directory

- Report contains 160 components
- Report is restricted to the following model technologies: Implementation IP

IP Type	Component	Vendor	Description
Implementation	DW01_absval	Synopsys	Absolute Value
Implementation	DW01_add	Synopsys	Adder
Implementation	DW01_addsub	Synopsys	Adder-Subtractor
Implementation	DW01_ash	Synopsys	Arithmetic Shifter
Implementation	DW01_binenc	Synopsys	Binary Encoder
Implementation	DW01_bsh	Synopsys	Barrel Shifter
Implementation	DW01_cmp2	Synopsys	2-Function Comparator
Implementation	DW01_cmp6	Synopsys	6-Function Comparator
Implementation	DW01_csa	Synopsys	Carry Save Adder
Implementation	DW01_dec	Synopsys	Decrementer
Implementation	DW01_decode	Synopsys	Decoder
Implementation	DW01_inc	Synopsys	Incrementer
Implementation	DW01_incdec	Synopsys	Incrementer-Decrementer
Implementation	DW01_mux_any	Synopsys	Universal Multiplexer
Implementation	DW01_prienc	Synopsys	Priority Encoder
Implementation	DW01_satrnd	Synopsys	Arithmetic Saturation and Rounding Logic
Implementation	DW01_sub	Synopsys	Subtractor
Implementation	DW02_cos	Synopsys	Combinational Cosine
Implementation	DW02_mac	Synopsys	Multiplier-Accumulator
Implementation	DW02_mult	Synopsys	Multiplier
Implementation	DW02_mult_2_stage	Synopsys	Two-Stage Pipelined Multiplier
Implementation	DW02_mult_3_stage	Synopsys	Three-Stage Pipelined Multiplier
Implementation	DW02_mult_4_stage	Synopsys	Four-Stage Pipelined Multiplier
Implementation	DW02_mult_5_stage	Synopsys	Five-Stage Pipelined

			Multiplier
Implementation	DW02_mult_6_stage	Synopsys	Six-Stage Pipelined Multiplier
Implementation	DW02_multp	Synopsys	Partial Product Multiplier
Implementation	DW02_prod_sum	Synopsys	Generalized Sum of Products
Implementation	DW02_prod_sum1	Synopsys	Multiplier-Adder
Implementation	DW02_sin	Synopsys	Combinational Sine
Implementation	DW02_sincos	Synopsys	Combinational Sine - Cosine
Implementation	DW02_sum	Synopsys	Vector Adder
Implementation	DW02_tree	Synopsys	Wallace Tree Compressor
Implementation	DW03_bictr_dcnto	Synopsys	Up/Down Binary Counter with Dynamic Count-to Flag
Implementation	DW03_bictr_decode	Synopsys	Up/Down Binary Counter with Output Decode
Implementation	DW03_bictr_scnto	Synopsys	Up/Down Binary Counter with Static Count-to Flag
Implementation	DW03_lfsr_dcnto	Synopsys	LFSR Counter with Dynamic Count-to Flag
Implementation	DW03_lfsr_load	Synopsys	LFSR Counter with Loadable Input
Implementation	DW03_lfsr_scnto	Synopsys	LFSR Counter with Static Count-to Flag
Implementation	DW03_lfsr_updn	Synopsys	LFSR Up/Down Counter
Implementation	DW03_pipe_reg	Synopsys	Pipeline Register
Implementation	DW03_reg_s_pl	Synopsys	Register with Synchronous Enable Reset
Implementation	DW03_shftreg	Synopsys	Shift Register
Implementation	DW03_updn_ctr	Synopsys	Up/Down Counter
Implementation	DW04_par_gen	Synopsys	Parity Generator and Checker
Implementation	DW04_shad_reg	Synopsys	Shadow and Multibit Register
Implementation	DW04_sync	Synopsys	Variable Input Synchronizer
Implementation	DW8051	Synopsys	8-bit Micro Controller
Implementation	DW_16550	Synopsys	Universal Asynchronous Receiver/Transmitter

Implementation	DW_8b10b_dec	Synopsys	8b/10b Decoder
Implementation	DW_8b10b_enc	Synopsys	8b/10b Encoder
Implementation	DW_8b10b_unbal	Synopsys	8b/10b Coding Balance Predictor
Implementation	DW_add_fp	Synopsys	Floating Point Adder (Module Compiler Only)
Implementation	DW_addsub_dx	Synopsys	Duplex Adder-Subtractor with Saturation and Rounding
Implementation	DW_ahb	Synopsys	ARM AMBA 2.0 AHB Bus IP
Implementation	DW_ahb_icm	Synopsys	ARM AMBA 2.0 Multilayer Interconnection Matrix
Implementation	DW_amba_ictl	Synopsys	ARM AMBA 2.0 Interrupt Controller
Implementation	DW_apb	Synopsys	ARM AMBA 2.0 APB Bus IP and AHB/APB Bridge
Implementation	DW_apb_gpio	Synopsys	ARM AMBA 2.0 APB GPIO
Implementation	DW_apb_rap	Synopsys	ARM AMBA 2.0 APB Remap & Pause
Implementation	DW_apb_rtc	Synopsys	ARM AMBA 2.0 Real Time Clock
Implementation	DW_apb_ssi	Synopsys	ARM AMBA 2.0 Synchronous Serial Interface; Supporting Motorola SPI, TI SSP & National Microwire
Implementation	DW_apb_timers	Synopsys	ARM AMBA 2.0 APB Timer
Implementation	DW_apb_uart	Synopsys	ARM AMBA 2.0 APB UART
Implementation	DW_arbiter_2t	Synopsys	Two-Tier Arbiter with Dynamic/Fair-Among-Equal Scheme
Implementation	DW_arbiter_dp	Synopsys	Arbiter with Priority Scheme
Implementation	DW_arbiter_fcfs	Synopsys	Arbiter with First-Come-First-Served Priority Scheme
Implementation	DW_arbiter_sp	Synopsys	Arbiter with Static Priority Scheme
Implementation	DW_asymfifo_s1_df	Synopsys	Asymmetric I/O

			Synchronous (Single Clock) FIFO with Dynamic Flags
Implementation	DW_asymfifo_s1_sf	Synopsys	Asymmetric I/O Synchronous (Single Clock) FIFO with Static Flags
Implementation	DW_asymfifo_s2_sf	Synopsys	Asymmetric Synchronous (Dual Clock) FIFO with Static Flags
Implementation	DW_asymfifoctl_s1_df	Synopsys	Asymmetric I/O Synchronous (Single Clock) FIFO Controller with Dynamic Flags
Implementation	DW_asymfifoctl_s1_sf	Synopsys	Asymmetric I/O Synchronous (Single Clock) FIFO Controller with Static Flags
Implementation	DW_asymfifoctl_s2_sf	Synopsys	Asymmetric Synchronous (Dual Clock)FIFO Controller with Static Flags
Implementation	DW_bc_1	Synopsys	Boundary Scan Cell Type BC_1
Implementation	DW_bc_2	Synopsys	Boundary Scan Cell Type BC_2
Implementation	DW_bc_3	Synopsys	Boundary Scan Cell Type BC_3
Implementation	DW_bc_4	Synopsys	Boundary Scan Cell Type BC_4
Implementation	DW_bc_5	Synopsys	Boundary Scan Cell Type BC_5
Implementation	DW_bc_7	Synopsys	Boundary Scan Cell Type BC_7
Implementation	DW_bin2gray	Synopsys	Binary to Gray Converter
Implementation	DW_C166S	Synopsys	16-bit Microcontroller from Infineon
Implementation	DW_cmp_dx	Synopsys	Duplex Comparator
Implementation	DW_cmp_fp	Synopsys	Floating Point Comparator (Module Compiler Only)
Implementation	DW_cntr_gray	Synopsys	Gray Counter
Implementation	DW_crc_p	Synopsys	Universal Parallel (Combinational) CRC

			Generator/Checker
Implementation	DW_crc_s	Synopsys	Universal Synchronous (Clocked) CRC Generator/Checker
Implementation	DW_debugger	Synopsys	On-Chip ASCII Debugger
Implementation	DW_div	Synopsys	Combinational Divider/Remainder/Modulus
Implementation	DW_div_fp	Synopsys	Floating Point Divider (Module Compiler Only)
Implementation	DW_div_pipe	Synopsys	Stallable pipelined Divider
Implementation	DW_div_seq	Synopsys	Sequential Divider
Implementation	DW_dpll_sd	Synopsys	Digital Phase Locked Loop with static divisor
Implementation	DW_ecc	Synopsys	Error Checking and Correction
Implementation	DW_fifo_s1_df	Synopsys	Synchronous (Single Clock) FIFO with Dynamic Flags
Implementation	DW_fifo_s1_sf	Synopsys	Synchronous (Single Clock) FIFO with Static Flags
Implementation	DW_fifo_s2_sf	Synopsys	Synchronous (Dual Clock) FIFO with Static Flags
Implementation	DW_fifoctl_s1_df	Synopsys	Synchronous (Single Clock) FIFO Controller with Dynamic Flags
Implementation	DW_fifoctl_s1_sf	Synopsys	Synchronous (Single Clock) FIFO Controller with Static Flags
Implementation	DW_fifoctl_s2_sf	Synopsys	Synchronous (Dual Clock) FIFO Controller with Static Flags
Implementation	DW_flt2i_fp	Synopsys	Floating Point to Integer Converter (Module Compiler Only)
Implementation	DW_gray2bin	Synopsys	Gray to Binary Converter
Implementation	DW_i2flt_fp	Synopsys	Integer to Floating Point Converter (Module Compiler Only)
Implementation	DW_inc_gray	Synopsys	Gray Incrementer
Implementation	DW_llfifocntl_s1_df	Synopsys	Synchronous Linked-List

			FIFO Controller with Dynamic Flags
Implementation	DW_memctl	Synopsys	Memory Controller Core
Implementation	DW_minmax	Synopsys	Minimum/Maximum Value
Implementation	DW_MIPS4KE	Synopsys	MIPS32 4KE Processor Core
Implementation	DW_mult_dx	Synopsys	Duplex Multiplier
Implementation	DW_mult_fp	Synopsys	Floating Point Multiplier (Module Compiler Only)
Implementation	DW_mult_pipe	Synopsys	Stallable pipelined Multiplier
Implementation	DW_mult_seq	Synopsys	Sequential Multiplier
Implementation	DW_prod_sum_pipe	Synopsys	Stallable pipelined Generalized Sum of Products
Implementation	DW_ram_2r_w_a_dff	Synopsys	Asynchronous Three-Port RAM (Flip-Flop Based)
Implementation	DW_ram_2r_w_a_lat	Synopsys	Asynchronous Three-Port RAM (Latch-Based)
Implementation	DW_ram_2r_w_s_dff	Synopsys	Synchronous Write-Port, Asynchronous Dual Read-Port RAM (Flip-Flop Based)
Implementation	DW_ram_2r_w_s_lat	Synopsys	Synchronous Write-Port, Asynchronous Dual Read-Port RAM (Latch-Based)
Implementation	DW_ram_r_w_a_dff	Synopsys	Asynchronous Dual-Port RAM (Flip-Flop Based)
Implementation	DW_ram_r_w_a_lat	Synopsys	Asynchronous Dual-Port RAM (Latch-Based)
Implementation	DW_ram_r_w_s_dff	Synopsys	Synchronous Write-Port, Asynchronous Read-Port RAM (Flip-Flop Based)
Implementation	DW_ram_r_w_s_lat	Synopsys	Synchronous Write-Port, Asynchronous Read-Port RAM (Latch-Based)
Implementation	DW_ram_rw_a_dff	Synopsys	Asynchronous Single-Port RAM (Flip-Flop Based)
Implementation	DW_ram_rw_a_lat	Synopsys	Asynchronous Single-Port RAM (Latch-Based)

Implementation	DW_ram_rw_s_dff	Synopsys	Synchronous Single-Port, Read/Write RAM (Flip-Flop Based)
Implementation	DW_ram_rw_s_lat	Synopsys	Synchronous Single-Port, Read/Write RAM (Latch-Based)
Implementation	DW_rambist	Synopsys	Embedded Memory BIST Controller Core
Implementation	DW_shifter	Synopsys	Combined Arithmetic and Barrel Shifter
Implementation	DW_sqrt	Synopsys	Combinational Square Root
Implementation	DW_sqrt_pipe	Synopsys	Stallable pipelined Square Root
Implementation	DW_sqrt_seq	Synopsys	Sequential SquareRoot
Implementation	DW_square	Synopsys	Integer Square
Implementation	DW_squarep	Synopsys	Partial Product Integer Squarer
Implementation	DW_stack	Synopsys	Synchronous (Single Clock) Stack
Implementation	DW_stackctl	Synopsys	Synchronous (Single Clock) Stack Controller
Implementation	DW_tap	Synopsys	TAP Controller
Implementation	DW_tap_uc	Synopsys	TAP Controller with USERCODE support
Implementation	DW_TriCore1	Synopsys	TriCore1 32-Bit Processor Core from Infineon
Implementation	DW_usbd	Synopsys	SMSC USB 2.0 PHY
Implementation	dwcore_1394_avlink	Synopsys	IEEE 1394 AVLink
Implementation	dwcore_1394_cphy	Synopsys	IEEE 1394 Cable PHY
Implementation	dwcore_1394_device	Synopsys	IEEE 1394 Device Link Controller
Implementation	dwcore_1394_ohci	Synopsys	IEEE 1394 OHCI Link
Implementation	dwcore_blueiq	Synopsys	Bluetooth Baseband and Link Manager
Implementation	dwcore_blueiq_devkit	Synopsys	Bluetooth Development Kit
Implementation	dwcore_gmac	Synopsys	10/100-Mbps and 1-Gbps Operation
Implementation	dwcore_gmac_subsys	Synopsys	Gigabit Ethernet MAC (GMAC) Subsystem

Implementation	dwcore_jpeg2_codec	Synopsys	JPEG2000 CODEC
Implementation	dwcore_jpeg2_encod	Synopsys	JPEG2000 Encoder
Implementation	dwcore_jpeg_codec	Synopsys	JPEG, CODEC
Implementation	dwcore_jvxtreme	Synopsys	Java™ Acceleration
Implementation	dwcore_mac	Synopsys	10/100 Mbps Operation
Implementation	dwcore_mac_subsys	Synopsys	Ethernet MAC Subsystem
Implementation	dwcore_pci	Synopsys	32/64 bit 33/66 MHz PCI Core
Implementation	dwcore_pcix	Synopsys	32/64 bit 133 MHz PCIX Core
Implementation	dwcore_usb1_device	Synopsys	USB 1.1. Device Controller
Implementation	dwcore_usb1_host	Synopsys	USB 1.1 OHCI Host Controller
Implementation	dwcore_usb1_hub	Synopsys	USB 1.1. Hub Controller
Implementation	dwcore_usb2_device	Synopsys	USB 2.0 Device Controller
Implementation	dwcore_usb2_host	Synopsys	USB 2.0 Host Controller (UHOST2)
Implementation	dwcore_usb2_otg	Synopsys	USB 2.0 Full Speed On-The-Go Controller Subsystem
Implementation	dwcore_usb2_phy	Synopsys	USB 2.0 PHY