TEACHING CUSTOM AND AUTOMATED CELL DESIGN

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1. Introduction

Custom design and verification of leaf-cells for standard-height and bit-slice libraries can be used to provide students with experience in performing these physical level tasks manually. We describe a one-semester graduate course [1] in which students compare their own custom layouts with automated results in terms of area, delay and design time. The availability of valid automated solutions provides the students with targets that serve as feasible bounds on the layouts and also inspire competition between the student and the design automation software. Projects are combined into TinyChips and submitted for fabrication via MOSIS [2] for testing during the subsequent semester.

2. Design and Verification Flow

The Cadence Design Systems [3] custom integrated circuit design bundle was selected to support the laboratory assignments in this course because it provides students with an integrated flow for custom design and verification. As shown in part of Figure 1, the designer begins by entering a hierarchical schematic to specify the desired logic and the W/L of each transistor. The resulting net-list is then simulated using detailed transistor models (Spectre).

ProGenesis [4] is an automatic leaf-cell generator. As shown in Figure 1, ProGenesis accepts the same transistor-level net-list as Virtuoso (after a format conversion). The tool also reads a process rule file so that it is cognizant of the desired spacings and thus produces layout that is free of geometric design rule errors. It can also read in a constraint file so that the layout can be compliant with standard-height constraints for power and ground spacing as well as pin locations. The resulting layout is then verified in the same manner as a custom layout.

For bit-slice leaf-cells, a color plan must be followed so that power, ground and control signals will automatically form buses when the cells are tiled in a vertical dimension to form a data-path with the desired number of bits in a data-path. Signals enter each cell from the left and exit to the right.

3. Projects

Typical projects for this course include counters, shift-registers, flip-flops, multipliers and dividers. These digital circuits are suitable for both standard-height and bit-slice formats. The automated layouts using ProGenesis are performed first to serve as targets for the students when manually composing their standard-height leaf-cells. These targets provide hints to the students but also inspire competition between the student and the design automation software.

Table 1 below shows a comparison of various projects in terms of area in square microns and delay in nanoseconds. The last column in the table shows the percent difference between the automatic and manual layouts. This value was calculated by taking the product of area and delay for the automated layout minus the product of area and delay for the manual layout divided by the area-delay product for the manual case. The results show that the manual and automated layouts differ by 15 percent or less and that ProGenesis appears to be better for more complex circuits. Since the students are novices at both using ProGenesis and in producing manual layouts, these results should not be used to make definitive judgments about the quality of the tool. However, the availability of the automated solutions is a powerful aid to learning (and grading). The students readily observe that the automated layouts are *generated within minutes* (sometimes taking up to two hours on a Sun Enterprise 220) with almost no effort on the part of the student whereas manual layout of circuits like these generally requires *at least ten hours of tedious labor*.

4. Comparison of Bit-Slice and Standard-Height Designs

In addition to comparing their custom standard-height leaf-cells with those produced automatically using ProGenesis, it is also desirable for each student to compare his/her bit-slice data-path design to one produced automatically using standard-height placement and routing. Since we have yet to learn how to get ProGenesis to produce layouts conforming to the bit-slice constraints, each student is asked to tile his custom single bit-slice into an 8-bit data-path and measure the resulting area and delay using a standard load (fan-out of four inverters). He then uses his single-bit standard-height cell and Silicon Ensemble to produce an 8-bit macro consisting of several rows of standard cells. In some cases, the data-path layout has half the area-delay product of the standard-height macro layout. For example, one student's data-path had an area-delay product of 22 units (square microns * nanoseconds * 10 **5) while the corresponding standard-height macro was 53 units.

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REFERENCES

[1] *ECE 651*, University of Tennessee, http://vlsi1.engr.utk.edu/ece/bouldin_courses/

[2] *MOSIS*, http://www.mosis.org/

[3] *Cadence University Program,* Cadence Design Systems, http://www.cadence.com/company/university/

[4] *Prolific, Inc., http://www.prolificinc.com/*

[5] *Smartframe and Standard-Cell Library*, University of Tennessee, http://vlsi1.engr.utk.edu/ece/cadence.html

Circuit Number	Complexity (Trans.+Nets)	Manual Area	Auto Area	Manual Delay	Auto Delay	Percent Difference
1	20	461	518	239	244	15
2	27	899	1037	6244	6232	15
3	41	1037	1181	209	184	0
4	57	1267	1315	861	884	7
5	65	1660	1830	2598	2584	10
6	67	1728	1505	405	462	-1
7	77	2419	2087	780	811	-10
8	84	1901	1613	194	202	-12
9	85	1728	1723	536	521	-3
10	86	2354	2117	413	404	-12
11	104	2242	2247	1036	1003	-3

Table 1. Comparison of Manual and Automatic Designs

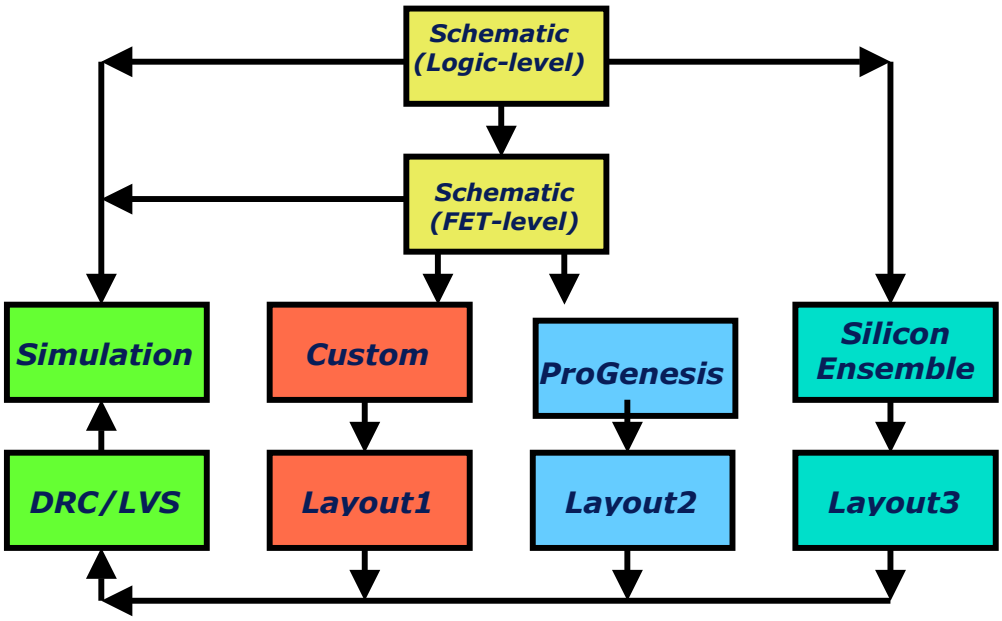

Fig. 1. Design Flow.

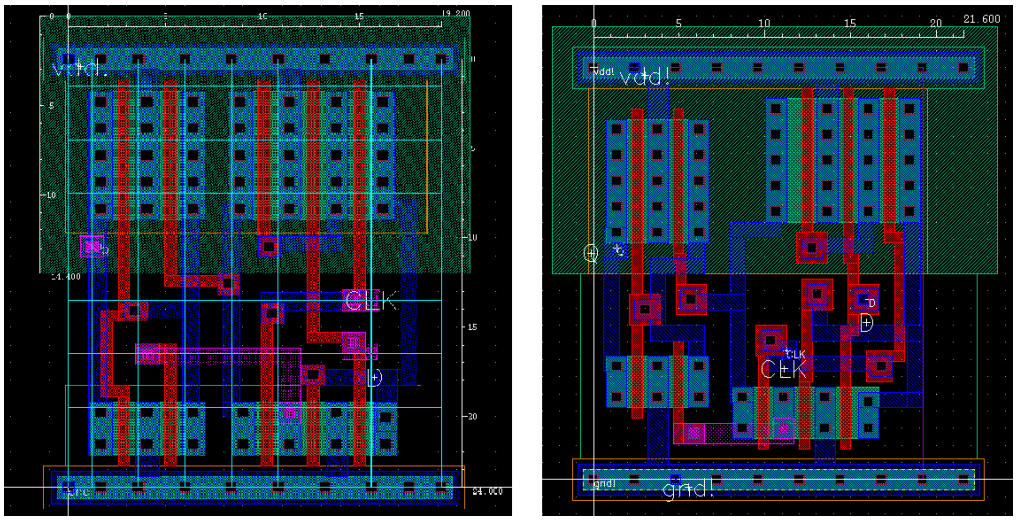

Fig. 2. Standard-height cell layouts: (a) Manual and (b) Automatic.