VI. Summary and Conclusions

MTL as a novel bipolar logic concept has been discussed and experimentally verified. It is based on inverters having decoupled multicollector outputs for the logical combinations. These inverters are powered by a direct injection of minority carriers into their common n-emitter plane. MTL is a self-isolated structure requiring no ohmic load resistors. This simple structure offers considerable advantages of which the most significant ones are

1) high noise immunity and good driving capabilities (TTL compatible);
2) fabrication substantially simplified (only four mask steps through metalization);
3) extremely high functional density (about 1000 gates on 130 × 130-mils^2 chip with present manufacturing tolerances, such as 0.3-mil metal lines, 0.15-mil spacing, and 0.2 × 0.2-mil contact holes);
4) excellent power-delay product (0.35 pJ above 100-ns delay, 0.7 pJ in the 15–20-ns range, and power speed externally alterable).

These results have been obtained on a very simple structure implemented by using readily available processing facilities. By taking advantage of modern technological accomplishments, improvements can be expected without increasing the processing complexity.

VII. Acknowledgment

The authors are indebted to D. Young[3] and his department for the test chip artwork and to H. Rupprecht[3] and his department for test chip fabrication. Special thanks are due to C. S. Chang[3] for valuable contributions.

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Integrated Injection Logic: A New Approach to LSI

KEES HART AND ARIE SLOB

Abstract—**Logic gates suitable for large-scale integration (LSI) should satisfy three important requirements. Processing has to be simple and under good control to obtain an acceptable yield of reliable IC's containing about 1000 gates. The basic gate must be as simple and compact as possible to avoid extreme chip dimensions. Finally, the power-delay time product must be so high that operation at a resonable speed does not cause excessive chip dissipation.**

Multicollector transistors fed by carrier injection proved to be a novel and attractive solution. A simplified (five masks) standard bipolar process is used resulting in a packing density of 400 gates/mm^2 with interconnection widths and spacings of 5 μm. The power-delay time product is 0.4 pJ per gate. An additional advantage is a very low supply voltage (less than 1 V). This, combined with the possibility of choosing the current level within several decades enables use in very low-power applications. With a normal seven-mask technology, analog circuitry has been combined with integrated injection logic (I^{2}L).

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The authors are with the Philips Research Laboratories, Eindhoven, the Netherlands.

Introduction

LOGIC gates suitable for large-scale integration (LSI) must satisfy three important requirements.

1) The processing has to be simple and under good control in order to obtain an acceptable yield of reliable IC's containing about 1000 gates.

2) The basic gate must be as simple and compact as possible to avoid extreme chip dimensions.

3) The power-delay time product must be such that operation at a reasonable speed does not cause excessive dissipation on the chip.

Multicollector transistors fed by carrier injection proved to be a novel and attractive solution that fulfills the previous three requirements [1]–[3]. Two ways of injection will be discussed, viz., injection by light and injection with a p-n diode. A number of realized LSI circuits will be mentioned.

Injection by Light

A junction diode, which is irradiated with light of a suitable wavelength, will act as a diode with a current source in parallel (see Fig. 1) tending to forward bias the junction. The effect is due to an increase in concentration of the minority carriers in the neighborhood of the junction, resulting from the hole–electron pairs created by light absorption.

The question is whether such a current source could be used in integrated circuits as distributed supply sources, occurring wherever they are needed.

In a transistor irradiated with light, two current sources occur, however, in the configuration of a conventional n-p-n planar transistor (Fig. 2) the current source across the normal collector–base junction (junction 2–3) is much stronger than that across the emitter–base junction (junction 1–2). There are four reasons.

1) Region 3 is much larger than region 1.

2) The lifetime of the minority carriers in region 3 is much longer than in region 1.

3) Region 1 is screened by the aluminum connections.

4) Carriers generated in region 2 will drift to region 3 owing to the built in electrical field and contribute to the photocurrent of junction 2–3. In practice it means that the photocurrent across junction 1–2 can be neglected.

When the transistor is used inversely, the result is a transistor with a forward-biasing current source between base and emitter (Fig. 3). With the base not connected externally, the collector can draw a current, which is the base current multiplied by the current gain. This collector current can be used to short circuit base–emitter photocurrents of other transistors of which the collector current is zero.

Logic circuits may now be built with the light-activated transistor: the transistor acting as an inverter, while the logic function is obtained from the way collectors are connected (wired AND). In this case, circuits are best taken together into standard arrangements in the manner shown by the dashed line in Fig. 4, i.e., bases and emitters each are connected into common regions whereas the collectors are laid out as multicollectors. Compare this with direct coupled transistor logic (DCTL) where collectors are combined and there are multiple base contacts and separate emitters. In both cases, the transistors act as inverters and the logical functions are obtained by wiring the collectors. However, since both the DCTL bases as well as the emitters must be provided with separate connections, the number of contact holes in a chip is much larger than in the corresponding circuit for light-activated logic.

Fig. 5 gives a cross section of a multicollector transistor. An n^+ substrate has been chosen together with n^+ isolations between the bases in order to improve the current gain and diminish parasitic lateral p-n-p action. Only four masks are required, since the homogeneous p diffusion is overdoped by the n^+ isolation to make separate bases. Fig. 6 is a microphotograph of a digital voltmeter chip in which the power supply is derived from absorbed light. Therefore, the aluminum pattern only contains logical wiring.

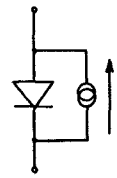

Fig. 1. Circuit diagram of a p-n junction irradiated with light consists of a diode in parallel with a current source.

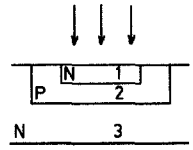

Fig. 2. Double diffused transistor irradiated with light. Current source across junction 2–3 is much stronger that that across junction 1–2, which can be neglected.

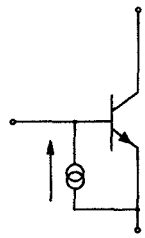

Fig. 3. Circuit diagram of an inversely used transistor irradiated with light. Current source tends to forward bias the emitter–base junction.

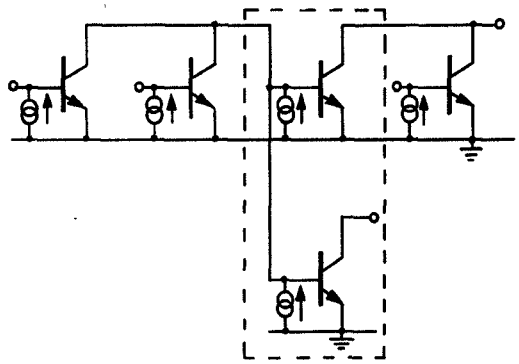

Fig. 4. Logic function is obtained by connecting collectors (wired AND). Between the dashed lines a multicollector transistor occurs, which is the standard arrangement.

p-n Injector

The function of the absorbed light was to generate holes (minority carriers) in the n layer. This function also can be accomplished by a forward-biased p-n junction, called the injector.

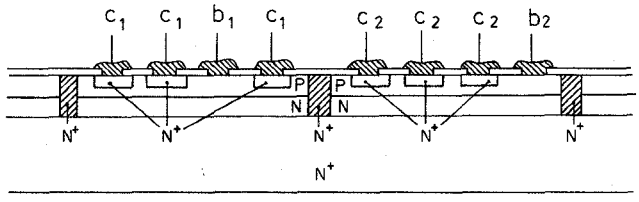

Fig. 5. Cross section of two multicollector transistors. p diffusion does not need a mask, thus, only four masks are needed.

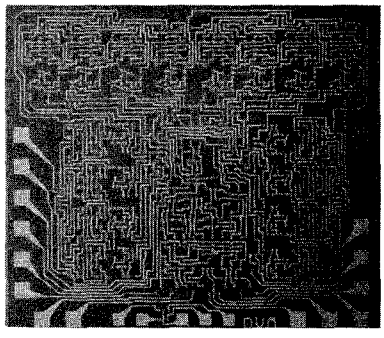

Fig. 6. Microphotograph of a digital voltmeter chip. Aluminum interconnection pattern is the logical wiring only as the power is derived from absorbed light. Chip size—2.2 × 2.4 mm².

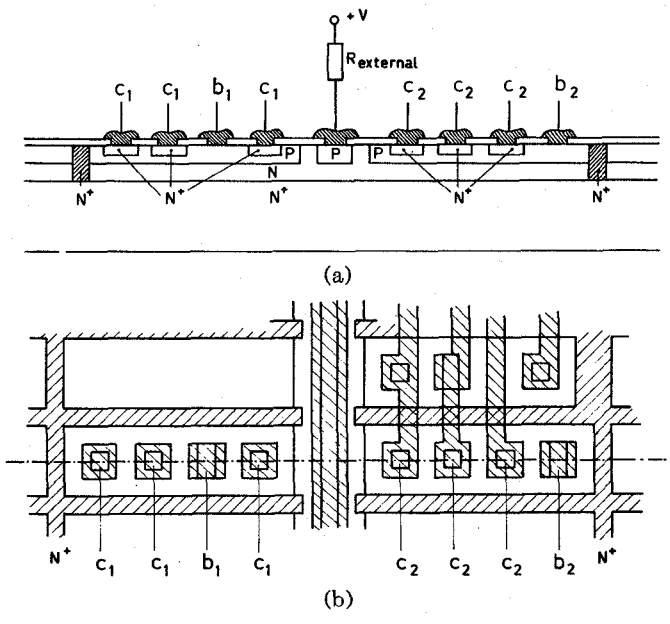

Fig. 7. (a) Cross section of multicollector transistors on both sides of the injector. Five masks are needed. (b) Layout.

Fig. 7(a) gives a cross section and Fig. 7(b) a layout of the multicollector transistors fed by a p-n injector. An additional mask for the p diffusion is necessary now.

Circuit Parameters and Technology

Each collector of a multicollector transistor must be able to short circuit one base current. This means that the current gain β per collector has to be ≥ 1, (if all base currents are assumed equal). The hole efficiency of the injector α determines the amount of base current.

To fulfill reliability and yield requirements, the choice has been made to use one of the available factory processes.

A first set of measurements showed that both the current gain β and the hole efficiency α improved with the application of an n^+ substrate and deep n^+ isolations.

To find the influence of the resistivity of the epitaxial layer and of the geometries on the current gain β and on the hole efficiency α, a second set of measurements have been carried out. The results given in Fig. 8 have been obtained under the following conditions.

1) Process Description: Epilayer thickness—5 μm with a variable resistivity; base diffusion depth—2.7 μm, resistivity $\rho_\square = 200\ \Omega/\square$.

2) Geometries: Collector area—20 × 20 μm², spaced on 10 μm; emitter area—width 40 μm, length dependent on number of collectors; aluminum—10-μm width and 10-μm spacings.

From these measurements the decision has been taken to limit the number of collectors per base area to four, which means a maximum fan-out of four. The maximum fan-in is not limited.

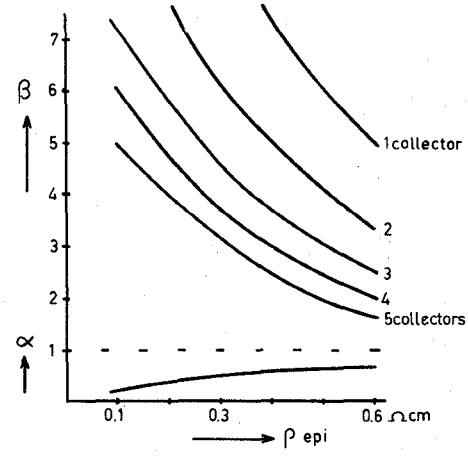

Fig. 8. Minimum current gain β and hole efficiency α as a function of epilayer resistivity and number of collectors.

Noise Margin

Since there are no resistors in the circuit, the absolute current levels are not fixed and the user can choose a certain current level for the injector, which distributes the current into equal portions over the transistors. Therefore, it is impossible to give absolute noise margins. The relative noise margins, however, can be calculated easily in the form of maximum noise currents, which can be translated into maximum noise voltages.

Fig. 9(a) shows a situation in which a noise current I_{S0} tends to switch transistor T_1 in ON. The critical point is reached if in the base of T_1 a current of Ic/β is flowing. It is easily derived that

$$\beta_0 I_0 = I_{S0} + I_1 - (I_c/\beta)$$

so

$$I_{S0} = \beta_0 I_0 - I_1 + (I_c/\beta).$$

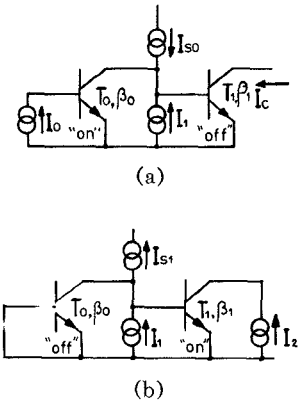

Fig. 9. Definition of noise current sources. (a) Low logical level. (b) High logical level.

The corresponding noise voltage V_{S0} is somewhat less than the forward base–emitter voltage V_j.

Fig. 9(b) shows a situation in which a noise current I_{S1} tends to switch transistors T_1 in OFF. Here the critical point is reached if in the base of transistor T_1 the base current becomes less than I_2/β. From the circuit diagram it is derived that

$$I_1 = (I_2/\beta) + I_{s1}$$

so

$$I_{S1} = I_1 - (I_2/\beta).$$

For T_1 the maximum (undisturbed) base current is I_1 and the minimum allowable base current is I_2/β, so the noise voltage will be $V_{S1} = (kT/q)\ln(\beta I_1/I_2)$.

Now two cases have to be distinguished, viz., the noise margin on the chip and the noise margin between the chips.

In the case of the noise margin on the chip, the noise production is very low and all the current sources are chosen equal for reasons of easy design. This results in

$$I_{S0} = I[\beta - 1 + (1/\beta)], \qquad V_{S0} \approx V_j.$$

and

$$I_{S1} = I[1 - (1/\beta)], \qquad V_{S1} = (kT/q)\ln\beta.$$

In the case of noise margin between the chips the noise production can be expected to be higher. To obtain correspondingly larger absolute noise margins, the first transistor on the chip and the last one on the previous chip are given a larger absolute current and a higher value of the current gain β. This can be achieved by choosing suitable geometries.

Propagation Delay Time Versus Power

The propagation delay time is determined by the amount of current supplied to the logic gates. Three current levels are to be distinguished, viz., low, medium, and high.

At low current levels the propagation delay time is determined by junction and parasitic capacitances. This propagation delay time τ will be proportional to the time t needed to charge or discharge the capacitances. As $Q = CV$ and $t = Q/I$, τ will be proportional to CV/I. The dissipation D will be $D = VI$, in which V is the voltage over a forward-biased junction. From this it follows that the power-delay time product $D\tau$ is proportional to CV^2, which is constant.

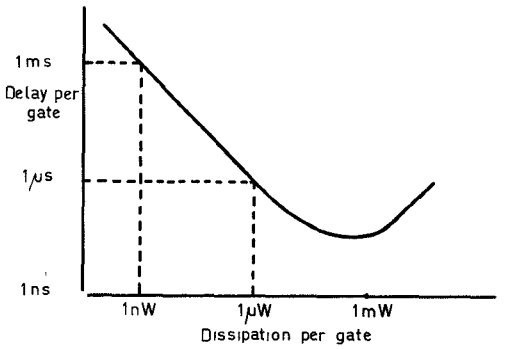

Fig. 10. Typical propagation delay time versus power. Diagram measured on a ring of five inverters.

At medium current levels the main influence on the propagation delay time comes from the active charge in the transistors. This charge is proportional to the current and, therefore, the propagation delay time is independent of the dissipation.

At high current levels there are two phenomena that cause a worse propagation delay, first, the series resistances of the bases prevent fast charging or discharging of the active charges, and, second, these active charges increase more than linearly with increasing currents.

In Fig. 10 a measured curve of the propagation delay time versus power is shown. The measured value of the power–delay time product is $D\tau = 1$ pJ for a dissipation below 1 μW/gate. This product has been measured in a ring of five inverters that will oscillate at a period of ten times the average stage delay and consume five times the gate dissipation. In this case the fan-in and fan-out are equal to one. A more realistic value of the $D\tau$ product was measured on a chip containing a 108-bit shift register in which case the average fan-in and fan-out were 2.5 per gate. Two versions of this shift register have been made, viz., one with 10- and one with 5-μm clearances. In the version with the 10-μm clearances a $D\tau$ product of 1.75 pJ has been measured whereas for the version with the 5-μm clearance 0.4 pJ has been obtained.

It is clear that both the $D\tau$ product and the minimum propagation delay time can be improved by the use of smaller dimensions and a more sophisticated technology.

Interface Circuits

In the five-mask technology described in the preceding paragraphs several interface circuits are possible (see Table I). Normally, the collectors of an integrated injection logic (I^2L) gate are fed by a current source, i.e., the current source between the base and the emitter of one of the other I^2L gates.

TABLE I
SURVEY OF THE DIFFERENT POSSIBILITIES OF INTERFACE CIRCUITS

Type of Interface	Maximum Logic Levels (V)	Maximum Output Current in ON State
Standard output [Fig. 11(a)]	0/+5	medium
Emitter follower [Fig. 11(b)]	0/−0.7	high
Lateral p-n-p followed by emitter follower [Fig. 11(c)]	0/−20	high
Lateral p-n-p followed by inverter [Fig. 11(d)]	0/+5	medium
Lateral p-n-p [Fig. 11(e)]	0/−40	low

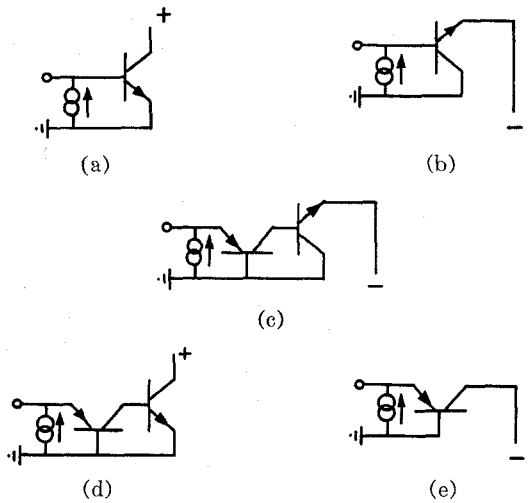

Fig. 11. Several types of interface circuits. Layouts of (a)–(d) are equal.

In a first type of interface, this collector might be connected via a resistor to a positive supply voltage [Fig. 11(a)]. However, if the resistor is connected to a negative supply voltage, the n^+ area will act as an emitter and the transistor will now behave as an emitter follower. In this case the much higher current gain of a noninverse transistor determines the output impedance [Fig. 11(b)].

By applying a p-n-p transistor between the injector and the output transistor [Fig. 11(c)], the difference in logic levels can be increased because the base of the n-p-n transistor is now driven by a current instead of a voltage. When a positive supply voltage is now used [Fig. 11(d)] this interface gets the same properties as the standard I^2L inverter of Fig. 11(a).

Finally in the last type of interface circuit the highest difference in logic levels can be obtained with a lateral p-n-p because of the high collector breakdown voltage [Fig. 11(e)].

APPLICATION TO ANALOG CIRCUITRY

The manufacturing process described is started from an n^+ substrate. When a p substrate is used with a n^+ buried layer for the common emitters together with the normal p isolations, linear or analog circuitry can be combined with the I^2L digital circuitry on the same chip.

TABLE II
LIST OF LSI CIRCUITS REALIZED WITH THE I^2L TECHNIQUE

Function	Number of Gates	Chip Dimensions (mm²)
Electronic organ tone generator	180	1.2 × 1.5
Liquid crystal display driver (Fig. 12)	200	2.2 × 2.4
Counter for digital voltmeter (Fig. 6)	325	2.2 × 2.4
108-bit shift register	820	2.96 × 2.85
1536-bit read only memory	about 1000	3 × 4
Control logic	980	4 × 4

With the latter three circuits a small calculator has been made, which works on a 1.5-V battery.

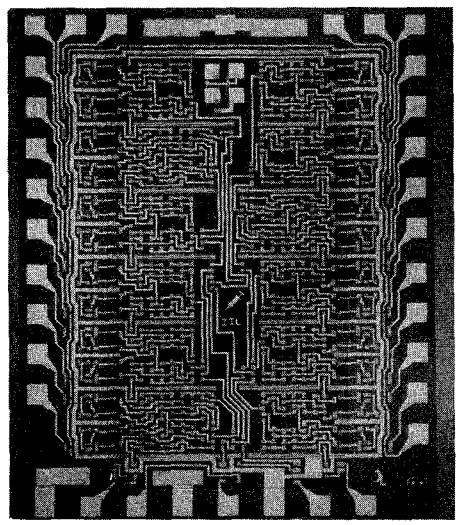

Fig. 12. Microphotograph of an ac liquid crystal driver chip. At the boundaries normally isolated transistors have been used. Middle part of the chip contains the I^2L circuits.

All types of interface circuits are possible then. In Fig. 12 a microphotograph of an ac liquid crystal driver is shown. At the boundaries of the chip, normally isolated transistors are used to deliver the ac voltage to the liquid crystal, whereas the middle of the chip contains the I^2L digital circuits.

RESULTS

To prove that I^2L is a realistic LSI approach, several circuits have been produced with complexities ranging from 180 to about 1000 gates as listed in Table II.

CONCLUSIONS

I^2L has shown that it can fulfill the following demands for LSI: 1) simple technology (five masks); 2) high packing density, 400 gates/mm² if 5-μm clearances are applied; 3) power-delay time product is 1.75 pJ in the system where 10-μm clearances are applied, which can be improved to 0.4 pJ if 5-μm clearances are applied. The average fan-in and fan-out in the system are equal to 2.5.

An extension to a seven-mask standard bipolar tech-

nology gives the freedom of using analog and digital circuitry on the same chip. The low power supply voltage of less than 1 V contributes to a high reliability.

ACKNOWLEDGMENT

The authors wish to thank A. Schmitz for many helpful discussions and for the fabrication of the slices.

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A New Complementary Bipolar Transistor Structure

STEPHEN C. SU AND JAMES D. MEINDL

Abstract—**A novel complementary monolithic bipolar transistor structure has been developed. By adding one extra diffusion to the standard monolithic bipolar transistor process, a complementary pair of high current gain and very low saturation resistance n-p-n and p-n-p transistors can be fabricated on the same chip. High sheet resistances are also present in this structure. Novel low-voltage (1.3 V) complementary digital circuits have been fabricated by this new process.**

I. INTRODUCTION

IT HAS BEEN well established that micropower operation is enhanced through the use of complementary transistor circuits [1]. In the past, monolithic integrated circuits have not been especially attractive for complementary circuit applications because of the difficulties associated with producing satisfactory complementary transistors and high value resistors in monolithic form. For example, use of the common lateral p-n-p transistor imposes severe limits on complementary circuit performance and previously described monolithic structures with vertical n-p-n and p-n-p transistors have suffered from excessive process complexity [2], [3]. This paper describes a simple new monolithic complementary transistor structure with vertical n-p-n and p-n-p transistors as well as high value resistors whose characteristics are essentially optimized for operation in the micropower range. In addition, several general purpose low-voltage complementary logic gates and flip-flops, which can serve as the basic building blocks for implementing digital functions using a 1.35-V supply, are described.

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The authors are with the Department of Electrical Engineering, Stanford University, Stanford, Calif. 94305.

II. DEVICE STRUCTURES AND FABRICATION

Fig. 1(a) illustrates the standard diffused epitaxial process for monolithic bipolar integrated circuits. Key drawbacks of this process for micropower operation are the inherently low frequency response and high saturation voltage of the lateral p-n-p transistor and the lack of high value resistors with low tolerance. Fig. 1(b) illustrates the steps that are necessary if the standard process is modified [3] in order to achieve vertical p-n-p transistors. Note that two extra diffusions are needed; the original epitaxial layer must be compensated three times to achieve a vertical p-n-p structure that does not have a buried p^+ layer. Fig. 1 (c) illustrates the Stanford complementary process. The diffusion steps are as follows: 1) an n^+ buried layer for the n-p-n collector; 2) a p^+ buried layer for the p-n-p- collector and p-isolation (followed by n epitaxial growth); 3) a p-diffusion for the n-p-n base, p-isolation, and p-n-p collector contact; 4) a p^+ emitter; and 5) an n^+ emitter.

Note that only one extra diffusion is needed; the p-n-p base is the original uncompensated epitaxial layer and both transistors have highly doped collector regions for low saturation resistances and minimum offset voltages. The dopants for the two buried layers are phosphorus and boron, respectively. Silane (low temperature) as well as silicon tectrachloride (high temperature) epitaxial growth has resulted in good devices. The low-temperature epitaxial deposition introduces negligible out diffusion (OD) of buried layers during the growth. However, the high-temperature deposition yields better uniformity of layer thickness. A typical set of fabrication data from this process is listed in Table I.

The out diffusion of the p^+ buried layer, which is an important parameter in determining the basewidth of the p-n-p transistor and device isolation, occurs mainly during the p base drive-in cycle (~1150°C). If a $SiCl_4$ epi-