

# Design Exploration Tutorial for HDL Designer Series

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# **Table of Contents**

Design Exploration Tutorial	5
Welcome to HDL Designer Series.	5
The Design Manager	5
Add the Fibonacci Design	6
Browse the Fibonacci Design	8
Create a Block Diagram View	10
Print the Diagram	13
Add Panels to the Block Diagram.	13
Object Linking and Embedding	14
Display the IBD View	15
Display the Symbol.	17
Create a State Diagram View	18
Relevel the State Diagram	20
Create a Flow Chart View	21
Visualizing your HDL Designs	23
Export the Design Hierarchy as HTML	27
View the Exported HTML Hierarchy	29
Export the Design Library as HTML	30
View the Exported HTML Library	30

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This tutorial introduces HDL Designer Series. It shows how to use it in design exploration and visualization.

Welcome to HDL Designer Series	<b>5</b> 5
Add the Fibonacci Design	6
Browse the Fibonacci Design	8
Create a Block Diagram View Print the Diagram	<b>10</b> 13
Add Panels to the Block Diagram.         Object Linking and Embedding         Display the IBD View	13 14 15
Display the Symbol.	17
Create a State Diagram View	<b>18</b> 20
Create a Flow Chart View	21
Visualizing your HDL Designs	23
Export the Design Hierarchy as HTML	<b>27</b> 29
Export the Design Library as HTML	<b>30</b> 30

# **Welcome to HDL Designer Series**

This tutorial shows how HDL Designer Series can be used to add a design described by VHDL or Verilog HDL text and visualize the design structure as a hierarchy of graphical design unit views. The graphical views can be printed or exported as HTML files for use in design documentation.

This tutorial can be performed by users of HDL Designer Series or by users of HDL Designer which incorporates all the features supported by HDL Designer Series.

## The Design Manager

The design manager is opened when the HDL Designer Series tool is invoked for the first time.

If the examples project is not active, it can be opened by choosing **Project** from the **Open** cascade of the **File** menu to display the Open Project dialog.

The procedures in this tutorial use the *SCRATCH\_LIB* library defined in the *examples* project although you can use any other empty writable library.

# Add the Fibonacci Design

- 1. In the Design Manager window select **Existing Design** from the **Add** cascade of the **File** menu to display the Add Existing Design wizard.
- 2. Specify the method to add your design by selecting **Copy Specified Files** from the left most section. Choose *VHDL Files* (if you are using VHDL) or *Verilog Files* (if you are using Verilog) from the Show Files of Type pulldown filter. In the Folders pane locate the Fibonacci sequencer design source code in the examples sub-directory of your installation. For example, if HDS is installed in the directory *D:\LatestBuild*, the path is:

🚜 Add Existing Design		
Please choose one of the following methods to add existing design	iles into your project:	
Point to Specified Files     Depy Specified Files     FileIst Format:	lelist ModelSim .ini file	~
Automatically creates new library directories and mappings and Click the check boxes in the browser below to specify the folder	opies the specified design files into these libraries. : or files vou wish to add.	
Please specify the required design files:		
Look in: D:\LatestBuild\examples\tutorial_ref\In	ort\Sequencer	owse
Show files of type: VHDL Files (*.vhdl, *.vhd, *.vho)	¥	
Folders	Content of D:\LatestBuild\examples\tutorial_ref\Import\Sequence	er 🔳
	[] Name Type Size ∠Date	Modified
dd_tutorial_ref	VHDL File 5 KB Fri Mar 20 2009	04:37:16
	Seq_TestBench.vhd VHDL File 1 KB Fri Mar 20 2009	04:37:16
	VHDL File 1 KB Fri Mar 20 2009	04:37:16
🖃 – 🗹 🔂 tutorial_ref		
🖻 – 💟 🚖 Import		
Calculator		
The source mixed avm2		
	×	
	Use advanced settings OK Cancel	Help

 $D: \label{eq:latestBuild} examples \tutorial\_ref \label{eq:latestBuild} examples \tutorial\_ref \label{eq:latestBuild} examples \tutorial\_ref \label{eq:latestBuild} examples \tutorial\_ref \tutorial$ 

3. Click **OK** to display the Target Libraries page of the Add Existing Design wizard.

🚜 Add Existing Design - Tar	get Libraries	×
Files are imported to one or more ta Choose the default target library:	rget libraries. SCRATCH_LIB Add	
The following Target Libraries have Click on a library to view the files the	been identified for these files. Nat will be imported there.	
Libraries:	Files:	
SCRATCH_LIB	D:\LatestBuild\examples\tutorial_ref\Import\Sequencer\Seq_Generator.vhd D:\LatestBuild\examples\tutorial_ref\Import\Sequencer\Seq_TestBench.vhd D:\LatestBuild\examples\tutorial_ref\Import\Sequencer\Seq_Tester.vhd	d
Target Library Click here to	change the target library for the selected files.	
	< Back Next > Cancel Help	

The Target Libraries page allows you to specify the library used for the added design when no library is explicitly specified in the source HDL. You can also change the library used for views added from one or more of the source files.

4. Choose the *SCRATCH\_LIB* library and click the **Next** button to display the Target Directories page.

🚯 Add Existing Design - Target Directories 🛛 🔀
Target Directories Files will be imported to directories below the root HDL mappings of the following libraries:
SCRATCH_LIB : \
Target Directory Click here to set the target directory for the selected library
Additional Options
Verwrite existing files
Split Source Design Units into Separate files
Create References to files
Import directory structure
Create graphical representations of source code
C Editable graphics that can generate code
Visual representations for documentation and understanding
< Back Finish Cancel Help

This page allows you to view or edit directory names used by the added files when you are adding HDL from a directory hierarchy.

5. Click the **Finish** button on the Target Directories page to complete the HDL adding.

The SCRATCH\_LIB library is automatically opened in a new design explorer window.

The HDL Log Window shows the progress of the add operation and the following summary report is displayed on completion:

HDL Import complete 3 files imported to 1 library

## **Browse the Fibonacci Design**

1. Examine the design in the design explorer *Design Units* pane using the icons to expand each design unit.

The following picture shows the added VHDL design:

Design Explorer [ Using v	iewpoint :	Default Vie	wpoint ]				? 4 ×
Design Unit	Language	Туре	Extends	Time Sta	mp	Design Hierarchy	Design Unit
I CO SCRATCH_LIB						🖃 💑 fibgen_tb	fibgen_tb
accumulator	VHDL	Component		Mon Apr (	06 20	⊡ <b>∆</b> ≌ fibgen_tb	fibgen_tb
💾 accumulator	VHDL	Entity		Mon Apr (	06 20	🖃 🔮 struct	fibgen_tb
⇒ 😫 spec	VHDL	Architecture		Mon Apr I	06 20	📲 Checke	er fibgen_tester
😑 — 📜 control	VHDL	Component		Mon Apr I	06 20	🖻 🏪 UUT	fibgen
😭 control	VHDL	Entity		Mon Apr I	06 20	- 🎦 acc	c_A accumulator
🕞 🎽 fsm	VHDL	Architecture		Mon Apr I	06 20	🎦 acc	c_B accumulator
🖻 — 📜 fibgen	VHDL	Component		Mon Apr I	06 20	aci	c_s accumulator
🔤 fibgen	VHDL	Entity		Mon Apr I	06 20	- 🎦 FSI	M control
->😭 struct	VHDL	Architecture		Mon Apr I	06 20		
⊜⊸ <b>∆¦</b> , fibgen_tb	VHDL	Component		Mon Apr I	06 20		
<b>∆</b> ≌ fibgen_tb	VHDL	Entity		Mon Apr I	06 20		
struct	VHDL	Architecture		Mon Apr I	06 20		
E-12 fibgen_tester	VHDL	Component		Mon Apr I	06 20		
fibgen_tester	VHDL	Entity		Mon Apr I	06 20		
⊶⊳ <b>≌</b> spec	VHDL	Architecture		Mon Apr I	06 20		
T							
<					>		
Files		Туре	Extend	ls Si	ze		
🗉 🐺 DesignChecker							
🖭 🐼 Documentation & Vi	sualization						
🗹 🥏 Design Files							
🖻 💭 SCRATCH_LIB							
🖲 s 🚍 Seq_Genera	tor.vhd	Source File	•	61	B		
🐑 s 🗾 Seq_TestBer	nch.vhd	Source File	•	21	(B		
🐑 s 🗾 Seq_Tester.v	/hd	Source File	•	1 1	(B		
<					>		>
Project SCRATCH_LIB							

Each Verilog module or VHDL entity in the source HDL code is partitioned into a separate design unit which also includes the corresponding VHDL architectures if you are using VHDL.

Notice that a  $\triangle$  icon is displayed adjacent to the *fibgen\_tb* design unit in the *Design Units* pane. This test bench component is marked as the top level design unit.

Both Verilog and VHDL designs are shown in the design explorer with the *Design Units*, *Files* and *Design Hierarchy* panes.

If the *Design Hierarchy* pane is not visible, select the *fibgen\_tb* design unit and use the Right mouse button to select **Show Hierarchy** from the popup menu.

#### Note \_

You can toggle the hierarchy for any object by choosing **Hide Hierarchy** or **Show Hierarchy** from the popup menu.

You can also add or remove objects in the **Design Hierarchy** pane by dragging and dropping with the **Left** mouse button.

2. Examine the design in the *Design Hierarchy* pane using the icons to expand each view.

The *Design Hierarchy* pane shows how each Verilog module or VHDL architecture is instantiated as a HDL text view in the hierarchy.

The test bench (*fibgen\_tb*) contains the *fibgen* design unit instantiated as the unit under test (*UUT*) and also the *fibgen\_tester* instantiated as the *Checker*.

The *UUT* hierarchy contains the *control* design unit (instantiated as *FSM*) and three instantiations (*acc\_A*, *acc\_B* and *acc\_sum*) of the accumulator.

# **Create a Block Diagram View**

- 1. Select the module view (if you are using Verilog) or the architecture view (if you are using VHDL) of the *fibgen* design unit in the *Design Units* pane of the design explorer.
- 2. Use the right mouse button to choose **Single Level** from the **Convert To Graphics** cascade in the popup menu (or use the **Convert HDL to Graphics** button) to display the View Styles page of the Convert To Graphics wizard:

👯 Convert To Graphics Wizard - View Styles	×
Specify the graphical view styles for the conversion. Hierarchy Descriptions Convert this hierarchy description as: Block Diagram IBD	
Leaf Level Descriptions No leaf level descriptions were specified.	]
<ul> <li>State Diagram</li> <li>If a State Machine cannot be recognized, create a Flow Chart</li> <li>Flow Chart</li> <li>Block Diagram</li> </ul>	
<ul> <li>Create Symbol Always</li> <li>Create a symbol even if no view styles are selected.</li> <li>Split Source Design Units into Different Files</li> </ul>	
Next > Finish Cancel Help	

3. Select the **Block Diagram** option for hierarchy descriptions and use the **Finish** button to convert the HDL text view to a graphical block diagram.

The HDL Log Window displays a summary report on completion:



Notice that the icon used for the default *fibgen* view in the design explorer changes to **R** indicating that it has been converted to a block diagram view.



4. Double-click to open the block diagram which should look similar to the following picture:



The block diagram shows the four components (*acc\_A*, *acc\_B*, *acc\_sum* and *FSM*) with the signals connected between them and an embedded block (*eb1*) containing concurrent assignment statements. All signal nets are connected by default.

#### Note \_

If you move the cursor over any object, a popup graphic tip is displayed showing information about the object.

For example, the port name and the connected net name are shown when the cursor is over a component port.

The block diagram is completed by a default title block.

You can open down into the HDL describing each component or embedded block by double-clicking over the instance on the diagram or by selecting the instance and choosing the view from the **Open As** or **Open** cascade of the popup menu.

Notice that the printer page boundaries for your default printer are shown by dotted lines on the diagram with the origin at the top left corner of the window. You can change the page layout and set options for page boundaries by choosing **Page Setup** from the **File** menu to display the **Page Setup** dialog box.

The **Layout** tab allows you to modify the page layout so that the diagram prints on a single page. For example by setting the **Adjust to** option to print at 75% of normal size or by setting the **Fit to** option to a specified number of pages.

🛺 Page Setup	X
Layout Boundaries Misc	
Margins Horizontal: 0.69''	Vertical: 0.69"
Scaling	
Adjust to: 100	% normal size
C Fit to:	page(s) wide by 1 tall
Paper size: Letter	<b>_</b>
Orientation	Panel Outline Visibility
O Portrait	C Show All Panels
C Landscape	Show Specified Panel
C Best Fit	<ul> <li>Hide All Panels</li> </ul>
Show Headers and Footers	
	OK Cancel Help

The **Boundaries** tab allows you to set options for how page boundaries are displayed and printed. Use the **Help** buttons on each tab to display a full description of the options available in this dialog box.

The page boundaries on the diagram are automatically updated when you change the page setup or you can choose **Refresh Page Boundaries** from the **File** menu to update them after changing the diagram.

HDL Designer Series allows you to make logical edits which would change the HDL description for a graphic editor view. However, you can make non-logical edits to

prepare a diagram for printing or export. If you have made any non-logical edits, you are prompted to save when you close the graphic editor view.

For example, you can move or resize objects, change the grid, port or signal text visibility, and edit the comment text in the title block.

5. Re-size the diagram to fit in a single printer page boundary:

	0	te	
•	v	i C	

You can make all text associated with an object visible by choosing **Show Text** from the popup menu or hide an individual text element by choosing **Hide Text**.

Refer to the *HDL Designer Series Graphical Editors User Manual* for more information about editing the diagram layout and changing the visibility of text objects.

### **Print the Diagram**

You can print an entire diagram view or the extent of the current window by choosing **Print** or **Print Window** from the **File** menu.

Note also that the Print dialog box includes an option to print selected pages or you can choose **Print Page** from the popup menu to print the area within the current page boundaries.

-Page Range	
O Pages:	
C Panels:	<b>_</b>

## Add Panels to the Block Diagram

- 1. Use the **Add Panel** button (or choose **Panel** from the **Add** menu) to add a panel (*Panel0*) on the diagram. Hold down the **Left** mouse button and drag the panel around the graphical objects on the diagram releasing the button when the panel encloses the required area. Click the **Right** mouse button to deselect the panel tool.
- 2. Click the **Right** mouse button in an empty part of the diagram to display the popup menu and choose **Object Visibility** to display the Object Visibility Settings dialog box.

🚜 Object Visibility Settings	
Declarations     Comment Text     Package List	OK Cancel
	Help

- 3. Select the Declarations option and choose **OK**.
- 4. Drag this text to an empty part of the diagram by dragging the Declarations label. (You cannot move this object by dragging the individual declaration statements.)

Note	

You can select text objects only by using the	•	on the	- ⊗	and choosing Select T	ext
from the drop down menu.					

5. Use the **Add Panel** button (or choose **Panel** from the **Add** menu) and drag a new panel (*Panel1*) around the signal declarations.

Pan	 el1						
	Declarations						
	Porte						
	10115.		1				
	clock	:	std_10g	ic			
	Teset .		'std log	ic			
	· · fibout · ·		std log	ic vector	(7 dommto	-0)	
	Dee Hees			-			
	Fre User:						
	Diagram Signals:						
	Interna	al signa	l declar	ations .			
	STONAL A			and logic	vector(7	DOLDER	0 01
	STCHAT B		<u>-</u> -			DOLDET	o oi -
	STORAL D		-	sca_rogre	_veccor()	D00001	0 0)
	STGNAL STR						
	DIVISION CI			std_logic			
	· · SIGNAL gro	i		std_logic std_logic			
	SIGNAL gnd	i		std_logic std_logic std_logic			
	SIGNAL gnd SIGNAL ind SIGNAL 14	і 		std_logic std_logic std_logic std_logic		· · ·	
	SIGNAL gra SIGNAL in SIGNAL 1d	A B		std_logic std_logic std_logic std_logic		· · ·	· · ·
	SIGNAL gnd SIGNAL ind SIGNAL 1d SIGNAL 1d	A B sum		std_logic std_logic std_logic std_logic std_logic			
	SIGNAL ind SIGNAL ind SIGNAL 14 SIGNAL 14 SIGNAL 34 SIGNAL 54	A B sum		std_logic std_logic std_logic std_logic std_logic std_logic	_vector(7	DOUBLE	0.0)
· · ·	SIGNAL GRA SIGNAL in SIGNAL 14 SIGNAL 14 SIGNAL 34 SIGNAL 34	A B Sum it buffe	r signal	std_logic std_logic std_logic std_logic std_logic std_logic declarat	_vector(?	DOUBLE	0.0)
	SIGNAL gm SIGNAL ind SIGNAL 1d SIGNAL 1d SIGNAL 3d Implic SIGNAL fil	A B sum it buffe	z signal ernal	std_logic std_logic std_logic std_logic std_logic std_logic declarat std_logic	_vector(7 ions yector(7	DOURT	0.0)
· · · · · · · · · · · · · · · · · · ·	SIGNAL GMA SIGNAL ind SIGNAL id SIGNAL id SIGNAL id SIGNAL su Implic SIGNAL fil	À B sum it buffe	r signal ernal,	std_logic std_logic std_logic std_logic std_logic std_logic declarat std_logic	_vector(7 ions _vector(7	DOUBIT	0.0)
	SIGNAL GM SIGNAL 14 SIGNAL 14 SIGNAL 14 SIGNAL 14 SIGNAL sup Implic: SIGNAL fill Post User:	A_B 	r signal ernal	std_logic std_logic std_logic std_logic std_logic std_logic declarat std_logic	_vector(7 ions _vector(7	DOUBIT	0.0)

The signal declarations are now displayed in a separate panel from the graphical diagram layout and can be printed or exported separately by specifying the panel name.

For example, the Print dialog box contains an option to select a named panel for printing.

– Page Range –	
C All	
O Pages:	
Panels:	Panel0 👻
	Panel0
	Panell R

## **Object Linking and Embedding**

On a Windows workstation, you can use Object Linking and Embedding (OLE) to drag a complete or partial graphic editor view directly on to a documentation tool such as Microsoft Word or Adobe FrameMaker.

This can be done by pressing the **Right** mouse button over the blue border on the left edge of a diagram to display a popup menu and choosing **Set Drag All** or **Set Drag Panel <panel name>**.



The diagram or panel can then be imported directly into the documentation tool by dragging the blue border using the **Left** mouse button. A diagram included in this way can be opened from within the documentation tool by simply double-clicking on the picture to invoke the HDL Designer Series tool.

## **Display the IBD View**

1. Use **Edit as IBD** button or choose **Edit as IBD** from the **Diagram** menu in the block diagram to open an alternative editor view which displays the interfaces and connections as a tabular Interface-Based Design view. You are prompted to save the block diagram prior to opening the IBD view (if it is not already saved).

Notice that each of the four components and the embedded block are shown as separate columns in the IBD view matrix.

A separate column (E in the example below) shows the external interface for the design unit.

18	SCF	ATCH_LIB/fibgen/	struct * (IBD)	(Syncl	ironiz	ed	View	)							
File	E	dit View HDL Table	Data Tasks	Add C	ptions	W	/indow	Help							
1 *															
1 6															
J	😃 판 팬 밴 🗄 🔚 🖃 펜 이 다. 다. 🐃 🏹 3월 3일 🖓 24 84 💥 백 맨 1월 1월 다)														
7	🖬 - 😸 - 🛂 - 🕅 -														
		A	В	С	E	F	G	н	I	J	м	P	s	Т	U
	1					-	Panel	0							
	2	Name	Туре	Bounds	fibge			ccumulat	or	accumulato	accumulato	control	eb 1	Initial	Comment
	3	Library:			-		SC	RATCH_	LIB	ATCH_	ATCH	ATCH			
	4	Instance Ref:						acc_A		acc_B	cc_sun	FSM			
щ	íM)	Port Map:					- 🗆	Port	Actua	+ +	+ +	+ +			
ă	6	clock	std_logic		I		I	clock		I	I	I			
	7	reset	std_logic		I							I			
	8	fibout	std_logic_vector	(7:0)	<u> </u>								0		
	9	A	std_logic_vector	(7:0)			U	op		I			I		
	10	B	std_logic_vector	(7:0)						U			I		
	11	cir	std_logic				I	clr		I	I	0			
	12	gnd	std_logic				I	inc			I		0		
	13	inc	std_logic							I		0			
	14	Id_A_B	std_logic				I	ld	L	I		0			
	15	ld_sum	std_logic	(7. 1)						-	I	0			
	16	sum	std_logic_vector	(7:0)		-					I		0		
	17	tibout_internal	std_logic_vector	(7:0)	<u> </u>	-	Ĩ	ip			0		1		
l	18														
] ]	<u>≫</u> × <u>A</u> × ⊠ ×   <u>A</u> <sub>A</sub> * <u>B</u> <u>I</u> <u>U</u>   ≡ ≡ ≡														
Rea	dy														

The rows in the matrix contain the signal declarations and interconnections are shown by the letter I (Input) or O (Output) in the interconnect cell for the external interface, embedded block or component interface. You can expand the interface column to display the connected ports for a component as shown for the *acc\_A* instance above by clicking on the + icon.

#### Note \_

Refer to the IBD View Notation section in the *HDL Designer Series Graphical Editors User Manual* for information about how more complex port mapping is represented in an IBD view.

# **Display the Symbol**

1. Click the **Open Up** button in the block diagram or IBD view window to display the symbol interface as a tabular IO view in a new window.

R	sc	RATCH	_LIB/f	ibgen/sy	mbol (Interf	ace)						×
Fil	e E	idit Vie	w HDL	Table	Tasks Add O	ptions \	Window	Help				
?	1		→ 🖬	5	- X 🗈 (		⊂× #	🖻	¥ • 🚿 •	M - 💆 - 🚺	2 - 1	ş •
] -	▶ ▶ ♦ ♦ 🖧 ☜ 🖃 賣 幸 🍞   荡 分 좌 🖨 隆   🔎											
		А	в	С	D	E	F	G	Structur	e Navigator		Ŀ
Щ	M	Group	Name	Mode	Туре	Bounds	Initial	Comment		nterface	^	Dia
0	1		clock	IN	std_logic					Symbol Generics		gran
	2		reset	IN	std_logic					Declarations		P
	3		fibout	OUT	std_logic_vector	(7:0)			<b>P</b> ] <b>I</b>	Package List	~	e wo
	4								<		>	ë
									Content		-	
],	<u>ی</u>	• <u>A</u> ·		A A	в <i>і</i> <u>и</u>							
Re	ady											//

2. Display the symbol by selecting **Symbol** in the Structure Navigator pane.

1	<b>R</b> s	icr <i>i</i>	<b>ATC</b>	н_	LIB	/fil	bge	n/	syı	nb	ol	•	(Sy	٨	bo	I)																			(			×
F	File	Edi	t١	/iew	H	XL.	Di	agr	am	٦	ask	s	A	dd	C	)pti	ion	s	Wi	ind	0%	1	Help	þ														
]	徻	) -	4		•	2	8		ð	•	X		Ēþ	ð	ß		n		ç)i	á	H		P	8	€	P	X	2	ø									
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3. Close the symbol/Interface, IBD view/Block diagram windows saving any non-logical edits.

# **Create a State Diagram View**

- 1. Select the module view (if you are using Verilog) or the architecture view (if you are using VHDL) of the *control* design unit in the *Design Units* pane in the design explorer.
- 2. Use the Right mouse button to choose **Single Level** from the **Convert To Graphics** cascade in the popup menu (or use the **Convert HDL to Graphics** button) to display the View Styles page of the Convert to Graphics wizard.

🌇 Convert To Graphics Wizard - View Styles	$\mathbf{X}$
Specify the graphical view styles for the conversion. Hierarchy Descriptions No hierarchy descriptions were specified. Block Diagram	
Leaf Level Descriptions Convert this leaf level description as: State Diagram If a State Machine cannot be recognized, create a Flow Chart Flow Chart Block Diagram	
<ul> <li>Create Symbol Always</li> <li>Create a symbol even if no view styles are selected.</li> <li>Split Source Design Units into Different Files</li> <li>Next &gt; Finish Cancel Help</li> </ul>	

3. Select the **State Diagram** option for leaf-level descriptions and use the **Finish** button to convert the HDL text view to a graphical state diagram.

The HDL Log Window displays a summary report on completion:

Convert To Graphics complete 1 HDS design unit saved, 1 component 1 state machine

Notice that the icon used for the *FSM* instance changes to indicating that it has been converted to a state diagram view.

4. Double-click to open the state diagram which should look similar to the following picture:



#### Note.

You can zoom in, zoom out or view all of the state diagram using the **Zoom In**, **Zoom Out** or **View All** buttons.

This simple state machine comprises a start state (*clr\_regs*) and three simple states (*inc\_accb*, *load\_acc\_sum* and *load\_acc\_A\_B*) connected by transitions.

You can move or resize objects, add panels and edit the title block or make any other non-logical edits which would not change the logical definition of the state machine.

Notice that there is a deliberate signal assignment error in the actions specified for the *clr\_regs* and *inc\_accb* states. To show the actions choose **Show Text** from the state popup menu.

HDL Designer Series allows you to correct these errors by changing the logical definition and the original source code to view the corrected state diagram.

## **Relevel the State Diagram**

The example used in this tutorial comprises only four states but state machines recovered from real designs may have many states. In these cases, it can be useful to break the initial flat state diagram into one or more hierarchical diagrams.

- 1. Select the *inc\_accb*, *load\_acc\_sum* and *load\_acc\_A\_B* states by holding down the **Shift** key as you select the three states.
- 2. Choose **Add Hierarchy** from the **Re-level** cascade in the **Diagram** or popup menu. Notice that the selected states are replaced by a hierarchical state (*s0*).



The selected states have been moved into a new child hierarchical state diagram. The child diagram is saved as part of the same design unit view and is logically identical to the original flat diagram.

3. Double-click the hierarchical state (s0) to open the child hierarchical state view.

You can remove state machine hierarchy by selecting the hierarchical state and choosing **Remove Hierarchy** from the **Re-level** cascade in the **Diagram** or popup menu. This operation brings all states in the child diagram up a level into the parent diagram.

Windows users can print or insert any hierarchical state diagram into a design document using OLE in the same way to that previously described for block diagrams.

You can also add a title block and comment text, comment graphics or panels to any diagram in the hierarchy.



For example, a title block and a panel have been added to the following child state diagram view:

4. Close the child and parent state diagrams saving any non-logical edits.

## **Create a Flow Chart View**

Any HDL text view can be optionally recovered as a flow chart. The alternative flow chart option is set by default when you set the state diagram HDL convert option (in the Add Existing Design wizard) and any HDL text view which is not recognized as a state machine is automatically converted to a flow chart.

- 1. Select the *accumulator* design unit in the design explorer and use the **Convert HDL to Graphics** button.
- 2. Select the **Flow Chart** check box in the **Leaf Level Descriptions** pane of the Convert to Graphics Wizard and click **Finish**.

The new flow chart is added to the *accumulator* component in the design explorer, represented by the  $\mathbb{R}$  icon.





#### Note.

If you are using Verilog, the decision box for the clock event is not present.

Notice how the HDL code is represented by a number of separate action boxes with conditional statements represented by decision boxes. A more complex design may also include case boxes, loops and wait boxes.

Windows users can print or insert a flow chart into a design document using OLE in the same way to that previously described for block diagrams and state diagrams. You can also add a title block and comment text, comment graphics or panels.

4. Close the flow chart saving any non-logical edits.

# Visualizing your HDL Designs

You have now added HDL code to HDS, converted it to block diagram, IBD, state diagram and flow chart views. You can also visualize your HDL text views by transforming your source code into graphical views known as visualization views. Only non-logical edits can be performed on the resulting graphical views. That is to say, you can make layout modifications and save them, yet you cannot perform logical edits that would reflect on the source code; however, any changes in the source HDL view can be easily updated in the visualization view.

 Select the *fibgen\_tb* design unit in the design explorer and use the **Document And** Visualize drop-down palette in the toolbar or choose **Document and Visualize** from the File menu. Choose the Document and Visualize through Components option. The Document and Visualize dialog box is displayed.

🚻 Document & Visualize 🛛 🔀
Visualize Your Code Generate graphical visualization views for your HDL source code
Create a Website (Export HTML) Create Design based Website Store at: \$HDS_PROJECT_DIR/HTMLExport Browse
Options OK Cancel Help

2. Click the **Options** button to display the Documentation and Visualization Options dialog box. Check that Block Diagram, Flow Chart and Open diagram after visualization options are selected and click **OK**.

💦 Documentation and V	isualization Options 🛛 🔀
<ul> <li>Website Options</li> <li>HTML Settings</li> <li>Graphics Settings</li> <li>Visualization Options</li> <li>Graphics Appearance</li> <li>Structural Diagram</li> <li>Placement Settings</li> </ul>	Option settings for use when visualizing HDL text views Hierarchy Descriptions Visualize design hierarchy descriptions as: <ul> <li>Block Diagram</li> <li>IBD</li> </ul>
Routing Settings	Leaf Level Descriptions Visualize leaf level descriptions as: State Machine If a State Machine cannot be recognized, visualize a Flow Chart Flow Chart Block Diagram
	Other  Other  Overwrite existing views  Copy existing views before overwriting them  Verbose (Display additional information during conversion)  Open diagram after visualization  Hide Symbol Ports
	OK Cancel Help

3. On the Document and Visualize dialog click **OK** to proceed with your visualization. A progress indicator is displayed showing the advancement of the visualization process, and then a message is raised informing you of the location of the visualization views; click **OK**.

R Document & Visualize Results
The results of running Document & Visualize will be displayed in the Files browser under Document & Visualize root node. You can open the created Visualizations or website pages any time by double clicking the displayed nodes.
Do not show this message again
OK

# **Note** If a graphical view already exists for the design object you wish to visualize, you will not be able to create a visualization view having the same name as that of the graphical view. In this case, a message is raised informing you that graphical views having the same name already exist and to replace these graphical views, you have to set the option "Overwrite Existing Views" in the Documentation and Visualization dialog box. Nevertheless, if you do not wish to override the existing graphical views, you can rename them before running the visualization process.

4. Consequently, a window is opened showing the top-level of the *fibgen\_tb* design unit visualized as a block diagram.



5. To view the source code of the visualization click on the **Open HDL Source** button in the toolbar of the visualization window. The DesignPad editor displays the current top-level design only.

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- <i>4</i> 4a	2	
Code Browser	3	LIBRARY ieee ;
	4	USE ieee.std_logic_1164.all;
Parser Level: Full	5	USE ieee.std_logic_arith.all;
- The Of Last	6	
	7	ENTITY fibgen_tb IS
Bottom Uf Text	8	Test bench has no external interface
hbgen_tb	9	
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6. In the Files pane of the Design Manager window expand the *Visualization* folder of the Documentation and Visualization node to explore the rendered visualized views.

Files	Туре
🖭 📝 DesignChecker	
🗹 🐼 Documentation & Visualization	
HTML	
🗄 🔄 Visualization	
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	Flow Chart
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🖉 🖓 🖁 struct	Block Diagram
🗄 🔤 fibgen_tester	Component
🔤 🛃 spec	Flow Chart
🛨 🥏 Design Files	
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On double-clicking on any of the visualized child views, a graphical editor window is opened to display the HDL visualized.

7

Refer to the "Documentation and Visualization" chapter in the *HDL Designer Series User Manual* for more information about visualizing HDL text views.

# **Export the Design Hierarchy as HTML**

You can print any of these views or you can export any view (or hierarchy of views) in HTML format as a fully browsable web site.

- 1. Select the *fibgen\_tb* design unit in the design explorer and use the **Document And Visualize Design** button or choose **Document and Visualize** from the **File** menu to display the Document and Visualize dialog box. Choose the Document and Visualize through Components option.
- 2. Choose the Create a Website (Export HTML) option.

🔐 Document & Visualize 🛛 🛛 🔀			
Generate graphical visualization views for your HDL source code			
Create a Website (Export HTML)			
Create Design based Website			
Store at:	\$HDS_PROJECT_DIR/HTMLExport  Browse	1	
Options			
	OK Cancel Help		

- 3. Click the **Options** button to display the Documentation and Visualization Options dialog box.
- 4. In the Website Options tab, set the depth of the Hierarchy Levels to Descend as All.

All Include options should be left set for this tutorial although these can be used to exclude specific view types. (For example, you might unset all options except **Block Diagram** or **IBD** when you only want to export structural views.)

🚯 Documentation and Visualization Options 🛛 🛛 🔀		
Visualization Options Graphics Settings Visualization Options Graphics Appearance Structural Diagram Placement Settings Routing Settings	Website Options         Hierarchy Levels to Descend         All       Specified         Graphics         Generate Graphics Files Only         Update graphical images of design units without generating HTML files.         Auto Export Visualizations         Create visual representations of source code for the website	
	(Only if Visualize Code option is selected or visualizations already exist)  Include  ASM  Block Diagram  Flow Chart  IBD  ModuleWare Symbol  State Diagram  Symbol  SystemC Include  Text Printing  Truth Table  VHDL Architecture  NHDL Gate Local	
	Elements checked in the above list will be included in the exported documentation.   Export referenced Packages  Include Standard Packages  Export included Verilog "include files  Include Standard "includes	

- 5. In the Graphics Settings tab, set the Graphics Format as **JPEG**.
- 6. Click the **OK** button to confirm the Documentation and Visualization Options dialog box.
- 7. In the Document and Visualize dialog box, enter (or use the Browse button to browse for) the location of the export target directory (for example, *D:\Temp\ExportHTML*) and click the **OK** button to confirm the Document and Visualize dialog box.

All other options should be left with their default settings. The export operation is monitored in the HDL Log Window ending with a summary report:

```
The design has been exported to the directory \texttt{D:}Temp\ExportHTML
```

To view the HTML load the following file into your Browser. SCRATCH\_LIBfibgen\_tbindex.htm Export HTML complete.

## **View the Exported HTML Hierarchy**

- 1. Your default web browser is automatically launched displaying the index file *SCRATCH\_LIBfibgen\_tbindex.htm* file. The exported HTML tree appears in the Files pane of your design explorer. The exported HTML is displayed in two frames:

  - The Design frame shows the graphical or HDL text view corresponding to the object selected in the Navigation frame. You can also use the tabs to display additional information including side data and generated HDL.

For example, the following Internet Explorer browser shows the expanded *fibgen\_tb* hierarchy and the *Fibgen* block diagram displayed in the Design frame.



When you have exported hierarchical views, hyperlinks are created on the parent diagram (for example, blocks and components on a block diagram or hierarchical states on a state diagram).

You can open down into the child views by clicking on these hotspots to display the corresponding HTML page. Alternatively, you can use the **Open Up** button to move up through the design hierarchy.

#### Note.

The **Open Up** button moves up through the design hierarchy displayed in the Navigation frame. For a component, the parent view is displayed unlike in a graphic editor when the symbol is displayed.

You can zoom in, zoom out or view all using the **Zoom In**, **Zoom Out** or **View Normal** buttons and navigate to the previous or next view using the **Back** or **Forward** buttons.

You can use the Information tab to display text information such as generation settings, local declarations, compiler directives or package references. Additional tabs allow you to display side data and generated HDL if these have been also exported.

# **Export the Design Library as HTML**

You can also export HTML for an entire library. This option allows you to export HTML for all design unit views in a library including symbols, non-default views and any views of design units which have no explicit hierarchical relationship.

- Select the SCRATCH\_LIB library in the design explorer the design explorer and use the button or choose Document and Visualize from the File menu to display the Document and Visualize dialog box.
- 2. Follow steps 2 to 7 in the previous section (Export the Design Hierarchy as HTML). When you confirm the dialog box, HTML is exported for each design unit in the library.

## **View the Exported HTML Library**

1. View the exported library by opening the HTML index file *SCRATCH\_LIBindex.htm* file from the HTML directory in the Files explorer pane.

Any of these views can be displayed in the Navigation frame and browsed in a similar way to the exported hierarchy.



For example, the following Internet Explorer browser shows the contents of the *SCRATCH\_LIB* library with the control state machine shown in the Design frame:

Refer to the "Printing Views" and the "Documentation and Visualization" chapters in the *HDL Designer Series User Manual* for more information about printing and exporting graphical views.

You have now completed the Design Exploration Tutorial.

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#### 11. INFRINGEMENT.

- 11.1. Mentor Graphics will defend or settle, at its option and expense, any action brought against Customer in the United States, Canada, Japan, or member state of the European Union which alleges that any standard, generally supported Software product infringes a patent or copyright or misappropriates a trade secret in such jurisdiction. Mentor Graphics will pay any costs and damages finally awarded against Customer that are attributable to the action. Customer understands and agrees that as conditions to Mentor Graphics' obligations under this section Customer must: (a) notify Mentor Graphics promptly in writing of the action; (b) provide Mentor Graphics all reasonable information and assistance to settle or defend the action; and (c) grant Mentor Graphics sole authority and control of the defense or settlement of the action.
- 11.2. If a claim is made under Subsection 11.1 Mentor Graphics may, at its option and expense, (a) replace or modify Software so that it becomes noninfringing, or (b) procure for Customer the right to continue using Software, or (c) require the return of Software and refund to Customer any license fee paid, less a reasonable allowance for use.
- 11.3. Mentor Graphics has no liability to Customer if the claim is based upon: (a) the combination of Software with any product not furnished by Mentor Graphics; (b) the modification of Software other than by Mentor Graphics; (c) the use of other than a current unaltered release of Software; (d) the use of Software as part of an infringing process; (e) a product that Customer makes, uses, or sells; (f) any Beta Code; (g) any Software provided by Mentor Graphics' licensors who do not provide such indemnification to Mentor Graphics' customers; or (h) infringement by Customer that is deemed willful. In the case of (h), Customer shall reimburse Mentor Graphics for its reasonable attorney fees and other costs related to the action.
- 11.4. THIS SECTION IS SUBJECT TO SECTION 8 ABOVE AND STATES THE ENTIRE LIABILITY OF MENTOR GRAPHICS AND ITS LICENSORS AND CUSTOMER'S SOLE AND EXCLUSIVE REMEDY WITH RESPECT TO ANY ALLEGED PATENT OR COPYRIGHT INFRINGEMENT OR TRADE SECRET MISAPPROPRIATION BY ANY SOFTWARE LICENSED UNDER THIS AGREEMENT.

#### 12. TERM.

- 12.1. This Agreement remains effective until expiration or termination. This Agreement will immediately terminate upon notice if you exceed the scope of license granted or otherwise fail to comply with the provisions of Sections 2, 3, or 5. For any other material breach under this Agreement, Mentor Graphics may terminate this Agreement upon 30 days written notice if you are in material breach and fail to cure such breach within the 30 day notice period. If a Software license was provided for limited term use, such license will automatically terminate at the end of the authorized term.
- 12.2. Mentor Graphics may terminate this Agreement immediately upon notice in the event Customer is insolvent or subject to a petition for (a) the appointment of an administrator, receiver or similar appointee; or (b) winding up, dissolution or bankruptcy.
- 12.3. Upon termination of this Agreement or any Software license under this Agreement, Customer shall ensure that all use of the affected Software ceases, and shall return it to Mentor Graphics or certify its deletion and destruction, including all copies, to Mentor Graphics' reasonable satisfaction.
- 12.4. Termination of this Agreement or any Software license granted hereunder will not affect Customer's obligation to pay for products shipped or licenses granted prior to the termination, which amounts shall immediately be payable at the date of termination.
- 13. **EXPORT.** Software is subject to regulation by local laws and United States government agencies, which prohibit export or diversion of certain products, information about the products, and direct products of the products to certain countries and certain persons. Customer agrees that it will not export Software or a direct product of Software in any manner without first obtaining all necessary approval from appropriate local and United States government agencies.
- 14. U.S. GOVERNMENT LICENSE RIGHTS. Software was developed entirely at private expense. All Software is commercial computer software within the meaning of the applicable acquisition regulations. Accordingly, pursuant to US FAR 48 CFR 12.212 and DFAR 48 CFR 227.7202, use, duplication and disclosure of the Software by or for the U.S. Government or a U.S. Government subcontractor is subject solely to the terms and conditions set forth in this Agreement, except for provisions which are contrary to applicable mandatory federal laws.
- 15. **THIRD PARTY BENEFICIARY.** Mentor Graphics Corporation, Mentor Graphics (Ireland) Limited, Microsoft Corporation and other licensors may be third party beneficiaries of this Agreement with the right to enforce the obligations set forth herein.
- 16. REVIEW OF LICENSE USAGE. Customer will monitor the access to and use of Software. With prior written notice and during Customer's normal business hours, Mentor Graphics may engage an internationally recognized accounting firm to review Customer's software monitoring system and records deemed relevant by the internationally recognized accounting firm to confirm Customer's compliance with the terms of this Agreement or U.S. or other local export laws. Such review may include FLEXIm or FLEXnet (or successor product) report log files that Customer shall capture and provide at Mentor Graphics' request. Customer shall make records available in electronic format and shall fully cooperate with data gathering to support the license review. Mentor Graphics shall bear the expense of any such review unless a material non-compliance is revealed. Mentor Graphics shall treat as confidential information all information gained as a result of any request or review and shall only use or disclose such information as required by law or to enforce its rights under this Agreement. The provisions of this section shall survive the termination of this Agreement.
- 17. CONTROLLING LAW, JURISDICTION AND DISPUTE RESOLUTION. The owners of the Mentor Graphics intellectual property rights licensed under this Agreement are located in Ireland and the United States. To promote consistency around the world, disputes shall be resolved as follows: This Agreement shall be governed by and construed under the laws of the State of Oregon, USA, if Customer is located in North or South America, and the laws of Ireland if Customer is located outside of North or South America. All disputes arising out of or in relation to this Agreement shall be submitted to the exclusive jurisdiction of Portland, Oregon when the laws of Oregon apply, or Dublin, Ireland when the laws of Ireland apply. Notwithstanding the foregoing, all disputes in Asia (except for Japan) arising out of or in relation to this Agreement shall be resolved by arbitration in Singapore before a single arbitrator to be appointed by the Chairman of the Singapore International Arbitration Centre ("SIAC") to be conducted in the English language, in accordance with the Arbitration Rules of the SIAC in effect at the time of the dispute, which rules are deemed to be incorporated by reference in this section. This section shall not restrict Mentor Graphics' right to bring an action against Customer in the jurisdiction where Customer's place of business is located. The United Nations Convention on Contracts for the International Sale of Goods does not apply to this Agreement.
- 18. **SEVERABILITY.** If any provision of this Agreement is held by a court of competent jurisdiction to be void, invalid, unenforceable or illegal, such provision shall be severed from this Agreement and the remaining provisions will remain in full force and effect.
- 19. MISCELLANEOUS. This Agreement contains the parties' entire understanding relating to its subject matter and supersedes all prior or contemporaneous agreements, including but not limited to any purchase order terms and conditions. Some Software may contain code distributed under a third party license agreement that may provide additional rights to Customer. Please see the applicable Software documentation for details. This Agreement may only be modified in writing by authorized representatives of the parties. All notices required or authorized under this Agreement must be in writing and shall be sent to the person who signs this Agreement, at the address specified below. Waiver of terms or excuse of breach must be in writing and shall not constitute subsequent consent, waiver or excuse.

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