

HOMEWORK —PLACE & ROUTE OF STD-CELLS

Prof. Don Bouldin – 19 November 2004



mkdir hw6a

cp /usr/cad/course/iit/ami035_tutorial/cds* hw6a

cp /usr/cad/course/iit/ami035_tutorial/.cds* hw6a

cd hw6a

cadence_tools; icfb&

Create a new library and attach to the existing tech library:

🗙 Create Library	
OK Cancel Apply	
Library	
Name: hw6a	
Path:	
Technology Library	
If this library will not contain physical design (i.e Otherwise, you must either attach to an existing Choose option:	., layout) data you do not need a tech library. tech library or compile one.
\diamond No tech library needed	
 ◆ Attach to existing tech library> ◇ Compile tech library 	TSMC 0.40u CMOS035 (4M, 2P, HV FET) 🚘

Next, create a new cell with a schematic view:

🗙 Create New File					
OK Cance	el Defaults	Help			
Library Name	hw6a	_			
Cell Name	macro				
View Name	schematic				
Tool	Composer-Schematic	=			
Library path file					
/tnfs/home/bo	uldin/hw6a/cds.libį́				
4					

Add the desired instances from the IIT_stdcells_ami035 library. Add wires to connect them and pins for the inputs and output:



Select: Design→Check and Save

When there are no errors or warnings, perform pre-layout simulation using VerilogXL by selecting

Tools \rightarrow Simulation \rightarrow Verilog-XL and then Simulation \rightarrow Start Interactive.

cds2

When the simulations show the desired results,

```
cd macro.run1/ihnl
cp –r /usr/cad/course/ami035_tutorial
cd cds2
cp netlist ami035_tutorial/macro.vh
```

cd ami035_tutorial

cadence_tools

run-seultra

cp macro.def ../../../

cd ../../../../

Import-def



🗙 Read DEF File into CellView 🔀						
OK Cancel Defaults A	pply He	elp				
Library Name	hw6a					
Cell Name	macroj					
View Name	autolayout					
Use 🔳 Ref. Library Names	_stdcells_ami035 NCSU_TechLib_tsmc04_4M2P					
	Browse					
DEF File Name	macro.def					
Map Names From	VERILOG 🖃					
Startup Name Mapping						
Target P&R Engine	🔷 Gate Ensemble 🔶 Silicon Ensemble	4				

The layout will initially look like this:



Be sure that cds.lib points to the correct location of the libraries:

synth_iit035 ./macro.run1/ihnl/cds2/ami035_tutorial/synth_iit035

Then, select Edit→Select-All

Then, select Edit→Search→Add-Criteria and select "cell-view" and fill in "abstract" and then Near "Replace" select "cell-view" and fill in "layout". Now press "Replace-All" and then "cancel".

Search			-
Apply Cancel I	Previous Next		Hel
Add Select	Select All	Replace	Replace All
coom To Figure	J Figiere Colent 0	Queren	t Figure 0
Search for	inst 🔤 in 🔤	current cellView	Add Criteria
view name 💷 🛛	== _ abstract		Delete
	J		
		1.000	
eplace view na	une 🔤 🛛 » 🛛 Layor	at	

Then, press "shift-f" to flatten the design:



Save-as-layout

Then, double-click on "layout" to open it and then in the LSW pane, select:

Edit→set-valid-layer and check "metal-2 pn" and then "OK": Then, select "metal2—pn".

X LSW	_ 🗆 🗵	Set	Valid Lay	/er								
Edit	Help	ок	Cance	Apply	r							
	-		aangro	ت روم	WILC	<u></u>		acorgia		inc corro	- no	-
J TechLib	2 pn tsmc04 4	9	rid	dg 🗆	wire	ft 🗆		designF	d3 🗆] metal4	nt	
■ Inst ■	Pin –	9	rid	d1 🗆	pin	11 🗆		designF	d4 🗆	ca	nt	
		а	nnotat	dg 🗆	pin	dg 🗆		designF	d5 🗆	cc	nt	
AV NV	AS NS	а	nnotat	d1 🗆	pin	ae 🗆		designF	d6 🗆	ср	nt	
nodrc	dg 🛆	а	nnotat	d2 🗆	axis	dg 🗆		designF	d7 🗆	ce	nt	
nolpe	dg	a	nnotat	d3 🗆	edgeLay	dg 🗆		designF	d8 🗆	via	nt	
<mark>M</mark> pad	dg	a	nnotat	d4 🗆	edgeLay	pn 🗆		designF	d9 🗆	via2	nt	
text	dg		nnotat	as 🗆	snap			changed	to C	via3	nt	
Lican id	da da	a	nnotat	d6 🗆	stretch	dg 🗆		changed	t1 🗆] 🗙 active	pn	
dio_id	dg	а	nnotat	d7 🗆	y 0	dg 🗆	\ge	marker	wg 🗆	ca	pn	
pwell	nt	a	nnotat	d8 🗆	y1	dg 🗆	\times	marker	er 🗆	cc	pn	
nwell	nt	а	nnotat	d9 🗆	y 2	dg 🗆		Row	dg 🗆	ср	pn	
active	nt	đ	efault	dg 🗆	y 3	dg 🗆		Row	11 🗆	ce	pn	
nactiv	e nt	i	nstanc	dg 🗆	y 4	dg 🗆		Group	dg 🗆] 🗙 gwell	pn	
pactiv tactiv	e nt	i	nstanc	11 🗆	y 5	dg 🗆		Group	11 🗆] 📉 metall	pn	
poly	nt	P	rBound	dg 🗆	y 6	dg 🗆		ca	11 🗆] 🗙 metal2	pn	
elec	nt	<u>p</u>	rBound	by 🗆	y7	dg 🗆		cc	11 🗆] 🗙 metal3	pn	

Create→pin→shape

🗙 Create Shape	Pin					
Hide Cancel						
Terminal Names	vd	d! gnd!				
🔟 Keep First N	ame	X Fitch	0	Y Fitch	0	
Mode	+	rectangle	🔷 dot	polygon	circle	🔷 auto pin
🔲 Display Pin I	lame		Displa	y Pin Name Oj	ption	[

Then add a rectangular pin on the vdd! bus and another pin on the gnd! Bus.

Also, you can add labels to the layout:



Now, save the layout and verify DRC . Then, extract the layout and perform LVS and Spectre simulation.