Artisan COMPONENTS

IBM 0.18μm (CMRF7SF) Process
1.8-Volt SAGE-X™
Standard Cell Library
Databook

August 2004

Revision 1.2

Part Number DB-SX-IBM009-1.2/18

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Revision History

This document contains the release history for the IBM 0.18µm CMRF7SF Process SAGE-X™ Standard Cell Library Databook.

Part Number	Revision Number	Date of Release	Updates
DB-SX-IBM009-1.0/18	1.0	March 2003	• Initial release
DB-SX-IBM009-1.1/18	1.1	April 2003	• Metal layer revision
DB-SX-IBM009-1.2/18	1.2	August 2004	• BENC update

Customer Support

For all customer service or technical support questions, please visit the Artisan Components Web site at www.artisan.com and click on Customer Support.

You may also contact Artisan by telephone or email, using the following information:

- United States and North America 877-ARTILIB (877-278-4542)
- International 408-548-3298
- Email support@artisan.com

Introduction

Artisan's SAGE-X™ standard cell library builds upon our SAGE architecture, producing the optimum combination of high-density with high-performance. The cell line-up is derived from extensive customer design, synthesis, and place-and-route benchmark analysis. Library optimization is achieved by carefully matching the library functions and drive strengths to leading synthesis and place-and-route tools, producing superior RTL-to-GDSII results.

How This Book Is Organized

This introduction is organized into three sections:

- ***Global Parameters*** provides an overview of parameters specific to your SAGE-X library.
- ***Special Cells*** details the types of special cells included in the library.
- ***Reading the Standard Cell Datasheet*** describes the components of each datasheet.

Datasheets for each cell in this library are provided after the introduction. The datasheets are included in alphabetical order within the following categories:

- Base Cells
- Advanced Arithmetic Cells
- Register File Cells
- Synthesis Optimized Arithmetic Cells

Global Parameters

This section specifies global parameters for the IBM 0.18µm CMRF7SF Process SAGE-X™ Standard Cell Library. It covers physical specifications, electrical specifications, derating factors, propagation delay calculation, timing constraints, power calculation, and power-rail strapping.

Physical Specifications

Table 1 shows the physical design specifications of this library.

Table 1. Physical Specifications

Drawn Gate Length (µm)	0.18
Layers of Metal	6
Layout Grid (µm)	0.01
Vertical Pin Grid (µm)	0.56
Horizontal Pin Grid (µm)	0.56
Cell Power and Ground Rail Width (µm)	0.8

In this library, all pins are located on the vertical and horizontal pin grids. Most place-and-route tools work more efficiently with all pins on grids, and some tools even require it.

The SAGE-X library also supports designs with six layers of metal. You may need to change the design rules in the technology file, because the top-level metal has a greater minimum width and greater minimum spacing requirement. See "CMOS7RF (CMRF7SF) Design Manual, ES #70P3342" design rule manual. You must define these rules correctly for the place-and-route tool.

Table 2 describes the electrical specifications for this library.

Table 2. Electrical Specifications

Parameter	Minimum	Maximum
DC Supply Voltage (Vdd)	1.62V	1.98V
Junction Temperature	0°C	125°C

Table 3 shows the derating factors for this SAGE-X Standard Cell Library.

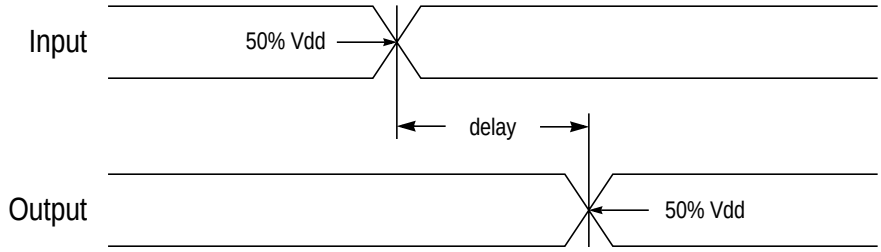
Table 3. Derating Factors

$K_{Process}$ (slow)	1.243
$K_{Process}$ (typical)	1.000 (by definition)
$K_{Process}$ (fast)	0.772
K_{Volt} (1.8V to 1.62V)	-0.747/V
K_{Volt} (1.8V to 1.98V)	-0.533/V
K_{Temp} (25°C to 0°C)	0.00179˚C
K_{Temp} (25°C to 125°C)	0.00173˚C

Propagation Delay and Transition Time

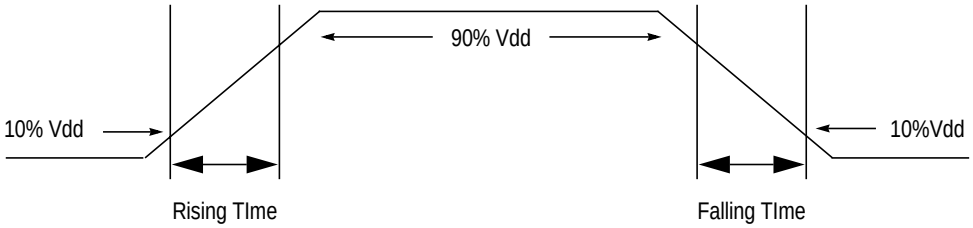
The propagation delay through a cell is the sum of the intrinsic delay, the load-dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing 50% of Vdd and the output crossing 50% of Vdd. Figure 1 illustrates the propagation delay.

Figure 1. Propagation Delay



The transition times (slews) on input and output pins are defined as the time interval between the signal crossing 10% of Vdd and 90% of Vdd. Figure 2 illustrates transition time measurements for rising and falling signals.

Figure 2. Transition Time



Factors that affect propagation delays and transition time include: temperature, supply voltage, process variations, fanout loading, interconnect loading, input-transition time, input-signal polarity, and timing constraints. The timing models provided with this library include the effects of input-transition time on propagation delays. Also, all timing models use a table lookup method to calculate accurate timing. To simplify calculations, the standard cell datasheets provide all timing numbers for an input slew of 0.03ns and a linearized load factor, K_{load}, which is not as accurate as the timing models. All cells have been characterized with a fully populated metal2 (0.56µm horizontal pitch) and metal3 (0.56µm vertical pitch) routing grid across the entire cell layout.

The SAGE-X Standard Cell Library may contain negative propagation delays. Although most third-party verification tools can handle negative propagation delays, some tools will turn negative delays into a zero value.

Derating Factors

Derating factors are coefficients that the typical process characterization data is multiplied by to arrive at timing data that reflects appropriate operating conditions. Table 3 on page 12 provides derating factors for variations in process case, temperature, and voltage.

Derating factors are derived by averaging the performance of many different cells in the library. A particular combination of cells may perform better or worse than indicated by these derating factors.

Delay Calculation

Using the delay data in the datasheets ($t_{intrinsic}$, K_{load}, and C_{load}) and the delay derating factors, the estimated total propagation delay is calculated as such:

$$t_{TPD} = (K_{Process}) \bullet [1+(K_{Volt} \bullet \Delta Vdd)] \bullet [1+(K_{Temp} \bullet \Delta T)] \bullet t_{typical}$$

$$t_{typical} = t_{intrinsic} + (K_{load} \bullet C_{load})$$

where:

t_{TPD} = total propagation delay (ns);

$t_{typical}$ = delay at typical corner—1.8V, 25^{o}C, typical process (ns);

$t_{intrinsic}$ = delay through the cell when there is no output load (ns);

K_{load} = load delay multiplier (ns/pF);

C_{load} = total output load capacitance (pF);

$K_{Process}$ = process derating factor, where process is slow, typical, or fast;

K_{Volt} = voltage derating factor (/V);

ΔVdd = Vdd - 1.8V;

K_{Temp} = temperature derating factor (/^{o}C);

ΔT = junction temperature - 25^{o}C.

Timing Constraints

Timing constraints define minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing constraints include: setup time, hold time, recovery time, and minimum pulse width.

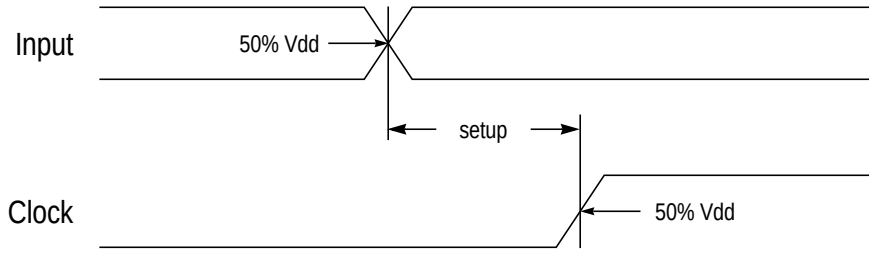
The sequential-cell timing models provided with this library include the effects of input-transition time and data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for 0.03ns data slew and 0.03ns clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process case variations. All cells have been characterized with a fully populated metal2 (0.56µm horizontal pitch) and metal3 (0.56µm vertical pitch) routing grid across the entire cell layout.

Timing constraints can affect propagation delays. The intrinsic delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, and pulse widths). The use of shorter timing constraint intervals may increase delay. Each cell is considered functional as long as the actual delay does not exceed the delay given in the datasheets by more than 10%.

Setup Time

The setup time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%. Setup-constraint values are measured as the interval between the data signal crossing 50% of Vdd and the clock signal crossing 50% of Vdd. For the measurement of setup time, the data input signal is kept stable after the active clock edge for an infinite hold time. Figure 3 illustrates setup time for a positive-edge-triggered sequential cell.

Figure 3. Setup Time

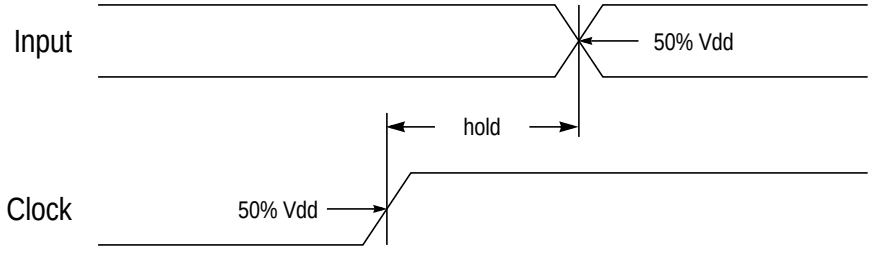


Hold Time

The hold time for a sequential cell is the minimum length of time the data-input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%. Hold-constraint values are measured as the interval between the data signal crossing 50% of Vdd and the clock signal crossing 50% of Vdd. For the measurement of hold time, the data input signal is held stable before the active clock edge for an infinite setup time. Figure 4 illustrates hold time for a positive-edge-triggered sequential cell.

NOTE: Artisan does not incorporate any hold time margins in the Synopsys, TLF, StarDC, or any other timing models. Chip designers should develop a timing methodology to account for chip-level timing inaccuracies inherent to extraction and timing analysis tools.

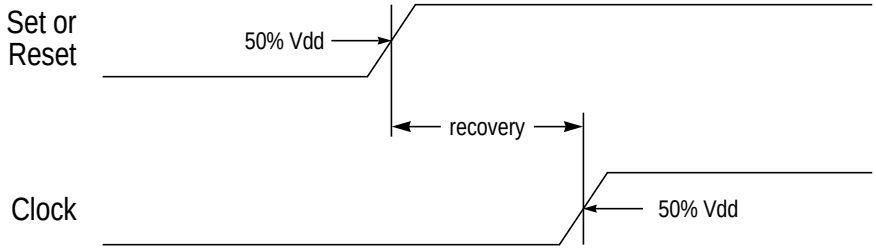
Figure 4. Hold Time



Recovery Time

Recovery time for sequential cells is the minimum length of time that the active-low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the set or reset signal crossing 50% of Vdd and the clock signal crossing 50% of Vdd. For the measurement of recovery time, the set or reset signal is held stable after the active clock edge for an infinite hold time.
Figure 5 illustrates recovery time.

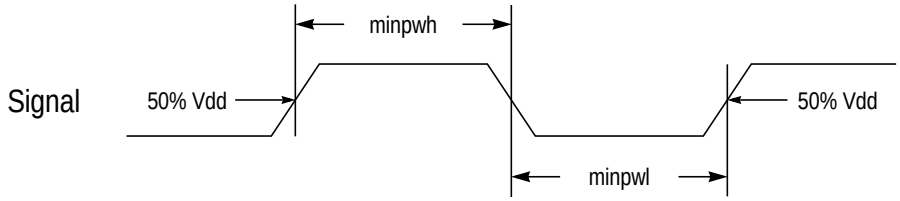
Figure 5. Recovery Time



Minimum Pulse Width

Minimum pulse width is the minimum length of time between the leading and trailing edges of a pulse waveform. Minimum pulse width high (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of Vdd and the falling edge of the signal crossing 50% of Vdd. Minimum pulse width low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of Vdd and the rising edge of the signal crossing 50% of Vdd. Figure 6 illustrates minimum pulse width.

Figure 6. Minimum Pulse Width



Minimum pulse width is defined as 0.520579ns for all set/reset pins (SN, RN) and 0.2145ns for all clock pins (G, GN, CK, CKN). These are the largest minimum pulse widths measured from all the cells in the library. An input pulse of shorter duration will produce unpredictable results.

Power Dissipation

The SAGE-X Standard Cell Library is designed to dissipate only AC power, except for the small reverse-bias leakage currents which are normally present in all CMOS circuits.

The power dissipation internal to a cell when a given input switches is primarily dependent upon the cell design itself. The power dissipation of a complete design, or part of a design, using cells from the library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

The SAGE-X library datasheets contain both an AC power table which documents the internal energy consumption of each cell and a pin capacitance table which gives input-pin capacitance data used to compute output loading. This information, coupled with design-specific information, can be used to estimate the total power dissipation of a cell within a design.

The AC power tables specify the amount of energy consumed within a cell (µW/MHz) when the corresponding pin changes state at 25^{o}C, 1.8V, and typical process. The energy data in the tables were measured for an input slew of 0.03ns and no loading at the outputs.

For combinatorial cells, energy values are provided for only input pins. The energy value for each input pin is the average of energies associated with the input transitions which result in an output transition.

For sequential cells, the energy associated with each input pin is the average energy of those input transitions which *do not* result in an output transition. The energy associated with the output pin of a sequential cell is the average energy of all cases where an output transition is the result of a clock-input transition, minus the energy associated with the clock input pin. In the event that a sequential cell has multiple outputs, all output energy data will be associated with only one output pin.

Power Calculation

Power dissipation is dependent upon the power-supply voltage, frequency of operation, internal capacitance, and output load. The power dissipated by each cell is:

$$P_{avg} = \sum_{n=1}^{x} (E_{in} \bullet f_{in}) + \sum_{n=1}^{y} \left(C_{on} \bullet Vdd^2 \bullet \frac{1}{2} f_{on} \right) + E_{os} \bullet f_{o1}$$

where:

P_{avg} = average power (µW);

x = number of input pins;

E_{in} = energy associated with the *n*th input pin (µW/MHz);

f_{in} = frequency at which the *n*th input pin changes state during the normal operation of the design (MHz);

y = number of output pins;

C_{on} = external capacitive loading on the *n*th output pin, including the capacitance of each input pin connected to the output driver, plus the route wire capacitance, actual or estimated (pF);

Vdd = operating voltage = 1.8V;

f_{on} = frequency at which the *n*th output pin changes state during the normal operation of the design (MHz);

E_{os} = energy associated with the output pin for sequential cells only (µW/MHz).

The switching frequency of inputs and outputs of a particular cell in a design can be obtained from a gate-level logic simulator (e.g. Verilog) by applying typical input stimuli and measuring the activity on each node of interest. The total average power for the design can be computed by adding the average power for each cell.

EXAMPLE: Calculating Power for a DFFXL Cell

For this exercise, assume that a DFFXL cell has clock switching at 133MHz, input and output pins switching at 20MHz, and an external capacitive loading on the output pin of 0.02pF. Using the AC Power table provided in the sample DFF datasheet on page 28, the power dissipated by the DFFXL can be calculated by using the following equation:

$$P_{avg} = \sum_{n=1}^{x} (E_{in} \bullet f_{in}) + \sum_{n=1}^{y} \left(C_{on} \bullet Vdd^2 \bullet \frac{1}{2} f_{on} \right) + E_{os} \bullet f_{o1}$$

Given:

x = 2;

E_{i1} = 0.0056 µW/MHz;

E_{i2} = 0.0063 µW/MHz;

f_{i1} = 20 MHz;

f_{i2} = 133 MHz;

y = 2;

C_{o1} = 0.02 pF;

C_{o2} = 0.02 pF;

Vdd= 1.0V;

f_{o1} = 20 MHz;

f_{o2} = 20 MHz;

E_{os} = 0.0060 µW/MHz,

we have:

$$P_{avg} = \sum_{n=1}^{2} (E_{in} \bullet f_{in}) + \sum_{n=1}^{2} \left(C_{on} \bullet Vdd^2 \bullet \frac{1}{2} f_{on} \right) + E_{os} \bullet f_{o1}$$

$$P_{avg} = (E_{i1} \bullet f_{i1}) + (E_{i2} \bullet f_{i2}) \left(C_{o1} \bullet VDD^2 \bullet \frac{1}{2} f_{o1} \right) + \left(C_{o2} \bullet VDD^2 \bullet \frac{1}{2} f_{o2} \right) + (E_{os} \bullet f_{o1})$$

$$P_{avg} = (0.0056 \bullet 20) + (0.0063 \bullet 133) + \left(0.02 \bullet 1.0 \bullet \frac{1}{2}(20)\right) + \left(0.02 \bullet 1.0 \bullet \frac{1}{2}(20)\right) + (0.0060 \bullet 20)$$

$$P_{avg} = 1.46 \ \mu W$$

Power-Rail Strapping

You must determine the required amount of vertical power-rail strapping to satisfy all requirements imposed by the design methodology for a given design. Power-rail strapping should be sized small enough to optimize standard cell height and maximize router efficiency, yet it must be large enough to provide sufficient power to the cells.

The guidelines below provide a rough estimate with many simplifying assumptions. For a given module design, you can estimate the amount of vertical power-rail strapping that is required to fulfill electromigration requirements.

Given:

I_{avg} = total average current for the module, calculated from previous section (mA);

w_{m1} = VSS/VDD metal1 wire width (μm), see Physical Specifications;

r = number of rows in module;

d_{m1} = maximum metal1 current density allowed for the process (mA/μm);

d_{m2} = maximum metal2 current density allowed for the process (mA/μm);

I_{m1} = maximum current that can be supported by all horizontal metal1 wires (mA);

I_{strap} = total current that must be supported by the vertical metal2 strapping (mA);

w_{m2} = metal2 wire width required for vertical strapping (μm);

c = minimum number of metal2 straps;

we have:

$I_{m1} = w_{m1} \bullet r \bullet 2 \bullet d_{m1}$,

where multiplying by 2 assumes metal1 wires are supplied from both ends;

$I_{strap} = \frac{(I_{avg} - I_{m1})}{2}$,

where dividing by 2 assumes the metal2 vertical strap wires are supplied from both ends;

$w_{m2} = \frac{I_{strap}}{d_{m2}}$,

It is recommended that the metal2 wire width, w_{m2}, be divided into c equal portions which are spaced equidistant across the module, where

$c = \frac{I_{avg}}{I_{m1}}$, rounded up to the next integer.

The same consideration must be given to the number of vias used to connect the metal1 and metal2 straps.

Adding Routing Channels

In the SAGE-X Standard Cell Library, each cell is designed with a uniform cell height of 5.04µm (i.e., 9 tracks tall with 0.56µm per track). The cell layouts allow neighboring rows of cells to share common power or ground rails when cells abut each other at the top and bottom edges of the cell bounding box. The sea-of-cells layout with no channels between rows will usually yield the minimum area. In case of extremely congested areas, you may want to separate some rows of cells to increase the number of routing channels within a particular layout region. Because geometries must overlap cell boundaries, a particular spacing between the rows may result in DRC violations for layer spacing. It is recommended that you do not use spacings that cause DRC violations. If these spacings must be used, the DRC violations must be fixed manually by filling the void between the rows with the appropriate layer(s).

Table 4 indicates which DRC violations to expect and how to correct them for a separation between rows of cells.

Table 4. Correcting DRC Violations

Row Separation in Number of Grids	Expected DRC Violations	Action to Correct DRC Violations
0 (Rows Abut)	None	None
1	PP space < 0.34µm	Draw NWELL layer between rows to merge NWELL regions above and below row separation.
2	NWELL space < 0.84µm M1 space < 0.2µm	Draw NWELL and Metal1 layers between rows to merge NWELL and Metal1 regions above and below row separation.
3	NWELL space < 0.84µm	Draw NWELL layer between rows to merge NWELL regions above and below row separation.
4	None	None
5 or more	None	None

IBM Top Metal Layer Parameters

In order to efficiently utilize Artisan Components products with IBM designs, consideration must be given to IBM's approach to metal layer functionality. The information below is provided as a guide to details about IBM-specific top metal layer options.

Table 5 shows the subdirectories and files to be used to achieve compatibility with the supported IBM CMRF7SF top layer metal options.

Table 5. CMRF7SF SAGE-X Process Files and Subdirectories

Total # of Metal Layers Used in Chip	IBM Top Metal Layer	Use This File from aci/sc-x/synopsys	Use These Files from aci/sc-x/apollo	Use These Files from aci/sc-x/LEF
6	ML	ibm18_6lm_ml.plib	gds2InLayer_6lm_ml.map	ibm18_6lm_ml.lef
			gds2OutLayer_6lm_ml.map	ibm18_6lm_ml_antenna.lef

Special Cells

This section discusses special cells in the SAGE-X Standard Cell Library.

Antenna-Fix Cell

The library contains an antenna-fix cell which must be inserted manually. However, most place and route tools will indicate which nets require the antenna-fix cell. The IBM antenna effect prevention guideline, "CMOS7RF (CMRF7SF) Design Manual, ES #70P3342," specifies a maximum wire length. During place and route, the router may connect wires to the input gates of cells that are longer than the maximum length allowable by the guideline. The antenna cell can be used in this case to add an optional diode on the net close to the input gates which do not meet the guideline. Pin A on the antenna cell connects to a diode, reverse biased to ground. A diode can be added to either P or N.

Fill Cells

The library contains several FILL cells: FILL1, FILL2, FILL4, FILL8, FILL16, FILL32, FILL64. The number appended to "FILL" in the cell name denotes the width of the cell in tracks.

During place and route, the FILL cells are used to connect power and ground rails across an area containing no cells. The FILL cells are also used to ensure gaps do not occur between well or implant layers which could cause design rule violations. Using wider cells where appropriate reduces the size of the layout database.

Low-Power (XL) Cells

The library contains a wide variety of cells, denoted by an "XL" suffix in the cell name, that are designed specifically for low-power applications. Input capacitance for the XL cells is much lower than that for corresponding X1 (1x drive strength) cells. Because XL cells have been designed for the sole purpose of reducing power consumption, output rise and fall times for these cells may not be equal, and due to the low-drive capability of the XL cells, these cells are not intended for use in critical timing paths, or to drive heavily loaded nets.

TIEHI/LO Cells

The library contains a TIEHI cell and a TIELO cell. The outputs of the TIEHI and TIELO cells are driven through diffusion to provide isolation from the power and ground rails for better ESD protection. The standard cell abstract methodology assumes that the TIEHI and TIELO cells are used to tie off any inputs to power and ground. If these cells are not used and the router is allowed to drop vias on the power rail, DRC errors or shorts may result.

Delay Cells

The library contains delay cells that have the same width. These delay cells allow you to adjust a given delay path with a simple cell substitution after place and route.

Reading the Standard Cell Datasheet

Please refer to the sample datasheet for DFF on pages 28 and 29 for the arrangement of each of the following datasheet sections.

NOTE: This datasheet contains sample characterization values.

1. Cell Name

The cell name field contains the cell name. The datasheets are presented alphabetically by cell name.

2. Cell Description

The cell description gives the function of the cell. When applicable, the equation(s) for the output pins are provided.

3. Functions

The function table gives all possible combinations of input and output signals for the cell. Table 6 defines the symbols used in datasheet function tables.

Table 6. Functions Key

Symbol	Description
0	Logic Low
1	Logic High
¯_	High to Low Transition
_/¯	Low to High Transition
x	Don't Care
IL	Illegal/Undefined
Z	High Impedance

4. Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

5. Cell Size

This cell size table gives the height and width (µm) for each drive strength of the cell.

6. Functional Schematic

The functional schematic provides a functional representation of the cell.

7. Drive Strength

The drive strength of each cell is indicated by an "X" followed by the unit strength.

8. AC Power

The AC power table shows the amount of energy consumed (µW/MHz) within the cell when the corresponding pin changes state. The energy data for each drive strength of the cell in the sample DFF datasheet are calculated at 25°C, 1.0V, typical process, input slew of 0.03ns, and no external load at the output pins.

9. Delay

The delay table shows the intrinsic delay (ns) which is the delay through the cell when there is no load on the output, and the load multiplier for load dependent delay, K_{load} (ns/pF). The delays and load multiplier for each drive strength of the cell in the sample DFF datasheet are calculated at 25°C, 1.0V, typical process, and input slew of 0.03ns.

10. Timing Constraints

The timing constraints table in the sample DFF datasheet shows the timing conditions (ns) required at 25°C, 1.0V, and typical process to maintain proper functionality. Setup constraint values are measured for 0.03ns data slew and 0.03ns clock slew. Hold constraint values are measured for 0.03ns data slew and 0.03ns clock slew. Minimum pulse width is defined to be 0.520579ns for all set/reset pins and 0.2145ns for all clock pins. These are the largest minimum pulse widths measured from all the cells in the library.

11. Pin Capacitance

The pin capacitance table shows the typical loading at the input pins of the cell (pF) for each drive strength of the cell.

▼ *This datasheet contains sample characterization values.* ▼

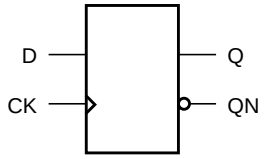
DFF

(1)

(2) **Cell Description**

The DFF cell is a positive-edge-triggered, static D-type flip-flop.

(4) **Logic Symbol**



(3) **Function**

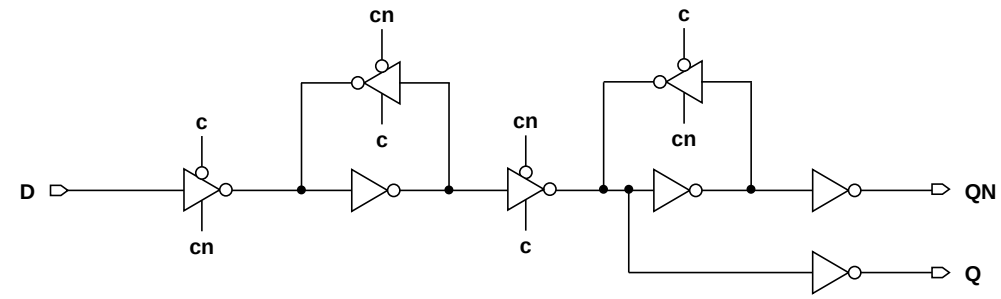
D	CK	Q[n+1]	QN[n+1]
0	↑	0	1
1	↑	1	0
x	↓	Q[n]	QN[n]

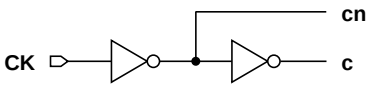
(5) **Cell Size**

Drive Strength	Height (µm)	Width (µm)
DFFXL	3.69	7.36
DFFX1	3.69	7.36
DFFX2	3.69	8.74
DFFX4	3.69	11.50

(7)

(6) **Functional Schematic**





▼ *This datasheet contains sample characterization values.* ▼

DFF

8

AC Power

7

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
D	0.0056	0.0063	0.0081	0.0133
CK	0.0063	0.0068	0.0087	0.0128
Q	0.0060	0.0080	0.0124	0.0223

11

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0013	0.0013	0.0015	0.0023
CK	0.0015	0.0019	0.0022	0.0035

9

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.1662	0.1427	0.1287	0.1105	7.8830	4.2853	1.9344	0.9666
CK → Q↓	0.1357	0.1098	0.0983	0.0920	4.3787	2.4148	1.1764	0.5884
CK → QN↑	0.1828	0.1515	0.1342	0.1292	7.8631	4.2693	1.9226	0.9616
CK → QN↓	0.2156	0.1947	0.1789	0.1547	3.9375	2.1923	1.1262	0.5569

10

Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → CK	0.0469	0.0547	0.0391	0.0391
	setup↓ → CK	0.1094	0.1250	0.1094	0.1016
	hold↑ → CK	-0.0312	-0.0312	-0.0234	-0.0234
	hold↓ → CK	-0.0312	-0.0469	-0.0312	-0.0312
CK	minpwh	0.0933	0.0835	0.0738	0.0641
	minpwl	0.1418	0.1224	0.1127	0.0835

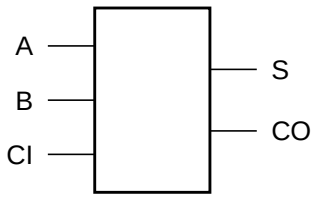
Cell Description

The ADDF cell provides the arithmetic sum (S) and carry out (CO) of two operands (A, B) with carry in (CI). The two outputs (S, CO) are represented by the logic equations:

$$S = (A \oplus B \oplus CI)$$

$$CO = (A \oplus B) \bullet CI + (A \bullet B)$$

Logic Symbol



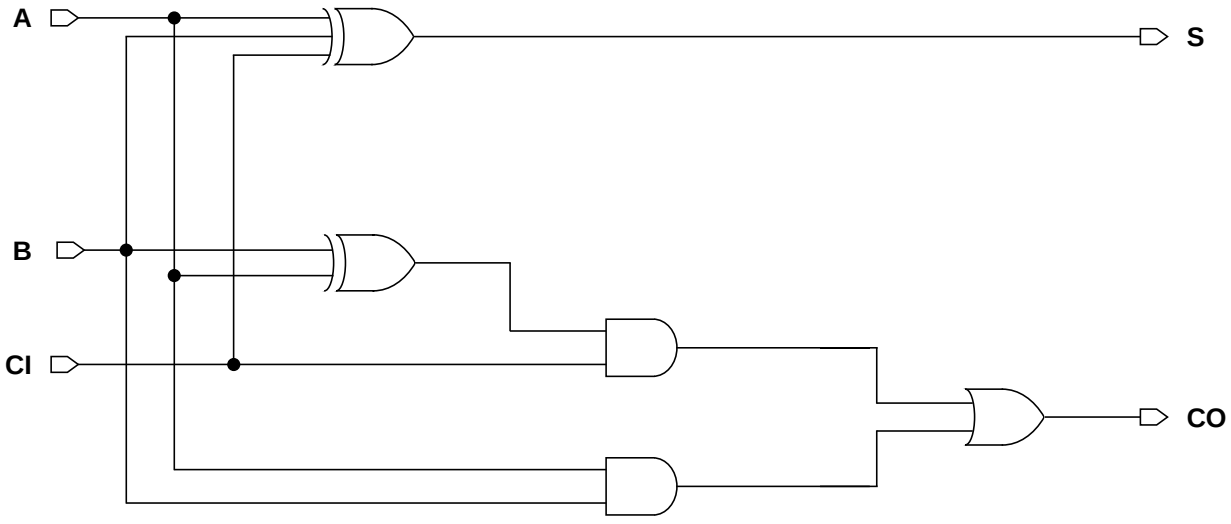
Functions

CI	A	B	S	CO
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Cell Size

Drive Strength	Height (µm)	Width (µm)
ADDFXL	5.04	12.88
ADDFX1	5.04	12.88
ADDFX2	5.04	12.88
ADDFX4	5.04	14.00

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A	0.1174	0.1052	0.1267	0.1865
B	0.1464	0.1358	0.1743	0.2507
CI	0.0669	0.0574	0.0810	0.1413

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A	0.0040	0.0058	0.0058	0.0058
B	0.0039	0.0058	0.0058	0.0058
CI	0.0068	0.0058	0.0058	0.0059

Delays at 25^{o}C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A → S↑	0.2609	0.1827	0.1959	0.2269	4.5290	3.9959	2.0280	1.0168
A → S↓	0.2933	0.2411	0.2636	0.3062	2.9165	2.3820	1.2281	0.6372
B → S↑	0.3060	0.2161	0.2290	0.2532	4.5395	3.9965	2.0303	1.0185
B → S↓	0.3507	0.2731	0.2959	0.3383	2.9354	2.3819	1.2280	0.6372
CI → S↑	0.1725	0.1438	0.1630	0.2039	4.5101	3.9929	2.0287	1.0178
CI → S↓	0.1316	0.1279	0.1490	0.1885	2.9066	2.3942	1.2400	0.6477
A → CO↑	0.2760	0.2204	0.2400	0.2805	4.4611	3.9767	2.0192	1.0112
A → CO↓	0.2861	0.2202	0.2414	0.2790	2.7389	2.3214	1.1987	0.6208
B → CO↑	0.3153	0.2519	0.2717	0.3119	4.4567	3.9762	2.0190	1.0111
B → CO↓	0.3284	0.2401	0.2582	0.2897	2.6228	2.2849	1.1738	0.6005
CI → CO↑	0.1390	0.1165	0.1349	0.1758	4.5013	3.9879	2.0259	1.0154
CI → CO↓	0.1830	0.1523	0.1728	0.2110	2.7833	2.3375	1.2064	0.6247

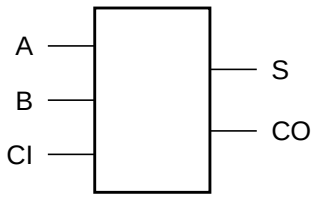
Cell Description

The ADDFH cell is a high-speed cell providing the arithmetic sum (S) and carry out (CO) of two operands (A, B) with carry in (CI). The two outputs (S, CO) are represented by the logic equations:

$$S = (A \oplus B \oplus CI)$$

$$CO = (A \oplus B) \bullet CI + (A \bullet B)$$

Logic Symbol



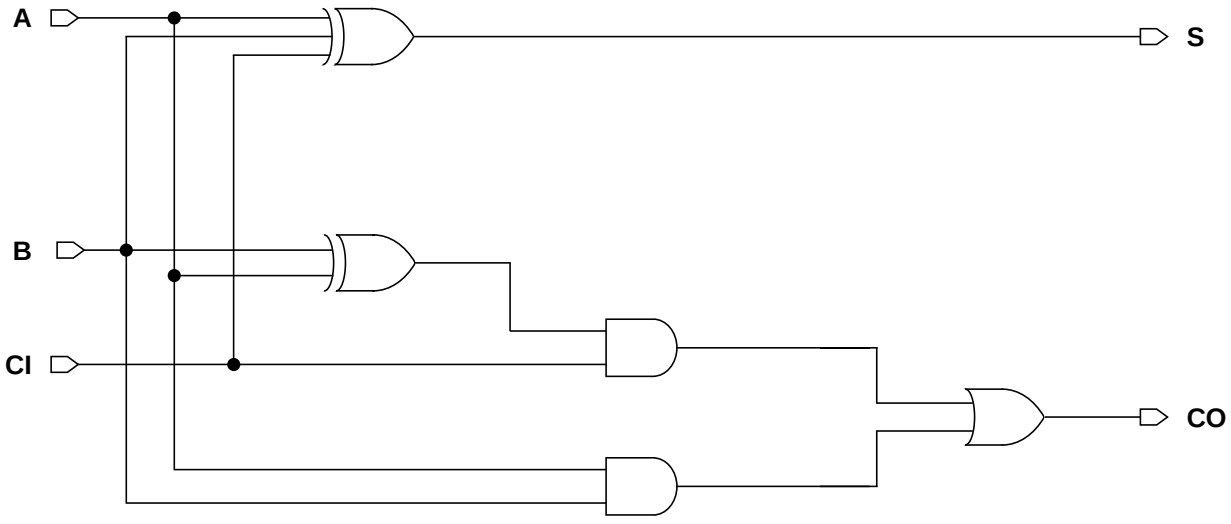
Functions

CI	A	B	S	CO
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Cell Size

Drive Strength	Height (µm)	Width (µm)
ADDFHXL	5.04	14.00
ADDFHX1	5.04	14.56
ADDFHX2	5.04	21.28
ADDFHX4	5.04	21.84

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A	0.1198	0.1278	0.2294	0.2647
B	0.1054	0.1150	0.2026	0.2336
CI	0.0677	0.0662	0.1118	0.1450

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A	0.0041	0.0053	0.0089	0.0088
B	0.0087	0.0121	0.0212	0.0204
CI	0.0023	0.0036	0.0065	0.0062

Delays at 25^{o}C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A → S↑	0.2885	0.1980	0.1981	0.2038	4.4771	3.9815	2.0201	1.0114
A → S↓	0.2765	0.2179	0.2146	0.2258	2.6799	2.3022	1.1645	0.5902
B → S↑	0.2029	0.1481	0.1333	0.1461	4.5005	3.9852	2.0217	1.0125
B → S↓	0.2494	0.1762	0.1579	0.1753	2.6603	2.3019	1.1643	0.5903
CI → S↑	0.2587	0.1630	0.1394	0.1602	4.4879	3.9851	2.0217	1.0125
CI → S↓	0.2275	0.1624	0.1383	0.1614	2.6828	2.3070	1.1666	0.5914
A → CO↑	0.2938	0.1999	0.1969	0.2037	4.4889	3.9809	2.0202	1.0114
A → CO↓	0.2921	0.2148	0.2107	0.2231	2.7367	2.2986	1.1630	0.5884
B → CO↑	0.1790	0.1303	0.1144	0.1320	4.5101	3.9824	2.0210	1.0117
B → CO↓	0.2636	0.1664	0.1468	0.1650	2.7552	2.2827	1.1579	0.5853
CI → CO↑	0.1238	0.0917	0.0770	0.0901	4.5086	3.9858	2.0217	1.0124
CI → CO↓	0.1784	0.1297	0.1098	0.1264	2.8463	2.3193	1.1708	0.5924

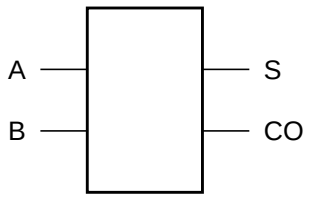
Cell Description

The ADDH cell provides the arithmetic sum (S) and carry out (CO) of two operands (A, B). The two outputs (S, CO) are represented by the logic equations:

$S = (\bar{A} \bullet B) + (A \bullet \bar{B})$

$CO = A \bullet B$

Logic Symbol



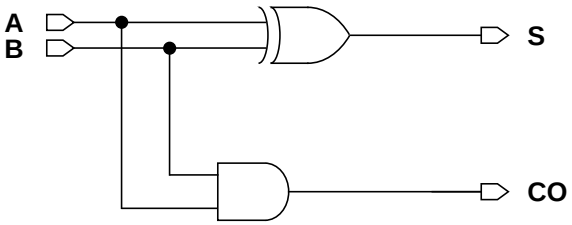
Functions

A	B	S	CO
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Cell Size

Drive Strength	Height (µm)	Width (µm)
ADDHXL	5.04	7.28
ADDHX1	5.04	7.84
ADDHX2	5.04	10.64
ADDHX4	5.04	16.24

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A	0.0639	0.0991	0.1761	0.3241
B	0.0472	0.0555	0.0950	0.1756

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A	0.0047	0.0087	0.0168	0.0320
B	0.0061	0.0078	0.0103	0.0191

Delays at 25°C, 1.8V, Typical Process

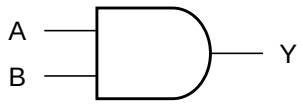
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A → S↑	0.1058	0.0727	0.0634	0.0597	5.0396	2.4686	1.2245	0.6096
A → S↓	0.1098	0.0774	0.0685	0.0640	2.9293	1.5264	0.7534	0.3738
B → S↑	0.0516	0.0476	0.0421	0.0380	4.9964	2.4582	1.2188	0.6069
B → S↓	0.0614	0.0612	0.0542	0.0491	2.7583	1.4622	0.7260	0.3615
A → CO↑	0.0612	0.0722	0.0660	0.0615	4.4717	3.9828	2.0213	1.0110
A → CO↓	0.0783	0.0942	0.0855	0.0813	2.7557	2.2700	1.1538	0.5772
B → CO↑	0.0589	0.0713	0.0637	0.0587	4.4723	3.9829	2.0214	1.0110
B → CO↓	0.0705	0.0880	0.0784	0.0735	2.7500	2.2665	1.1529	0.5767

Cell Description

The AND2 cell provides the logical AND of two inputs (A, B). The output (Y) is represented by the logic equation:

$Y = (A \bullet B)$

Logic Symbol



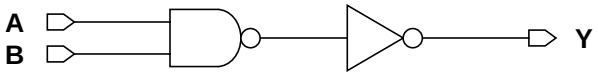
Functions

A	B	Y
0	x	0
x	0	0
1	1	1

Cell Size

Drive Strength	Height (µm)	Width (µm)
AND2XL	5.04	2.24
AND2X1	5.04	2.24
AND2X2	5.04	2.80
AND2X4	5.04	3.36

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A	0.0175	0.0182	0.0272	0.0482
B	0.0198	0.0204	0.0307	0.0549

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A	0.0021	0.0021	0.0029	0.0048
B	0.0021	0.0021	0.0029	0.0050

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)			
	XL	X1	X2	X4
A → Y↑	0.0730	0.0750	0.0626	0.0574
A → Y↓	0.0884	0.0931	0.0763	0.0718
B → Y↑	0.0776	0.0795	0.0659	0.0608
B → Y↓	0.0984	0.1033	0.0847	0.0805

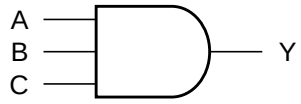
Description	K_{load} (ns/pF)			
	XL	X1	X2	X4
A → Y↑	4.4807	3.9849	2.0210	1.0110
A → Y↓	2.5315	2.2718	1.1516	0.5764
B → Y↑	4.4804	3.9848	2.0209	1.0110
B → Y↓	2.5385	2.2750	1.1528	0.5771

Cell Description

The AND3 cell provides the logical AND of three inputs (A, B, C). The output (Y) is represented by the logic equation:

$Y = (A \bullet B \bullet C)$

Logic Symbol



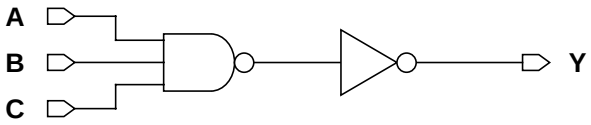
Functions

A	B	C	Y
0	x	x	0
x	0	x	0
x	x	0	0
1	1	1	1

Cell Size

Drive Strength	Height (µm)	Width (µm)
AND3XL	5.04	3.36
AND3X1	5.04	3.36
AND3X2	5.04	3.36
AND3X4	5.04	3.92

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A	0.0188	0.0188	0.0298	0.0497
B	0.0207	0.0213	0.0341	0.0567
C	0.0231	0.0235	0.0381	0.0647

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A	0.0023	0.0022	0.0030	0.0047
B	0.0022	0.0023	0.0031	0.0046
C	0.0023	0.0021	0.0032	0.0047

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)			
	XL	X1	X2	X4
A → Y↑	0.1030	0.0976	0.0776	0.0774
A → Y↓	0.0895	0.1083	0.0877	0.0825
B → Y↑	0.1121	0.1046	0.0834	0.0832
B → Y↓	0.0969	0.1192	0.0979	0.0915
C → Y↑	0.1160	0.1083	0.0876	0.0870
C → Y↓	0.1036	0.1284	0.1080	0.1002

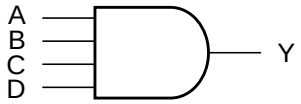
Description	K_{load} (ns/pF)			
	XL	X1	X2	X4
A → Y↑	4.5025	3.9920	2.0242	1.0131
A → Y↓	2.5317	2.2827	1.1555	0.5782
B → Y↑	4.5025	3.9920	2.0242	1.0131
B → Y↓	2.5372	2.2863	1.1571	0.5791
C → Y↑	4.5026	3.9920	2.0241	1.0130
C → Y↓	2.5443	2.2906	1.1592	0.5801

Cell Description

The AND4 cell provides the logical AND of four inputs (A, B, C, D). The output (Y) is represented by the logic equation:

$$Y = (A \bullet B \bullet C \bullet D)$$

Logic Symbol



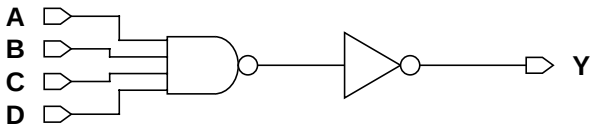
Functions

A	B	C	D	Y
0	x	x	x	0
x	0	x	x	0
x	x	0	x	0
x	x	x	0	0
1	1	1	1	1

Cell Size

Drive Strength	Height (µm)	Width (µm)
AND4XL	5.04	3.92
AND4X1	5.04	3.92
AND4X2	5.04	3.92
AND4X4	5.04	6.16

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A	0.0191	0.0191	0.0310	0.0552
B	0.0208	0.0216	0.0354	0.0649
C	0.0228	0.0242	0.0407	0.0750
D	0.0244	0.0264	0.0455	0.0825

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A	0.0024	0.0022	0.0032	0.0056
B	0.0023	0.0021	0.0032	0.0061
C	0.0024	0.0021	0.0033	0.0072
D	0.0023	0.0023	0.0033	0.0076

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)			
	XL	X1	X2	X4
A → Y↑	0.1241	0.1089	0.0869	0.0817
A → Y↓	0.0851	0.1124	0.0924	0.0884
B → Y↑	0.1351	0.1178	0.0954	0.0905
B → Y↓	0.0916	0.1240	0.1042	0.1007
C → Y↑	0.1425	0.1243	0.1013	0.0973
C → Y↓	0.0984	0.1349	0.1148	0.1123
D → Y↑	0.1468	0.1286	0.1059	0.1016
D → Y↓	0.1040	0.1451	0.1257	0.1227

Delays at 25°C, 1.8V, Typical Process

Description	K_{load} (ns/pF)			
	XL	X1	X2	X4
A → Y↑	4.5334	4.0003	2.0273	1.0141
A → Y↓	2.5285	2.2887	1.1571	0.5790
B → Y↑	4.5335	4.0003	2.0273	1.0141
B → Y↓	2.5341	2.2931	1.1590	0.5801
C → Y↑	4.5336	4.0003	2.0273	1.0141
C → Y↓	2.5408	2.2982	1.1614	0.5813
D → Y↑	4.5330	4.0000	2.0273	1.0141
D → Y↓	2.5499	2.3045	1.1646	0.5829

Cell Description

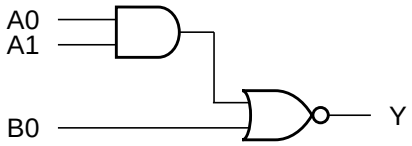
The AOI21 cell provides the logical inverted OR of one AND group and an additional input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 \bullet A1) + B0}$$

Functions

A0	A1	B0	Y
0	x	0	1
x	0	0	1
x	x	1	0
1	1	x	0

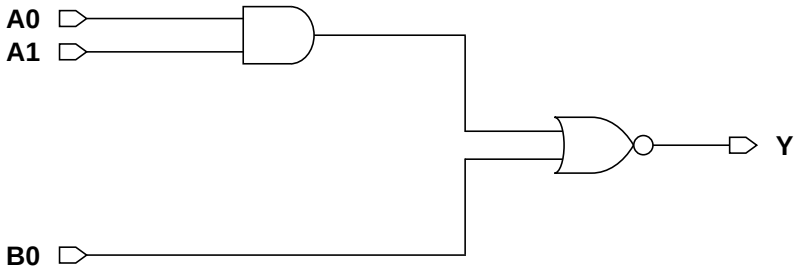
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
AOI21XL	5.04	2.80
AOI21X1	5.04	2.80
AOI21X2	5.04	4.48
AOI21X4	5.04	6.16

Functional Schematic



AC Power

Pin	Power (μW/MHz)			
	XL	X1	X2	X4
A0	0.0200	0.0200	0.0390	0.0730
A1	0.0235	0.0235	0.0477	0.0878
B0	0.0192	0.0192	0.0379	0.0698

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0039	0.0039	0.0079	0.0144
A1	0.0037	0.0037	0.0073	0.0145
B0	0.0037	0.0037	0.0067	0.0130

Delays at 25^{o}C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.0510	0.0514	0.0503	0.0469	5.7053	5.6954	2.7821	1.4060
A0 → Y↓	0.0271	0.0277	0.0276	0.0259	2.7445	2.7335	1.3676	0.6877
A1 → Y↑	0.0605	0.0607	0.0590	0.0564	5.6967	5.6916	2.7796	1.4052
A1 → Y↓	0.0316	0.0322	0.0320	0.0307	2.7525	2.7376	1.3696	0.6887
B0 → Y↑	0.0452	0.0457	0.0420	0.0416	5.7063	5.6960	2.7813	1.4060
B0 → Y↓	0.0189	0.0185	0.0175	0.0166	2.2354	2.2379	1.1408	0.5460

Cell Description

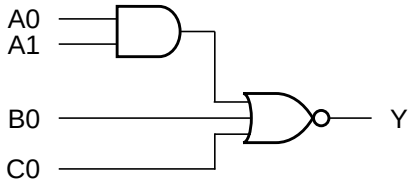
The AOI211 cell provides the logical inverted OR of one AND group and two additional inputs. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 \bullet A1) + B0 + C0}$$

Functions

A0	A1	B0	C0	Y
0	x	0	0	1
x	0	0	0	1
x	x	x	1	0
x	x	1	x	0
1	1	x	x	0

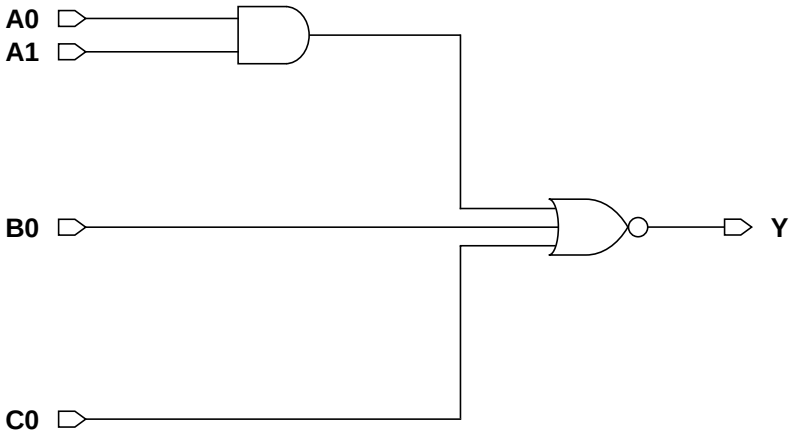
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
AOI211XL	5.04	3.36
AOI211X1	5.04	3.36
AOI211X2	5.04	5.60
AOI211X4	5.04	5.60

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A0	0.0284	0.0297	0.0611	0.0744
A1	0.0324	0.0336	0.0698	0.0778
B0	0.0216	0.0234	0.0471	0.0699
C0	0.0247	0.0276	0.0544	0.0760

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0040	0.0046	0.0085	0.0032
A1	0.0039	0.0044	0.0079	0.0031
B0	0.0039	0.0042	0.0074	0.0031
C0	0.0036	0.0039	0.0084	0.0030

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.0865	0.0830	0.0831	0.2171	7.4469	6.7745	3.4163	0.9779
A0 → Y↓	0.0384	0.0386	0.0379	0.1485	3.0826	2.7579	1.3791	0.5762
A1 → Y↑	0.0976	0.0943	0.0938	0.2297	7.4373	6.7699	3.4139	0.9779
A1 → Y↓	0.0436	0.0440	0.0429	0.1539	3.0836	2.7592	1.3798	0.5762
B0 → Y↑	0.0604	0.0607	0.0582	0.1943	7.4501	6.7756	3.4157	0.9779
B0 → Y↓	0.0233	0.0225	0.0218	0.1234	2.4496	2.2381	1.1405	0.5759
C0 → Y↑	0.0790	0.0783	0.0798	0.2120	7.4419	6.7718	3.4156	0.9779
C0 → Y↓	0.0279	0.0279	0.0286	0.1301	2.4607	2.2406	1.1422	0.5760

Cell Description

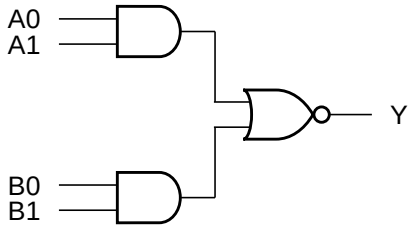
The AOI22 cell provides the logical inverted OR of two AND groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 \bullet A1) + (B0 \bullet B1)}$$

Functions

A0	A1	B0	B1	Y
0	x	0	x	1
0	x	x	0	1
x	0	0	x	1
x	0	x	0	1
x	x	1	1	0
1	1	x	x	0

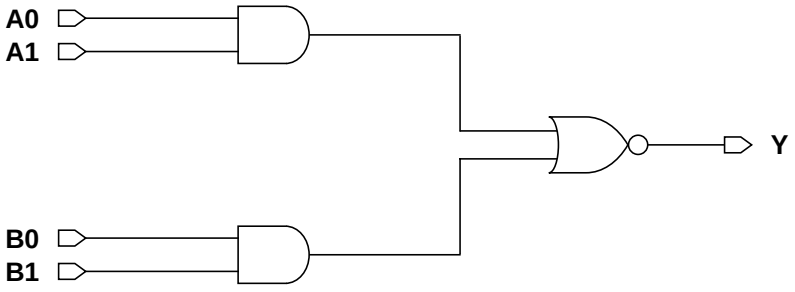
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
AOI22XL	5.04	3.36
AOI22X1	5.04	3.36
AOI22X2	5.04	5.60
AOI22X4	5.04	8.40

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A0	0.0213	0.0213	0.0415	0.0851
A1	0.0253	0.0253	0.0498	0.1006
B0	0.0267	0.0267	0.0527	0.1075
B1	0.0315	0.0315	0.0620	0.1262

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0039	0.0039	0.0074	0.0150
A1	0.0039	0.0039	0.0081	0.0152
B0	0.0037	0.0037	0.0073	0.0150
B1	0.0036	0.0036	0.0076	0.0150

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.0502	0.0506	0.0487	0.0493	5.8055	5.7940	2.7820	1.3738
A0 → Y↓	0.0233	0.0236	0.0233	0.0238	2.7313	2.7270	1.3635	0.6863
A1 → Y↑	0.0608	0.0610	0.0586	0.0586	5.7997	5.7915	2.7807	1.3731
A1 → Y↓	0.0287	0.0291	0.0286	0.0290	2.7400	2.7311	1.3656	0.6873
B0 → Y↑	0.0754	0.0758	0.0704	0.0706	5.8025	5.7927	2.7813	1.3736
B0 → Y↓	0.0376	0.0383	0.0372	0.0379	2.7468	2.7348	1.3665	0.6876
B1 → Y↑	0.0848	0.0850	0.0796	0.0799	5.7945	5.7892	2.7798	1.3729
B1 → Y↓	0.0421	0.0428	0.0419	0.0428	2.7547	2.7387	1.3686	0.6887

Cell Description

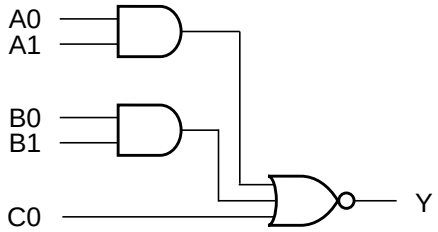
The AOI221 cell provides the logical inverted OR of two AND groups and a third input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 \bullet A1) + (B0 \bullet B1) + C0}$$

Functions

A0	A1	B0	B1	C0	Y
0	x	0	x	0	1
0	x	x	0	0	1
x	0	0	x	0	1
x	0	x	0	0	1
x	x	x	x	1	0
x	x	1	1	x	0
1	1	x	x	x	0

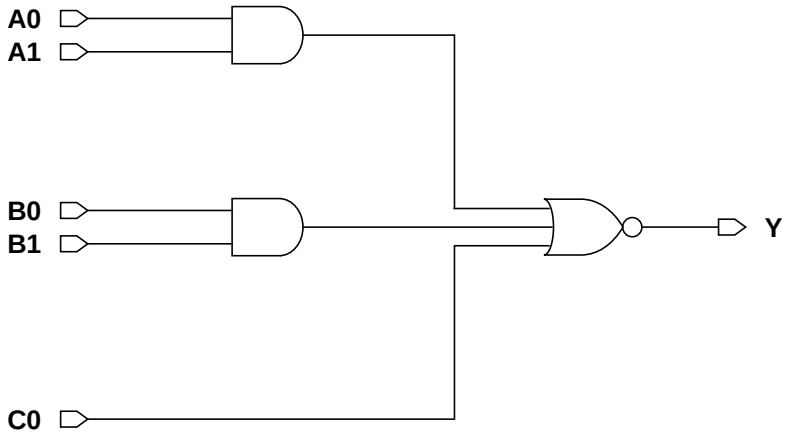
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
AOI221XL	5.04	4.48
AOI221X1	5.04	4.48
AOI221X2	5.04	7.28
AOI221X4	5.04	7.28

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A0	0.0293	0.0301	0.0594	0.0704
A1	0.0334	0.0341	0.0684	0.0737
B0	0.0371	0.0382	0.0759	0.0762
B1	0.0412	0.0423	0.0848	0.0798
C0	0.0277	0.0281	0.0553	0.0705

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0042	0.0043	0.0081	0.0027
A1	0.0042	0.0044	0.0085	0.0029
B0	0.0041	0.0042	0.0080	0.0028
B1	0.0040	0.0041	0.0085	0.0028
C0	0.0039	0.0041	0.0079	0.0028

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.0912	0.0888	0.0873	0.2235	6.9664	6.5271	3.3041	1.0098
A0 → Y↓	0.0362	0.0385	0.0372	0.1458	2.7529	2.7372	1.3692	0.5758
A1 → Y↑	0.1030	0.0995	0.0985	0.2364	6.9569	6.5232	3.3020	1.0097
A1 → Y↓	0.0410	0.0433	0.0420	0.1514	2.7617	2.7415	1.3715	0.5758
B0 → Y↑	0.1092	0.1065	0.1050	0.2459	6.9649	6.5266	3.3041	1.0098
B0 → Y↓	0.0413	0.0462	0.0444	0.1576	2.8278	2.7755	1.3883	0.5760
B1 → Y↑	0.1207	0.1171	0.1164	0.2583	6.9554	6.5228	3.3021	1.0097
B1 → Y↓	0.0465	0.0512	0.0500	0.1628	2.8289	2.7765	1.3890	0.5760
C0 → Y↑	0.0684	0.0652	0.0628	0.1970	6.9649	6.5267	3.3039	1.0097
C0 → Y↓	0.0233	0.0234	0.0228	0.1232	2.2429	2.2417	1.1426	0.5755

Cell Description

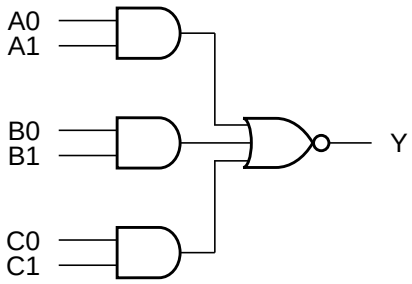
The AOI222 cell provides the logical inverted OR of three AND groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 \bullet A1) + (B0 \bullet B1) + (C0 \bullet C1)}$$

Functions

A0	A1	B0	B1	C0	C1	Y
0	x	0	x	0	x	1
0	x	0	x	x	0	1
0	x	x	0	0	x	1
0	x	x	0	x	0	1
x	0	0	x	0	x	1
x	0	0	x	x	0	1
x	0	x	0	0	x	1
x	0	x	0	x	0	1
x	x	x	x	1	1	0
x	x	1	1	x	x	0
1	1	x	x	x	x	0

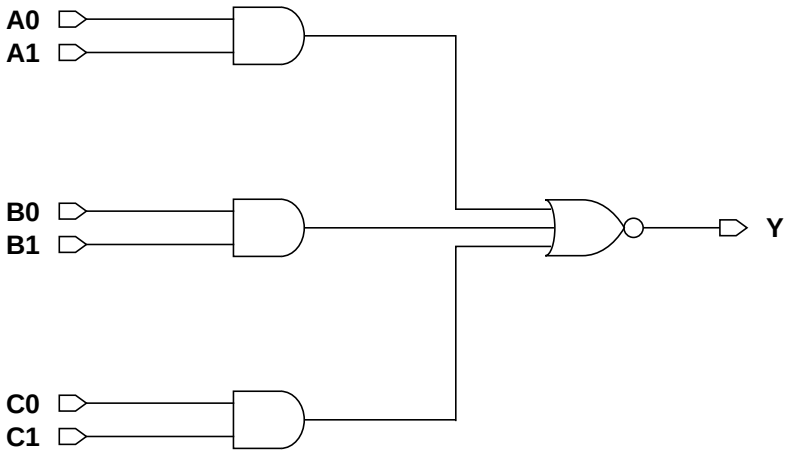
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
AOI222XL	5.04	5.04
AOI222X1	5.04	5.04
AOI222X2	5.04	8.40
AOI222X4	5.04	7.28

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A0	0.0323	0.0323	0.0608	0.0706
A1	0.0366	0.0366	0.0694	0.0744
B0	0.0401	0.0401	0.0750	0.0764
B1	0.0441	0.0441	0.0839	0.0799
C0	0.0481	0.0481	0.0905	0.0824
C1	0.0524	0.0524	0.0993	0.0851

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0043	0.0043	0.0084	0.0029
A1	0.0045	0.0045	0.0090	0.0031
B0	0.0044	0.0044	0.0081	0.0028
B1	0.0043	0.0043	0.0086	0.0028
C0	0.0042	0.0042	0.0079	0.0027
C1	0.0043	0.0043	0.0082	0.0028

Delays at 25°C, 1.8V, Typical Process

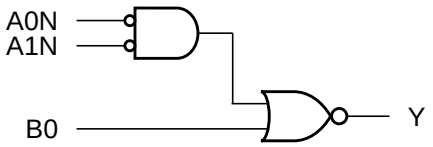
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.0730	0.0737	0.0762	0.1936	6.7055	6.6919	3.4547	0.9830
A0 → Y↓	0.0318	0.0318	0.0302	0.1374	2.7354	2.7306	1.3347	0.5555
A1 → Y↑	0.0859	0.0864	0.0887	0.2099	6.7004	6.6896	3.4531	0.9830
A1 → Y↓	0.0365	0.0374	0.0354	0.1420	2.7522	2.7355	1.3371	0.5555
B0 → Y↑	0.1231	0.1237	0.1197	0.2567	6.7028	6.6906	3.4538	0.9830
B0 → Y↓	0.0493	0.0503	0.0456	0.1598	2.7589	2.7407	1.3388	0.5556
B1 → Y↑	0.1343	0.1347	0.1324	0.2697	6.6959	6.6876	3.4521	0.9830
B1 → Y↓	0.0542	0.0553	0.0509	0.1655	2.7674	2.7448	1.3408	0.5557
C0 → Y↑	0.1424	0.1430	0.1381	0.2790	6.7028	6.6907	3.4538	0.9830
C0 → Y↓	0.0612	0.0633	0.0569	0.1732	2.8075	2.7654	1.3496	0.5557
C1 → Y↑	0.1545	0.1549	0.1495	0.2912	6.6966	6.6879	3.4519	0.9829
C1 → Y↓	0.0673	0.0693	0.0625	0.1785	2.8079	2.7656	1.3497	0.5557

Cell Description

The AOI2BB1 cell provides the logical inverted OR of one AND group of two inverted inputs (A0N, A1N) and an additional non-inverted input (B0). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{A0N} \bullet \overline{A1N}) + B0}$$

Logic Symbol



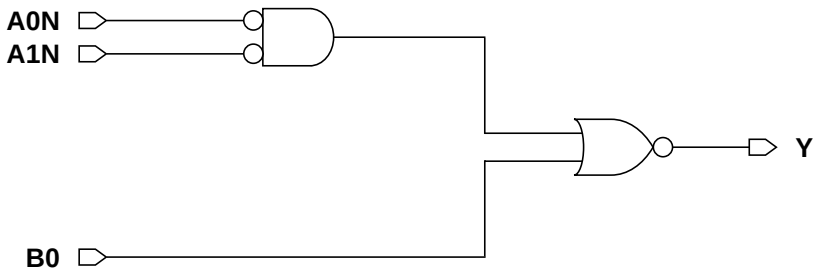
Functions

A0N	A1N	B0	Y
1	x	0	1
x	1	0	1
x	x	1	0
0	0	x	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
AOI2BB1XL	5.04	3.36
AOI2BB1X1	5.04	3.36
AOI2BB1X2	5.04	3.92
AOI2BB1X4	5.04	6.16

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A0N	0.0229	0.0228	0.0328	0.0660
A1N	0.0248	0.0248	0.0362	0.0745
B0	0.0174	0.0175	0.0323	0.0616

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0N	0.0025	0.0025	0.0033	0.0066
A1N	0.0024	0.0024	0.0035	0.0074
B0	0.0035	0.0035	0.0072	0.0127

Delays at 25^{o}C, 1.8V, Typical Process

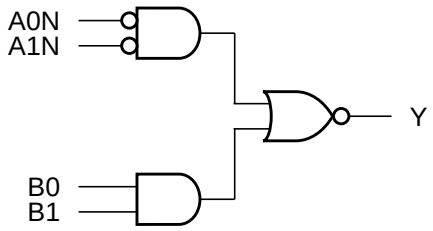
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0N → Y↑	0.0743	0.0750	0.0642	0.0631	5.9014	5.8867	2.8941	1.4577
A0N → Y↓	0.1173	0.1212	0.1069	0.1050	2.3693	2.2900	1.1625	0.5937
A1N → Y↑	0.0794	0.0802	0.0697	0.0684	5.9025	5.8875	2.8944	1.4579
A1N → Y↓	0.1274	0.1313	0.1168	0.1144	2.3693	2.2900	1.1625	0.5937
B0 → Y↑	0.0443	0.0446	0.0407	0.0392	5.8862	5.8800	2.8931	1.4569
B0 → Y↓	0.0204	0.0206	0.0197	0.0193	2.2398	2.2373	1.1407	0.5834

Cell Description

The AOI2BB2 cell provides the logical inverted OR of one AND group of two inverted inputs (A0N, A1N) and one AND group of two non-inverted inputs (B0, B1). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{A0N} \bullet \overline{A1N}) + (B0 \bullet B1)}$$

Logic Symbol



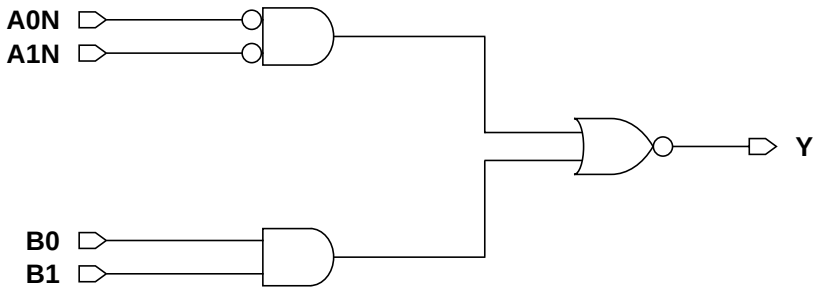
Functions

A0N	A1N	B0	B1	Y
1	x	0	x	1
1	x	x	0	1
x	1	0	x	1
x	1	x	0	1
x	x	1	1	0
0	0	x	x	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
AOI2BB2XL	5.04	3.92
AOI2BB2X1	5.04	3.92
AOI2BB2X2	5.04	5.60
AOI2BB2X4	5.04	8.40

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A0N	0.0207	0.0207	0.0333	0.0619
A1N	0.0225	0.0225	0.0371	0.0716
B0	0.0193	0.0193	0.0404	0.0745
B1	0.0238	0.0238	0.0481	0.0908

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0N	0.0024	0.0024	0.0036	0.0065
A1N	0.0021	0.0021	0.0034	0.0076
B0	0.0037	0.0037	0.0082	0.0143
B1	0.0037	0.0037	0.0084	0.0151

Delays at 25°C, 1.8V, Typical Process

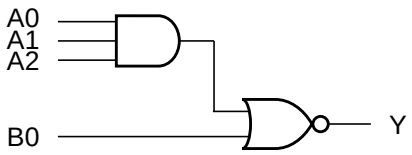
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0N → Y↑	0.0633	0.0637	0.0632	0.0576	4.4062	4.3971	2.1622	1.0511
A0N → Y↓	0.1076	0.1106	0.1115	0.1004	2.3454	2.2800	1.1617	0.5792
A1N → Y↑	0.0646	0.0651	0.0681	0.0634	4.4081	4.3982	2.1626	1.0513
A1N → Y↓	0.1150	0.1180	0.1200	0.1105	2.3453	2.2799	1.1616	0.5792
B0 → Y↑	0.0536	0.0540	0.0520	0.0484	5.8932	5.8830	2.8947	1.4061
B0 → Y↓	0.0270	0.0276	0.0270	0.0261	2.7457	2.7342	1.3663	0.6877
B1 → Y↑	0.0641	0.0643	0.0613	0.0583	5.8844	5.8791	2.8922	1.4053
B1 → Y↓	0.0320	0.0327	0.0315	0.0312	2.7538	2.7382	1.3683	0.6888

Cell Description

The AOI31 cell provides the logical inverted OR of one AND group and an additional input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 \bullet A1 \bullet A2) + B0}$$

Logic Symbol



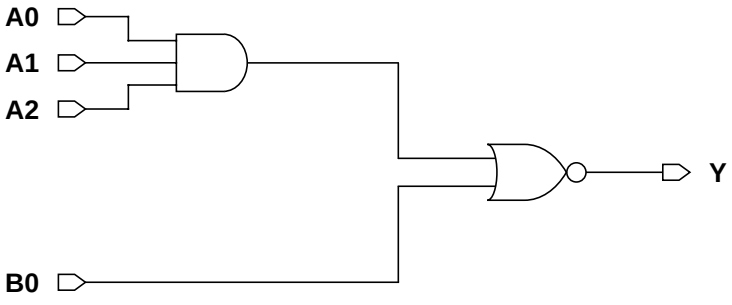
Functions

A0	A1	A2	B0	Y
0	x	x	0	1
x	0	x	0	1
x	x	0	0	1
x	x	x	1	0
1	1	1	x	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
AOI31XL	5.04	3.36
AOI31X1	5.04	3.36
AOI31X2	5.04	5.60
AOI31X4	5.04	5.60

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A0	0.0190	0.0204	0.0453	0.0591
A1	0.0239	0.0254	0.0544	0.0632
A2	0.0284	0.0306	0.0648	0.0689
B0	0.0233	0.0251	0.0513	0.0650

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0036	0.0039	0.0093	0.0028
A1	0.0038	0.0041	0.0087	0.0026
A2	0.0035	0.0039	0.0083	0.0026
B0	0.0034	0.0035	0.0068	0.0026

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.0593	0.0573	0.0594	0.1646	6.4246	5.8852	2.8487	1.0098
A0 → Y↓	0.0320	0.0309	0.0332	0.1342	3.3820	3.0413	1.5233	0.5758
A1 → Y↑	0.0726	0.0703	0.0708	0.1801	6.4160	5.8813	2.8466	1.0098
A1 → Y↓	0.0400	0.0386	0.0399	0.1398	3.3897	3.0450	1.5250	0.5758
A2 → Y↑	0.0833	0.0816	0.0826	0.1940	6.4194	5.8830	2.8476	1.0098
A2 → Y↓	0.0425	0.0414	0.0433	0.1430	3.3898	3.0451	1.5252	0.5758
B0 → Y↑	0.0628	0.0629	0.0593	0.1733	6.4295	5.8872	2.8492	1.0098
B0 → Y↓	0.0191	0.0188	0.0184	0.1130	2.4663	2.2464	1.1454	0.5756

Cell Description

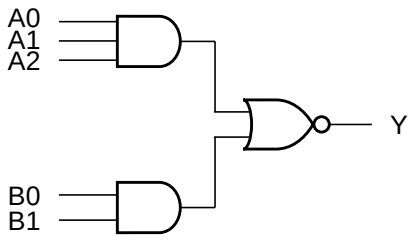
The AOI32 cell provides the logical inverted OR of two AND groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 \bullet A1 \bullet A2) + (B0 \bullet B1)}$$

Functions

A0	A1	A2	B0	B1	Y
0	x	x	0	x	1
0	x	x	x	0	1
x	0	x	0	x	1
x	0	x	x	0	1
x	x	0	0	x	1
x	x	0	x	0	1
x	x	x	1	1	0
1	1	1	x	x	0

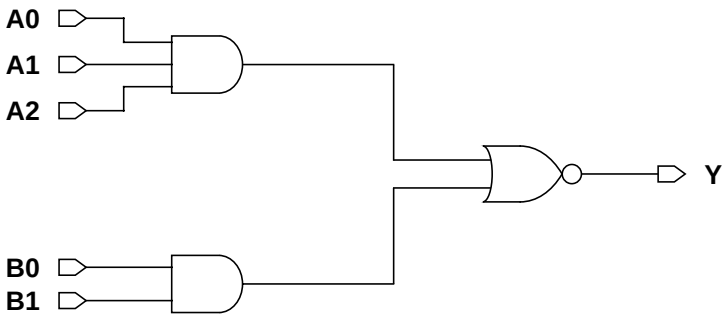
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
AOI32XL	5.04	3.92
AOI32X1	5.04	4.48
AOI32X2	5.04	6.72
AOI32X4	5.04	6.16

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A0	0.0275	0.0305	0.0556	0.0658
A1	0.0322	0.0359	0.0678	0.0691
A2	0.0363	0.0405	0.0782	0.0750
B0	0.0254	0.0287	0.0547	0.0663
B1	0.0293	0.0331	0.0629	0.0686

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0038	0.0041	0.0080	0.0028
A1	0.0037	0.0042	0.0084	0.0029
A2	0.0035	0.0040	0.0090	0.0027
B0	0.0037	0.0039	0.0074	0.0028
B1	0.0038	0.0042	0.0079	0.0030

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.0840	0.0861	0.0794	0.1928	6.4232	5.8846	2.9185	1.0097
A0 → Y↓	0.0450	0.0457	0.0422	0.1465	3.3805	3.0424	1.5204	0.5755
A1 → Y↑	0.0967	0.0990	0.0922	0.2081	6.4156	5.8812	2.9167	1.0097
A1 → Y↓	0.0526	0.0536	0.0499	0.1552	3.3885	3.0464	1.5224	0.5756
A2 → Y↑	0.1078	0.1102	0.1046	0.2205	6.4181	5.8823	2.9174	1.0097
A2 → Y↓	0.0553	0.0562	0.0537	0.1576	3.3883	3.0463	1.5224	0.5755
B0 → Y↑	0.0680	0.0704	0.0672	0.1782	6.4300	5.8876	2.9201	1.0097
B0 → Y↓	0.0247	0.0258	0.0239	0.1276	3.0285	2.7382	1.3694	0.5755
B1 → Y↑	0.0793	0.0823	0.0777	0.1916	6.4247	5.8855	2.9186	1.0097
B1 → Y↓	0.0303	0.0316	0.0294	0.1318	3.0391	2.7434	1.3713	0.5755

Cell Description

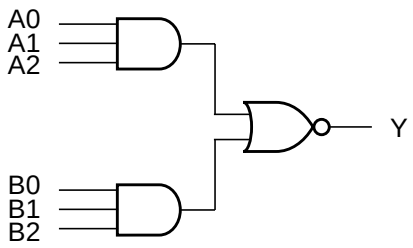
The AOI33 cell provides the logical inverted OR of two AND groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 \bullet A1 \bullet A2) + (B0 \bullet B1 \bullet B2)}$$

Functions

A0	A1	A2	B0	B1	B2	Y
0	x	x	0	x	x	1
0	x	x	x	0	x	1
0	x	x	x	x	0	1
x	0	x	0	x	x	1
x	0	x	x	0	x	1
x	0	x	x	x	0	1
x	x	0	0	x	x	1
x	x	0	x	0	x	1
x	x	0	x	x	0	1
x	x	x	1	1	1	0
1	1	1	x	x	x	0

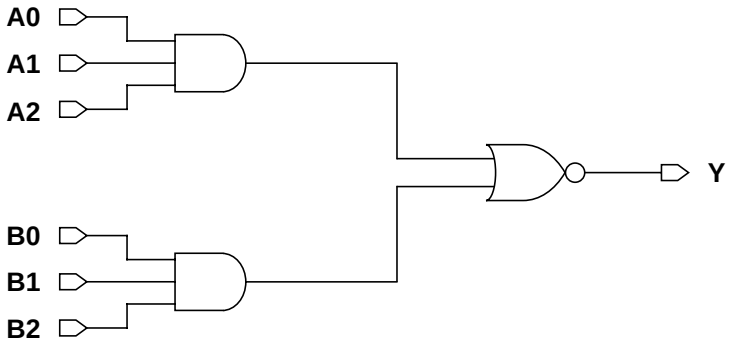
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
AOI33XL	5.04	5.04
AOI33X1	5.04	5.04
AOI33X2	5.04	7.84
AOI33X4	5.04	6.72

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A0	0.0282	0.0309	0.0593	0.0686
A1	0.0326	0.0358	0.0693	0.0731
A2	0.0369	0.0406	0.0795	0.0779
B0	0.0355	0.0392	0.0761	0.0752
B1	0.0402	0.0444	0.0863	0.0779
B2	0.0442	0.0491	0.0968	0.0830

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0037	0.0040	0.0079	0.0028
A1	0.0037	0.0041	0.0084	0.0029
A2	0.0038	0.0043	0.0091	0.0030
B0	0.0036	0.0040	0.0076	0.0028
B1	0.0038	0.0040	0.0083	0.0028
B2	0.0036	0.0039	0.0087	0.0026

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.0793	0.0800	0.0746	0.1946	6.4290	5.8877	2.9202	1.0098
A0 → Y↓	0.0324	0.0323	0.0296	0.1441	3.3786	3.0432	1.5219	0.5760
A1 → Y↑	0.0920	0.0931	0.0874	0.2094	6.4229	5.8849	2.9186	1.0098
A1 → Y↓	0.0401	0.0402	0.0373	0.1527	3.3884	3.0480	1.5241	0.5760
A2 → Y↑	0.1044	0.1062	0.1012	0.2241	6.4253	5.8863	2.9195	1.0097
A2 → Y↓	0.0436	0.0440	0.0414	0.1566	3.3888	3.0484	1.5246	0.5761
B0 → Y↑	0.1114	0.1135	0.1062	0.2309	6.4276	5.8871	2.9198	1.0098
B0 → Y↓	0.0558	0.0558	0.0519	0.1680	3.3793	3.0445	1.5224	0.5762
B1 → Y↑	0.1240	0.1261	0.1188	0.2451	6.4206	5.8838	2.9182	1.0098
B1 → Y↓	0.0642	0.0642	0.0603	0.1762	3.3799	3.0446	1.5224	0.5762
B2 → Y↑	0.1351	0.1377	0.1314	0.2578	6.4218	5.8845	2.9185	1.0097
B2 → Y↓	0.0669	0.0671	0.0642	0.1788	3.3797	3.0446	1.5224	0.5762

Cell Description

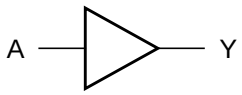
The BUF cell provides the logical buffer of a single input (A). The output (Y) is represented by the logic equation:

$Y = A$

Functions

A	Y
0	0
1	1

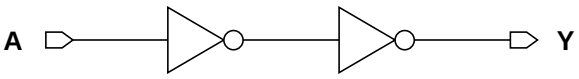
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
BUFXL	5.04	2.24
BUFX1	5.04	2.24
BUFX2	5.04	2.24
BUFX3	5.04	2.80
BUFX4	5.04	2.80
BUFX8	5.04	4.48
BUFX12	5.04	6.16
BUFX16	5.04	7.84
BUFX20	5.04	8.96

Functional Schematic



AC Power

Pin	Power (μW/MHz)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A	0.0161	0.0171	0.0258	0.0386	0.0495	0.0931	0.1414	0.1872	0.2376

Pin Capacitance

Pin	Capacitance (pF)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A	0.0021	0.0023	0.0026	0.0038	0.0048	0.0089	0.0132	0.0169	0.0212

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A → Y↑	0.0485	0.0507	0.0534	0.0496	0.0487	0.0437	0.0428	0.0440	0.0430
A → Y↓	0.0629	0.0670	0.0735	0.0696	0.0679	0.0593	0.0597	0.0585	0.0594

Description	K_{load} (ns/pF)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A → Y↑	4.4667	3.9780	2.0193	1.3393	1.0098	0.4902	0.3270	0.2448	0.1953
A → Y↓	2.4862	2.2533	1.1505	0.7626	0.5753	0.2751	0.1843	0.1375	0.1101

Cell Description

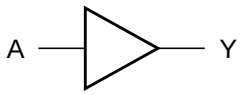
The CLKBUF cell provides the logical buffer of a single input (A), with balanced delays for clock signals. The output (Y) is represented by the logic equation:

$$Y = A$$

Functions

A	Y
0	0
1	1

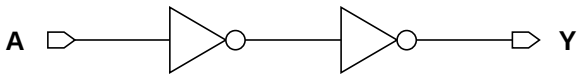
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
CLKBUFXL	5.04	2.24
CLKBUFX1	5.04	2.24
CLKBUFX2	5.04	2.24
CLKBUFX3	5.04	2.80
CLKBUFX4	5.04	2.80
CLKBUFX8	5.04	4.48
CLKBUFX12	5.04	8.96
CLKBUFX16	5.04	10.64
CLKBUFX20	5.04	14.00

Functional Schematic



AC Power

Pin	Power (µW/MHz)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A	0.0193	0.0215	0.0256	0.0298	0.0357	0.0655	0.1821	0.2295	0.3081

Pin Capacitance

Pin	Capacitance (pF)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A	0.0021	0.0031	0.0031	0.0033	0.0033	0.0057	0.0152	0.0192	0.0262

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A → Y↑	0.0462	0.0519	0.0575	0.0644	0.0691	0.0649	0.0556	0.0596	0.0593
A → Y↓	0.1044	0.0537	0.0589	0.0659	0.0708	0.0652	0.0589	0.0646	0.0615

Description	K_{load} (ns/pF)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A → Y↑	2.1943	3.2712	2.0414	1.3402	1.0108	0.4911	0.1958	0.1335	0.1015
A → Y↓	3.6482	3.6023	2.1776	1.4901	1.1386	0.5501	0.1927	0.1640	0.1160

Cell Description

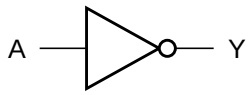
The CLKINV cell provides the logical inversion of a single input (A), with balanced delays for clock signals. The output (Y) is represented by the logic equation:

$$Y = \overline{A}$$

Functions

A	Y
0	1
1	0

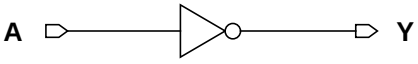
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
CLKINVXL	5.04	1.68
CLKINVX1	5.04	1.68
CLKINVX2	5.04	1.68
CLKINVX3	5.04	2.24
CLKINVX4	5.04	2.24
CLKINVX8	5.04	3.36
CLKINVX12	5.04	10.64
CLKINVX16	5.04	13.44
CLKINVX20	5.04	15.12

Functional Schematic



AC Power

Pin	Power (μW/MHz)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A	0.0104	0.0104	0.0165	0.0224	0.0289	0.0575	0.2210	0.2816	0.3520

Pin Capacitance

Pin	Capacitance (pF)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A	0.0030	0.0030	0.0045	0.0073	0.0087	0.0167	0.0054	0.0074	0.0082

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A → Y↑	0.0194	0.0195	0.0193	0.0170	0.0166	0.0160	0.1161	0.1115	0.1135
A → Y↓	0.0187	0.0188	0.0191	0.0163	0.0160	0.0154	0.1168	0.1129	0.1149

Description	K_{load} (ns/pF)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A → Y↑	3.2704	3.2682	2.0392	1.3281	1.0086	0.5030	0.1659	0.1317	0.1008
A → Y↓	3.5923	3.5934	2.3024	1.4851	1.1344	0.5728	0.1895	0.1507	0.1158

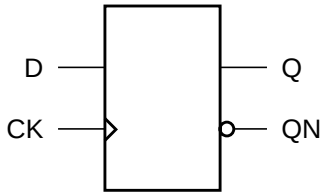
Cell Description

The DFF cell is a positive-edge triggered, static D-type flip-flop.

Function Table

D	CK	Q[n+1]	QN[n+1]
0	↑	0	1
1	↑	1	0
x	↓	Q[n]	QN[n]

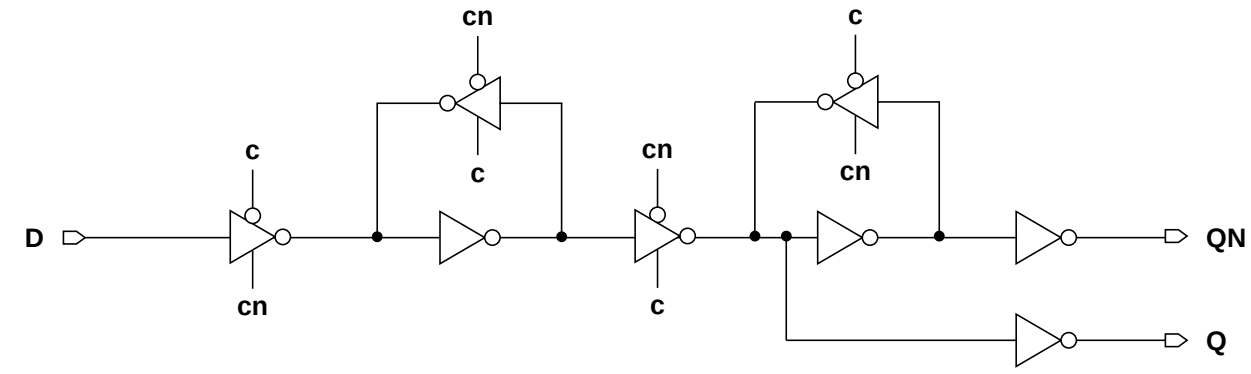
Logic Symbol

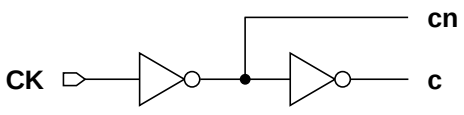


Cell Size

Drive Strength	Height (µm)	Width (µm)
DFFXL	5.04	9.52
DFFX1	5.04	9.52
DFFX2	5.04	11.76
DFFX4	5.04	14.00

Functional Schematic





AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
D	0.0286	0.0289	0.0371	0.0531
CK	0.0330	0.0339	0.0419	0.0579
Q	0.0372	0.0390	0.0620	0.1029

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0021	0.0021	0.0023	0.0034
CK	0.0022	0.0027	0.0037	0.0053

Delays at 25^{o}C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.1837	0.1691	0.1529	0.1336	4.5119	3.9965	2.0132	1.0112
CK → Q↓	0.1543	0.1426	0.1280	0.1138	2.6026	2.2943	1.1427	0.5815
CK → QN↑	0.2042	0.1908	0.1681	0.1532	4.4748	3.9821	2.0192	1.0099
CK → QN↓	0.2417	0.2314	0.2079	0.1864	2.5199	2.2665	1.1517	0.5758

Timing Constraints at 25^{o}C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → CK	0.0469	0.0547	0.0508	0.0430
	setup↓ → CK	0.1016	0.1133	0.1172	0.1016
	hold↑ → CK	-0.0312	-0.0352	-0.0352	-0.0273
	hold↓ → CK	-0.0234	-0.0352	-0.0391	-0.0273
CK	minpwh	0.0930	0.0882	0.0785	0.0688
	minpwl	0.1465	0.1271	0.1222	0.0979

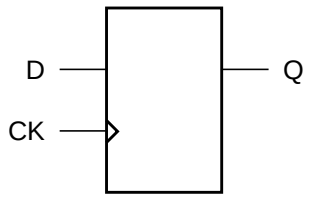
Cell Description

The DFFHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop. The cell has a single output (Q) and fast clock-to-out path.

Functions

D	CK	Q[n+1]
0	⎍	0
1	⎍	1
x	⎎	Q[n]

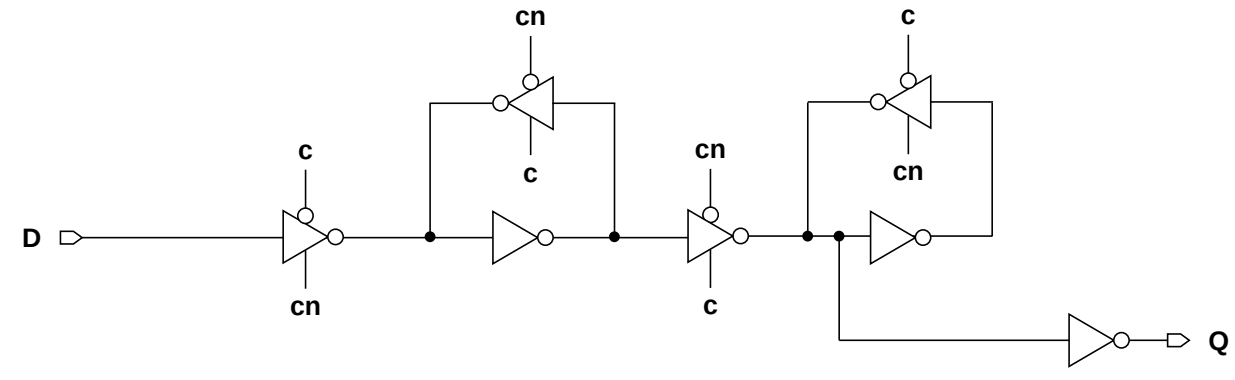
Logic Symbol

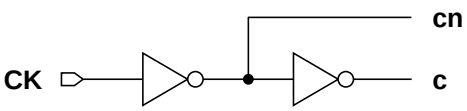


Cell Size

Drive Strength	Height (µm)	Width (µm)
DFFHQXL	5.04	8.96
DFFHQX1	5.04	8.96
DFFHQX2	5.04	9.52
DFFHQX4	5.04	12.88

Functional Schematic





AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
D	0.0319	0.0364	0.0441	0.0638
CK	0.0338	0.0346	0.0376	0.0456
Q	0.0271	0.0272	0.0370	0.0526

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0021	0.0021	0.0021	0.0025
CK	0.0021	0.0023	0.0029	0.0041

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.1766	0.1593	0.1537	0.1347	4.5211	3.9947	2.0129	1.0103
CK → Q↓	0.1776	0.1505	0.1378	0.1222	2.6983	2.2953	1.1456	0.5868

Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → CK	0.0508	0.0547	0.0664	0.0664
	setup↓ → CK	0.1250	0.1289	0.1445	0.1523
	hold↑ → CK	-0.0234	-0.0273	-0.0352	-0.0352
	hold↓ → CK	-0.0156	-0.0234	-0.0273	-0.0273
CK	minpwh	0.0930	0.0882	0.0882	0.0785
	minpwl	0.1416	0.1368	0.1319	0.1076

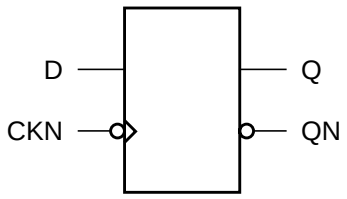
Cell Description

The DFFN cell is a negative-edge triggered, static D-type flip-flop.

Functions

D	CKN	Q[n+1]	QN[n+1]
0	↓	0	1
1	↓	1	0
x	↑	Q[n]	QN[n]

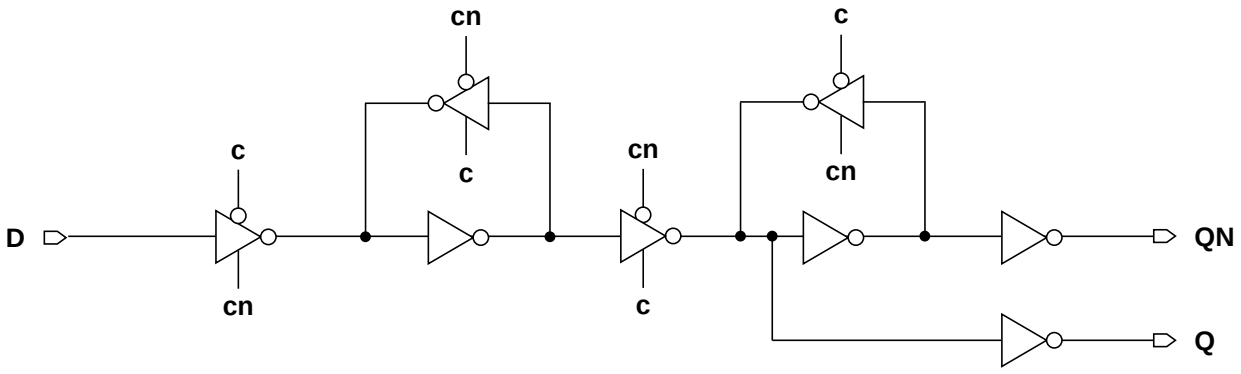
Logic Symbol

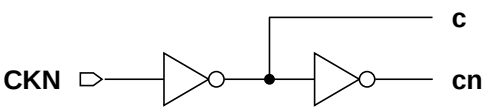


Cell Size

Drive Strength	Height (µm)	Width (µm)
DFFNXL	5.04	9.52
DFFNX1	5.04	9.52
DFFNX2	5.04	11.76
DFFNX4	5.04	13.44

Functional Schematic





AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
D	0.0276	0.0280	0.0354	0.0543
CKN	0.0371	0.0386	0.0501	0.0729
Q	0.0385	0.0415	0.0686	0.1086

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0019	0.0019	0.0020	0.0032
CKN	0.0022	0.0027	0.0036	0.0053

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CKN → Q↑	0.1433	0.1245	0.1121	0.0968	4.5171	3.9975	2.0156	1.0116
CKN → Q↓	0.2459	0.2291	0.2020	0.1730	2.5935	2.2917	1.1452	0.5817
CKN → QN↑	0.2944	0.2754	0.2442	0.2138	4.4750	3.9819	2.2393	1.0100
CKN → QN↓	0.2007	0.1856	0.1685	0.1518	2.5192	2.2662	1.1517	0.5762

Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → CKN	0.0391	0.0508	0.0586	0.0508
	setup↓ → CKN	0.0820	0.0898	0.0977	0.0781
	hold↑ → CKN	0.0508	0.0352	0.0273	0.0234
	hold↓ → CKN	-0.0625	-0.0703	-0.0781	-0.0625
CKN	minpwl	0.1173	0.1028	0.0930	0.0833
	minpwh	0.1173	0.1173	0.1076	0.0833

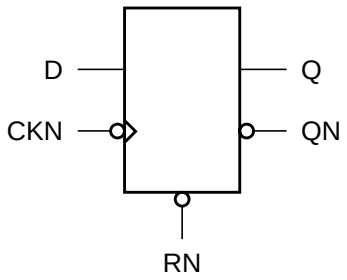
Cell Description

The DFFNR cell is a negative-edge triggered, static D-type flip-flop with asynchronous active-low reset (RN).

Functions

RN	D	CKN	Q[n+1]	QN[n+1]
0	x	x	0	1
1	0	↓	0	1
1	1	↓	1	0
1	x	↑	Q[n]	QN[n]

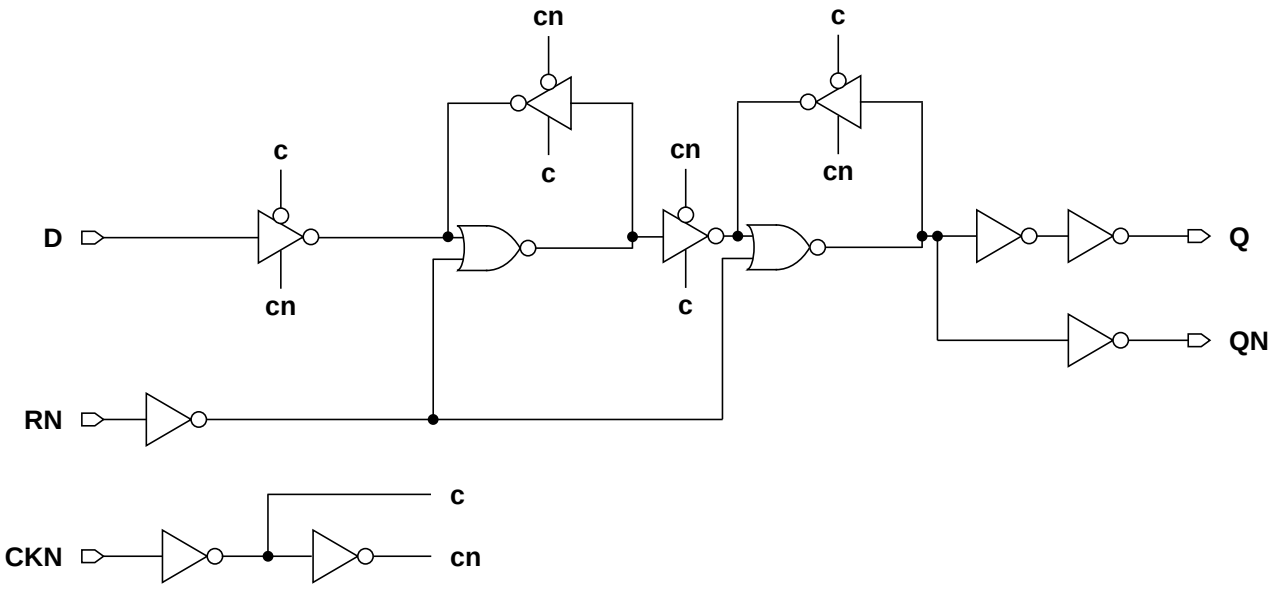
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
DFFNRXL	5.04	12.88
DFFNRX1	5.04	13.44
DFFNRX2	5.04	13.44
DFFNRX4	5.04	17.36

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
D	0.0294	0.0280	0.0305	0.0412
CKN	0.0373	0.0357	0.0389	0.0535
RN	0.0150	0.0165	0.0187	0.0297
Q	0.0456	0.0496	0.0737	0.1258

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0021	0.0021	0.0024	0.0029
CKN	0.0023	0.0028	0.0027	0.0036
RN	0.0020	0.0022	0.0028	0.0046

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CKN → Q↑	0.2729	0.2555	0.2504	0.2288	4.4698	3.9785	2.0192	1.0098
CKN → Q↓	0.3271	0.3312	0.3253	0.2974	2.4861	2.2539	1.1523	0.5757
RN → Q↓	0.1858	0.1817	0.1833	0.1686	2.4866	2.2540	1.1524	0.5758
CKN → QN↑	0.2922	0.2903	0.2674	0.2446	4.4695	3.9790	2.0200	1.0103
CKN → QN↓	0.2468	0.2286	0.2084	0.1898	2.6457	2.2977	1.1681	0.5833
RN → QN↑	0.1513	0.1416	0.1260	0.1164	4.4782	3.9822	2.0215	1.0113

Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → CKN	0.0469	0.0586	0.0703	0.0703
	setup↓ → CKN	0.0898	0.0977	0.1094	0.0977
	hold↑ → CKN	0.0469	0.0273	0.0234	0.0234
	hold↓ → CKN	-0.0703	-0.0781	-0.0859	-0.0742
CKN	minpwl	0.1222	0.1125	0.1028	0.0930
	minpwh	0.1173	0.1125	0.1222	0.1076
RN	minpwl	0.1416	0.1465	0.1562	0.2437
	recovery	0.0352	0.0508	0.0547	0.0586

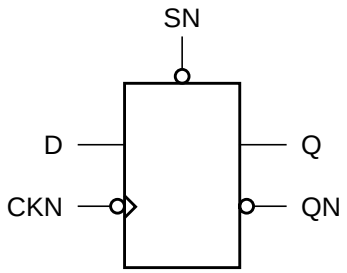
Cell Description

The DFFNS cell is a negative-edge triggered, static D-type flip-flop with asynchronous active-low set (SN).

Functions

SN	D	CKN	Q[n+1]	QN[n+1]
0	x	x	1	0
1	0	↓	0	1
1	1	↓	1	0
1	x	↑	Q[n]	QN[n]

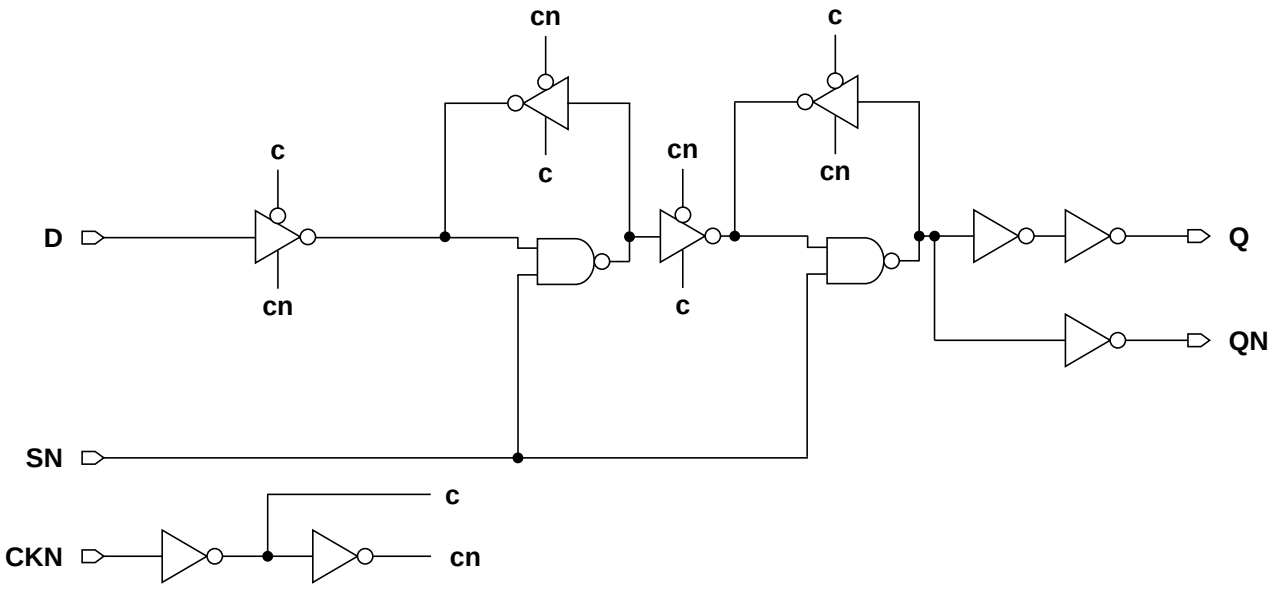
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
DFFNSXL	5.04	11.20
DFFNSX1	5.04	11.20
DFFNSX2	5.04	11.76
DFFNSX4	5.04	16.24

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
D	0.0285	0.0254	0.0276	0.0337
CKN	0.0341	0.0333	0.0360	0.0445
SN	0.0064	0.0064	0.0089	0.0150
Q	0.0451	0.0467	0.0684	0.1241

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0017	0.0017	0.0018	0.0019
CKN	0.0021	0.0027	0.0027	0.0031
SN	0.0048	0.0050	0.0062	0.0103

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CKN → Q↑	0.2308	0.2145	0.2181	0.2093	4.4697	3.9792	2.2392	1.0098
CKN → Q↓	0.3154	0.3113	0.3116	0.3012	2.4866	2.2528	1.1520	0.5757
SN → Q↑	0.1302	0.1172	0.1246	0.1179	4.4691	3.9792	2.2392	1.0098
CKN → QN↑	0.2822	0.2747	0.2583	0.2484	4.4775	3.9814	2.2150	1.0113
CKN → QN↓	0.2037	0.1864	0.1764	0.1703	2.5426	2.2623	1.1547	0.5773
SN → QN↓	0.1036	0.0898	0.0832	0.0795	2.5413	2.2637	1.1562	0.5788

Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → CKN	0.0273	0.0469	0.0469	0.0508
	setup↓ → CKN	0.0859	0.0977	0.0977	0.1016
	hold↑ → CKN	0.0430	0.0273	0.0273	0.0273
	hold↓ → CKN	-0.0742	-0.0781	-0.0820	-0.0820
CKN	minpwl	0.1125	0.1028	0.0979	0.0979
	minpwh	0.1076	0.1028	0.1076	0.1076
SN	minpwl	0.1028	0.0882	0.0930	0.1125
	recovery	-0.0508	-0.0312	-0.0352	-0.0352

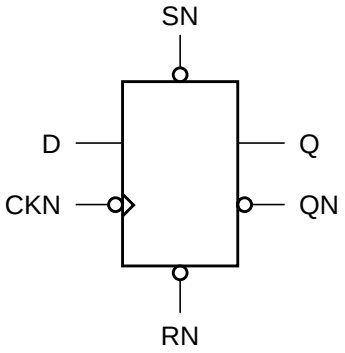
Cell Description

The DFFNSR cell is a negative-edge triggered, static D-type flip-flop with asynchronous active-low reset (RN) and set (SN), and set dominating reset.

Functions

RN	SN	D	CKN	Q[n+1]	QN[n+1]
0	1	x	x	0	1
1	0	x	x	1	0
0	0	x	x	1	0
1	1	0	↓	0	1
1	1	1	↓	1	0
1	1	x	↑	Q[n]	QN[n]

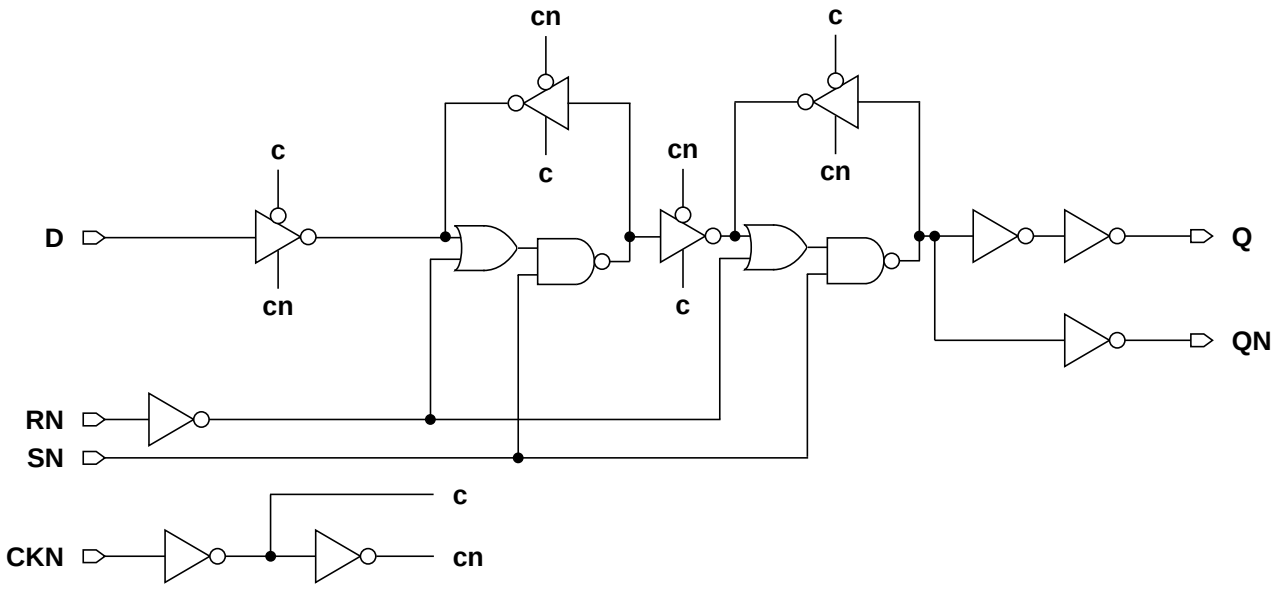
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
DFFNSRXL	5.04	14.56
DFFNSRX1	5.04	14.56
DFFNSRX2	5.04	15.12
DFFNSRX4	5.04	19.60

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
D	0.0286	0.0259	0.0287	0.0421
CKN	0.0385	0.0384	0.0408	0.0579
SN	0.0072	0.0074	0.0091	0.0148
RN	0.0179	0.0188	0.0226	0.0357
Q	0.0480	0.0508	0.0773	0.1364

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0021	0.0021	0.0021	0.0029
CKN	0.0021	0.0027	0.0028	0.0037
SN	0.0061	0.0063	0.0074	0.0129
RN	0.0024	0.0026	0.0033	0.0051

Delays at 25^{o}C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CKN → Q↑	0.2975	0.2623	0.2549	0.2430	4.4663	3.9779	2.0191	1.0044
CKN → Q↓	0.3611	0.3420	0.3299	0.3115	2.4997	2.2575	1.1522	0.5760
SN → Q↑	0.1610	0.1423	0.1408	0.1332	4.4661	3.9778	2.0192	1.0044
SN → Q↓	0.1514	0.1400	0.1408	0.1337	2.5007	2.2578	1.1523	0.5760
RN → Q↓	0.2199	0.2035	0.1960	0.1865	2.5004	2.2578	1.1523	0.5760
CKN → QN↑	0.3155	0.2934	0.2730	0.2571	4.4935	3.9860	2.0225	1.0064
CKN → QN↓	0.2610	0.2298	0.2126	0.2044	2.7096	2.3741	1.1708	0.5867
SN → QN↑	0.1062	0.0923	0.0846	0.0799	4.5174	3.9954	2.0270	1.0096
SN → QN↓	0.1242	0.1074	0.0979	0.0946	2.5861	2.3445	1.1593	0.5828
RN → QN↑	0.1745	0.1556	0.1396	0.1325	4.5152	3.9948	2.0268	1.0094

Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → CKN	0.0469	0.0898	0.0742	0.0703
	setup↓ → CKN	0.0859	0.0938	0.1016	0.0820
	hold↑ → CKN	0.0469	0.0234	0.0234	0.0312
	hold↓ → CKN	-0.0625	-0.0625	-0.0703	-0.0586
CKN	minpwl	0.1271	0.1125	0.1028	0.0979
	minpwh	0.1173	0.1222	0.1173	0.0979
SN	minpwl	0.1222	0.1076	0.1076	0.1368
	recovery	-0.0430	-0.0195	-0.0234	-0.0312
	removal	0.0508	0.0273	0.0312	0.0391
RN	minpwl	0.1659	0.1513	0.1611	0.2582
	recovery	0.0430	0.0859	0.0664	0.0664
	removal	0.0625	0.0234	0.0391	0.0430

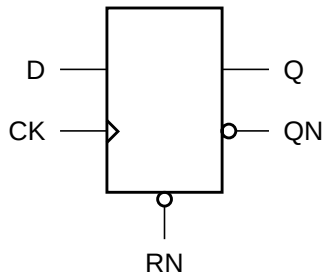
Cell Description

The DFFR cell is a positive-edge triggered, static D-type flip-flop with asynchronous active-low reset (RN).

Functions

RN	D	CK	Q[n+1]	QN[n+1]
0	x	x	0	1
1	0	⎍	0	1
1	1	⎍	1	0
1	x	⎎	Q[n]	QN[n]

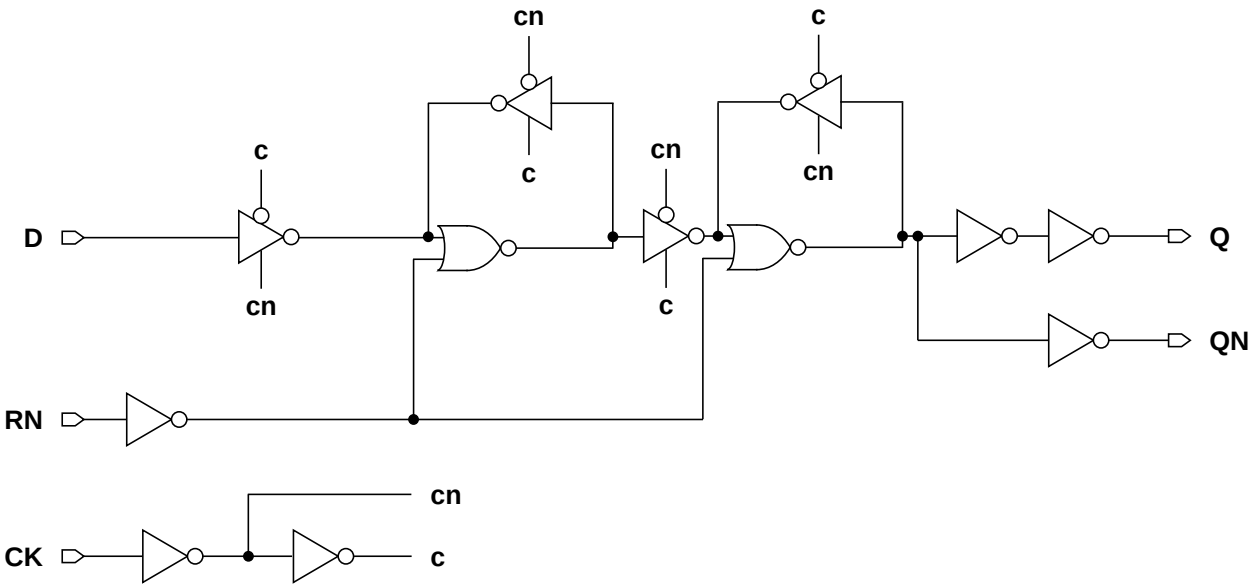
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
DFFRXL	5.04	13.44
DFFRX1	5.04	13.44
DFFRX2	5.04	13.44
DFFRX4	5.04	17.36

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
D	0.0304	0.0294	0.0294	0.0419
CK	0.0366	0.0374	0.0333	0.0444
RN	0.0153	0.0164	0.0188	0.0294
Q	0.0472	0.0509	0.0737	0.1291

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0023	0.0023	0.0021	0.0028
CK	0.0023	0.0028	0.0029	0.0037
RN	0.0020	0.0022	0.0028	0.0047

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.3396	0.3162	0.2929	0.2721	4.4690	3.9792	2.0192	1.0098
CK → Q↓	0.2431	0.2493	0.2342	0.2165	2.4901	2.2543	1.1523	0.5758
RN → Q↓	0.1951	0.1846	0.1833	0.1693	2.4905	2.2544	1.1524	0.5758
CK → QN↑	0.2048	0.2077	0.1763	0.1634	4.4721	3.9793	2.0201	1.0103
CK → QN↓	0.3081	0.2867	0.2508	0.2329	2.6727	2.3000	1.1681	0.5833
RN → QN↑	0.1571	0.1438	0.1259	0.1168	4.4817	3.9830	2.0215	1.0113

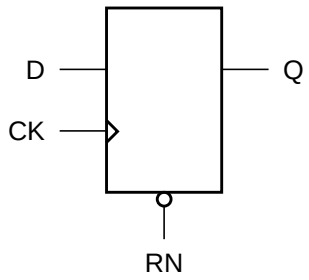
Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → CK	0.0586	0.0625	0.0625	0.0625
	setup↓ → CK	0.1055	0.1133	0.1172	0.1133
	hold↑ → CK	-0.0391	-0.0508	-0.0469	-0.0430
	hold↓ → CK	-0.0234	-0.0391	-0.0352	-0.0312
CK	minpwh	0.1028	0.1028	0.0882	0.0833
	minpwl	0.1708	0.1416	0.1368	0.1222
RN	minpwl	0.1513	0.1465	0.1562	0.2485
	recovery	0.0312	0.0391	0.0469	0.0469
	removal	-0.0156	-0.0234	-0.0273	-0.0234

Cell Description

The DFFRHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with asynchronous active-low reset (RN). The cell has a single output (Q) and fast clock-to-out path.

Logic Symbol



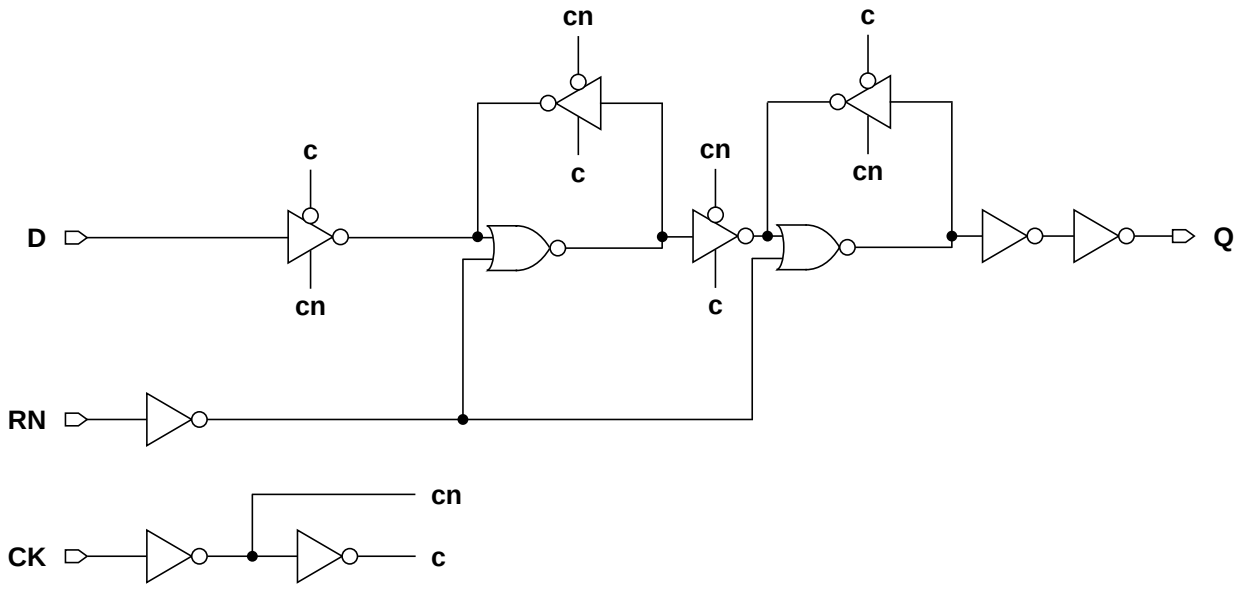
Functions

RN	D	CK	Q[n+1]
0	x	x	0
1	0	↑	0
1	1	↑	1
1	x	↓	Q[n]

Cell Size

Drive Strength	Height (µm)	Width (µm)
DFFRHQXL	5.04	12.32
DFFRHQX1	5.04	12.32
DFFRHQX2	5.04	15.12
DFFRHQX4	5.04	19.04

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
D	0.0312	0.0351	0.0539	0.0795
CK	0.0336	0.0360	0.0413	0.0573
RN	0.0188	0.0223	0.0304	0.0472
Q	0.0271	0.0307	0.0437	0.0731

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0021	0.0021	0.0022	0.0035
CK	0.0021	0.0025	0.0031	0.0046
RN	0.0023	0.0032	0.0045	0.0069

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.1842	0.1701	0.1564	0.1426	6.4274	5.8839	2.8920	1.5926
CK → Q↓	0.1850	0.1601	0.1345	0.1195	2.6754	2.2985	1.1628	0.5790
RN → Q↓	0.1547	0.1152	0.1061	0.0863	2.4193	1.8508	1.0254	0.5608

Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → CK	0.0820	0.0859	0.0938	0.0820
	setup↓ → CK	0.1406	0.1523	0.1719	0.1406
	hold↑ → CK	-0.0273	-0.0312	-0.0391	-0.0312
	hold↓ → CK	-0.0117	-0.0195	-0.0234	-0.0078
CK	minpwh	0.0930	0.0882	0.0882	0.0736
	minpwl	0.1416	0.1271	0.1222	0.1028
RN	minpwl	0.2631	0.2534	0.3360	0.5206
	recovery	0.0898	0.0820	0.0820	0.0781
	removal	-0.0273	-0.0234	-0.0156	-0.0078

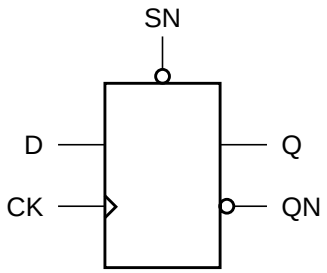
Cell Description

The DFFS cell is a positive-edge triggered, static D-type flip-flop with asynchronous active-low set (SN).

Functions

SN	D	CK	Q[n+1]	QN[n+1]
0	x	x	1	0
1	0	↑	0	1
1	1	↑	1	0
1	x	↓	Q[n]	QN[n]

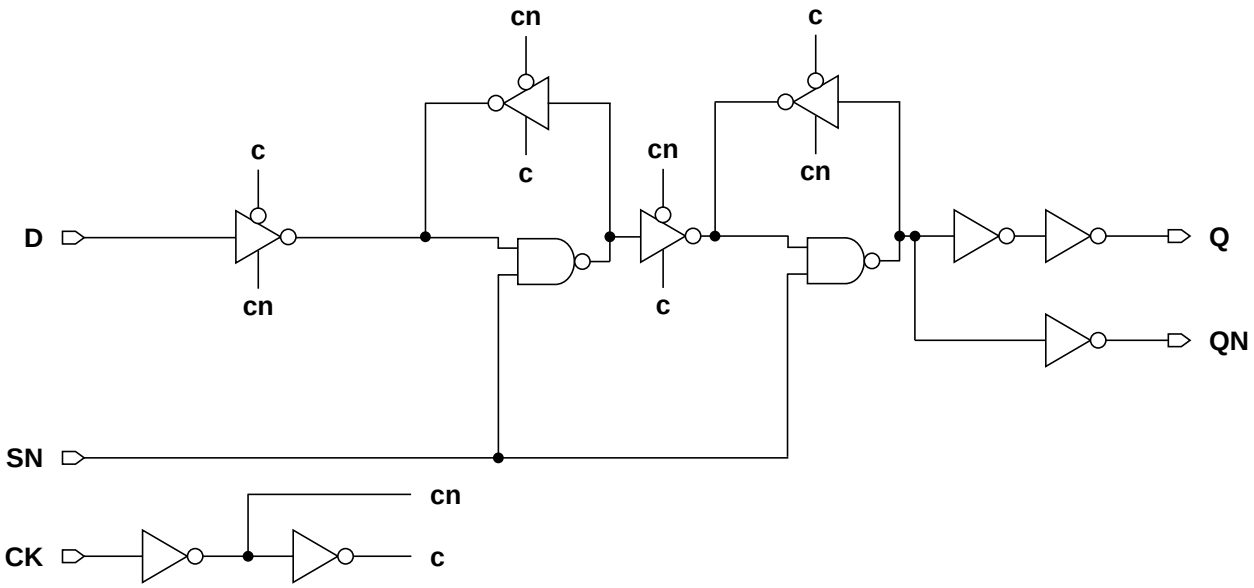
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
DFFSXL	5.04	11.20
DFFSX1	5.04	11.20
DFFSX2	5.04	12.32
DFFSX4	5.04	16.80

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
D	0.0258	0.0258	0.0289	0.0335
CK	0.0301	0.0319	0.0337	0.0394
SN	0.0061	0.0069	0.0093	0.0150
Q	0.0420	0.0457	0.0724	0.1208

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0021	0.0021	0.0020	0.0022
CK	0.0022	0.0028	0.0027	0.0031
SN	0.0051	0.0055	0.0066	0.0109

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.2780	0.2581	0.2711	0.2550	4.4684	3.9787	2.0192	1.0097
CK → Q↓	0.2419	0.2293	0.2412	0.2226	2.4875	2.2531	1.1519	0.5752
SN → Q↑	0.1305	0.1173	0.1282	0.1179	4.4682	3.9788	2.0192	1.0097
CK → QN↑	0.2087	0.1930	0.1844	0.1708	4.4773	3.9810	2.0222	1.0112
CK → QN↓	0.2514	0.2306	0.2293	0.2165	2.5432	2.2624	1.1549	0.5770
SN → QN↓	0.1041	0.0904	0.0869	0.0799	2.5354	2.2634	1.1568	0.5786

Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → CK	0.0469	0.0508	0.0547	0.0508
	setup↓ → CK	0.1016	0.1133	0.1211	0.1211
	hold↑ → CK	-0.0312	-0.0391	-0.0391	-0.0391
	hold↓ → CK	-0.0352	-0.0469	-0.0430	-0.0430
CK	minpwh	0.0930	0.0930	0.0882	0.0833
	minpwl	0.1368	0.1173	0.1271	0.1222
SN	minpwl	0.1028	0.0882	0.0979	0.1125
	recovery	-0.0117	0.0000	0.0000	0.0000
	removal	0.0898	0.0781	0.0820	0.0820

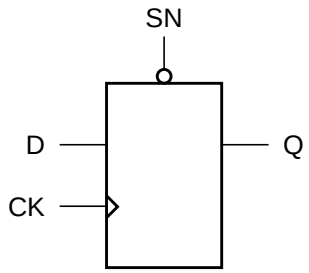
Cell Description

The DFFSHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with asynchronous active-low set (SN). The cell has a single output (Q) and fast clock-to-out path.

Functions

SN	D	CK	Q[n+1]
0	x	x	1
1	0	⎍	0
1	1	⎍	1
1	x	⎎	Q[n]

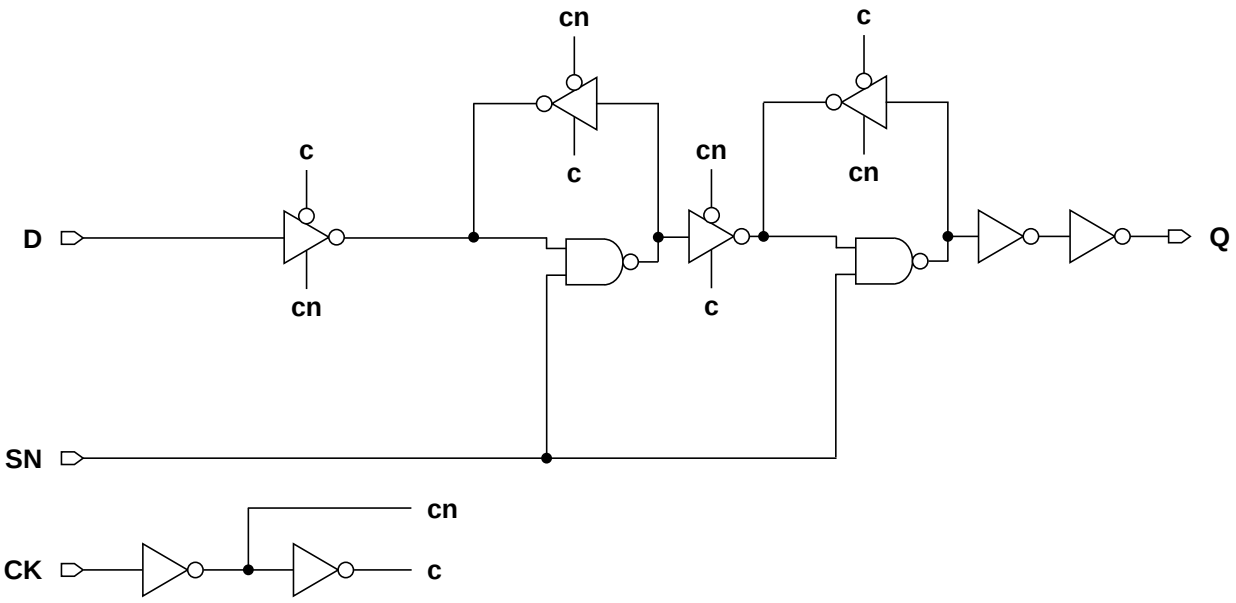
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
DFFSHQXL	5.04	11.20
DFFSHQX1	5.04	11.76
DFFSHQX2	5.04	13.44
DFFSHQX4	5.04	15.68

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
D	0.0316	0.0368	0.0498	0.0749
CK	0.0332	0.0345	0.0376	0.0537
SN	0.0087	0.0093	0.0166	0.0239
Q	0.0282	0.0300	0.0405	0.0667

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0021	0.0020	0.0023	0.0030
CK	0.0021	0.0021	0.0027	0.0042
SN	0.0076	0.0080	0.0128	0.0180

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.1920	0.1791	0.1640	0.1402	4.5046	4.0737	2.0437	1.0159
CK → Q↓	0.1992	0.1689	0.1435	0.1248	3.2560	2.7814	1.3842	0.6935
SN → Q↑	0.0608	0.0727	0.0756	0.0802	2.5712	2.1683	1.1221	0.5815

Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → CK	0.0664	0.0703	0.0664	0.0625
	setup↓ → CK	0.1562	0.1680	0.1680	0.1523
	hold↑ → CK	-0.0312	-0.0352	-0.0312	-0.0273
	hold↓ → CK	-0.0234	-0.0312	-0.0273	-0.0273
CK	minpwh	0.1028	0.0979	0.0930	0.0785
	minpwl	0.1416	0.1513	0.1271	0.1076
SN	minpwl	0.0979	0.1028	0.1222	0.1659
	recovery	0.0352	0.0430	0.0508	0.0469
	removal	0.0938	0.0938	0.1016	0.0898

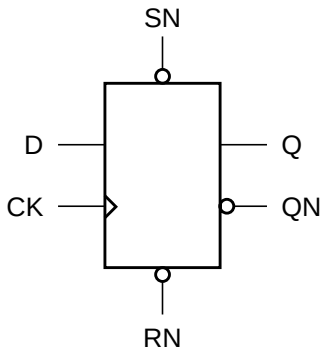
Cell Description

The DFFSR cell is a positive-edge triggered, static D-type flip-flop with asynchronous active-low reset (RN) and set (SN), and set dominating reset.

Functions

RN	SN	D	CK	Q[n+1]	QN[n+1]
0	1	x	x	0	1
1	0	x	x	1	0
0	0	x	x	1	0
1	1	0	↑	0	1
1	1	1	↑	1	0
1	1	x	↓	Q[n]	QN[n]

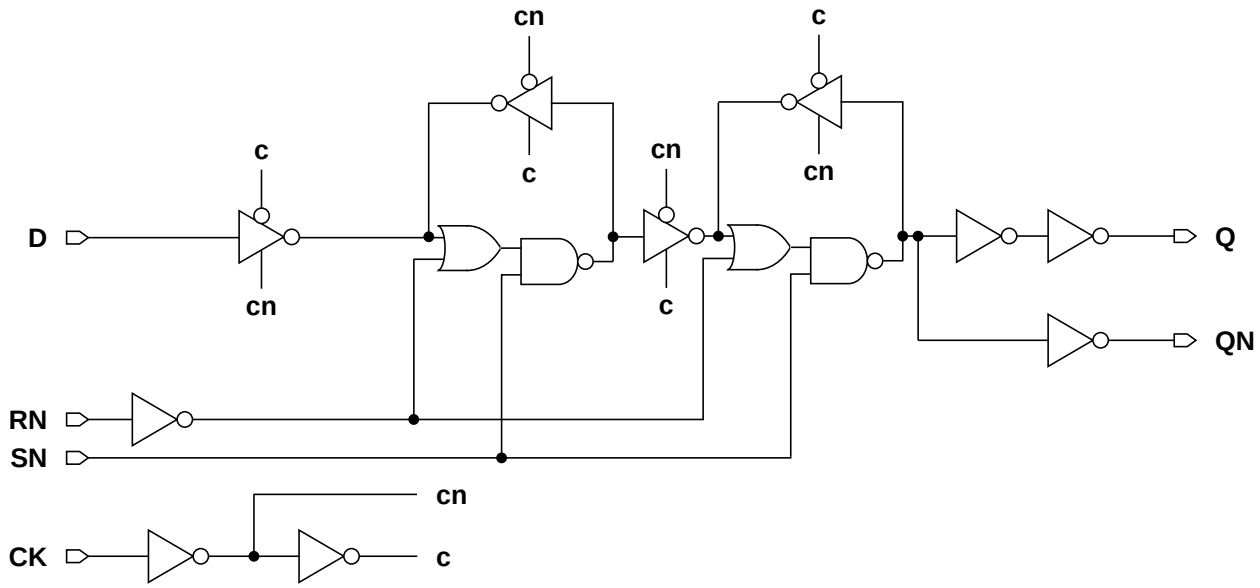
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
DFFSRXL	5.04	14.56
DFFSRX1	5.04	14.56
DFFSRX2	5.04	15.12
DFFSRX4	5.04	20.16

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
D	0.0296	0.0264	0.0311	0.0434
CK	0.0344	0.0352	0.0360	0.0463
SN	0.0081	0.0082	0.0104	0.0167
RN	0.0174	0.0184	0.0212	0.0335
Q	0.0490	0.0507	0.0767	0.1362

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0020	0.0020	0.0020	0.0028
CK	0.0023	0.0028	0.0027	0.0037
SN	0.0061	0.0064	0.0078	0.0133
RN	0.0024	0.0026	0.0032	0.0053

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.3411	0.3110	0.2991	0.2844	4.4660	3.9778	2.0190	1.0098
CK → Q↓	0.2521	0.2492	0.2405	0.2368	2.4958	2.2562	1.1520	0.5760
SN → Q↑	0.1589	0.1405	0.1400	0.1357	4.4661	3.9779	2.0190	1.0098
SN → Q↓	0.1493	0.1379	0.1412	0.1363	2.4969	2.2564	1.1521	0.5760
RN → Q↓	0.2173	0.2015	0.1953	0.1838	2.4968	2.2564	1.1521	0.5760
CK → QN↑	0.2078	0.2022	0.1834	0.1827	4.4935	3.9858	2.0224	1.0121
CK → QN↓	0.3059	0.2791	0.2583	0.2461	2.7042	2.3070	1.1704	0.5872
SN → QN↑	0.1055	0.0920	0.0849	0.0828	4.5174	3.9953	2.0269	1.0153
SN → QN↓	0.1234	0.1064	0.0984	0.0973	2.5840	2.2778	1.1591	0.5833
RN → QN↑	0.1734	0.1553	0.1388	0.1302	4.5153	3.9947	2.0266	1.0151

Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → CK	0.0625	0.0859	0.0781	0.0625
	setup↓ → CK	0.1094	0.1211	0.1250	0.1094
	hold↑ → CK	-0.0430	-0.0547	-0.0508	-0.0391
	hold↓ → CK	-0.0117	-0.0156	-0.0273	-0.0195
CK	minpwh	0.0979	0.1028	0.0882	0.0785
	minpwl	0.1611	0.1513	0.1465	0.1222
SN	minpwl	0.1222	0.1076	0.1076	0.1368
	recovery	-0.0039	0.0117	0.0117	0.0078
	removal	0.1016	0.0820	0.0820	0.0820
RN	minpwl	0.1611	0.1513	0.1611	0.2534
	recovery	0.0508	0.0781	0.0625	0.0586
	removal	-0.0352	-0.0586	-0.0469	-0.0312

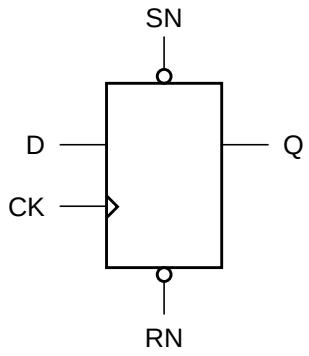
Cell Description

The DFFSRHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with asynchronous active-low reset (RN) and set (SN), and set dominating reset. The cell has a single output (Q) and fast clock-to-out path.

Functions

RN	SN	D	CK	Q[n+1]
0	1	x	x	0
1	0	x	x	1
0	0	x	x	1
1	1	0	↑	0
1	1	1	↑	1
1	1	x	↓	Q[n]

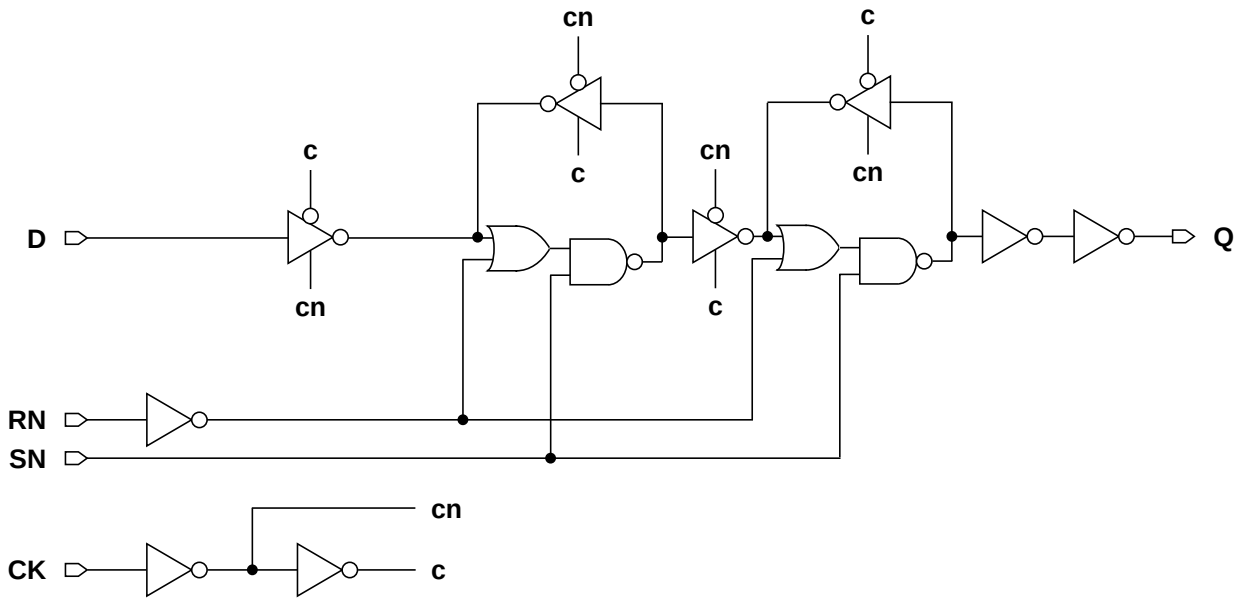
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
DFFSRHQXL	5.04	14.56
DFFSRHQX1	5.04	14.56
DFFSRHQX2	5.04	19.60
DFFSRHQX4	5.04	24.64

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
D	0.0325	0.0378	0.0570	0.0889
CK	0.0337	0.0349	0.0422	0.0595
SN	0.0107	0.0114	0.0161	0.0247
RN	0.0240	0.0258	0.0378	0.0586
Q	0.0322	0.0360	0.0502	0.0790

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0021	0.0021	0.0023	0.0034
CK	0.0021	0.0023	0.0035	0.0051
SN	0.0103	0.0106	0.0152	0.0231
RN	0.0026	0.0031	0.0044	0.0077

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.2045	0.1796	0.1666	0.1563	6.4319	5.8842	2.9169	1.4584
CK → Q↓	0.2059	0.1572	0.1339	0.1222	3.2382	2.7940	1.3760	0.6915
SN → Q↑	0.0704	0.0782	0.0884	0.0866	2.9402	2.5029	1.3230	0.6992
SN → Q↓	0.0432	0.0548	0.0456	0.0375	2.9095	2.4325	1.3170	0.6896
RN → Q↓	0.1371	0.1265	0.1000	0.0858	2.9261	2.4304	1.3142	0.6885

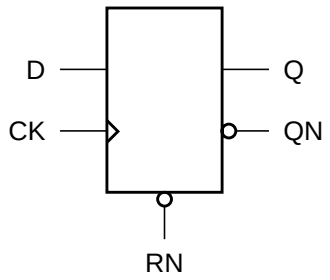
Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → CK	0.1055	0.1016	0.1055	0.1016
	setup↓ → CK	0.1523	0.1680	0.1758	0.1602
	hold↑ → CK	-0.0352	-0.0391	-0.0391	-0.0312
	hold↓ → CK	-0.0117	-0.0195	-0.0195	-0.0195
CK	minpwh	0.1028	0.0930	0.0882	0.0833
	minpwl	0.1513	0.1465	0.1222	0.1028
SN	minpwl	0.1173	0.1173	0.1805	0.2534
	recovery	0.0469	0.0586	0.0625	0.0625
	removal	0.0859	0.0742	0.0977	0.0977
RN	minpwl	0.1951	0.1902	0.2534	0.4428
	recovery	0.1133	0.1016	0.0977	0.0977
	removal	-0.0469	-0.0469	-0.0234	-0.0039

Cell Description

The DFFTR cell is a positive-edge triggered, static D-type flip-flop with synchronous active-low reset (RN).

Logic Symbol



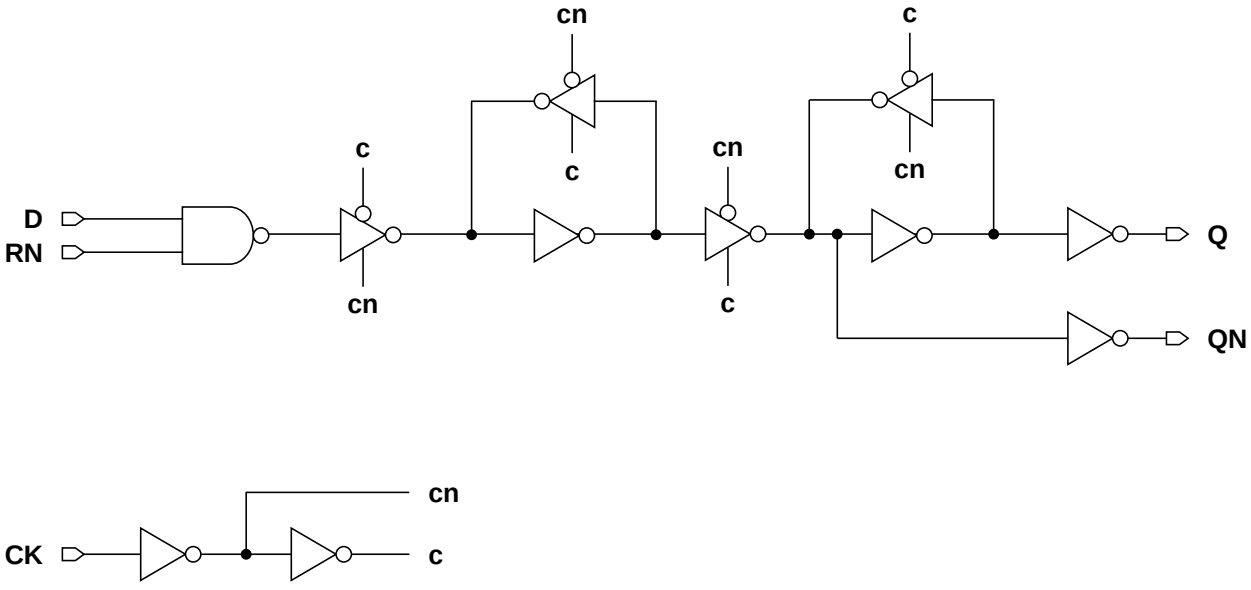
Functions

RN	D	CK	Q[n+1]	QN[n+1]
0	x	↑	0	1
x	x	↓	Q[n]	QN[n]
1	0	↑	0	1
1	1	↑	1	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
DFFTRXL	5.04	10.08
DFFTRX1	5.04	10.08
DFFTRX2	5.04	12.88
DFFTRX4	5.04	15.12

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
D	0.0312	0.0283	0.0353	0.0536
CK	0.0371	0.0374	0.0442	0.0584
RN	0.0332	0.0300	0.0372	0.0560
Q	0.0329	0.0360	0.0613	0.1073

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0029	0.0022	0.0022	0.0029
CK	0.0022	0.0029	0.0036	0.0054
RN	0.0023	0.0017	0.0017	0.0025

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.1863	0.1706	0.1634	0.1397	4.4713	3.9812	2.0216	1.0110
CK → Q↓	0.1443	0.1349	0.1246	0.1143	2.5695	2.2838	1.1646	0.5812
CK → QN↑	0.1844	0.1749	0.1692	0.1535	4.4722	3.9811	2.0194	1.0098
CK → QN↓	0.2348	0.2242	0.2223	0.1919	2.5089	2.2627	1.1524	0.5754

Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → CK	0.0469	0.0742	0.0859	0.0742
	setup↓ → CK	0.1211	0.1680	0.1758	0.1445
	hold↑ → CK	-0.0352	-0.0547	-0.0664	-0.0547
	hold↓ → CK	-0.0430	-0.0938	-0.0938	-0.0703
CK	minpwh	0.0930	0.0882	0.0882	0.0736
	minpwl	0.1513	0.1465	0.1465	0.1271
RN	setup↑ → CK	0.0547	0.0742	0.0859	0.0781
	setup↓ → CK	0.1523	0.1836	0.1914	0.1562
	hold↑ → CK	-0.0391	-0.0547	-0.0664	-0.0586
	hold↓ → CK	-0.0625	-0.1016	-0.1016	-0.0781

Cell Description

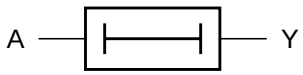
The DLY1 cell provides the logical delay of a single input (A). The output (Y) is represented by the logic equation:

$Y = A$

Functions

A	Y
0	0
1	1

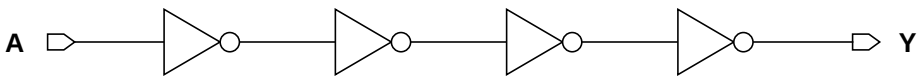
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
DLY1X1	5.04	4.48

Functional Schematic



AC Power

Pin	Power (µW/MHz)
	X1
A	0.0305

Pin Capacitance

Pin	Capacitance (pF)
	X1
A	0.0021

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)	K_{load} (ns/pF)
	X1	X1
A → Y↑	0.1079	3.2707
A → Y↓	0.1337	3.6082

Cell Description

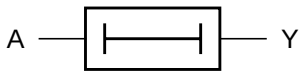
The DLY2 cell provides the logical delay of a single input (A). The output (Y) is represented by the logic equation:

$Y = A$

Functions

A	Y
0	0
1	1

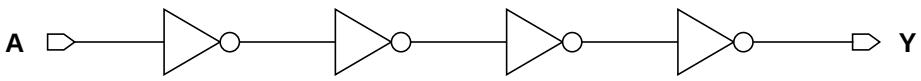
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
DLY2X1	5.04	4.48

Functional Schematic



AC Power

Pin	Power (µW/MHz)
	X1
A	0.0354

Pin Capacitance

Pin	Capacitance (pF)
	X1
A	0.0021

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)	K_{load} (ns/pF)
	X1	X1
A → Y↑	0.2219	3.2784
A → Y↓	0.2486	3.6338

Cell Description

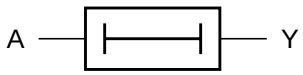
The DLY3 cell provides the logical delay of a single input (A). The output (Y) is represented by the logic equation:

$Y = A$

Functions

A	Y
0	0
1	1

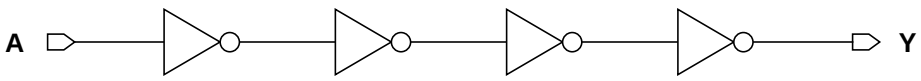
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
DLY3X1	5.04	4.48

Functional Schematic



AC Power

Pin	Power (µW/MHz)
	X1
A	0.0426

Pin Capacitance

Pin	Capacitance (pF)
	X1
A	0.0022

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)	K_{load} (ns/pF)
	X1	X1
A → Y↑	0.3740	3.2919
A → Y↓	0.3833	3.6796

Cell Description

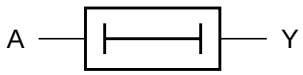
The DLY4 cell provides the logical delay of a single input (A). The output (Y) is represented by the logic equation:

$Y = A$

Functions

A	Y
0	0
1	1

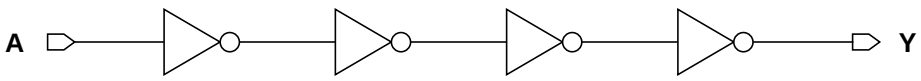
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
DLY4X1	5.04	4.48

Functional Schematic



AC Power

Pin	Power (µW/MHz)
	X1
A	0.0498

Pin Capacitance

Pin	Capacitance (pF)
	X1
A	0.0022

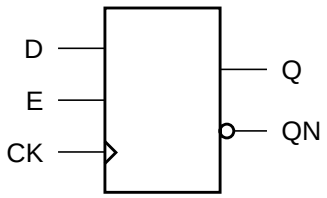
Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)	K_{load} (ns/pF)
	X1	X1
A → Y↑	0.5488	3.3119
A → Y↓	0.5233	3.7355

Cell Description

The EDFF cell is a positive-edge triggered, static D-type flip-flop with synchronous active-high enable (E).

Logic Symbol



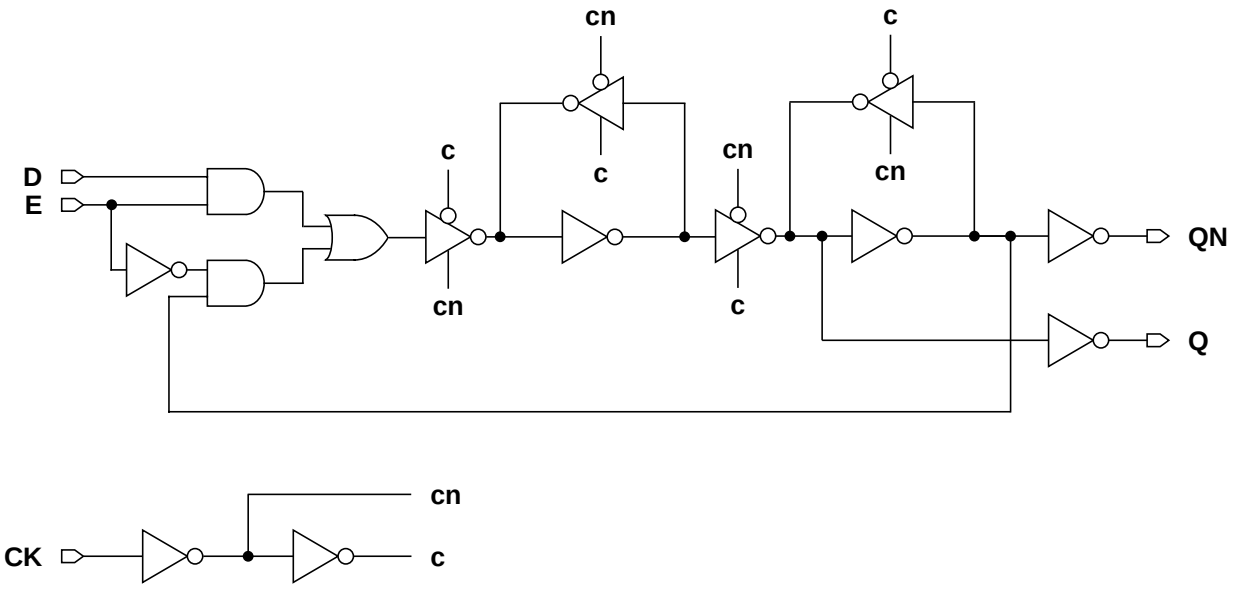
Functions

E	D	CK	Q[n+1]	QN[n+1]
0	x	x	Q[n]	QN[n]
1	0	↑	0	1
1	1	↑	1	0
1	x	↓	Q[n]	QN[n]

Cell Size

Drive Strength	Height (µm)	Width (µm)
EDFFXL	5.04	12.88
EDFFX1	5.04	12.88
EDFFX2	5.04	15.12
EDFFX4	5.04	17.36

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
D	0.0390	0.0357	0.0441	0.0683
CK	0.0454	0.0423	0.0501	0.0679
E	0.0566	0.0492	0.0585	0.0867
Q	0.0415	0.0418	0.0687	0.1198

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0032	0.0020	0.0023	0.0034
CK	0.0020	0.0028	0.0036	0.0053
E	0.0056	0.0045	0.0047	0.0056

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.2014	0.1792	0.1587	0.1415	4.4730	3.9803	2.0221	1.0114
CK → Q↓	0.1521	0.1370	0.1262	0.1166	2.5873	2.4958	1.1656	0.5825
CK → QN↑	0.2229	0.1920	0.1751	0.1652	4.4809	3.9834	2.0202	1.0105
CK → QN↓	0.2862	0.2548	0.2242	0.2021	2.5915	2.2811	1.1556	0.5771

Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → CK	0.0820	0.0938	0.1172	0.1055
	setup↓ → CK	0.1641	0.3242	0.2539	0.2109
	hold↑ → CK	-0.0625	-0.0703	-0.0898	-0.0781
	hold↓ → CK	-0.0664	-0.2227	-0.1602	-0.1250
CK	minpwh	0.1076	0.0979	0.0833	0.0736
	minpwl	0.1756	0.1562	0.1659	0.1513
E	setup↑ → CK	0.1992	0.3516	0.2812	0.2461
	setup↓ → CK	0.1289	0.2539	0.1836	0.1484
	hold↑ → CK	-0.0742	-0.0859	-0.1055	-0.0898
	hold↓ → CK	-0.0586	-0.1133	-0.1367	-0.1289

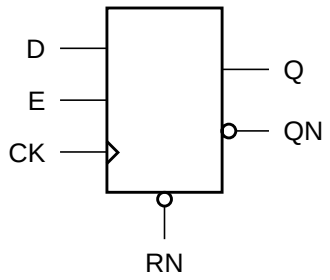
Cell Description

The EDFFTR cell is a positive-edge triggered, static D-type flip-flop with synchronous active-high enable (E) and synchronous active-low reset (RN).

Functions

RN	E	D	CK	Q[n+1]	QN[n+1]
0	x	x	↑	0	1
x	x	x	↓	Q[n]	QN[n]
1	0	x	↑	Q[n]	QN[n]
1	1	0	↑	0	1
1	1	1	↑	1	0

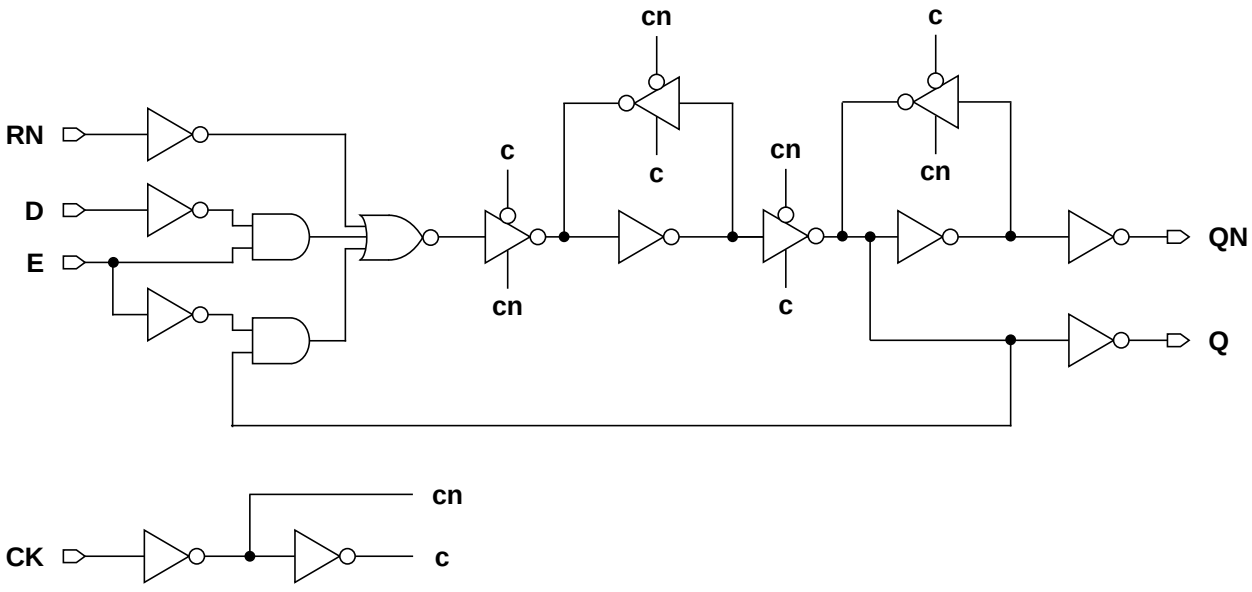
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
EDFFTRXL	5.04	14.00
EDFFTRX1	5.04	14.00
EDFFTRX2	5.04	15.68
EDFFTRX4	5.04	16.80

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
D	0.0436	0.0400	0.0488	0.0488
CK	0.0478	0.0442	0.0530	0.0587
E	0.0625	0.0544	0.0650	0.0651
RN	0.0516	0.0450	0.0545	0.0547
Q	0.0424	0.0448	0.0685	0.1144

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0032	0.0018	0.0022	0.0022
CK	0.0023	0.0030	0.0038	0.0047
E	0.0061	0.0048	0.0053	0.0053
RN	0.0029	0.0020	0.0021	0.0021

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.1980	0.1776	0.1573	0.1433	4.4767	3.9824	2.0219	1.0122
CK → Q↓	0.1537	0.1409	0.1277	0.1450	2.6027	2.2943	1.1656	0.5887
CK → QN↑	0.2343	0.1970	0.1745	0.1993	4.4795	3.9818	2.0206	1.0104
CK → QN↓	0.2924	0.2504	0.2202	0.2001	2.6029	2.2743	1.1557	0.5766

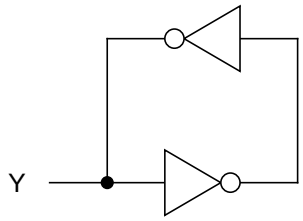
Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → CK	0.1094	0.1406	0.1523	0.1602
	setup↓ → CK	0.1914	0.3711	0.2852	0.2891
	hold↑ → CK	-0.0859	-0.1055	-0.1172	-0.1211
	hold↓ → CK	-0.0898	-0.2656	-0.1914	-0.2031
CK	minpwh	0.1028	0.0930	0.0833	0.0736
	minpwl	0.1951	0.1854	0.1902	0.1854
E	setup↑ → CK	0.2227	0.3984	0.3125	0.3164
	setup↓ → CK	0.1602	0.3086	0.2227	0.2422
	hold↑ → CK	-0.1016	-0.1328	-0.1406	-0.1406
	hold↓ → CK	-0.0859	-0.1602	-0.1758	-0.1797
RN	setup↑ → CK	0.1211	0.1562	0.1641	0.1719
	setup↓ → CK	0.1680	0.2969	0.2617	0.2656
	hold↑ → CK	-0.1055	-0.1289	-0.1328	-0.1367
	hold↓ → CK	-0.0430	-0.1797	-0.1562	-0.1758

Cell Description

The HOLD cell holds data at a known value. This cell is often used for holding data on a tri-state bus.

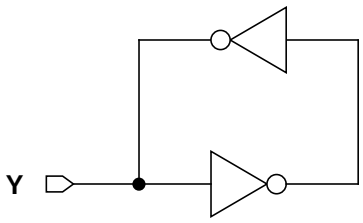
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
HOLDX1	5.04	2.24

Functional Schematic



AC Power

Pin	Power (µW/MHz)
	X1
Y	0.0245

Pin Capacitance

Pin	Capacitance (pF)
	X1
Y	0.0992

Cell Description

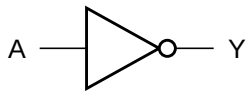
The INV cell provides the logical inversion of a single input (A). The output (Y) is represented by the logic equation:

$Y = \overline{A}$

Functions

A	Y
0	1
1	0

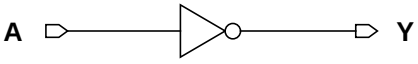
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
INVXL	5.04	1.68
INVX1	5.04	1.68
INVX2	5.04	1.68
INVX3	5.04	2.24
INVX4	5.04	2.24
INVX8	5.04	3.36
INVX12	5.04	7.28
INVX16	5.04	8.96
INVX20	5.04	10.64

Functional Schematic



AC Power

Pin	Power (μW/MHz)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A	0.0101	0.0109	0.0210	0.0304	0.0362	0.0721	0.1398	0.1940	0.2408

Pin Capacitance

Pin	Capacitance (pF)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A	0.0027	0.0031	0.0056	0.0081	0.0106	0.0214	0.0056	0.0075	0.0089

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A → Y↑	0.0229	0.0224	0.0219	0.0217	0.0188	0.0181	0.0964	0.0936	0.0929
A → Y↓	0.0132	0.0130	0.0129	0.0127	0.0109	0.0104	0.0891	0.0871	0.0860

Description	K_{load} (ns/pF)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A → Y↑	4.4624	3.9755	2.0179	1.3381	1.0090	0.4898	0.3366	0.2447	0.2017
A → Y↓	2.4460	2.2340	1.1388	0.7544	0.5697	0.2737	0.1915	0.1401	0.1149

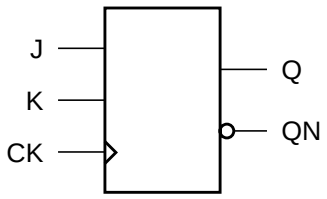
Cell Description

The JKFF cell is a positive-edge triggered JK-type flip-flop.

Functions

J	K	CK	Q[n+1]	QN[n+1]
x	x	↓	Q[n]	QN[n]
0	0	↑	Q[n]	QN[n]
0	1	↑	0	1
1	0	↑	1	0
1	1	↑	QN[n]	Q[n]

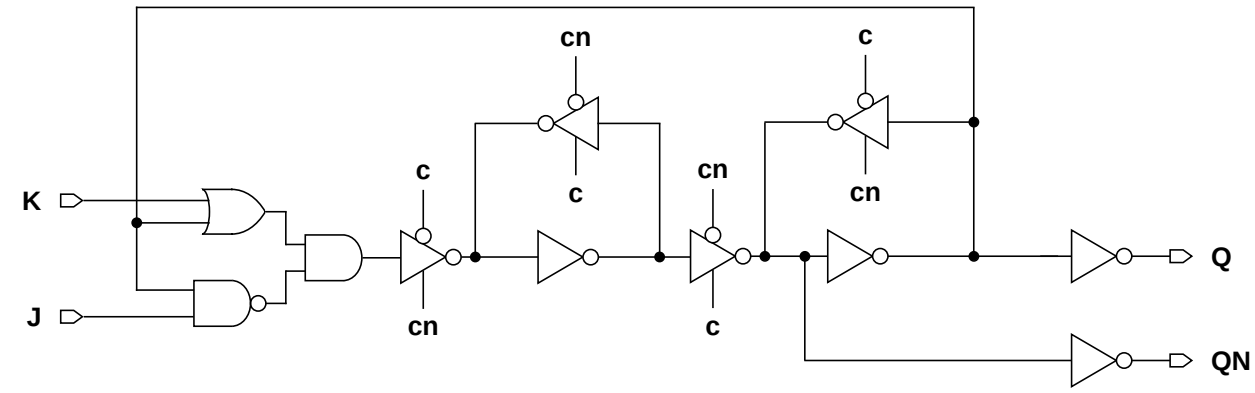
Logic Symbol

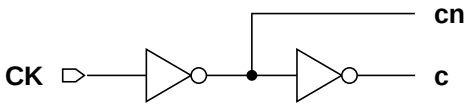


Cell Size

Drive Strength	Height (µm)	Width (µm)
JKFFXL	5.04	12.88
JKFFX1	5.04	12.88
JKFFX2	5.04	15.12
JKFFX4	5.04	17.36

Functional Schematic





AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
J	0.0316	0.0292	0.0380	0.0590
K	0.0302	0.0272	0.0359	0.0522
CK	0.0412	0.0395	0.0461	0.0630
Q	0.0485	0.0489	0.0806	0.1255

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
J	0.0015	0.0013	0.0014	0.0014
K	0.0029	0.0020	0.0022	0.0032
CK	0.0021	0.0029	0.0033	0.0055

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.2194	0.1911	0.1848	0.1522	4.4852	3.9845	2.1872	0.9887
CK → Q↓	0.2762	0.2509	0.2329	0.1943	2.6136	2.2859	1.1900	0.5526
CK → QN↑	0.1814	0.1694	0.1674	0.1370	4.4698	4.1594	2.1885	0.9897
CK → QN↓	0.1411	0.1295	0.1322	0.1086	2.9170	2.5730	1.1995	0.5573

Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
J	setup↑ → CK	0.1250	0.1953	0.1797	0.1719
	setup↓ → CK	0.1133	0.1211	0.1328	0.1367
	hold↑ → CK	-0.0625	-0.1445	-0.1250	-0.1172
	hold↓ → CK	-0.1055	-0.1133	-0.1211	-0.1250
K	setup↑ → CK	0.0742	0.0898	0.1055	0.0938
	setup↓ → CK	0.1016	0.2617	0.1719	0.1406
	hold↑ → CK	-0.0703	-0.0820	-0.0938	-0.0820
	hold↓ → CK	-0.0898	-0.2383	-0.1523	-0.1211
CK	minpwh	0.1028	0.0930	0.0979	0.0736
	minpwl	0.1611	0.1999	0.1659	0.1416

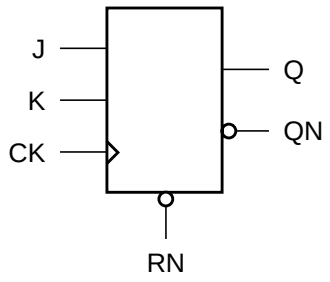
Cell Description

The JKFFR cell is a positive-edge triggered JK-type flip-flop with asynchronous active-low reset (RN).

Functions

RN	J	K	CK	Q[n+1]	QN[n+1]
1	x	x	↓	Q[n]	QN[n]
0	x	x	x	0	1
1	0	0	↑	Q[n]	QN[n]
1	0	1	↑	0	1
1	1	0	↑	1	0
1	1	1	↑	QN[n]	Q[n]

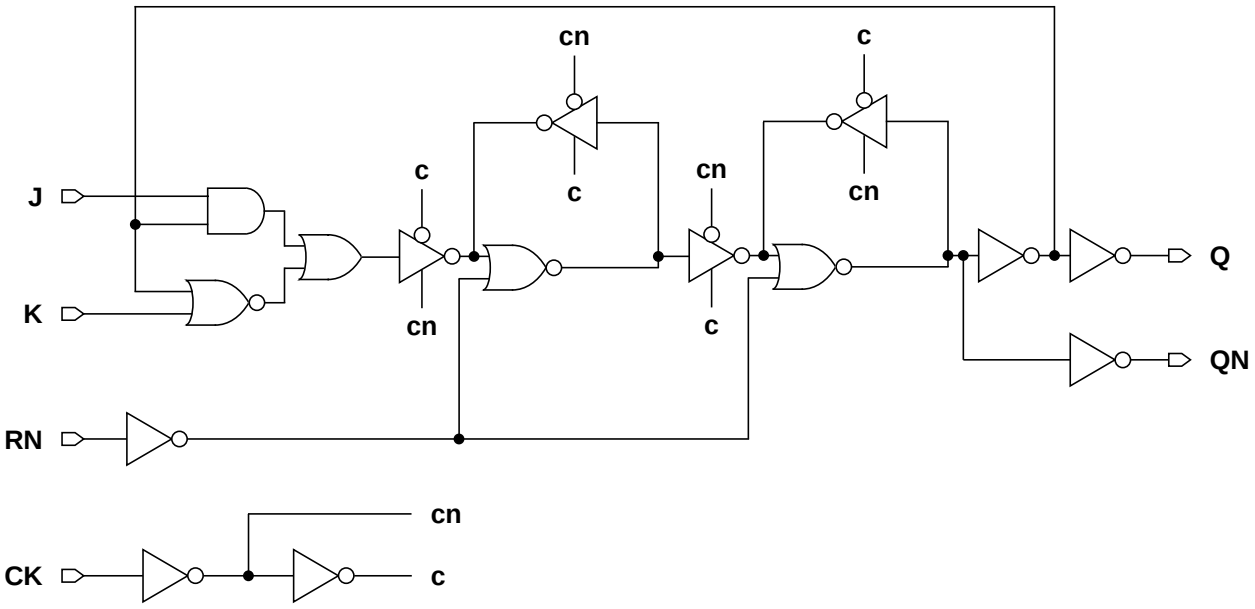
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
JKFFRXL	5.04	16.24
JKFFRX1	5.04	16.24
JKFFRX2	5.04	16.80
JKFFRX4	5.04	20.16

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
J	0.0319	0.0259	0.0285	0.0388
K	0.0382	0.0330	0.0346	0.0441
CK	0.0433	0.0406	0.0415	0.0480
RN	0.0166	0.0187	0.0206	0.0336
Q	0.0744	0.0745	0.0979	0.1509

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
J	0.0029	0.0018	0.0020	0.0023
K	0.0026	0.0026	0.0024	0.0027
CK	0.0020	0.0025	0.0028	0.0037
RN	0.0023	0.0027	0.0033	0.0050

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.3958	0.3399	0.3112	0.2802	4.4811	3.9824	1.8966	1.0161
CK → Q↓	0.3016	0.2758	0.2550	0.2390	2.6189	2.2802	1.2086	0.5634
RN → Q↓	0.2612	0.2222	0.2021	0.2000	2.6151	2.2786	1.2076	0.5630
CK → QN↑	0.1982	0.1953	0.1857	0.1645	4.4710	4.4608	2.0209	1.0161
CK → QN↓	0.3034	0.2732	0.2607	0.2293	2.8174	2.6686	1.2049	0.5668
RN → QN↑	0.1543	0.1398	0.1318	0.1245	4.4785	4.4638	2.0230	1.0171

Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
J	setup↑ → CK	0.0898	0.1016	0.1172	0.1289
	setup↓ → CK	0.0664	0.2305	0.2070	0.1484
	hold↑ → CK	-0.0820	-0.0938	-0.1055	-0.1133
	hold↓ → CK	-0.0469	-0.1992	-0.1719	-0.1172
K	setup↑ → CK	0.1172	0.2227	0.2109	0.1758
	setup↓ → CK	0.1289	0.1289	0.1328	0.1445
	hold↑ → CK	-0.0469	-0.1680	-0.1562	-0.1133
	hold↓ → CK	-0.1172	-0.1172	-0.1250	-0.1367
CK	minpwh	0.1028	0.0979	0.0930	0.0833
	minpwl	0.1805	0.1659	0.1756	0.1756
RN	minpwl	0.1513	0.1513	0.1805	0.2437
	recovery	0.0352	0.0469	0.0547	0.0547

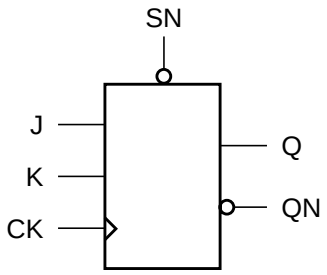
Cell Description

The JKFFS cell is a positive-edge triggered JK-type flip-flop with asynchronous active-low set (SN).

Functions

SN	J	K	CK	Q[n+1]	QN[n+1]
1	x	x	↓	Q[n]	QN[n]
0	x	x	x	1	0
1	0	0	↑	Q[n]	QN[n]
1	0	1	↑	0	1
1	1	0	↑	1	0
1	1	1	↑	QN[n]	Q[n]

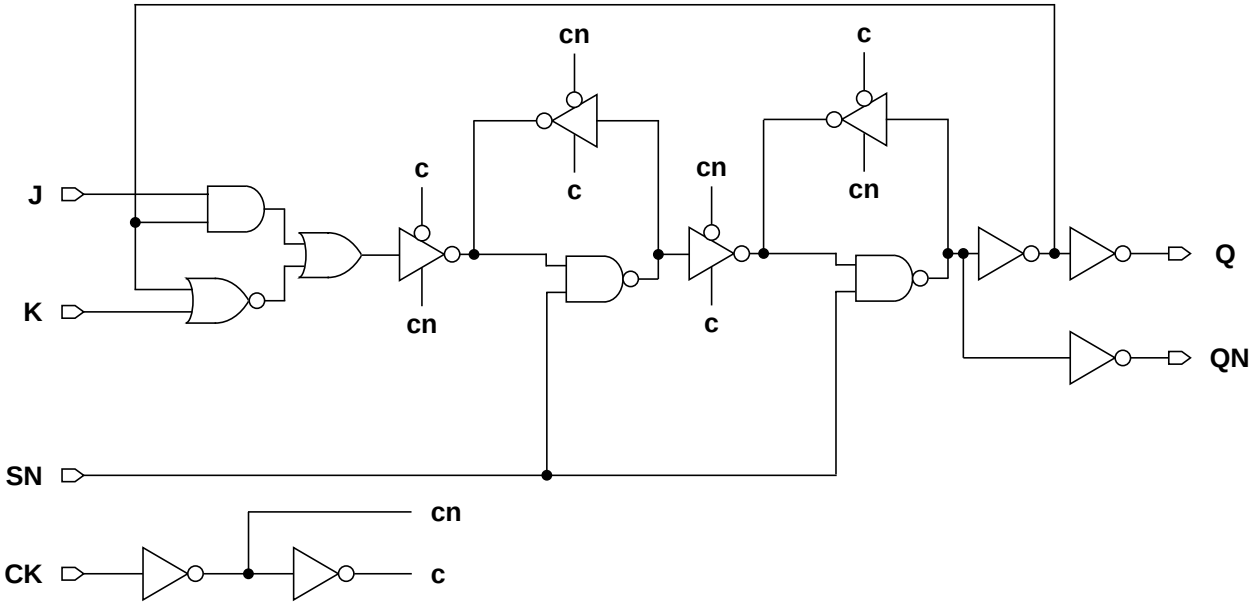
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
JKFFSXL	5.04	15.12
JKFFSX1	5.04	15.68
JKFFSX2	5.04	16.24
JKFFSX4	5.04	17.92

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
J	0.0255	0.0248	0.0268	0.0307
K	0.0346	0.0355	0.0387	0.0417
CK	0.0382	0.0405	0.0415	0.0456
SN	0.0050	0.0062	0.0079	0.0129
Q	0.0665	0.0749	0.0986	0.1418

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
J	0.0017	0.0017	0.0017	0.0020
K	0.0025	0.0024	0.0025	0.0024
CK	0.0021	0.0025	0.0028	0.0034
SN	0.0051	0.0058	0.0072	0.0112

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.3473	0.3254	0.2964	0.2724	4.4808	3.9831	2.0208	0.9995
CK → Q↓	0.3548	0.2981	0.2620	0.2350	2.6058	2.2832	1.1566	0.5952
SN → Q↑	0.1917	0.1626	0.1411	0.1273	4.4774	3.9822	2.0207	0.9994
CK → QN↑	0.2541	0.2106	0.1910	0.1689	4.4955	3.9870	2.0238	1.0008
CK → QN↓	0.2648	0.2570	0.2427	0.2242	2.5762	2.2747	1.1574	0.5952
SN → QN↓	0.1102	0.0951	0.0883	0.0801	2.5641	2.2742	1.1588	0.5969

Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
J	setup↑ → CK	0.1016	0.1094	0.1094	0.1133
	setup↓ → CK	0.2539	0.2656	0.2812	0.1680
	hold↑ → CK	-0.0938	-0.1016	-0.0977	-0.1055
	hold↓ → CK	-0.2305	-0.2422	-0.2539	-0.1445
K	setup↑ → CK	0.2500	0.2578	0.2734	0.1914
	setup↓ → CK	0.1211	0.1289	0.1289	0.1328
	hold↑ → CK	-0.1875	-0.1992	-0.2109	-0.1289
	hold↓ → CK	-0.1133	-0.1172	-0.1172	-0.1211
CK	minpwh	0.1028	0.0979	0.0930	0.0882
	minpwl	0.1854	0.1756	0.1708	0.1562
SN	minpwl	0.1222	0.1076	0.1076	0.1173
	recovery	-0.0234	-0.0117	-0.0039	-0.0078

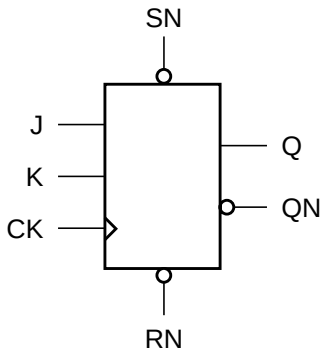
Cell Description

The JKFFSR cell is a positive-edge triggered JK-type flip-flop with asynchronous active-low reset (RN) and set (SN), and set dominating reset.

Functions

RN	SN	J	K	CK	Q[n+1]	QN[n+1]
1	1	x	x	↓	Q[n]	QN[n]
1	0	x	x	x	1	0
0	1	x	x	x	0	1
0	0	x	x	x	1	0
1	1	0	0	↑	Q[n]	QN[n]
1	1	0	1	↑	0	1
1	1	1	0	↑	1	0
1	1	1	1	↑	QN[n]	Q[n]

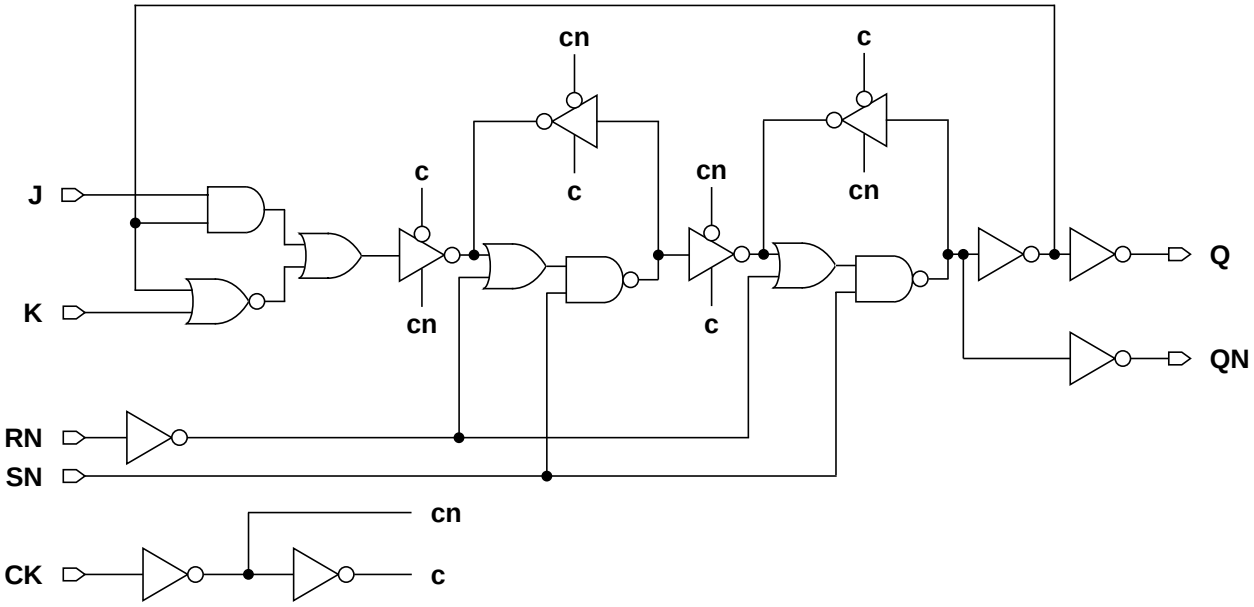
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
JKFFSRXL	5.04	17.92
JKFFSRX1	5.04	17.92
JKFFSRX2	5.04	19.04
JKFFSRX4	5.04	24.08

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
J	0.0366	0.0301	0.0327	0.0464
K	0.0408	0.0334	0.0384	0.0526
CK	0.0435	0.0406	0.0412	0.0523
SN	0.0050	0.0057	0.0075	0.0128
RN	0.0160	0.0172	0.0195	0.0323
Q	0.0766	0.0787	0.1090	0.1634

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
J	0.0029	0.0018	0.0020	0.0026
K	0.0027	0.0027	0.0027	0.0027
CK	0.0020	0.0025	0.0028	0.0040
SN	0.0044	0.0049	0.0063	0.0094
RN	0.0028	0.0032	0.0034	0.0044

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.4341	0.3728	0.3473	0.3311	4.4858	3.9850	2.0209	1.0106
CK → Q↓	0.3385	0.3040	0.2897	0.2557	2.6314	2.2856	1.1613	0.5792
SN → Q↑	0.2081	0.1719	0.1576	0.1432	4.4820	3.9839	2.0205	1.0103
SN → Q↓	0.2153	0.1778	0.1788	0.1661	2.6153	2.2786	1.1585	0.5782
RN → Q↓	0.2750	0.2340	0.2271	0.2224	2.6155	2.2788	1.1585	0.5782
CK → QN↑	0.2355	0.2233	0.2067	0.1832	4.4873	4.4636	2.0235	1.0127
CK → QN↓	0.3419	0.3078	0.2841	0.2765	2.7140	2.6811	1.1736	0.5885
SN → QN↑	0.1102	0.0958	0.0949	0.0926	4.5121	4.4731	2.0280	1.0156
SN → QN↓	0.1272	0.1099	0.0974	0.0911	2.5872	2.6536	1.1605	0.5817
RN → QN↑	0.1699	0.1520	0.1432	0.1488	4.5107	4.4727	2.0278	1.0154

Timing Constraints at 25°C, 1.8V, Typical Process

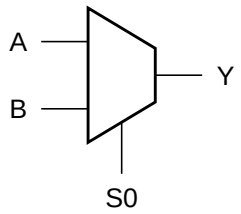
Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
J	setup↑ → CK	0.0977	0.1328	0.1328	0.1250
	setup↓ → CK	0.0703	0.2344	0.1875	0.1250
	hold↑ → CK	-0.0938	-0.1172	-0.1172	-0.1094
	hold↓ → CK	-0.0391	-0.1914	-0.1484	-0.0938
K	setup↑ → CK	0.1250	0.2461	0.2109	0.1758
	setup↓ → CK	0.1328	0.1523	0.1484	0.1523
	hold↑ → CK	-0.0469	-0.1758	-0.1406	-0.0938
	hold↓ → CK	-0.1289	-0.1328	-0.1367	-0.1445
CK	minpwh	0.1173	0.1076	0.1028	0.1028
	minpwl	0.1999	0.1999	0.1902	0.1708
SN	minpwl	0.1416	0.1173	0.1125	0.1271
	recovery	-0.0195	0.0078	0.0039	0.0078
	removal	0.1172	0.0781	0.0820	0.0977
RN	minpwl	0.1611	0.1562	0.1756	0.2485

Cell Description

The MX2 cell is a 2-to-1 multiplexer. The state of the select input (S0) determines which data input (A, B) is presented to the output (Y).The output (Y) is represented by the logic equation:

$$Y = (\overline{S0} \bullet A) + (S0 \bullet B)$$

Logic Symbol



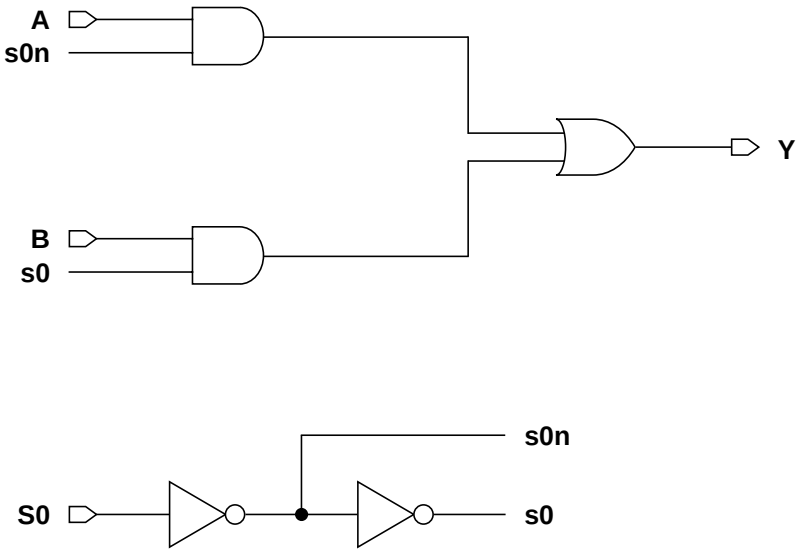
Functions

S0	A	B	Y
0	0	x	0
0	1	x	1
1	x	0	0
1	x	1	1

Cell Size

Drive Strength	Height (µm)	Width (µm)
MX2XL	5.04	5.04
MX2X1	5.04	5.04
MX2X2	5.04	5.04
MX2X4	5.04	6.16

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
S0	0.0322	0.0353	0.0567	0.0759
A	0.0232	0.0261	0.0450	0.0668
B	0.0255	0.0288	0.0504	0.0730

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
S0	0.0053	0.0056	0.0076	0.0083
A	0.0026	0.0030	0.0050	0.0057
B	0.0024	0.0027	0.0045	0.0050

Delay Tables at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)			
	XL	X1	X2	X4
S0 → Y↑	0.1096	0.1043	0.1070	0.1085
S0 → Y↓	0.1131	0.1036	0.0960	0.1078
A → Y↑	0.0895	0.0796	0.0721	0.0752
A → Y↓	0.1198	0.1097	0.0959	0.1031
B → Y↑	0.0892	0.0790	0.0716	0.0761
B → Y↓	0.1240	0.1142	0.1003	0.1133

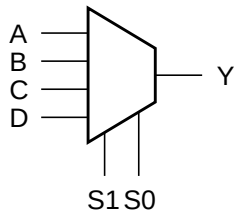
Description	K_{load} (ns/pF)			
	XL	X1	X2	X4
S0 → Y↑	4.4779	3.9816	2.0206	1.0221
S0 → Y↓	2.6406	2.2977	1.1657	0.5890
A → Y↑	4.4795	3.9817	2.0211	1.0226
A → Y↓	2.6482	2.2993	1.1654	0.5868
B → Y↑	4.4817	3.9826	2.0214	1.0229
B → Y↓	2.6603	2.3025	1.1658	0.5891

Cell Description

The MX4 cell is a 4-to-1 multiplexer. The state of the select inputs (S1, S0) determines which data input (A, B, C, D) is presented to the output (Y). The output (Y) is represented by the logic equation:

$$Y = (\overline{S0} \bullet \overline{S1} \bullet A) + (S0 \bullet \overline{S1} \bullet B) + (\overline{S0} \bullet S1 \bullet C) + (S0 \bullet S1 \bullet D)$$

Logic Symbol



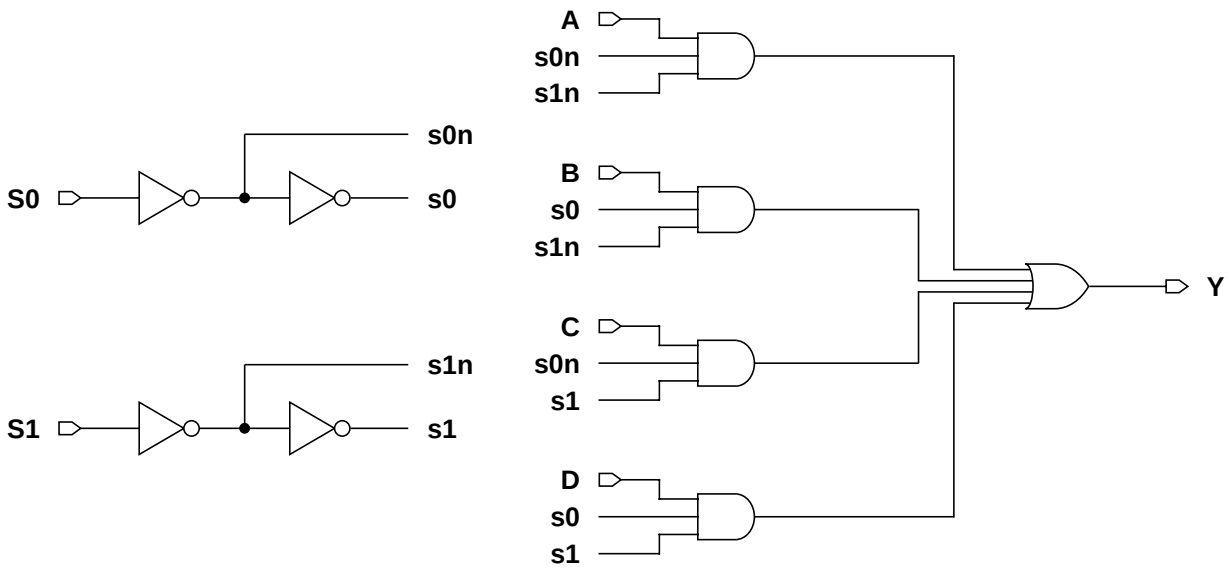
Functions

S1	S0	A	B	C	D	Y
0	0	0	x	x	x	0
0	0	1	x	x	x	1
0	1	x	0	x	x	0
0	1	x	1	x	x	1
1	0	x	x	0	x	0
1	0	x	x	1	x	1
1	1	x	x	x	0	0
1	1	x	x	x	1	1

Cell Size

Drive Strength	Height (µm)	Width (µm)
MX4XL	5.04	11.76
MX4X1	5.04	11.76
MX4X2	5.04	12.88
MX4X4	5.04	13.44

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
S0	0.0485	0.0657	0.1012	0.1291
S1	0.0286	0.0377	0.0602	0.0707
A	0.0327	0.0436	0.0695	0.0963
B	0.0347	0.0471	0.0747	0.1025
C	0.0366	0.0487	0.0807	0.1089
D	0.0392	0.0528	0.0840	0.1163

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
S0	0.0079	0.0117	0.0180	0.0180
S1	0.0047	0.0062	0.0097	0.0096
A	0.0022	0.0036	0.0057	0.0057
B	0.0020	0.0035	0.0045	0.0044
C	0.0022	0.0035	0.0055	0.0055
D	0.0020	0.0035	0.0045	0.0045

Delays at 25°C, 1.8V, Typical Process

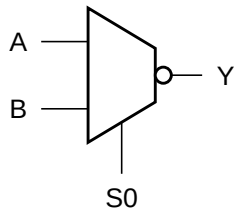
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
S0 → Y↑	0.1821	0.1484	0.1351	0.1451	4.5200	3.9910	2.0259	1.0148
S0 → Y↓	0.2010	0.1677	0.1619	0.1799	2.9942	2.3829	1.2159	0.6129
S1 → Y↑	0.1152	0.1081	0.1077	0.1165	4.5174	3.9901	2.0253	1.0148
S1 → Y↓	0.1149	0.1084	0.1063	0.1241	2.9189	2.3721	1.2120	0.6096
A → Y↑	0.1437	0.1165	0.1100	0.1199	4.5173	3.9911	2.0249	1.0143
A → Y↓	0.1879	0.1582	0.1496	0.1658	2.9562	2.3793	1.2042	0.6048
B → Y↑	0.1421	0.1150	0.1175	0.1283	4.5175	3.9909	2.0261	1.0151
B → Y↓	0.1899	0.1605	0.1667	0.1842	2.9591	2.3802	1.2146	0.6111
C → Y↑	0.1503	0.1185	0.1137	0.1243	4.5229	3.9919	2.0262	1.0150
C → Y↓	0.1981	0.1651	0.1602	0.1777	2.9968	2.3847	1.2098	0.6083
D → Y↑	0.1476	0.1157	0.1211	0.1327	4.5224	3.9916	2.0276	1.0159
D → Y↓	0.1993	0.1660	0.1765	0.1956	2.9967	2.3842	1.2206	0.6149

Cell Description

The MXI2 cell is a 2-to-1 multiplexer with inverted output. The state of the select input (S0) determines which data input (A, B) is presented to the output (Y). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{S0} \bullet A) + (S0 \bullet B)}$$

Logic Symbol



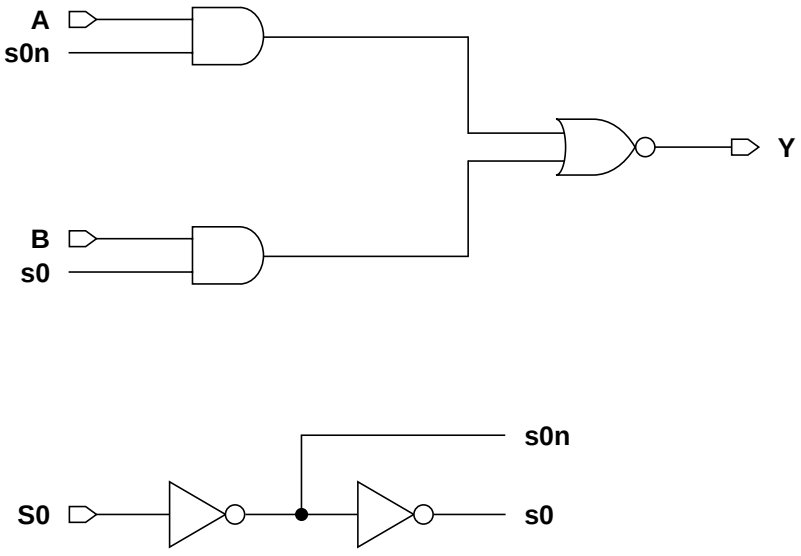
Functions

S0	A	B	Y
0	0	x	1
0	1	x	0
1	x	0	1
1	x	1	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
MXI2XL	5.04	3.92
MXI2X1	5.04	3.92
MXI2X2	5.04	5.04
MXI2X4	5.04	6.72

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
S0	0.0205	0.0267	0.0444	0.0812
A	0.0150	0.0190	0.0346	0.0736
B	0.0175	0.0226	0.0419	0.0838

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
S0	0.0050	0.0060	0.0082	0.0156
A	0.0028	0.0030	0.0053	0.0105
B	0.0028	0.0030	0.0048	0.0107

Delay Tables at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)			
	XL	X1	X2	X4
S0 → Y↑	0.0444	0.0446	0.0409	0.0432
S0 → Y↓	0.0508	0.0528	0.0534	0.0513
A → Y↑	0.0438	0.0478	0.0473	0.0462
A → Y↓	0.0314	0.0343	0.0347	0.0347
B → Y↑	0.0459	0.0503	0.0529	0.0493
B → Y↓	0.0300	0.0326	0.0336	0.0317

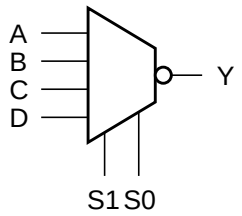
Description	K_{load} (ns/pF)			
	XL	X1	X2	X4
S0 → Y↑	6.1804	4.7825	2.6505	1.2149
S0 → Y↓	3.9184	2.8841	1.5484	0.7341
A → Y↑	6.1797	4.7971	2.5249	1.2177
A → Y↓	3.9727	2.9285	1.4979	0.7448
B → Y↑	6.1812	4.7974	2.6855	1.2178
B → Y↓	3.9693	2.9272	1.6147	0.7446

Cell Description

The MXI4 cell is a 4-to-1 multiplexer with inverted output. The state of the select inputs (S1, S0) determines which data input (A, B, C, D) is presented to the output (Y). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{S0} \bullet \overline{S1} \bullet A)+(S0 \bullet \overline{S1} \bullet B)+(\overline{S0} \bullet S1 \bullet C)+(S0 \bullet S1 \bullet D)}$$

Logic Symbol



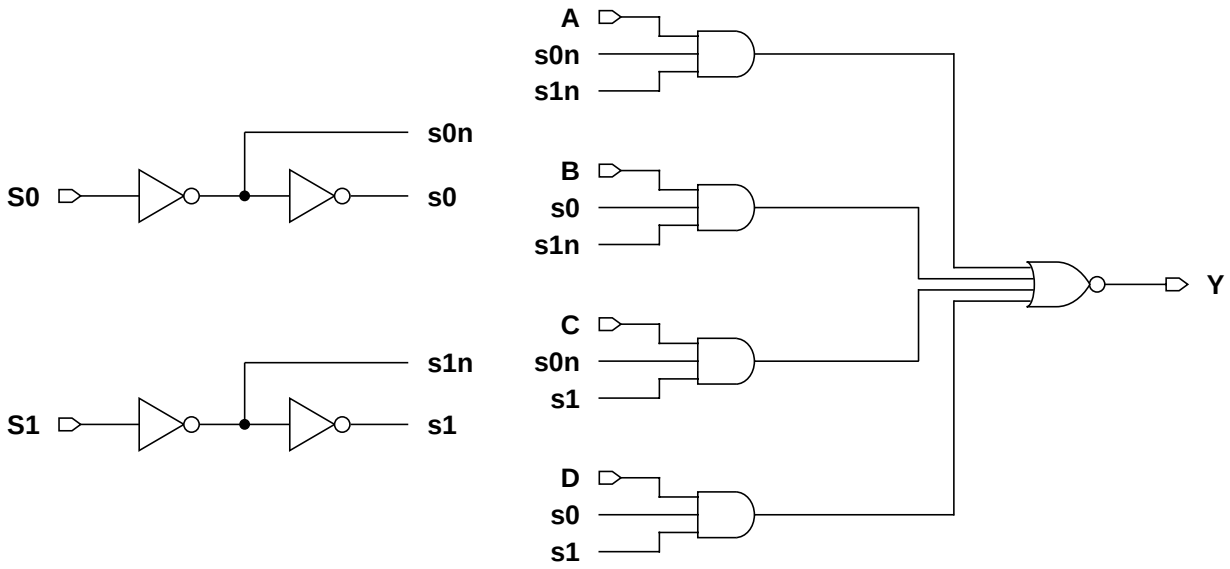
Functions

S1	S0	A	B	C	D	Y
0	0	0	x	x	x	1
0	0	1	x	x	x	0
0	1	x	0	x	x	1
0	1	x	1	x	x	0
1	0	x	x	0	x	1
1	0	x	x	1	x	0
1	1	x	x	x	0	1
1	1	x	x	x	1	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
MXI4XL	5.04	12.32
MXI4X1	5.04	12.32
MXI4X2	5.04	13.44
MXI4X4	5.04	14.00

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
S0	0.0554	0.0596	0.0979	0.1331
S1	0.0312	0.0357	0.0553	0.0739
A	0.0399	0.0449	0.0782	0.1051
B	0.0423	0.0474	0.0831	0.1096
C	0.0354	0.0397	0.0673	0.0917
D	0.0377	0.0423	0.0711	0.0956

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
S0	0.0079	0.0081	0.0120	0.0139
S1	0.0037	0.0039	0.0046	0.0048
A	0.0022	0.0023	0.0036	0.0044
B	0.0022	0.0023	0.0037	0.0045
C	0.0025	0.0026	0.0039	0.0048
D	0.0021	0.0022	0.0036	0.0044

Delays at 25°C, 1.8V, Typical Process

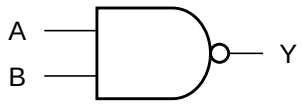
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
S0 → Y↑	0.2096	0.2006	0.1769	0.1739	4.4848	3.9846	2.0215	1.0117
S0 → Y↓	0.2311	0.2230	0.1978	0.2012	2.6666	2.3067	1.1684	0.5885
S1 → Y↑	0.1112	0.1066	0.1055	0.1061	4.4831	3.9835	2.0209	1.0113
S1 → Y↓	0.1133	0.1067	0.0953	0.1020	2.6569	2.3034	1.1654	0.5869
A → Y↑	0.2089	0.1986	0.1787	0.1783	4.4847	3.9844	2.0214	1.0117
A → Y↓	0.1970	0.1868	0.1678	0.1725	2.6662	2.3066	1.1683	0.5885
B → Y↑	0.2107	0.2006	0.1809	0.1785	4.4847	3.9845	2.0214	1.0116
B → Y↓	0.1953	0.1851	0.1661	0.1698	2.6662	2.3065	1.1683	0.5885
C → Y↑	0.1945	0.1849	0.1575	0.1560	4.4840	3.9842	2.0213	1.0114
C → Y↓	0.1881	0.1788	0.1534	0.1601	2.6640	2.3056	1.1657	0.5877
D → Y↑	0.1953	0.1861	0.1577	0.1575	4.4840	3.9841	2.0213	1.0114
D → Y↓	0.1859	0.1769	0.1508	0.1582	2.6641	2.3056	1.1656	0.5877

Cell Description

The NAND2 cell provides the logical NAND of two inputs (A, B). The output (Y) is represented by the logic equation:

$Y = \overline{(A \bullet B)}$

Logic Symbol



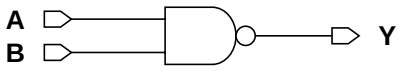
Functions

A	B	Y
0	x	1
x	0	1
1	1	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
NAND2XL	5.04	1.68
NAND2X1	5.04	2.24
NAND2X2	5.04	3.36
NAND2X4	5.04	4.48

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A	0.0129	0.0128	0.0226	0.0460
B	0.0163	0.0163	0.0314	0.0626

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A	0.0032	0.0035	0.0062	0.0131
B	0.0032	0.0032	0.0070	0.0126

Delay at 25^{o}C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)			
	XL	X1	X2	X4
A → Y↑	0.0302	0.0278	0.0250	0.0245
A → Y↓	0.0202	0.0175	0.0156	0.0157
B → Y↑	0.0368	0.0335	0.0322	0.0307
B → Y↓	0.0240	0.0215	0.0209	0.0204

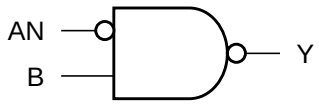
Description	K_{load} (ns/pF)			
	XL	X1	X2	X4
A → Y↑	4.4673	4.0656	2.0327	0.9854
A → Y↓	2.9919	2.7225	1.3613	0.6852
B → Y↑	4.4625	4.0627	2.0322	0.9849
B → Y↓	3.0075	2.7265	1.3635	0.6863

Cell Description

The NAND2B cell provides the logical NAND of one inverted input (AN) and one non-inverted input (B). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{AN} \bullet B)}$$

Logic Symbol



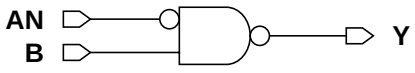
Functions

AN	B	Y
1	x	1
x	0	1
0	1	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
NAND2BXL	5.04	2.80
NAND2BX1	5.04	2.80
NAND2BX2	5.04	3.92
NAND2BX4	5.04	5.04

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
AN	0.0184	0.0197	0.0324	0.0589
B	0.0131	0.0143	0.0266	0.0492

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
AN	0.0022	0.0022	0.0029	0.0051
B	0.0029	0.0032	0.0070	0.0123

Delays at 25°C, 1.8V, Typical Process

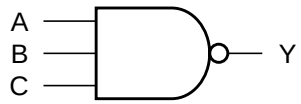
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
AN → Y↑	0.0557	0.0572	0.0589	0.0543	4.4696	4.0668	2.0338	1.0129
AN → Y↓	0.0690	0.0714	0.0767	0.0707	3.0289	2.7370	1.3703	0.7271
B → Y↑	0.0337	0.0341	0.0321	0.0298	4.4637	4.0643	2.0329	1.0125
B → Y↓	0.0236	0.0240	0.0234	0.0229	3.0151	2.7307	1.3661	0.7255

Cell Description

The NAND3 cell provides the logical NAND of three inputs (A, B, C). The output (Y) is represented by the logic equation:

$$Y = \overline{(A \bullet B \bullet C)}$$

Logic Symbol



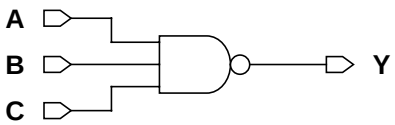
Functions

A	B	C	Y
0	x	x	1
x	0	x	1
x	x	0	1
1	1	1	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
NAND3XL	5.04	2.24
NAND3X1	5.04	2.24
NAND3X2	5.04	3.92
NAND3X4	5.04	6.16

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A	0.0169	0.0176	0.0271	0.0550
B	0.0219	0.0230	0.0365	0.0723
C	0.0254	0.0270	0.0465	0.0901

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A	0.0039	0.0041	0.0067	0.0138
B	0.0038	0.0040	0.0075	0.0136
C	0.0035	0.0037	0.0082	0.0136

Delays at 25^{o}C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)			
	XL	X1	X2	X4
A → Y↑	0.0368	0.0374	0.0300	0.0301
A → Y↓	0.0282	0.0264	0.0194	0.0202
B → Y↑	0.0433	0.0452	0.0389	0.0381
B → Y↓	0.0354	0.0337	0.0272	0.0275
C → Y↑	0.0495	0.0515	0.0470	0.0456
C → Y↓	0.0375	0.0359	0.0307	0.0308

Description	K_{load} (ns/pF)			
	XL	X1	X2	X4
A → Y↑	3.9013	3.8139	2.0190	1.0322
A → Y↓	3.3470	3.0270	1.5131	0.8075
B → Y↑	3.8167	3.8119	2.0186	1.0317
B → Y↓	3.3557	3.0312	1.5156	0.8086
C → Y↑	3.9009	3.8136	2.0200	1.0324
C → Y↓	3.3548	3.0310	1.5158	0.8086

Cell Description

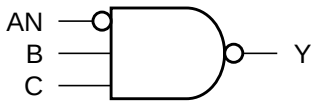
The NAND3B cell provides the logical NAND of one inverted input (AN) and two non-inverted inputs (B, C). The output (Y) is represented by the logic equation:

$$Y = (\overline{\overline{AN} \bullet B \bullet C})$$

Functions

AN	B	C	Y
1	x	x	1
x	0	x	1
x	x	0	1
0	1	1	0

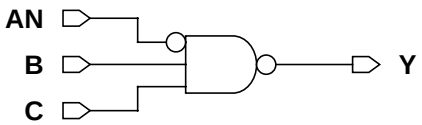
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
NAND3BXL	5.04	3.36
NAND3BX1	5.04	3.36
NAND3BX2	5.04	4.48
NAND3BX4	5.04	7.28

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
AN	0.0227	0.0236	0.0375	0.0731
B	0.0154	0.0172	0.0306	0.0585
C	0.0194	0.0214	0.0399	0.0753

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
AN	0.0023	0.0023	0.0032	0.0055
B	0.0032	0.0035	0.0073	0.0134
C	0.0034	0.0036	0.0084	0.0135

Delays at 25^{o}C, 1.8V, Typical Process

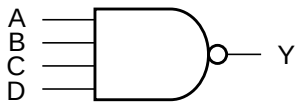
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
AN → Y↑	0.0660	0.0670	0.0619	0.0630	4.4715	3.9797	2.0200	1.0443
AN → Y↓	0.0795	0.0816	0.0756	0.0768	3.3701	3.0382	1.5193	0.8104
B → Y↑	0.0421	0.0422	0.0381	0.0382	4.4676	3.9780	2.0196	1.0440
B → Y↓	0.0314	0.0321	0.0291	0.0301	3.3610	3.0344	1.5174	0.8096
C → Y↑	0.0503	0.0500	0.0467	0.0467	4.4711	3.9797	2.0206	1.0444
C → Y↓	0.0352	0.0357	0.0334	0.0346	3.3618	3.0346	1.5177	0.8097

Cell Description

The NAND4 cell provides a logical NAND of four inputs (A, B, C, D). The output (Y) is represented by the logic equation:

$$Y = \overline{(A \bullet B \bullet C \bullet D)}$$

Logic Symbol



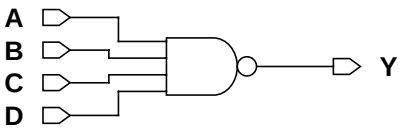
Functions

A	B	C	D	Y
0	x	x	x	1
x	0	x	x	1
x	x	0	x	1
x	x	x	0	1
1	1	1	1	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
NAND4XL	5.04	3.36
NAND4X1	5.04	3.36
NAND4X2	5.04	5.60
NAND4X4	5.04	9.52

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A	0.0163	0.0176	0.0318	0.0618
B	0.0214	0.0233	0.0428	0.0823
C	0.0262	0.0284	0.0514	0.0980
D	0.0308	0.0335	0.0641	0.1228

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A	0.0036	0.0038	0.0073	0.0155
B	0.0036	0.0038	0.0077	0.0153
C	0.0036	0.0039	0.0081	0.0158
D	0.0034	0.0038	0.0085	0.0170

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)			
	XL	X1	X2	X4
A → Y↑	0.0395	0.0395	0.0348	0.0347
A → Y↓	0.0264	0.0263	0.0228	0.0234
B → Y↑	0.0493	0.0492	0.0448	0.0439
B → Y↓	0.0360	0.0361	0.0329	0.0330
C → Y↑	0.0586	0.0584	0.0547	0.0530
C → Y↓	0.0418	0.0417	0.0392	0.0388
D → Y↑	0.0667	0.0665	0.0641	0.0624
D → Y↓	0.0450	0.0448	0.0435	0.0434

Delays at 25°C, 1.8V, Typical Process

Description	K_{load} (ns/pF)			
	XL	X1	X2	X4
A → Y↑	4.4698	4.0668	2.0196	1.0210
A → Y↓	3.6555	3.3482	1.6740	0.8664
B → Y↑	4.4648	4.0645	2.0186	1.0204
B → Y↓	3.6639	3.3523	1.6763	0.8675
C → Y↑	4.4702	4.0670	2.0202	1.0211
C → Y↓	3.6640	3.3525	1.6764	0.8675
D → Y↑	4.4840	4.0732	2.0238	1.0229
D → Y↓	3.6642	3.3524	1.6767	0.8677

Cell Description

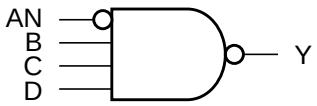
The NAND4B cell provides a logical NAND of one inverted input (AN) and three non-inverted inputs (B, C, D). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{AN} \bullet B \bullet C \bullet D)}$$

Functions

AN	B	C	D	Y
1	x	x	x	1
x	0	x	x	1
x	x	0	x	1
x	x	x	0	1
0	1	1	1	0

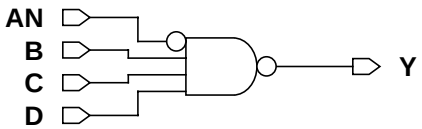
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
NAND4BXL	5.04	3.92
NAND4BX1	5.04	3.92
NAND4BX2	5.04	5.60
NAND4BX4	5.04	10.08

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
AN	0.0226	0.0234	0.0425	0.0839
B	0.0187	0.0198	0.0353	0.0686
C	0.0229	0.0243	0.0445	0.0856
D	0.0275	0.0294	0.0553	0.1065

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
AN	0.0022	0.0021	0.0034	0.0058
B	0.0037	0.0039	0.0075	0.0154
C	0.0035	0.0037	0.0080	0.0158
D	0.0036	0.0038	0.0087	0.0171

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
AN → Y↑	0.0679	0.0687	0.0663	0.0659	4.3646	4.0672	2.0200	1.0214
AN → Y↓	0.0790	0.0793	0.0794	0.0789	3.6705	3.3554	1.7367	0.8684
B → Y↑	0.0479	0.0482	0.0435	0.0431	4.3640	4.0669	2.0197	1.0211
B → Y↓	0.0378	0.0376	0.0355	0.0350	3.6691	3.3546	1.7362	0.8682
C → Y↑	0.0577	0.0581	0.0531	0.0526	4.3671	4.0683	2.0205	1.0215
C → Y↓	0.0447	0.0443	0.0424	0.0418	3.6692	3.3548	1.7364	0.8683
D → Y↑	0.0663	0.0674	0.0629	0.0622	4.3795	4.0744	2.0238	1.0230
D → Y↓	0.0485	0.0482	0.0470	0.0462	3.6698	3.3550	1.7366	0.8684

Cell Description

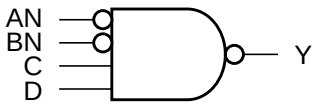
The NAND4BB cell provides a logical NAND of two inverted inputs (AN, BN) and two non-inverted inputs (C, D). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{AN} \bullet \overline{BN} \bullet C \bullet D)}$$

Functions

AN	BN	C	D	Y
1	x	x	x	1
x	1	x	x	1
x	x	0	x	1
x	x	x	0	1
0	0	1	1	0

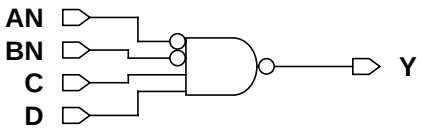
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
NAND4BBXL	5.04	5.04
NAND4BBX1	5.04	5.04
NAND4BBX2	5.04	6.72
NAND4BBX4	5.04	11.20

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
AN	0.0236	0.0247	0.0435	0.0849
BN	0.0284	0.0301	0.0509	0.1012
C	0.0204	0.0221	0.0405	0.0782
D	0.0249	0.0269	0.0498	0.0965

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
AN	0.0021	0.0021	0.0033	0.0058
BN	0.0022	0.0022	0.0030	0.0058
C	0.0034	0.0038	0.0082	0.0162
D	0.0034	0.0037	0.0086	0.0173

Delays at 25°C, 1.8V, Typical Process

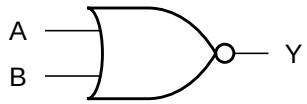
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
AN → Y↑	0.0709	0.0724	0.0675	0.0671	4.4690	4.0669	2.0202	1.0158
AN → Y↓	0.0805	0.0828	0.0789	0.0770	3.6676	3.3546	1.6779	0.8390
BN → Y↑	0.0834	0.0847	0.0786	0.0790	4.4709	4.0675	2.0198	1.0158
BN → Y↓	0.0937	0.0961	0.0902	0.0900	3.6812	3.3608	1.6804	0.8403
C → Y↑	0.0597	0.0595	0.0541	0.0539	4.4764	4.0701	2.0217	1.0165
C → Y↓	0.0469	0.0472	0.0434	0.0434	3.6725	3.3566	1.6786	0.8393
D → Y↑	0.0684	0.0684	0.0640	0.0640	4.4871	4.0752	2.0245	1.0179
D → Y↓	0.0505	0.0509	0.0484	0.0486	3.6727	3.3568	1.6789	0.8395

Cell Description

The NOR2 cell provides a logical NOR of two inputs (A, B). The output (Y) is represented by the logic equation:

$Y = \overline{(A + B)}$

Logic Symbol



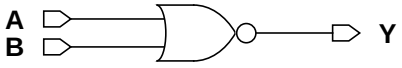
Functions

A	B	Y
0	0	1
x	1	0
1	x	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
NOR2XL	5.04	2.24
NOR2X1	5.04	2.24
NOR2X2	5.04	2.80
NOR2X4	5.04	4.48

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A	0.0132	0.0139	0.0251	0.0509
B	0.0159	0.0168	0.0316	0.0635

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A	0.0033	0.0035	0.0066	0.0137
B	0.0031	0.0033	0.0069	0.0129

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)			
	XL	X1	X2	X4
A → Y↑	0.0360	0.0357	0.0304	0.0319
A → Y↓	0.0172	0.0170	0.0151	0.0157
B → Y↑	0.0432	0.0429	0.0393	0.0400
B → Y↓	0.0205	0.0204	0.0195	0.0197

Description	K_{load} (ns/pF)			
	XL	X1	X2	X4
A → Y↑	6.4193	5.8828	2.8933	1.4574
A → Y↓	2.4454	2.2337	1.1388	0.5694
B → Y↑	6.4119	5.8795	2.8928	1.4569
B → Y↓	2.4519	2.2368	1.1404	0.5702

Cell Description

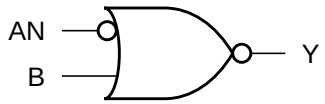
The NOR2B cell provides a logical NOR of one inverted input (AN) and one non-inverted input (B). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{AN} + B)}$$

Functions

AN	B	Y
1	0	1
x	1	0
0	x	0

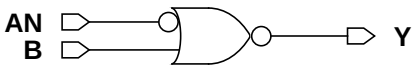
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
NOR2BXL	5.04	2.80
NOR2BX1	5.04	2.80
NOR2BX2	5.04	3.36
NOR2BX4	5.04	5.60

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
AN	0.0188	0.0193	0.0297	0.0624
B	0.0158	0.0165	0.0319	0.0650

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
AN	0.0023	0.0023	0.0031	0.0055
B	0.0032	0.0034	0.0072	0.0130

Delays at 25°C, 1.8V, Typical Process

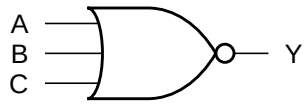
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
AN → Y↑	0.0639	0.0640	0.0592	0.0616	6.4220	5.8839	2.8939	1.4577
AN → Y↓	0.0740	0.0756	0.0748	0.0753	2.4907	2.2546	1.1497	0.5747
B → Y↑	0.0439	0.0435	0.0409	0.0420	6.4137	5.8804	2.8934	1.4571
B → Y↓	0.0201	0.0199	0.0194	0.0197	2.4539	2.2376	1.1409	0.5704

Cell Description

The NOR3 cell provides a logical NOR of three inputs (A, B, C). The output (Y) is represented by the logic equation:

$$Y = \overline{(A + B + C)}$$

Logic Symbol



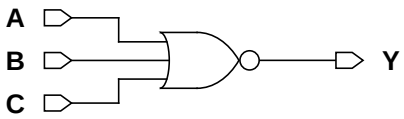
Functions

A	B	C	Y
0	0	0	1
x	x	1	0
x	1	x	0
1	x	x	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
NOR3XL	5.04	2.80
NOR3X1	5.04	2.80
NOR3X2	5.04	4.48
NOR3X4	5.04	6.16

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A	0.0181	0.0194	0.0357	0.0599
B	0.0210	0.0226	0.0428	0.0728
C	0.0254	0.0275	0.0529	0.0878

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A	0.0040	0.0043	0.0078	0.0144
B	0.0035	0.0038	0.0082	0.0138
C	0.0035	0.0038	0.0083	0.0136

Delays at 25^{o}C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)			
	XL	X1	X2	X4
A → Y↑	0.0497	0.0490	0.0416	0.0424
A → Y↓	0.0228	0.0218	0.0195	0.0190
B → Y↑	0.0673	0.0665	0.0612	0.0607
B → Y↓	0.0271	0.0270	0.0256	0.0242
C → Y↑	0.0746	0.0739	0.0698	0.0690
C → Y↓	0.0292	0.0296	0.0297	0.0280

Description	K_{load} (ns/pF)			
	XL	X1	X2	X4
A → Y↑	7.4509	6.7762	3.3872	1.9809
A → Y↓	2.4406	2.2343	1.1388	0.6252
B → Y↑	7.4406	6.7716	3.3860	1.9799
B → Y↓	2.4530	2.2373	1.1407	0.6261
C → Y↑	7.4394	6.7711	3.3863	1.9800
C → Y↓	2.4907	2.2539	1.1472	0.6291

Cell Description

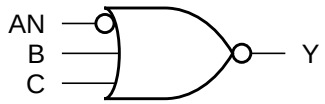
The NOR3B cell provides a logical NOR of one inverted input (AN) and two non-inverted inputs (B, C). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{AN} + B + C)}$$

Functions

AN	B	C	Y
1	0	0	1
x	x	1	0
x	1	x	0
0	x	x	0

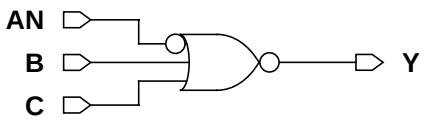
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
NOR3BXL	5.04	3.36
NOR3BX1	5.04	3.36
NOR3BX2	5.04	5.04
NOR3BX4	5.04	7.28

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
AN	0.0215	0.0224	0.0362	0.0648
B	0.0211	0.0227	0.0427	0.0719
C	0.0249	0.0269	0.0533	0.0875

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
AN	0.0022	0.0022	0.0035	0.0054
B	0.0036	0.0039	0.0081	0.0136
C	0.0036	0.0038	0.0088	0.0141

Delays at 25^{o}C, 1.8V, Typical Process

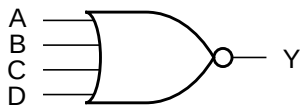
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
AN → Y↑	0.0781	0.0785	0.0704	0.0691	7.4504	6.7760	3.3877	1.9590
AN → Y↓	0.0841	0.0869	0.0802	0.0797	2.4893	2.2540	1.1481	0.6736
B → Y↑	0.0684	0.0678	0.0628	0.0606	7.4424	6.7724	3.3862	1.9581
B → Y↓	0.0269	0.0269	0.0255	0.0252	2.4558	2.2386	1.1412	0.6702
C → Y↑	0.0757	0.0752	0.0726	0.0700	7.4406	6.7717	3.3871	1.9584
C → Y↓	0.0291	0.0296	0.0302	0.0299	2.4912	2.2541	1.1474	0.6732

Cell Description

The NOR4 cell provides a logical NOR of four inputs (A, B, C, D). The output (Y) is represented by the logic equation:

$$Y = \overline{(A + B + C + D)}$$

Logic Symbol



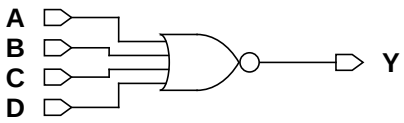
Functions

A	B	C	D	Y
0	0	0	0	1
x	x	x	1	0
x	x	1	x	0
x	1	x	x	0
1	x	x	x	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
NOR4XL	5.04	3.36
NOR4X1	5.04	3.36
NOR4X2	5.04	5.60
NOR4X4	5.04	10.08

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A	0.0197	0.0212	0.0404	0.0798
B	0.0239	0.0259	0.0505	0.0996
C	0.0274	0.0297	0.0587	0.1151
D	0.0326	0.0354	0.0711	0.1392

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A	0.0042	0.0046	0.0079	0.0165
B	0.0039	0.0042	0.0085	0.0180
C	0.0039	0.0042	0.0091	0.0181
D	0.0037	0.0040	0.0095	0.0186

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)			
	XL	X1	X2	X4
A → Y↑	0.0569	0.0556	0.0478	0.0494
A → Y↓	0.0243	0.0232	0.0214	0.0215
B → Y↑	0.0859	0.0846	0.0806	0.0825
B → Y↓	0.0295	0.0294	0.0288	0.0288
C → Y↑	0.1042	0.1028	0.0996	0.1006
C → Y↓	0.0332	0.0337	0.0332	0.0327
D → Y↑	0.1111	0.1098	0.1093	0.1109
D → Y↓	0.0336	0.0349	0.0353	0.0350

Delays at 25°C, 1.8V, Typical Process

Description	K_{load} (ns/pF)			
	XL	X1	X2	X4
A → Y↑	9.1566	8.2853	4.1412	2.1204
A → Y↓	2.4409	2.2344	1.1389	0.5694
B → Y↑	9.1451	8.2804	4.1407	2.1201
B → Y↓	2.4533	2.2374	1.1408	0.5704
C → Y↑	9.1458	8.2806	4.1404	2.1198
C → Y↓	2.4830	2.2535	1.1500	0.5749
D → Y↑	9.1437	8.2798	4.1414	2.1204
D → Y↓	2.5254	2.2732	1.1598	0.5797

Cell Description

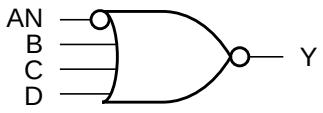
The NOR4B cell provides a logical NOR of one inverted input (AN) and three non-inverted inputs (B, C, D). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{AN} + B + C + D)}$$

Functions

AN	B	C	D	Y
1	0	0	0	1
x	x	x	1	0
x	x	1	x	0
x	1	x	x	0
0	x	x	x	0

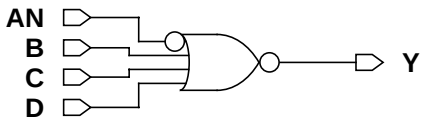
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
NOR4BXL	5.04	3.92
NOR4BX1	5.04	3.92
NOR4BX2	5.04	6.16
NOR4BX4	5.04	11.20

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
AN	0.0238	0.0247	0.0411	0.0774
B	0.0238	0.0254	0.0491	0.1000
C	0.0277	0.0297	0.0569	0.1189
D	0.0326	0.0349	0.0681	0.1369

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
AN	0.0023	0.0023	0.0037	0.0056
B	0.0039	0.0041	0.0083	0.0179
C	0.0038	0.0041	0.0090	0.0182
D	0.0039	0.0041	0.0093	0.0182

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
AN → Y↑	0.0892	0.0902	0.0765	0.0795	9.1571	8.4839	4.1418	2.0709
AN → Y↓	0.0937	0.0964	0.0846	0.0904	2.4959	2.2568	1.1482	0.5831
B → Y↑	0.0862	0.0862	0.0786	0.0820	9.1471	8.4796	4.1404	2.0705
B → Y↓	0.0291	0.0288	0.0276	0.0290	2.4562	2.2387	1.1413	0.5794
C → Y↑	0.1056	0.1055	0.0983	0.1006	9.1465	8.4792	4.1410	2.0703
C → Y↓	0.0331	0.0331	0.0325	0.0335	2.4850	2.2555	1.1492	0.5837
D → Y↑	0.1132	0.1132	0.1061	0.1103	9.1450	8.4787	4.1409	2.0707
D → Y↓	0.0336	0.0344	0.0346	0.0362	2.5286	2.2744	1.1583	0.5882

Cell Description

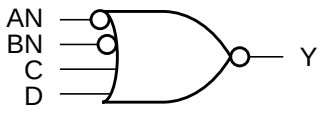
The NOR4BB cell provides a logical NOR of two inverted inputs (AN, BN) and two non-inverted inputs (C, D). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{AN} + \overline{BN} + C + D)}$$

Functions

AN	BN	C	D	Y
1	1	0	0	1
x	x	x	1	0
x	x	1	x	0
x	0	x	x	0
0	x	x	x	0

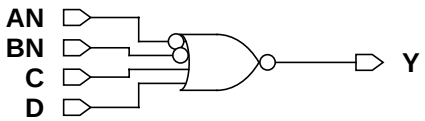
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
NOR4BBXL	5.04	5.04
NOR4BBX1	5.04	5.04
NOR4BBX2	5.04	6.72
NOR4BBX4	5.04	12.32

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
AN	0.0225	0.0235	0.0407	0.0785
BN	0.0260	0.0278	0.0500	0.0996
C	0.0304	0.0325	0.0607	0.1203
D	0.0351	0.0376	0.0711	0.1375

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
AN	0.0023	0.0022	0.0037	0.0056
BN	0.0023	0.0023	0.0038	0.0055
C	0.0038	0.0041	0.0085	0.0181
D	0.0038	0.0040	0.0091	0.0181

Delays at 25°C, 1.8V, Typical Process

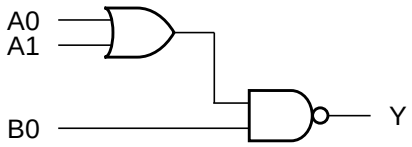
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
AN → Y↑	0.0919	0.0901	0.0801	0.0796	9.1533	8.2836	4.2415	2.0710
AN → Y↓	0.0909	0.0929	0.0841	0.0906	2.4858	2.2524	1.1476	0.5831
BN → Y↑	0.1253	0.1234	0.1139	0.1167	9.1466	8.2806	4.2397	2.0711
BN → Y↓	0.0961	0.0987	0.0928	0.1023	2.4850	2.2525	1.1481	0.5836
C → Y↑	0.1132	0.1109	0.1038	0.1024	9.1458	8.2807	4.2398	2.0704
C → Y↓	0.0349	0.0352	0.0327	0.0333	2.4839	2.2522	1.1495	0.5837
D → Y↑	0.1212	0.1189	0.1130	0.1121	9.1446	8.2803	4.2401	2.0707
D → Y↓	0.0357	0.0367	0.0347	0.0356	2.5266	2.2743	1.1597	0.5889

Cell Description

The OAI21 cell provides the logical inverted AND of one OR group and an additional input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 + A1) \bullet B0}$$

Logic Symbol



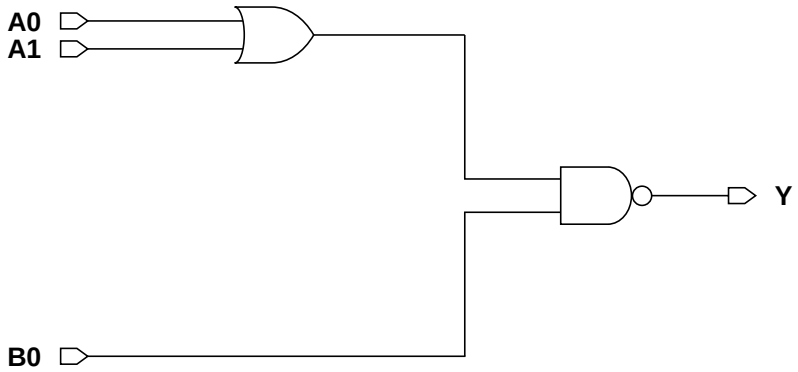
Functions

A0	A1	B0	Y
0	0	x	1
x	x	0	1
x	1	1	0
1	x	1	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
OAI21XL	5.04	2.80
OAI21X1	5.04	2.80
OAI21X2	5.04	4.48
OAI21X4	5.04	6.16

Functional Schematic



AC Power

Pin	Power (μW/MHz)			
	XL	X1	X2	X4
A0	0.0202	0.0226	0.0429	0.0752
A1	0.0237	0.0263	0.0499	0.0870
B0	0.0159	0.0178	0.0314	0.0590

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0034	0.0038	0.0078	0.0145
A1	0.0032	0.0035	0.0070	0.0139
B0	0.0032	0.0036	0.0063	0.0118

Delays at 25^{o}C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.0579	0.0598	0.0586	0.0504	6.4196	5.8832	2.8944	1.4575
A0 → Y↓	0.0289	0.0288	0.0291	0.0257	3.0090	2.6658	1.3483	0.6843
A1 → Y↑	0.0667	0.0683	0.0665	0.0589	6.4167	5.8819	2.8937	1.4572
A1 → Y↓	0.0340	0.0337	0.0339	0.0308	3.0153	2.6686	1.3497	0.6851
B0 → Y↑	0.0311	0.0318	0.0302	0.0273	4.4942	3.9918	2.0199	1.0158
B0 → Y↓	0.0250	0.0249	0.0239	0.0223	3.0086	2.6652	1.3479	0.6842

Cell Description

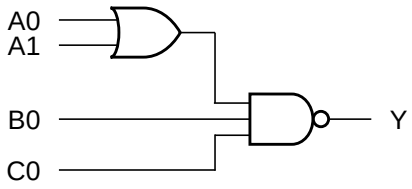
The OAI211 cell provides the logical inverted OR of one OR group and two additional inputs. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 + A1) \bullet B0 \bullet C0}$$

Functions

A0	A1	B0	C0	Y
0	0	x	x	1
x	x	0	x	1
x	x	x	0	1
x	1	1	1	0
1	x	1	1	0

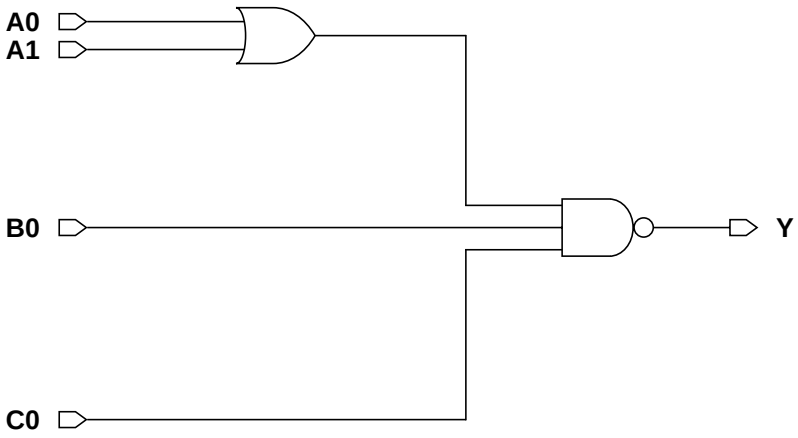
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
OAI211XL	5.04	3.36
OAI211X1	5.04	3.36
OAI211X2	5.04	5.60
OAI211X4	5.04	5.60

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A0	0.0282	0.0312	0.0586	0.0694
A1	0.0319	0.0352	0.0663	0.0705
B0	0.0176	0.0196	0.0362	0.0610
C0	0.0224	0.0249	0.0470	0.0642

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0037	0.0041	0.0084	0.0028
A1	0.0036	0.0039	0.0078	0.0028
B0	0.0033	0.0037	0.0069	0.0028
C0	0.0032	0.0035	0.0074	0.0024

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.0844	0.0867	0.0820	0.2038	6.4344	5.8899	2.8972	1.0097
A0 → Y↓	0.0410	0.0405	0.0401	0.1444	3.3566	2.9748	1.5160	0.5757
A1 → Y↑	0.0935	0.0955	0.0902	0.2122	6.4320	5.8887	2.8966	1.0097
A1 → Y↓	0.0471	0.0464	0.0460	0.1517	3.3620	2.9773	1.5172	0.5758
B0 → Y↑	0.0372	0.0377	0.0366	0.1352	4.4957	3.9925	2.0261	1.0098
B0 → Y↓	0.0309	0.0306	0.0304	0.1384	3.3554	2.9740	1.5154	0.5758
C0 → Y↑	0.0462	0.0465	0.0455	0.1440	4.4899	3.9899	2.0253	1.0097
C0 → Y↓	0.0386	0.0382	0.0382	0.1428	3.3636	2.9780	1.5176	0.5758

Cell Description

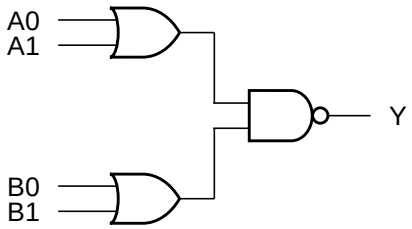
The OAI22 cell provides the logical inverted AND of two OR groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 + A1) \bullet (B0 + B1)}$$

Functions

A0	A1	B0	B1	Y
0	0	x	x	1
x	x	0	0	1
x	1	x	1	0
x	1	1	x	0
1	x	x	1	0
1	x	1	x	0

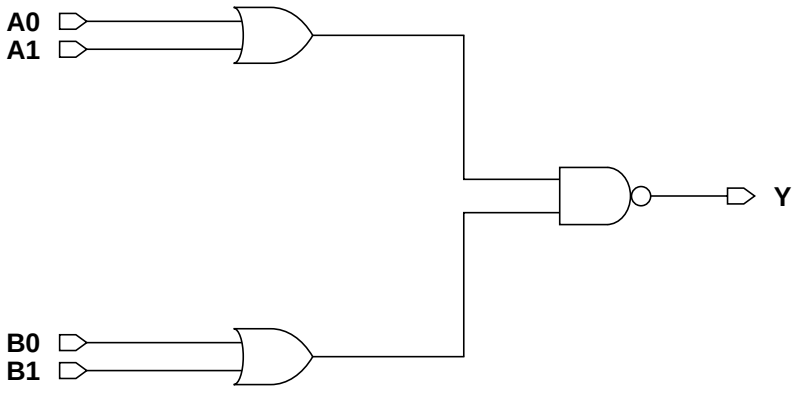
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
OAI22XL	5.04	3.36
OAI22X1	5.04	3.36
OAI22X2	5.04	5.60
OAI22X4	5.04	8.40

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A0	0.0187	0.0201	0.0417	0.0800
A1	0.0215	0.0231	0.0481	0.0913
B0	0.0275	0.0294	0.0622	0.1134
B1	0.0311	0.0334	0.0698	0.1289

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0036	0.0039	0.0082	0.0150
A1	0.0035	0.0037	0.0072	0.0144
B0	0.0035	0.0037	0.0080	0.0150
B1	0.0033	0.0036	0.0072	0.0145

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.0463	0.0470	0.0512	0.0477	6.4601	5.9017	2.9038	1.4623
A0 → Y↓	0.0279	0.0276	0.0299	0.0278	3.0079	2.7268	1.3478	0.6593
A1 → Y↑	0.0554	0.0560	0.0585	0.0556	6.4595	5.9011	2.9023	1.4619
A1 → Y↓	0.0337	0.0333	0.0347	0.0327	3.0131	2.7293	1.3488	0.6598
B0 → Y↑	0.0744	0.0741	0.0803	0.0722	6.4432	5.8947	2.9000	1.4603
B0 → Y↓	0.0400	0.0394	0.0425	0.0382	3.0176	2.7315	1.3501	0.6604
B1 → Y↑	0.0829	0.0825	0.0880	0.0805	6.4400	5.8934	2.8993	1.4600
B1 → Y↓	0.0452	0.0446	0.0474	0.0433	3.0214	2.7333	1.3509	0.6609

Cell Description

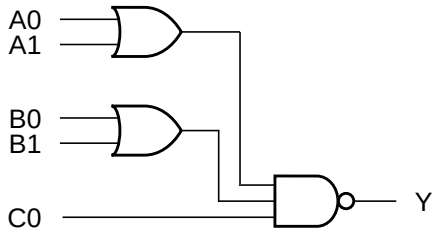
The OAI221 cell provides the logical inverted AND of two OR groups and an additional input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 + A1) \bullet (B0 + B1) \bullet C0}$$

Functions

A0	A1	B0	B1	C0	Y
0	0	x	x	x	1
x	x	0	0	x	1
x	x	x	x	0	1
x	1	x	1	1	0
x	1	1	x	1	0
1	x	x	1	1	0
1	x	1	x	1	0

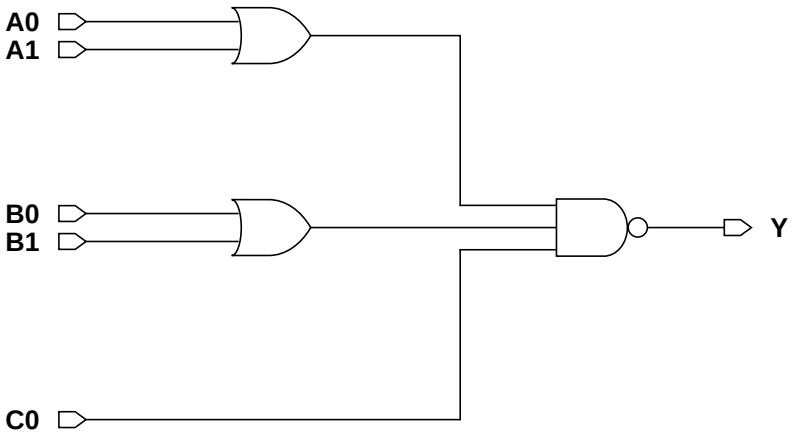
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
OAI221XL	5.04	4.48
OAI221X1	5.04	4.48
OAI221X2	5.04	7.84
OAI221X4	5.04	7.28

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A0	0.0291	0.0315	0.0569	0.0701
A1	0.0322	0.0354	0.0644	0.0723
B0	0.0385	0.0419	0.0767	0.0792
B1	0.0423	0.0461	0.0850	0.0797
C0	0.0220	0.0245	0.0431	0.0614

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0037	0.0040	0.0079	0.0029
A1	0.0037	0.0040	0.0083	0.0027
B0	0.0036	0.0039	0.0079	0.0027
B1	0.0035	0.0038	0.0082	0.0027
C0	0.0034	0.0037	0.0071	0.0025

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.0827	0.0836	0.0739	0.2028	6.4585	5.9007	2.9029	1.0095
A0 → Y↓	0.0486	0.0471	0.0430	0.1558	3.3653	2.9788	1.4757	0.5755
A1 → Y↑	0.0919	0.0928	0.0823	0.2102	6.4569	5.9001	2.9024	1.0095
A1 → Y↓	0.0551	0.0534	0.0489	0.1630	3.3690	2.9806	1.4765	0.5755
B0 → Y↑	0.1088	0.1106	0.0997	0.2312	6.4714	5.9072	2.9056	1.0095
B0 → Y↓	0.0573	0.0557	0.0512	0.1647	3.3655	2.9790	1.4757	0.5755
B1 → Y↑	0.1170	0.1188	0.1084	0.2387	6.4689	5.9061	2.9050	1.0095
B1 → Y↓	0.0632	0.0615	0.0571	0.1720	3.3686	2.9804	1.4765	0.5755
C0 → Y↑	0.0416	0.0415	0.0379	0.1405	4.5216	4.0055	2.0246	1.0096
C0 → Y↓	0.0387	0.0376	0.0348	0.1486	3.3616	2.9769	1.4747	0.5755

Cell Description

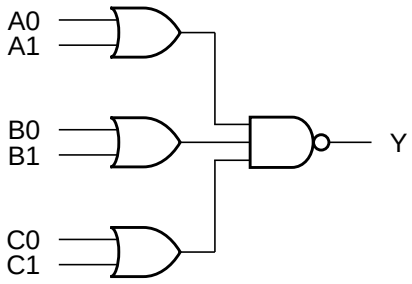
The OAI222 cell provides the logical inverted AND of three OR groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 + A1) \bullet (B0 + B1) \bullet (C0 + C1)}$$

Functions

A0	A1	B0	B1	C0	C1	Y
0	0	x	x	x	x	1
x	x	0	0	x	x	1
x	x	x	x	0	0	1
x	1	x	1	1	x	0
x	1	x	1	x	1	0
x	1	1	x	1	x	0
x	1	1	x	x	1	0
1	x	x	1	1	x	0
1	x	x	1	x	1	0
1	x	1	x	1	x	0
1	x	1	x	x	1	0

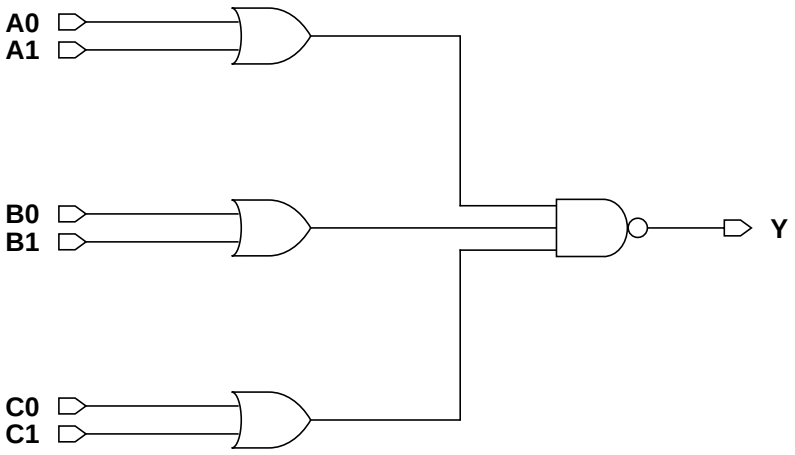
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
OAI222XL	5.04	5.60
OAI222X1	5.04	5.60
OAI222X2	5.04	8.96
OAI222X4	5.04	7.84

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A0	0.0366	0.0394	0.0754	0.0796
A1	0.0402	0.0432	0.0832	0.0827
B0	0.0455	0.0491	0.0948	0.0879
B1	0.0492	0.0531	0.1034	0.0894
C0	0.0251	0.0269	0.0523	0.0658
C1	0.0278	0.0300	0.0591	0.0687

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0040	0.0042	0.0079	0.0028
A1	0.0039	0.0041	0.0083	0.0027
B0	0.0039	0.0042	0.0079	0.0027
B1	0.0037	0.0039	0.0085	0.0026
C0	0.0040	0.0042	0.0080	0.0030
C1	0.0038	0.0041	0.0084	0.0028

Delays at 25°C, 1.8V, Typical Process

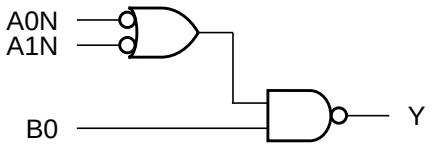
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.0977	0.0985	0.0911	0.2309	6.4901	5.9146	2.9098	1.0094
A0 → Y↓	0.0614	0.0603	0.0578	0.1708	3.3701	3.0381	1.5192	0.5756
A1 → Y↑	0.1061	0.1069	0.0997	0.2390	6.4878	5.9136	2.9094	1.0094
A1 → Y↓	0.0674	0.0663	0.0640	0.1775	3.3724	3.0394	1.5199	0.5756
B0 → Y↑	0.1264	0.1269	0.1193	0.2590	6.4709	5.9084	2.9069	1.0094
B0 → Y↓	0.0696	0.0684	0.0661	0.1807	3.3698	3.0381	1.5193	0.5756
B1 → Y↑	0.1345	0.1349	0.1284	0.2667	6.4685	5.9073	2.9062	1.0093
B1 → Y↓	0.0756	0.0743	0.0725	0.1879	3.3720	3.0392	1.5198	0.5756
C0 → Y↑	0.0640	0.0653	0.0605	0.1850	6.4994	5.9191	2.9119	1.0095
C0 → Y↓	0.0426	0.0419	0.0405	0.1487	3.3606	3.0335	1.5169	0.5756
C1 → Y↑	0.0711	0.0724	0.0692	0.1918	6.4941	5.9169	2.9118	1.0095
C1 → Y↓	0.0472	0.0465	0.0462	0.1552	3.3703	3.0386	1.5195	0.5756

Cell Description

The OAI2BB1 cell provides the logical inverted AND of one OR group of two inverted inputs (A0N, A1N) and an additional non-inverted input (B0). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{A0N} + \overline{A1N}) \bullet B0}$$

Logic Symbol



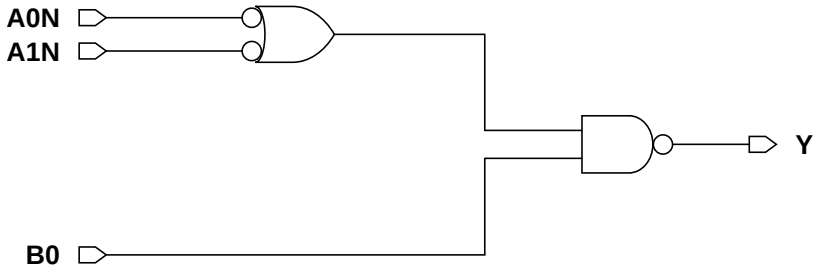
Functions

A0N	A1N	B0	Y
1	1	x	1
x	x	0	1
x	0	1	0
0	x	1	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
OAI2BB1XL	5.04	3.36
OAI2BB1X1	5.04	3.36
OAI2BB1X2	5.04	3.92
OAI2BB1X4	5.04	5.60

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A0N	0.0232	0.0223	0.0375	0.0700
A1N	0.0209	0.0198	0.0335	0.0629
B0	0.0131	0.0147	0.0249	0.0508

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0N	0.0019	0.0016	0.0029	0.0043
A1N	0.0015	0.0013	0.0022	0.0034
B0	0.0026	0.0028	0.0055	0.0097

Delays at 25^{o}C, 1.8V, Typical Process

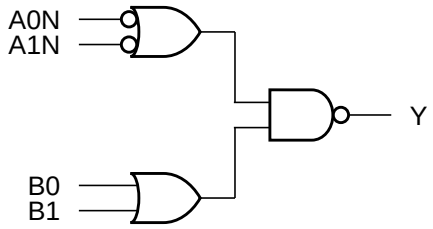
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0N → Y↑	0.0721	0.0817	0.0732	0.0748	4.4778	4.0722	2.0444	1.0166
A0N → Y↓	0.0868	0.0996	0.0902	0.0820	3.0433	2.7478	1.3732	0.6899
A1N → Y↑	0.0688	0.0784	0.0697	0.0718	4.4781	4.0724	2.0445	1.0166
A1N → Y↓	0.0783	0.0911	0.0817	0.0750	3.0396	2.7459	1.3722	0.6895
B0 → Y↑	0.0342	0.0347	0.0304	0.0323	4.4632	4.0642	2.0408	1.0148
B0 → Y↓	0.0235	0.0246	0.0221	0.0245	3.0166	2.7331	1.3667	0.6878

Cell Description

The OAI2BB2 cell provides the logical inverted AND of one OR group of two inverted inputs (A0N, A1N) and one OR group of two non-inverted inputs (B0, B1). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{A0N} + \overline{A1N}) \bullet (B0 + B1)}$$

Logic Symbol



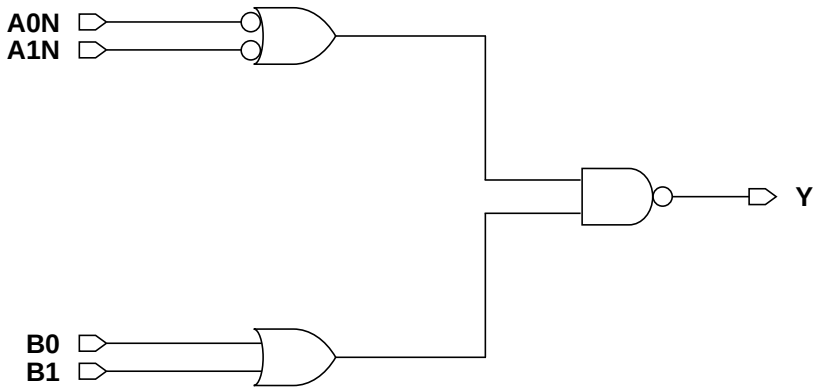
Functions

A0N	A1N	B0	B1	Y
1	1	x	x	1
x	x	0	0	1
x	0	x	1	0
x	0	1	x	0
0	x	x	1	0
0	x	1	x	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
OAI2BB2XL	5.04	3.92
OAI2BB2X1	5.04	3.92
OAI2BB2X2	5.04	6.16
OAI2BB2X4	5.04	8.96

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A0N	0.0253	0.0251	0.0454	0.0880
A1N	0.0209	0.0208	0.0362	0.0698
B0	0.0175	0.0195	0.0370	0.0645
B1	0.0206	0.0228	0.0441	0.0765

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0N	0.0022	0.0019	0.0030	0.0065
A1N	0.0025	0.0022	0.0034	0.0059
B0	0.0036	0.0039	0.0081	0.0151
B1	0.0035	0.0037	0.0081	0.0143

Delays at 25°C, 1.8V, Typical Process

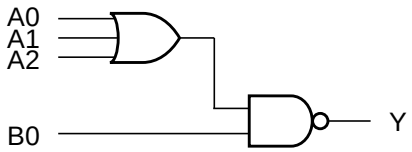
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0N → Y↑	0.0755	0.0836	0.0789	0.0764	4.5009	3.9964	2.0222	1.0130
A0N → Y↓	0.0918	0.1075	0.0999	0.0966	3.0365	2.7445	1.3556	0.6717
A1N → Y↑	0.0718	0.0796	0.0748	0.0713	4.4754	3.9834	2.0155	1.0097
A1N → Y↓	0.0776	0.0928	0.0853	0.0809	3.0337	2.7440	1.3552	0.6715
B0 → Y↑	0.0584	0.0597	0.0573	0.0520	6.4213	5.8841	2.8949	1.4578
B0 → Y↓	0.0309	0.0323	0.0319	0.0295	3.0185	2.7341	1.3515	0.6697
B1 → Y↑	0.0671	0.0681	0.0660	0.0606	6.4184	5.8827	2.8944	1.4574
B1 → Y↓	0.0363	0.0377	0.0373	0.0351	3.0230	2.7361	1.3523	0.6702

Cell Description

The OAI31 cell provides the logical inverted AND of one OR group and an additional input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 + A1 + A2) \bullet B0}$$

Logic Symbol



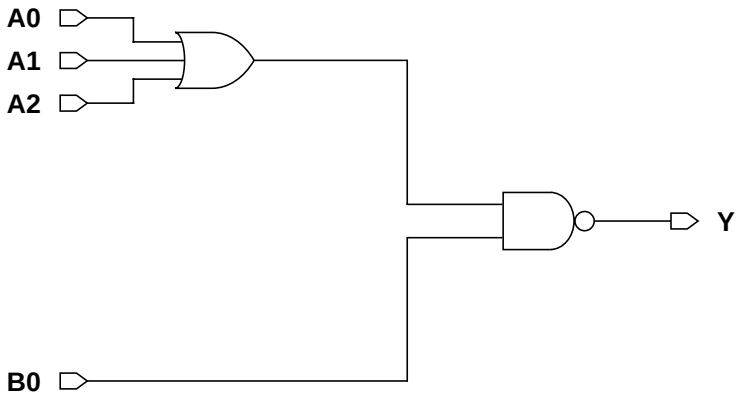
Functions

A0	A1	A2	B0	Y
0	0	0	x	1
x	x	x	0	1
x	x	1	1	0
x	1	x	1	0
1	x	x	1	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
OAI31XL	5.04	3.36
OAI31X1	5.04	3.36
OAI31X2	5.04	5.60
OAI31X4	5.04	5.60

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A0	0.0234	0.0255	0.0502	0.0695
A1	0.0266	0.0290	0.0578	0.0739
A2	0.0314	0.0343	0.0691	0.0764
B0	0.0220	0.0238	0.0440	0.0638

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0042	0.0046	0.0082	0.0033
A1	0.0040	0.0043	0.0086	0.0030
A2	0.0037	0.0040	0.0088	0.0029
B0	0.0032	0.0035	0.0065	0.0027

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.0734	0.0736	0.0710	0.2050	7.4521	6.7768	3.3892	0.9777
A0 → Y↓	0.0343	0.0335	0.0322	0.1353	3.0121	2.6671	1.3490	0.5554
A1 → Y↑	0.0917	0.0919	0.0909	0.2232	7.4451	6.7738	3.3882	0.9777
A1 → Y↓	0.0413	0.0404	0.0398	0.1443	3.0177	2.6698	1.3505	0.5555
A2 → Y↑	0.0986	0.0988	0.0992	0.2300	7.4441	6.7733	3.3883	0.9777
A2 → Y↓	0.0448	0.0444	0.0445	0.1501	3.0469	2.6835	1.3577	0.5555
B0 → Y↑	0.0352	0.0348	0.0305	0.1310	4.5051	4.0041	2.0239	0.9777
B0 → Y↓	0.0348	0.0345	0.0312	0.1416	3.0400	2.6801	1.3560	0.5556

Cell Description

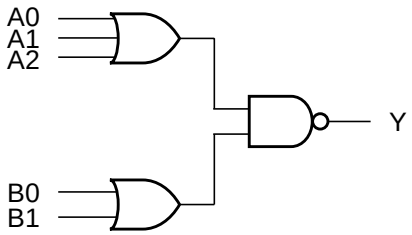
The OAI32 cell provides the logical inverted AND of two OR groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 + A1 + A2) \bullet (B0 + B1)}$$

Functions

A0	A1	A2	B0	B1	Y
0	0	0	x	x	1
x	x	x	0	0	1
x	x	1	x	1	0
x	x	1	1	x	0
x	1	x	1	x	0
x	1	x	x	1	0
1	x	x	1	x	0
1	x	x	x	1	0

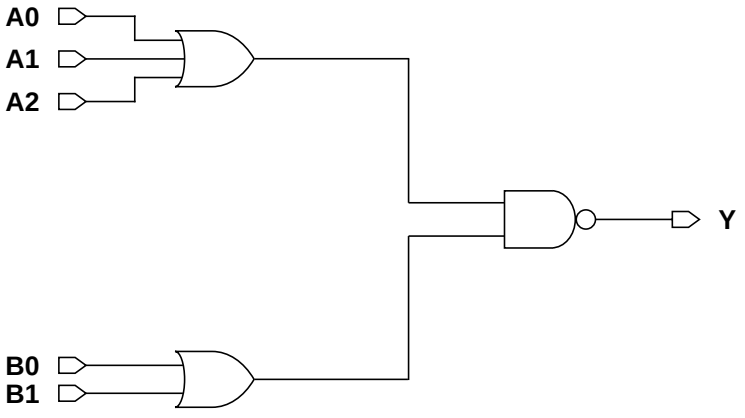
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
OAI32XL	5.04	3.92
OAI32X1	5.04	3.92
OAI32X2	5.04	6.72
OAI32X4	5.04	6.16

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A0	0.0308	0.0331	0.0681	0.0769
A1	0.0341	0.0367	0.0755	0.0834
A2	0.0391	0.0422	0.0858	0.0831
B0	0.0241	0.0259	0.0518	0.0672
B1	0.0273	0.0296	0.0588	0.0692

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0042	0.0045	0.0078	0.0029
A1	0.0040	0.0043	0.0083	0.0031
A2	0.0039	0.0042	0.0092	0.0027
B0	0.0036	0.0038	0.0071	0.0029
B1	0.0037	0.0039	0.0075	0.0027

Delays at 25^{o}C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.0912	0.0902	0.1014	0.2316	7.4787	6.7886	3.7255	0.9776
A0 → Y↓	0.0447	0.0440	0.0446	0.1498	3.0192	2.7322	1.3839	0.5597
A1 → Y↑	0.1100	0.1091	0.1228	0.2518	7.4724	6.7862	3.7247	0.9776
A1 → Y↓	0.0522	0.0516	0.0524	0.1597	3.0230	2.7341	1.3851	0.5597
A2 → Y↑	0.1174	0.1165	0.1313	0.2589	7.4724	6.7863	3.7250	0.9776
A2 → Y↓	0.0565	0.0565	0.0569	0.1641	3.0476	2.7460	1.3830	0.5598
B0 → Y↑	0.0503	0.0507	0.0515	0.1761	6.4870	5.9298	3.0130	0.9779
B0 → Y↓	0.0369	0.0371	0.0360	0.1420	3.0392	2.7416	1.3808	0.5598
B1 → Y↑	0.0600	0.0603	0.0609	0.1846	6.4873	5.9302	3.0130	0.9779
B1 → Y↓	0.0436	0.0437	0.0423	0.1491	3.0397	2.7421	1.3810	0.5598

Cell Description

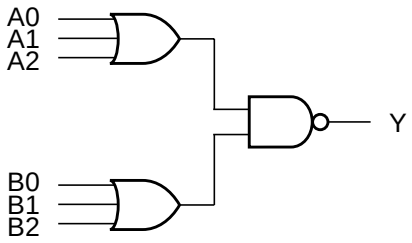
The OAI33 cell provides the logical inverted AND of two OR groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 + A1 + A2) \bullet (B0 + B1 + B2)}$$

Functions

A0	A1	A2	B0	B1	B2	Y
0	0	0	x	x	x	1
x	x	x	0	0	0	1
x	x	1	x	x	1	0
x	x	1	x	1	x	0
x	x	1	1	x	x	0
x	1	x	x	x	1	0
x	1	x	x	1	x	0
x	1	x	1	x	x	0
1	x	x	x	x	1	0
1	x	x	x	1	x	0
1	x	x	1	x	x	0

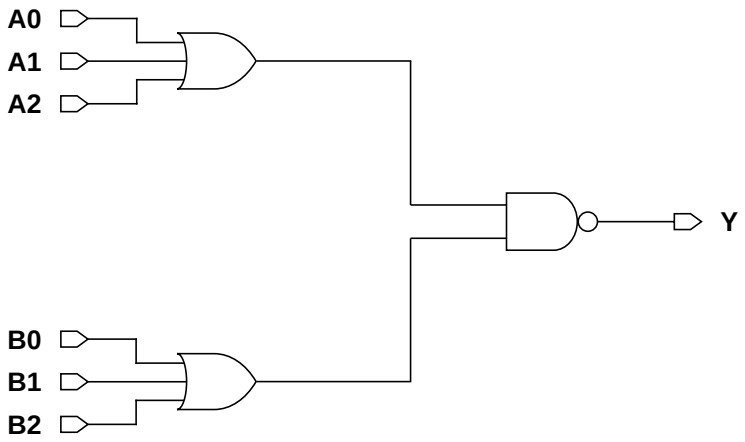
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
OAI33XL	5.04	4.48
OAI33X1	5.04	4.48
OAI33X2	5.04	7.28
OAI33X4	5.04	6.72

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A0	0.0288	0.0319	0.0579	0.0719
A1	0.0326	0.0360	0.0646	0.0773
A2	0.0371	0.0409	0.0744	0.0788
B0	0.0417	0.0454	0.0826	0.0854
B1	0.0453	0.0494	0.0901	0.0907
B2	0.0503	0.0548	0.1000	0.0916

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0041	0.0046	0.0075	0.0032
A1	0.0040	0.0044	0.0081	0.0033
A2	0.0040	0.0043	0.0089	0.0029
B0	0.0040	0.0044	0.0073	0.0032
B1	0.0040	0.0044	0.0081	0.0030
B2	0.0038	0.0041	0.0083	0.0030

Delays at 25°C, 1.8V, Typical Process

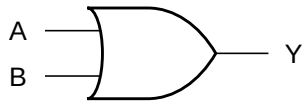
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.0627	0.0649	0.0661	0.2019	7.5320	6.8318	3.8009	0.9780
A0 → Y↓	0.0409	0.0421	0.0415	0.1514	3.0382	2.7411	1.4844	0.5560
A1 → Y↑	0.0839	0.0859	0.0864	0.2223	7.5278	6.8297	3.8000	0.9780
A1 → Y↓	0.0499	0.0510	0.0500	0.1591	3.0385	2.7416	1.4844	0.5560
A2 → Y↑	0.0927	0.0943	0.0955	0.2278	7.5304	6.8302	3.8008	0.9780
A2 → Y↓	0.0551	0.0565	0.0552	0.1652	3.0661	2.7541	1.4784	0.5560
B0 → Y↑	0.1127	0.1119	0.1135	0.2528	7.4896	6.8136	3.7898	0.9779
B0 → Y↓	0.0558	0.0562	0.0547	0.1657	3.0402	2.7420	1.4821	0.5560
B1 → Y↑	0.1326	0.1314	0.1349	0.2715	7.4848	6.8113	3.7888	0.9779
B1 → Y↓	0.0662	0.0665	0.0657	0.1766	3.0482	2.7463	1.4835	0.5560
B2 → Y↑	0.1395	0.1384	0.1429	0.2794	7.4850	6.8115	3.7891	0.9780
B2 → Y↓	0.0690	0.0697	0.0709	0.1820	3.0626	2.7535	1.4791	0.5561

Cell Description

The OR2 cell provides the logical OR of two inputs (A, B). The output (Y) is represented by the logic equation:

$Y = (A + B)$

Logic Symbol



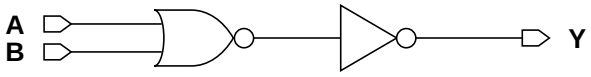
Functions

A	B	Y
0	0	0
x	1	1
1	x	1

Cell Size

Drive Strength	Height (µm)	Width (µm)
OR2XL	5.04	2.80
OR2X1	5.04	2.80
OR2X2	5.04	2.80
OR2X4	5.04	3.36

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A	0.0167	0.0173	0.0279	0.0496
B	0.0187	0.0197	0.0320	0.0551

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A	0.0023	0.0023	0.0029	0.0052
B	0.0025	0.0025	0.0030	0.0052

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)			
	XL	X1	X2	X4
A → Y↑	0.0519	0.0529	0.0570	0.0510
A → Y↓	0.0889	0.0941	0.1056	0.0980
B → Y↑	0.0577	0.0588	0.0628	0.0559
B → Y↓	0.0997	0.1049	0.1159	0.1070

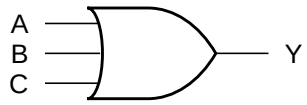
Description	K_{load} (ns/pF)			
	XL	X1	X2	X4
A → Y↑	4.4677	3.9782	2.0195	1.1337
A → Y↓	2.5425	2.2763	1.1642	0.5626
B → Y↑	4.4706	3.9795	2.0200	1.1339
B → Y↓	2.5425	2.2763	1.1642	0.5626

Cell Description

The OR3 cell provides the logical OR of three inputs (A, B, C). The output (Y) is represented by the logic equation:

$Y = (A + B + C)$

Logic Symbol



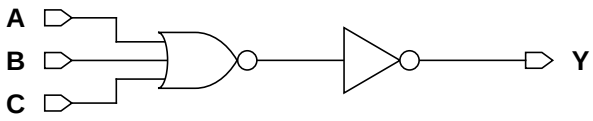
Functions

A	B	C	Y
0	0	0	0
x	x	1	1
x	1	x	1
1	x	x	1

Cell Size

Drive Strength	Height (µm)	Width (µm)
OR3XL	5.04	3.36
OR3X1	5.04	3.36
OR3X2	5.04	3.36
OR3X4	5.04	5.04

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A	0.0193	0.0210	0.0334	0.0589
B	0.0225	0.0239	0.0379	0.0686
C	0.0249	0.0263	0.0407	0.0758

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A	0.0029	0.0029	0.0034	0.0064
B	0.0028	0.0028	0.0032	0.0068
C	0.0027	0.0027	0.0033	0.0072

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)			
	XL	X1	X2	X4
A → Y↑	0.0602	0.0616	0.0634	0.0551
A → Y↓	0.1166	0.1251	0.1332	0.1166
B → Y↑	0.0670	0.0684	0.0704	0.0628
B → Y↓	0.1353	0.1437	0.1517	0.1367
C → Y↑	0.0690	0.0706	0.0730	0.0651
C → Y↓	0.1442	0.1526	0.1612	0.1454

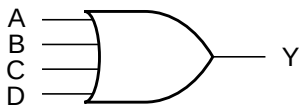
Description	K_{load} (ns/pF)			
	XL	X1	X2	X4
A → Y↑	4.4684	3.9786	2.0199	0.9679
A → Y↓	2.6350	2.3153	1.1836	0.6024
B → Y↑	4.4711	3.9801	2.0205	0.9683
B → Y↓	2.6351	2.3154	1.1837	0.6023
C → Y↑	4.4787	3.9837	2.0222	0.9692
C → Y↓	2.6352	2.3153	1.1836	0.6023

Cell Description

The OR4 cell provides the logical OR of four inputs (A, B, C, D). The output (Y) is represented by the logic equation:

$Y = (A + B + C + D)$

Logic Symbol



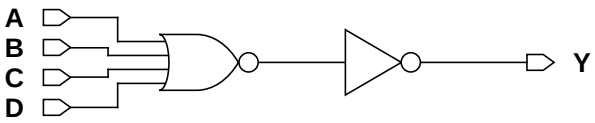
Functions

A	B	C	D	Y
0	0	0	0	0
x	x	x	1	1
x	x	1	x	1
x	1	x	x	1
1	x	x	x	1

Cell Size

Drive Strength	Height (µm)	Width (µm)
OR4XL	5.04	3.36
OR4X1	5.04	3.36
OR4X2	5.04	3.92
OR4X4	5.04	6.16

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A	0.0233	0.0247	0.0365	0.0669
B	0.0268	0.0281	0.0405	0.0754
C	0.0299	0.0311	0.0454	0.0834
D	0.0331	0.0347	0.0483	0.0926

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A	0.0031	0.0031	0.0035	0.0065
B	0.0030	0.0030	0.0037	0.0069
C	0.0031	0.0031	0.0034	0.0073
D	0.0033	0.0033	0.0036	0.0081

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)			
	XL	X1	X2	X4
A → Y↑	0.0681	0.0692	0.0667	0.0583
A → Y↓	0.1527	0.1652	0.1584	0.1404
B → Y↑	0.0738	0.0749	0.0728	0.0646
B → Y↓	0.1843	0.1968	0.1910	0.1731
C → Y↑	0.0825	0.0838	0.0782	0.0703
C → Y↓	0.2049	0.2174	0.2086	0.1922
D → Y↑	0.0858	0.0873	0.0825	0.0747
D → Y↓	0.2154	0.2279	0.2182	0.2028

Delay Table at 25°C, 1.8V, Typical Process

Description	K_{load} (ns/pF)			
	XL	X1	X2	X4
A → Y↑	4.4708	3.9798	2.0203	0.9784
A → Y↓	2.7972	2.3891	1.2131	0.5844
B → Y↑	4.4733	3.9812	2.0209	0.9788
B → Y↓	2.7973	2.3890	1.2131	0.5844
C → Y↑	4.4807	3.9847	2.0227	0.9798
C → Y↓	2.7974	2.3891	1.2131	0.5844
D → Y↑	4.4914	3.9896	2.0257	0.9816
D → Y↓	2.7960	2.3885	1.2131	0.5844

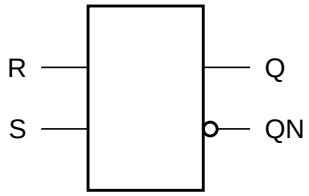
Cell Description

The RSLAT cell is an RS-type latch with active-high set (S) and reset (R).

Functions

R	S	Q[n+1]	QN[n+1]
0	0	Q[n]	QN[n]
0	1	1	0
1	0	0	1
1	1	IL	IL

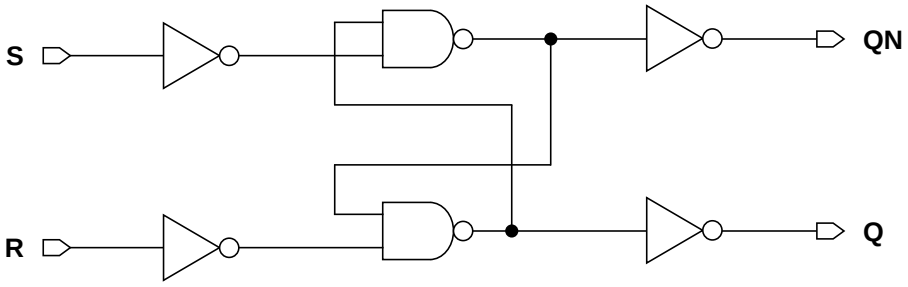
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
RSLATXL	5.04	5.60
RSLATX1	5.04	5.60
RSLATX2	5.04	7.28
RSLATX4	5.04	10.08

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
S	0.0096	0.0099	0.0117	0.0231
R	0.0105	0.0111	0.0140	0.0223
Q	0.0450	0.0490	0.0800	0.1385

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
S	0.0022	0.0022	0.0019	0.0037
R	0.0023	0.0023	0.0021	0.0036

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
S → Q↑	0.1895	0.1812	0.1609	0.1488	4.4846	3.9853	2.0213	1.0110
R → Q↑	0.1281	0.1260	0.1228	0.1108	4.4845	3.9852	2.0212	1.0110
R → Q↓	0.1258	0.1236	0.1094	0.1020	2.5485	2.2710	1.1515	0.5764
S → QN↑	0.1191	0.1175	0.1223	0.1084	4.4808	3.9835	2.0213	1.0109
S → QN↓	0.1167	0.1153	0.1103	0.0995	2.5433	2.2695	1.1516	0.5762
R → QN↑	0.1908	0.1821	0.1636	0.1496	4.4811	3.9839	2.0214	1.0109

Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
S	minpwh	0.0979	0.0930	0.0785	0.0736
R	minpwh	0.0979	0.0930	0.0785	0.0785

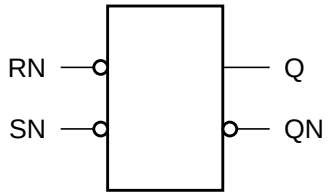
Cell Description

The RSLATN cell is an RS-type latch with active-low set (SN) and reset (RN).

Function

RN	SN	Q[n+1]	QN[n+1]
0	0	IL	IL
0	1	0	1
1	0	1	0
1	1	Q[n]	QN[n]

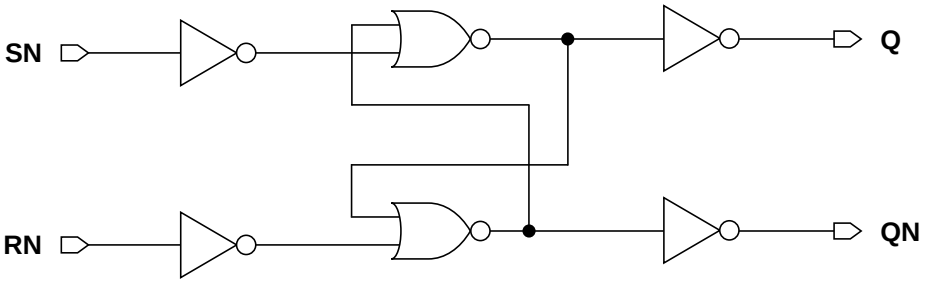
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
RSLATNXL	5.04	6.72
RSLATNX1	5.04	6.72
RSLATNX2	5.04	6.72
RSLATNX4	5.04	11.20

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
SN	0.0112	0.0117	0.0138	0.0271
RN	0.0098	0.0110	0.0158	0.0271
Q	0.0406	0.0450	0.0799	0.1379

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
SN	0.0022	0.0022	0.0024	0.0039
RN	0.0021	0.0021	0.0025	0.0039

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
SN → Q↑	0.1222	0.1209	0.1180	0.1066	4.4778	3.9815	2.0207	1.0104
SN → Q↓	0.1539	0.1464	0.1352	0.1233	2.6287	2.2960	1.1654	0.5819
RN → Q↓	0.2315	0.2214	0.2157	0.1937	2.6286	2.2960	1.1654	0.5819
SN → QN↓	0.2344	0.2240	0.2124	0.1951	2.6297	2.2970	1.1645	0.5819
RN → QN↑	0.1200	0.1186	0.1201	0.1075	4.4786	3.9818	2.0206	1.0104
RN → QN↓	0.1525	0.1452	0.1358	0.1244	2.6296	2.2969	1.1646	0.5819

Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
SN	minpwl	0.1076	0.1028	0.1028	0.0979
RN	minpwl	0.1125	0.1076	0.1076	0.0979

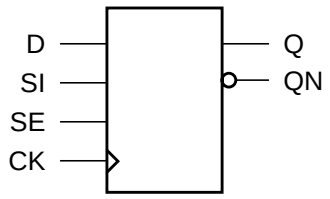
Cell Description

The SDFF cell is a positive-edge triggered, static D-type flip-flop with scan input (SI) and active-high scan enable (SE).

Functions

D	SI	SE	CK	Q[n+1]	QN[n+1]
1	x	0	↑	1	0
0	x	0	↑	0	1
x	x	x	↓	Q[n]	QN[n]
x	1	1	↑	1	0
x	0	1	↑	0	1

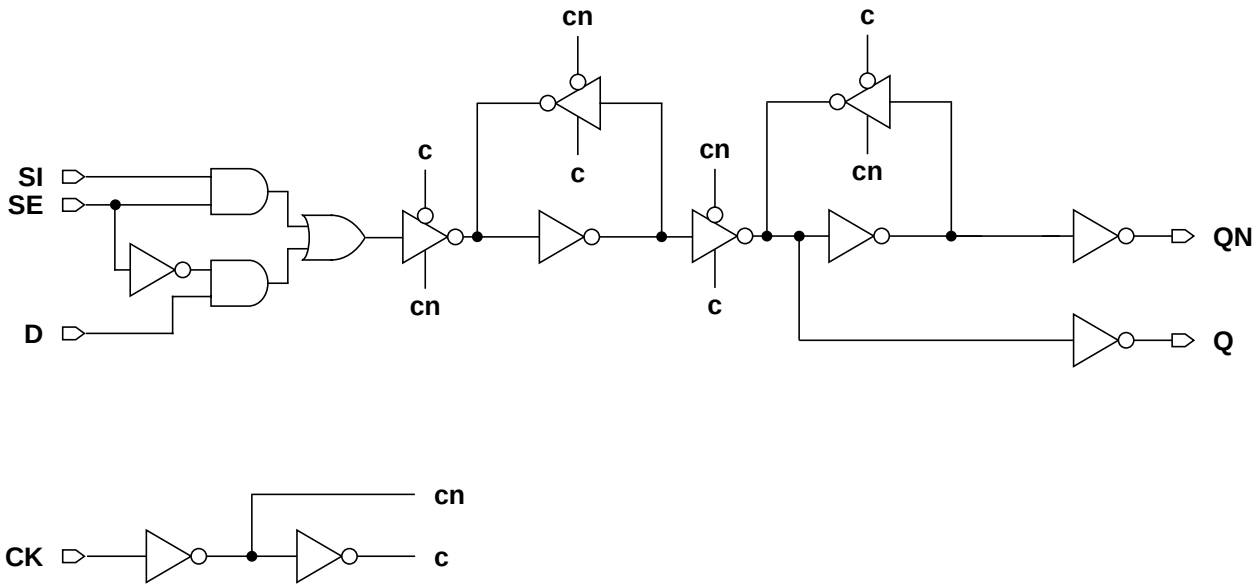
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
SDFFXL	5.04	12.32
SDFFX1	5.04	12.32
SDFFX2	5.04	14.56
SDFFX4	5.04	16.24

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
SI	0.0459	0.0413	0.0496	0.0708
SE	0.0528	0.0480	0.0553	0.0732
D	0.0390	0.0365	0.0431	0.0596
CK	0.0426	0.0405	0.0465	0.0626
Q	0.0358	0.0375	0.0631	0.1032

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
SI	0.0024	0.0024	0.0024	0.0022
SE	0.0050	0.0042	0.0043	0.0048
D	0.0031	0.0020	0.0022	0.0029
CK	0.0021	0.0026	0.0035	0.0052

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.1909	0.1735	0.1574	0.1350	4.5101	3.9961	2.0133	1.0112
CK → Q↓	0.1540	0.1446	0.1288	0.1152	2.5954	2.2933	1.1426	0.5815
CK → QN↑	0.2021	0.1915	0.1691	0.1541	4.4714	3.9804	2.0192	1.0099
CK → QN↓	0.2477	0.2349	0.2124	0.1873	2.5185	2.2658	1.1517	0.5757

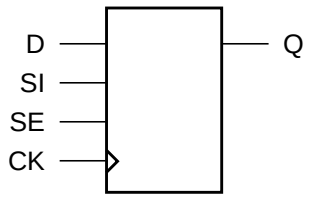
Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
SI	setup↑ → CK	0.1211	0.1094	0.1250	0.1445
	setup↓ → CK	0.2617	0.2812	0.2852	0.3203
	hold↑ → CK	-0.1016	-0.0820	-0.0938	-0.1094
	hold↓ → CK	-0.1680	-0.1914	-0.1953	-0.2305
SE	setup↑ → CK	0.2773	0.3008	0.3008	0.3398
	setup↓ → CK	0.1484	0.2969	0.2422	0.1914
	hold↑ → CK	-0.0938	-0.0703	-0.0820	-0.1016
	hold↓ → CK	-0.0547	-0.1172	-0.1289	-0.1094
D	setup↑ → CK	0.0742	0.0938	0.1055	0.0898
	setup↓ → CK	0.1523	0.3086	0.2461	0.1914
	hold↑ → CK	-0.0586	-0.0703	-0.0820	-0.0664
	hold↓ → CK	-0.0547	-0.2188	-0.1602	-0.1133
CK	minpwh	0.0979	0.0882	0.0785	0.0688
	minpwl	0.1708	0.1611	0.1659	0.1319

Cell Description

The SDFFHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with scan input (SI) and active-high scan enable (SE). The cell has a single output (Q) and fast clock-to-out path.

Logic Symbol



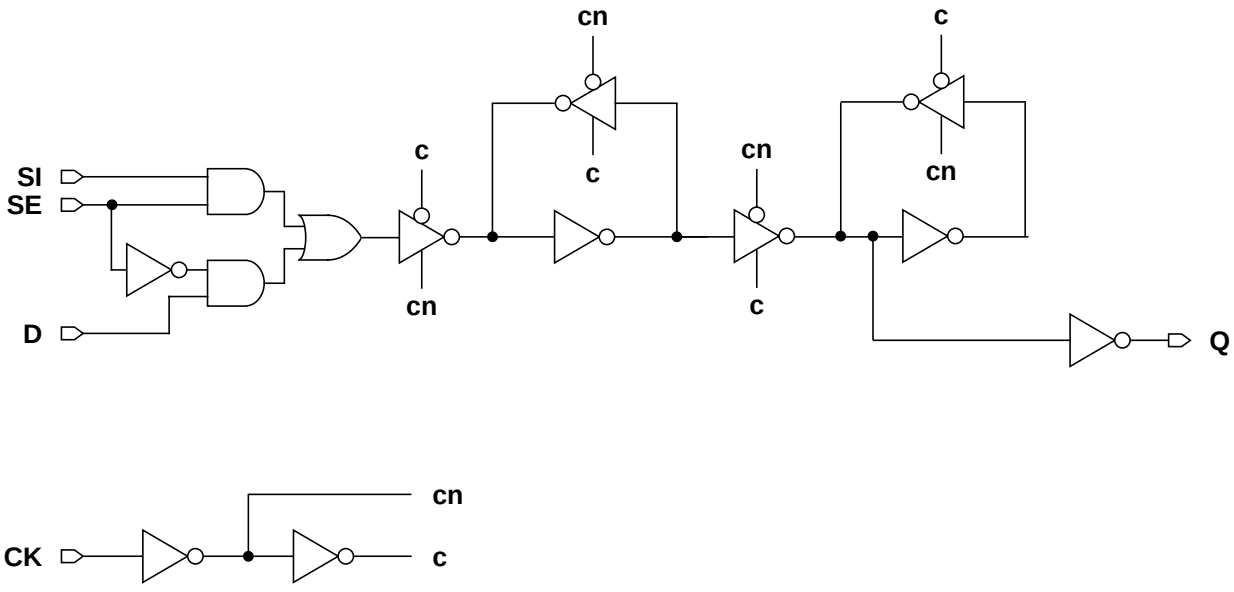
Functions

D	SI	SE	CK	Q[n+1]
1	x	0	↑	1
0	x	0	↑	0
x	x	x	↓	Q[n]
x	1	1	↑	1
x	0	1	↑	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
SDFFHQXL	5.04	11.76
SDFFHQX1	5.04	11.76
SDFFHQX2	5.04	12.32
SDFFHQX4	5.04	15.68

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
SI	0.0414	0.0479	0.0584	0.0832
SE	0.0484	0.0534	0.0645	0.0838
D	0.0389	0.0445	0.0541	0.0745
CK	0.0364	0.0365	0.0422	0.0519
Q	0.0243	0.0246	0.0322	0.0465

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
SI	0.0019	0.0019	0.0020	0.0019
SE	0.0035	0.0035	0.0037	0.0040
D	0.0018	0.0015	0.0016	0.0023
CK	0.0019	0.0023	0.0029	0.0040

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.1875	0.1688	0.1570	0.1349	4.4243	3.9932	2.0130	1.0102
CK → Q↓	0.1821	0.1472	0.1397	0.1194	2.7442	2.2895	1.1427	0.5852

Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
SI	setup↑ → CK	0.1328	0.1445	0.1445	0.1602
	setup↓ → CK	0.3945	0.3828	0.3750	0.3945
	hold↑ → CK	-0.0859	-0.0977	-0.0977	-0.1133
	hold↓ → CK	-0.2188	-0.2227	-0.2266	-0.2500
SE	setup↑ → CK	0.4414	0.4062	0.3945	0.4219
	setup↓ → CK	0.4258	0.4102	0.3633	0.2734
	hold↑ → CK	-0.0703	-0.0820	-0.0820	-0.1016
	hold↓ → CK	-0.1055	-0.1406	-0.1367	-0.1328
D	setup↑ → CK	0.0977	0.1289	0.1250	0.1172
	setup↓ → CK	0.4453	0.4219	0.3711	0.2773
	hold↑ → CK	-0.0508	-0.0820	-0.0820	-0.0781
	hold↓ → CK	-0.2734	-0.2617	-0.2227	-0.1445
CK	minpwh	0.0979	0.0979	0.0930	0.0785
	minpwl	0.1805	0.1756	0.1659	0.1416

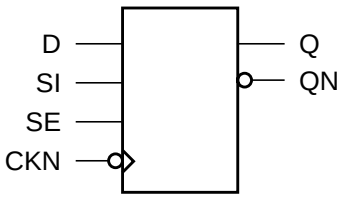
Cell Description

The SDFFN cell is a negative-edge triggered, static D-type flip-flop with scan input (SI) and active-high scan enable (SE).

Functions

D	SI	SE	CKN	Q[n+1]	QN[n+1]
1	x	0	↓	1	0
0	x	0	↓	0	1
x	x	x	↑	Q[n]	QN[n]
x	1	1	↓	1	0
x	0	1	↓	0	1

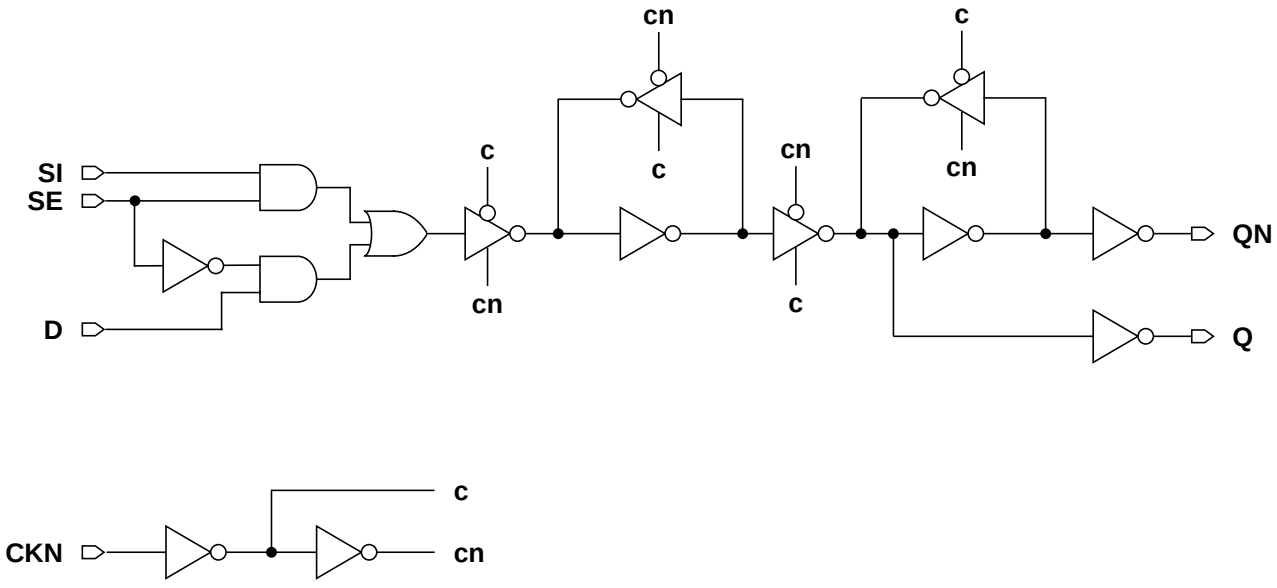
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
SDFFNXL	5.04	12.32
SDFFNX1	5.04	12.32
SDFFNX2	5.04	14.00
SDFFNX4	5.04	16.24

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
SI	0.0459	0.0417	0.0494	0.0720
SE	0.0524	0.0493	0.0552	0.0743
D	0.0393	0.0371	0.0428	0.0605
CKN	0.0378	0.0384	0.0495	0.0729
Q	0.0379	0.0408	0.0692	0.1099

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
SI	0.0021	0.0021	0.0021	0.0021
SE	0.0044	0.0041	0.0041	0.0046
D	0.0027	0.0018	0.0017	0.0026
CKN	0.0021	0.0026	0.0034	0.0051

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CKN → Q↑	0.1479	0.1248	0.1151	0.0985	4.5215	3.9985	2.0156	1.0116
CKN → Q↓	0.2528	0.2284	0.2056	0.1766	2.5888	2.2921	1.1452	0.5815
CKN → QN↑	0.3036	0.2730	0.2488	0.2162	4.4700	3.9805	2.2394	1.0155
CKN → QN↓	0.2075	0.1844	0.1723	0.1520	2.5213	2.2651	1.1517	0.5802

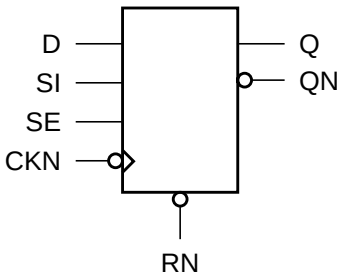
Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
SI	setup↑ → CKN	0.1133	0.1055	0.1211	0.1523
	setup↓ → CKN	0.2539	0.2773	0.2734	0.3125
	hold↑ → CKN	0.0156	0.0039	-0.0117	-0.0391
	hold↓ → CKN	-0.2227	-0.2422	-0.2344	-0.2656
SE	setup↑ → CKN	0.2695	0.2969	0.2891	0.3320
	setup↓ → CKN	0.1328	0.2969	0.2266	0.1797
	hold↑ → CKN	0.0234	0.0117	0.0000	-0.0312
	hold↓ → CKN	-0.0039	-0.0430	-0.0547	-0.0547
D	setup↑ → CKN	0.0664	0.0977	0.1094	0.1016
	setup↓ → CKN	0.1328	0.3008	0.2305	0.1797
	hold↑ → CKN	0.0391	0.0078	-0.0078	-0.0078
	hold↓ → CKN	-0.1133	-0.2578	-0.1953	-0.1484
CKN	minpwl	0.1173	0.1028	0.0979	0.0833
	minpwh	0.1222	0.1368	0.1319	0.1125

Cell Description

The SDFFNR cell is a negative-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low reset (RN).

Logic Symbol



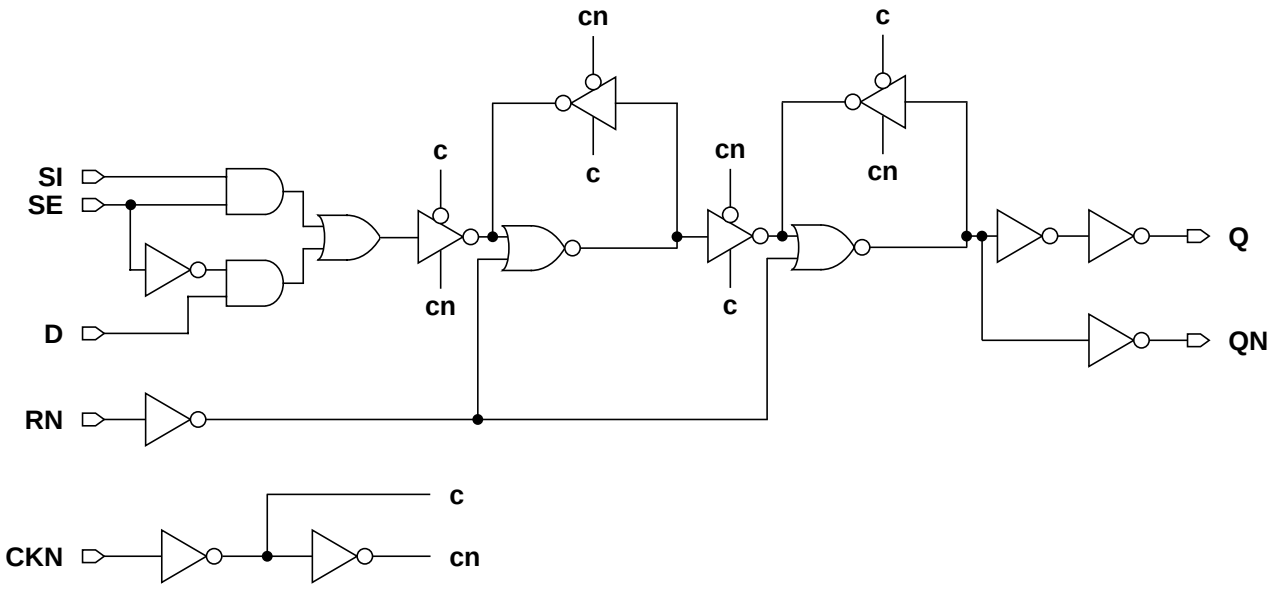
Functions

RN	D	SI	SE	CKN	Q[n+1]	QN[n+1]
1	1	x	0	↓	1	0
1	0	x	0	↓	0	1
1	x	x	x	↑	Q[n]	QN[n]
1	x	1	1	↓	1	0
1	x	0	1	↓	0	1
0	x	x	x	x	0	1

Cell Size

Drive Strength	Height (µm)	Width (µm)
SDFFNRXL	5.04	16.24
SDFFNRX1	5.04	16.24
SDFFNRX2	5.04	16.24
SDFFNRX4	5.04	20.16

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
SI	0.0457	0.0413	0.0421	0.0546
SE	0.0526	0.0472	0.0494	0.0596
D	0.0389	0.0358	0.0368	0.0480
CKN	0.0387	0.0371	0.0400	0.0547
RN	0.0162	0.0173	0.0187	0.0301
Q	0.0466	0.0516	0.0735	0.1266

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
SI	0.0019	0.0019	0.0020	0.0019
SE	0.0047	0.0040	0.0044	0.0043
D	0.0026	0.0017	0.0019	0.0023
CKN	0.0022	0.0027	0.0027	0.0034
RN	0.0021	0.0023	0.0029	0.0048

Delays at 25^{o}C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CKN → Q↑	0.2945	0.2644	0.2524	0.2365	4.4703	3.9796	2.0192	0.9883
CKN → Q↓	0.3822	0.3428	0.3273	0.3069	2.4910	2.2544	1.1523	0.5759
RN → Q↓	0.1978	0.1871	0.1834	0.1707	2.4914	2.2545	1.1524	0.5759
CKN → QN↑	0.3440	0.3015	0.2694	0.2527	4.4718	3.9792	2.0201	0.9887
CKN → QN↓	0.2659	0.2376	0.2104	0.1969	2.6785	2.3014	1.1682	0.5834
RN → QN↑	0.1601	0.1466	0.1260	0.1171	4.4813	3.9827	2.0216	0.9897

Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
SI	setup↑ → CKN	0.1094	0.1133	0.1250	0.1445
	setup↓ → CKN	0.2578	0.2773	0.2852	0.2969
	hold↑ → CKN	0.0156	-0.0039	-0.0117	-0.0273
	hold↓ → CKN	-0.2305	-0.2422	-0.2539	-0.2578
SE	setup↑ → CKN	0.2773	0.2930	0.2969	0.3125
	setup↓ → CKN	0.1328	0.2656	0.2773	0.2188
	hold↑ → CKN	0.0234	0.0039	0.0000	-0.0156
	hold↓ → CKN	-0.0039	-0.0469	-0.0508	-0.0625
D	setup↑ → CKN	0.0625	0.1016	0.1133	0.1250
	setup↓ → CKN	0.1367	0.2734	0.2812	0.2227
	hold↑ → CKN	0.0391	-0.0039	-0.0078	-0.0195
	hold↓ → CKN	-0.1172	-0.2344	-0.2461	-0.1875
CKN	minpwl	0.1319	0.1173	0.1076	0.0979
	minpwh	0.1173	0.1368	0.1416	0.1416
RN	minpwl	0.1562	0.1513	0.1562	0.2437
	recovery	0.0273	0.0469	0.0547	0.0547

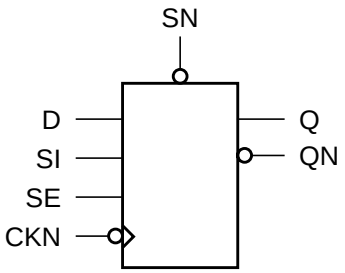
Cell Description

The SDFFNS cell is a negative-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low set (SN).

Functions

SN	D	SI	SE	CKN	Q[n+1]	QN[n+1]
1	1	x	0	↓	1	0
1	0	x	0	↓	0	1
1	x	x	x	↑	Q[n]	QN[n]
1	x	1	1	↓	1	0
1	x	0	1	↓	0	1
0	x	x	x	x	1	0

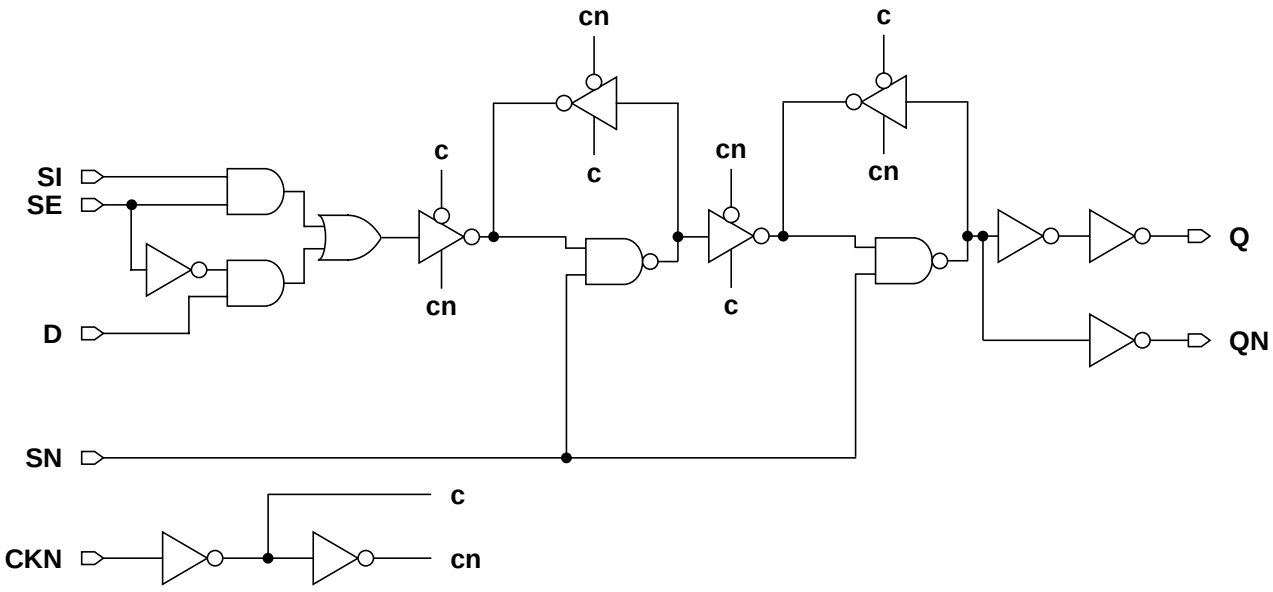
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
SDFFNSXL	5.04	14.56
SDFFNSX1	5.04	14.56
SDFFNSX2	5.04	15.12
SDFFNSX4	5.04	19.60

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
SI	0.0467	0.0384	0.0408	0.0472
SE	0.0537	0.0449	0.0477	0.0539
D	0.0396	0.0336	0.0359	0.0414
CKN	0.0377	0.0354	0.0372	0.0466
SN	0.0065	0.0065	0.0089	0.0152
Q	0.0429	0.0469	0.0701	0.1265

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
SI	0.0019	0.0019	0.0018	0.0020
SE	0.0048	0.0041	0.0041	0.0043
D	0.0025	0.0016	0.0016	0.0018
CKN	0.0020	0.0026	0.0026	0.0031
SN	0.0048	0.0050	0.0062	0.0105

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CKN → Q↑	0.2396	0.2180	0.2219	0.2137	4.4696	3.9789	2.0191	1.0098
CKN → Q↓	0.3296	0.3177	0.3195	0.3074	2.4872	2.2530	1.1518	0.5756
SN → Q↑	0.1301	0.1162	0.1259	0.1185	4.4694	3.9789	2.0192	1.0098
CKN → QN↑	0.2964	0.2817	0.2638	0.2553	4.4770	3.9810	2.0221	1.0113
CKN → QN↓	0.2126	0.1908	0.1813	0.1754	2.5424	2.2622	1.1549	0.5774
SN → QN↓	0.1036	0.0897	0.0856	0.0808	2.5406	2.2638	1.1563	0.5792

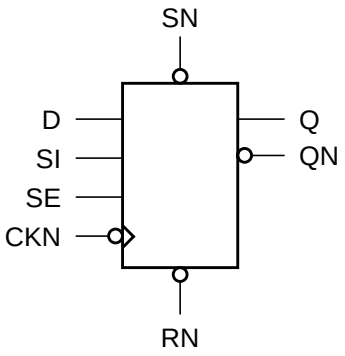
Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
SI	setup↑ → CKN	0.0938	0.0977	0.1016	0.1133
	setup↓ → CKN	0.2539	0.2812	0.2852	0.2734
	hold↑ → CKN	0.0156	-0.0039	-0.0039	-0.0117
	hold↓ → CKN	-0.2305	-0.2539	-0.2578	-0.2461
SE	setup↑ → CKN	0.2695	0.3008	0.3086	0.2891
	setup↓ → CKN	0.1328	0.2969	0.3008	0.2383
	hold↑ → CKN	0.0234	0.0039	0.0039	-0.0039
	hold↓ → CKN	-0.0039	-0.0469	-0.0508	-0.0547
D	setup↑ → CKN	0.0508	0.0859	0.0898	0.1016
	setup↓ → CKN	0.1328	0.3086	0.3125	0.2422
	hold↑ → CKN	0.0391	-0.0039	-0.0039	-0.0117
	hold↓ → CKN	-0.1172	-0.2734	-0.2773	-0.2148
CKN	minpwl	0.1173	0.1076	0.1028	0.0979
	minpwh	0.1125	0.1222	0.1271	0.1319
SN	minpwl	0.1028	0.0882	0.0979	0.1173
	recovery	-0.0781	-0.0391	-0.0352	-0.0352

Cell Description

The SDFFNSR cell is a negative-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low reset (RN) and set (SN). Set (SN) dominates reset (RN).

Logic Symbol



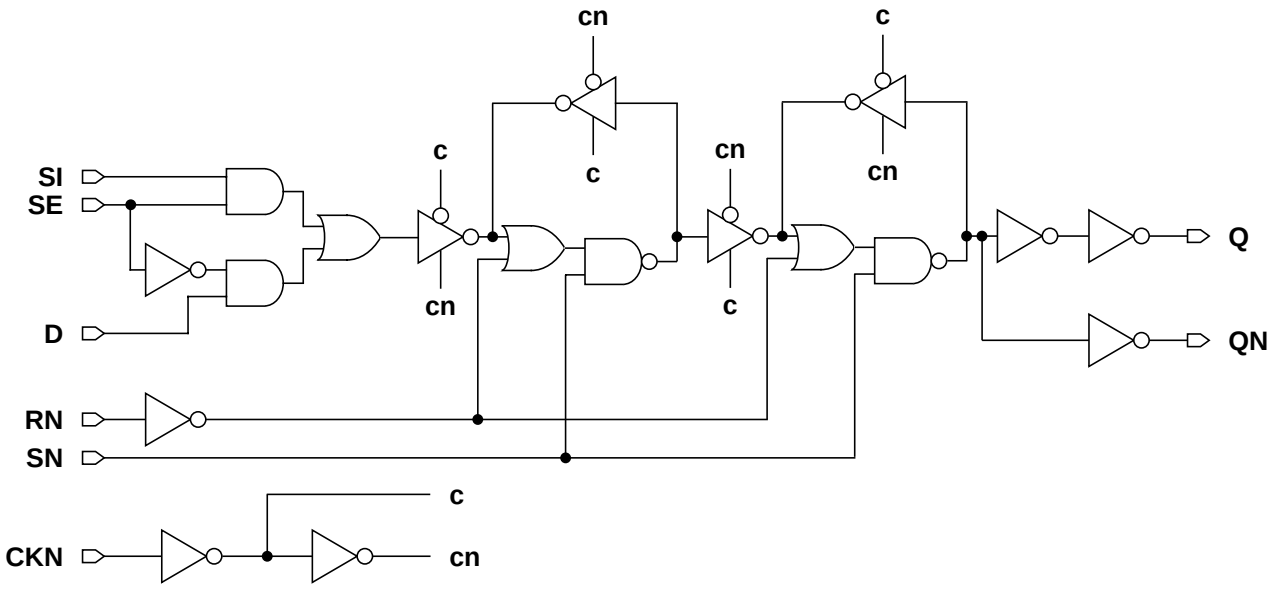
Functions

RN	SN	D	SI	SE	CKN	Q[n+1]	QN[n+1]
1	1	1	x	0	↓	1	0
1	1	0	x	0	↓	0	1
1	1	x	x	x	↑	Q[n]	QN[n]
1	1	x	1	1	↓	1	0
1	1	x	0	1	↓	0	1
0	1	x	x	x	x	0	1
1	0	x	x	x	x	1	0
0	0	x	x	x	x	1	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
SDFFNSRXL	5.04	16.80
SDFFNSRX1	5.04	16.80
SDFFNSRX2	5.04	16.80
SDFFNSRX4	5.04	22.96

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
SI	0.0408	0.0378	0.0430	0.0572
SE	0.0478	0.0458	0.0518	0.0635
D	0.0349	0.0326	0.0375	0.0499
CKN	0.0329	0.0357	0.0384	0.0541
SN	0.0070	0.0071	0.0094	0.0144
RN	0.0181	0.0186	0.0233	0.0364
Q	0.0455	0.0509	0.0772	0.1391

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
SI	0.0017	0.0016	0.0017	0.0018
SE	0.0046	0.0045	0.0046	0.0046
D	0.0017	0.0015	0.0016	0.0021
CKN	0.0021	0.0025	0.0026	0.0035
SN	0.0059	0.0061	0.0076	0.0128
RN	0.0026	0.0027	0.0036	0.0051

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CKN → Q↑	0.3052	0.2547	0.2521	0.2421	4.4662	3.9779	2.0191	1.0044
CKN → Q↓	0.3762	0.3322	0.3307	0.3099	2.4965	2.2568	1.1693	0.5760
SN → Q↑	0.1555	0.1360	0.1404	0.1359	4.4659	3.9779	2.0191	1.0044
SN → Q↓	0.1462	0.1398	0.1419	0.1360	2.4972	2.2571	1.1694	0.5761
RN → Q↓	0.2156	0.2034	0.1977	0.1891	2.4971	2.2571	1.1694	0.5761
CKN → QN↑	0.3329	0.2836	0.2731	0.2552	4.4900	3.9858	2.0228	1.0066
CKN → QN↓	0.2708	0.2212	0.2112	0.2034	2.6939	2.3067	1.1551	0.5873
SN → QN↑	0.1037	0.0923	0.0851	0.0818	4.5119	3.9948	2.0276	1.0096
SN → QN↓	0.1205	0.1001	0.0989	0.0970	2.5718	2.2739	1.1437	0.5830
RN → QN↑	0.1729	0.1557	0.1407	0.1347	4.5096	3.9941	2.0273	1.0095

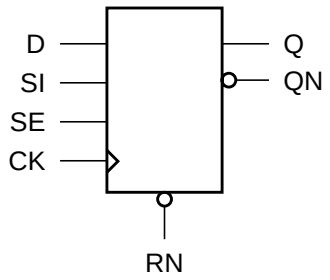
Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
SI	setup↑ → CKN	0.1094	0.1484	0.1445	0.1602
	setup↓ → CKN	0.2617	0.2891	0.2930	0.3008
	hold↑ → CKN	0.0000	-0.0234	-0.0195	-0.0352
	hold↓ → CKN	-0.2266	-0.2500	-0.2539	-0.2578
SE	setup↑ → CKN	0.2852	0.3203	0.3164	0.3164
	setup↓ → CKN	0.2188	0.3086	0.2773	0.2031
	hold↑ → CKN	0.0078	-0.0117	-0.0078	-0.0273
	hold↓ → CKN	-0.0469	-0.0703	-0.0664	-0.0625
D	setup↑ → CKN	0.0977	0.1367	0.1289	0.1289
	setup↓ → CKN	0.2188	0.3125	0.2773	0.2031
	hold↑ → CKN	0.0039	-0.0156	-0.0117	-0.0156
	hold↓ → CKN	-0.1875	-0.2656	-0.2383	-0.1680
CKN	minpwl	0.1416	0.1028	0.1028	0.0930
	minpwh	0.1368	0.1465	0.1513	0.1368
SN	minpwl	0.1173	0.1028	0.1076	0.1368
	recovery	-0.0547	-0.0195	-0.0273	-0.0312
	removal	0.0586	0.0273	0.0352	0.0391
RN	minpwl	0.1562	0.1513	0.1611	0.2534
	recovery	0.0430	0.0898	0.0703	0.0703
	removal	0.0586	0.0195	0.0430	0.0391

Cell Description

The SDFFR cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low reset (RN).

Logic Symbol



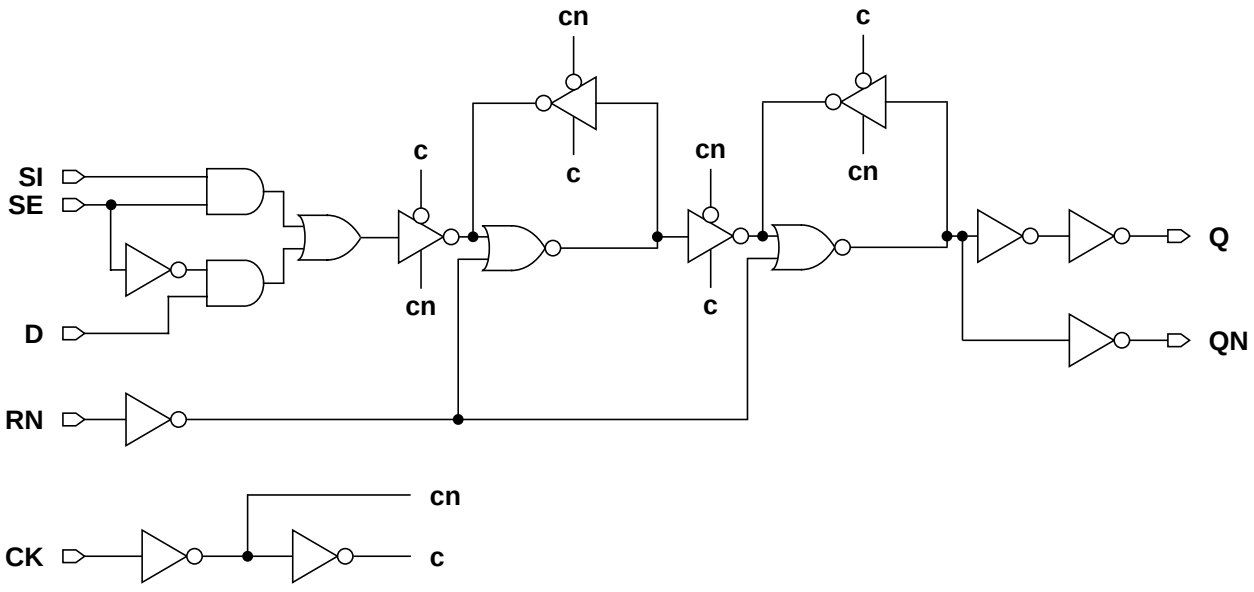
Functions

RN	D	SI	SE	CK	Q[n+1]	QN[n+1]
1	1	x	0	↑	1	0
1	0	x	0	↑	0	1
1	x	x	x	↓	Q[n]	QN[n]
1	x	1	1	↑	1	0
1	x	0	1	↑	0	1
0	x	x	x	x	0	1

Cell Size

Drive Strength	Height (µm)	Width (µm)
SDFFRXL	5.04	16.24
SDFFRX1	5.04	16.24
SDFFRX2	5.04	16.24
SDFFRX4	5.04	20.16

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
SI	0.0469	0.0418	0.0408	0.0543
SE	0.0536	0.0478	0.0481	0.0600
D	0.0404	0.0364	0.0358	0.0478
CK	0.0456	0.0436	0.0418	0.0514
RN	0.0152	0.0164	0.0182	0.0296
Q	0.0476	0.0512	0.0742	0.1272

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
SI	0.0022	0.0022	0.0023	0.0021
SE	0.0050	0.0043	0.0046	0.0046
D	0.0031	0.0021	0.0021	0.0027
CK	0.0022	0.0027	0.0027	0.0034
RN	0.0020	0.0021	0.0028	0.0047

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.3412	0.3165	0.2965	0.2770	4.4689	3.9796	2.0191	1.0098
CK → Q↓	0.2485	0.2519	0.2370	0.2204	2.4904	2.2547	1.1521	0.5758
RN → Q↓	0.1939	0.1850	0.1832	0.1695	2.4908	2.2548	1.1522	0.5758
CK → QN↑	0.2101	0.2102	0.1791	0.1672	4.4703	3.9791	2.0201	1.0103
CK → QN↓	0.3119	0.2887	0.2544	0.2378	2.6698	2.2991	1.1682	0.5833
RN → QN↑	0.1558	0.1441	0.1259	0.1169	4.4800	3.9827	2.0216	1.0113

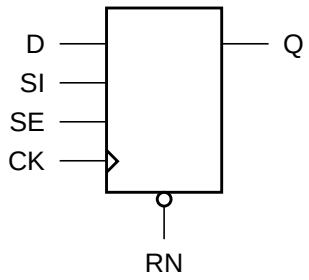
Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
SI	setup↑ → CK	0.1328	0.1250	0.1289	0.1484
	setup↓ → CK	0.2695	0.2812	0.2930	0.3047
	hold↑ → CK	-0.1094	-0.1016	-0.1055	-0.1211
	hold↓ → CK	-0.1719	-0.1953	-0.2031	-0.2148
SE	setup↑ → CK	0.2891	0.2969	0.3047	0.3203
	setup↓ → CK	0.1484	0.2734	0.2852	0.2305
	hold↑ → CK	-0.1055	-0.0859	-0.0898	-0.1055
	hold↓ → CK	-0.0508	-0.1328	-0.1367	-0.1445
D	setup↑ → CK	0.0820	0.1094	0.1133	0.1250
	setup↓ → CK	0.1484	0.2852	0.2891	0.2383
	hold↑ → CK	-0.0664	-0.0859	-0.0898	-0.1016
	hold↓ → CK	-0.0586	-0.2031	-0.2031	-0.1523
CK	minpwh	0.1076	0.1028	0.0882	0.0833
	minpwl	0.1854	0.1756	0.1756	0.1756
RN	minpwl	0.1513	0.1465	0.1562	0.2437
	recovery	0.0234	0.0391	0.0391	0.0430
	removal	-0.0078	-0.0234	-0.0234	-0.0156

Cell Description

The SDFFRHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low reset (RN). The cell has a single output (Q) and fast clock-to-out path.

Logic Symbol



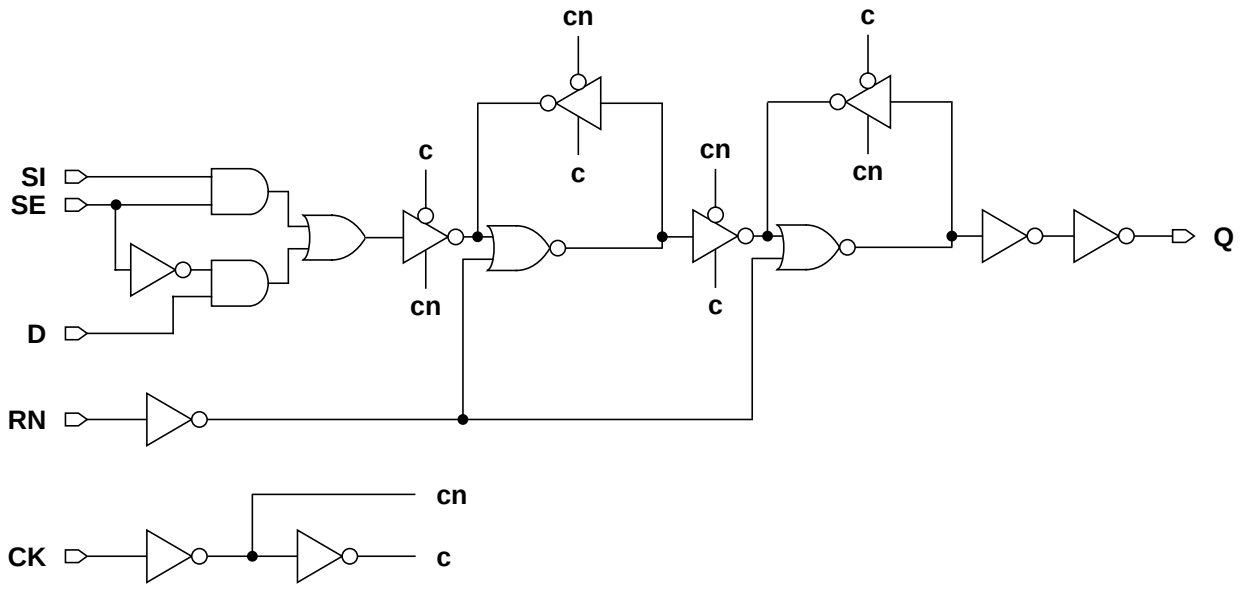
Functions

RN	D	SI	SE	CK	Q[n+1]
1	1	x	0	↑	1
1	0	x	0	↑	0
1	x	x	x	↓	Q[n]
1	x	1	1	↑	1
1	x	0	1	↑	0
0	x	x	x	x	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
SDFFRHQXL	5.04	15.12
SDFFRHQX1	5.04	15.12
SDFFRHQX2	5.04	17.92
SDFFRHQX4	5.04	21.84

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
SI	0.0390	0.0474	0.0683	0.1054
SE	0.0464	0.0543	0.0740	0.1073
D	0.0338	0.0440	0.0625	0.0930
CK	0.0408	0.0413	0.0487	0.0639
RN	0.0182	0.0228	0.0308	0.0485
Q	0.0291	0.0306	0.0432	0.0712

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
SI	0.0019	0.0019	0.0019	0.0019
SE	0.0043	0.0037	0.0040	0.0047
D	0.0022	0.0016	0.0019	0.0030
CK	0.0017	0.0023	0.0031	0.0047
RN	0.0020	0.0032	0.0044	0.0073

Delays at 25^{o}C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.2257	0.1856	0.1568	0.1446	6.4321	5.8798	2.8923	1.5927
CK → Q↓	0.2366	0.1575	0.1331	0.1206	2.8380	2.2905	1.1608	0.5786
RN → Q↓	0.1514	0.1154	0.1011	0.0806	2.4123	1.8562	1.0257	0.5620

Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
SI	setup↑ → CK	0.1562	0.1602	0.1875	0.2070
	setup↓ → CK	0.3516	0.3867	0.4062	0.4453
	hold↑ → CK	-0.1055	-0.1016	-0.1211	-0.1367
	hold↓ → CK	-0.1602	-0.2188	-0.2344	-0.2812
SE	setup↑ → CK	0.3633	0.3984	0.4180	0.4766
	setup↓ → CK	0.2305	0.3828	0.3203	0.2539
	hold↑ → CK	-0.0977	-0.0898	-0.1094	-0.1328
	hold↓ → CK	-0.0508	-0.1406	-0.1484	-0.1094
D	setup↑ → CK	0.1055	0.1445	0.1602	0.1289
	setup↓ → CK	0.2266	0.3789	0.3203	0.2539
	hold↑ → CK	-0.0586	-0.0898	-0.0977	-0.0703
	hold↓ → CK	-0.0586	-0.2148	-0.1562	-0.1133
CK	minpwh	0.1222	0.1028	0.0882	0.0785
	minpwl	0.1951	0.1854	0.1708	0.1368
RN	minpwl	0.2534	0.2534	0.3311	0.5206
	recovery	0.0859	0.0781	0.0898	0.0820
	removal	-0.0195	-0.0234	-0.0195	-0.0039

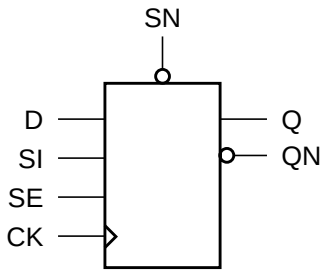
Cell Description

The SDFFS cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low set (SN).

Functions

SN	D	SI	SE	CK	Q[n+1]	QN[n+1]
1	1	x	0	↑	1	0
1	0	x	0	↑	0	1
1	x	x	x	↓	Q[n]	QN[n]
1	x	1	1	↑	1	0
1	x	0	1	↑	0	1
0	x	x	x	x	1	0

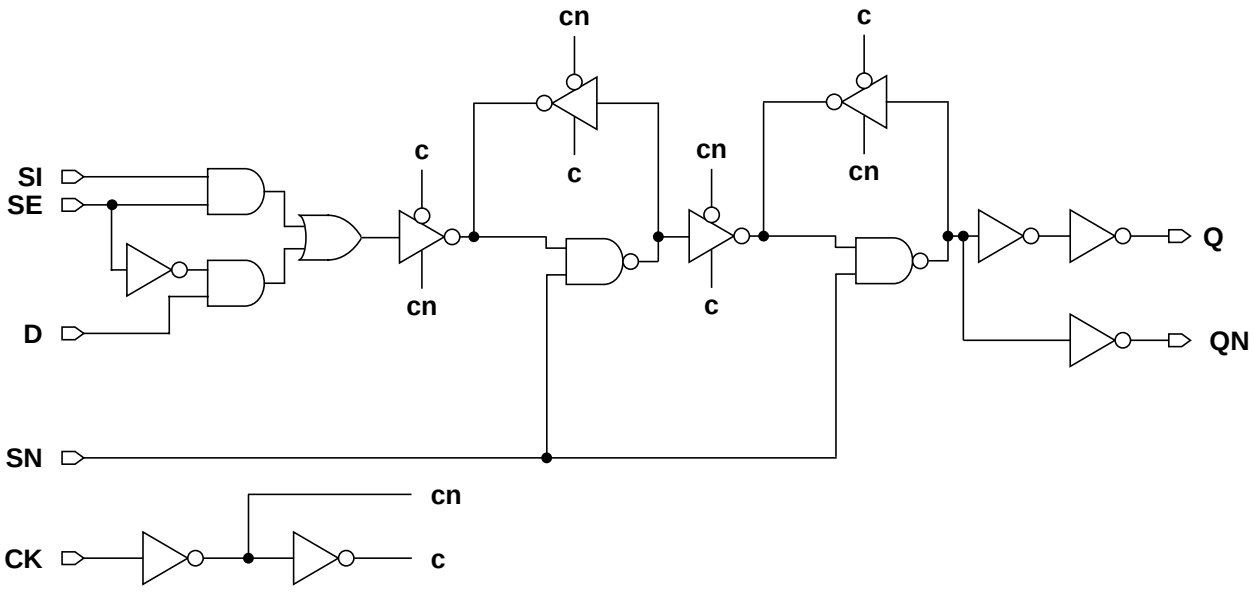
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
SDFFSXL	5.04	14.00
SDFFSX1	5.04	14.56
SDFFSX2	5.04	15.12
SDFFSX4	5.04	19.04

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
SI	0.0450	0.0377	0.0390	0.0452
SE	0.0520	0.0447	0.0457	0.0518
D	0.0380	0.0329	0.0341	0.0392
CK	0.0453	0.0420	0.0444	0.0469
SN	0.0069	0.0070	0.0090	0.0152
Q	0.0413	0.0445	0.0733	0.1168

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
SI	0.0021	0.0020	0.0021	0.0022
SE	0.0054	0.0046	0.0045	0.0046
D	0.0029	0.0019	0.0019	0.0020
CK	0.0024	0.0029	0.0029	0.0032
SN	0.0052	0.0054	0.0066	0.0108

Delays at 25^{o}C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.2883	0.2649	0.2786	0.2554	4.4679	3.9784	2.0192	1.0098
CK → Q↓	0.2348	0.2390	0.2501	0.2207	2.4877	2.2532	1.1521	0.5755
SN → Q↑	0.1303	0.1180	0.1302	0.1161	4.4676	3.9784	2.0191	1.0097
CK → QN↑	0.2008	0.2020	0.1925	0.1692	4.4774	3.9812	2.0222	1.0113
CK → QN↓	0.2610	0.2371	0.2364	0.2177	2.5433	2.2627	1.1553	0.5772
SN → QN↓	0.1033	0.0907	0.0883	0.0789	2.5393	2.2638	1.1569	0.5789

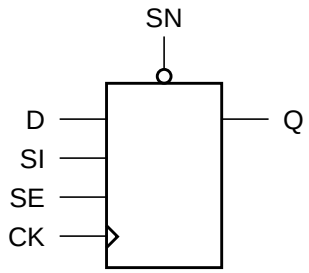
Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
SI	setup↑ → CK	0.1172	0.1055	0.1055	0.1172
	setup↓ → CK	0.2656	0.2930	0.2852	0.2812
	hold↑ → CK	-0.1016	-0.0859	-0.0859	-0.0938
	hold↓ → CK	-0.1875	-0.2227	-0.2148	-0.1992
SE	setup↑ → CK	0.2812	0.3125	0.3047	0.2969
	setup↓ → CK	0.1445	0.3086	0.3047	0.2461
	hold↑ → CK	-0.0898	-0.0703	-0.0703	-0.0820
	hold↓ → CK	-0.0703	-0.1250	-0.1211	-0.1289
D	setup↑ → CK	0.0781	0.0938	0.0938	0.1016
	setup↓ → CK	0.1445	0.3203	0.3125	0.2500
	hold↑ → CK	-0.0664	-0.0742	-0.0742	-0.0820
	hold↓ → CK	-0.0703	-0.2578	-0.2461	-0.1719
CK	minpwh	0.0979	0.0930	0.0882	0.0833
	minpwl	0.1805	0.1611	0.1659	0.1611
SN	minpwl	0.1028	0.0882	0.0979	0.1125
	recovery	-0.0234	-0.0078	-0.0078	0.0000
	removal	0.1172	0.0781	0.0820	0.0781

Cell Description

The SDFFSHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low set (SN). The cell has a single output (Q) and fast clock-to-out path.

Logic Symbol



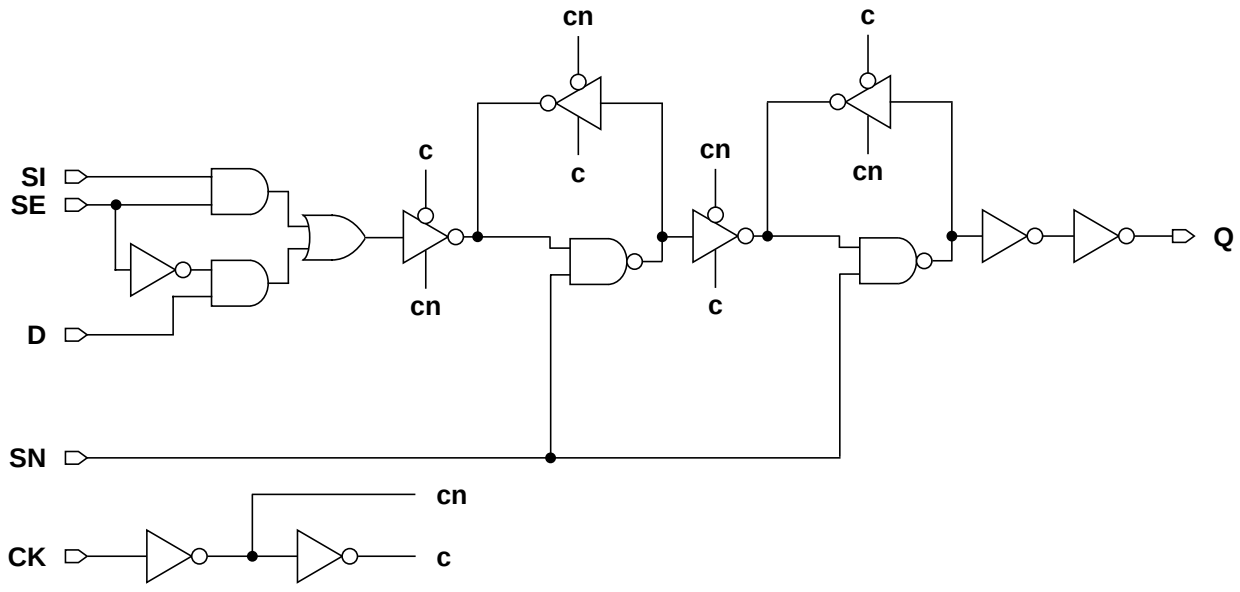
Functions

SN	D	SI	SE	CK	Q[n+1]
1	1	x	0	↑	1
1	0	x	0	↑	0
1	x	x	x	↓	Q[n]
1	x	1	1	↑	1
1	x	0	1	↑	0
0	x	x	x	x	1

Cell Size

Drive Strength	Height (µm)	Width (µm)
SDFFSHQXL	5.04	14.00
SDFFSHQX1	5.04	14.00
SDFFSHQX2	5.04	16.24
SDFFSHQX4	5.04	18.48

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
SI	0.0415	0.0469	0.0620	0.1003
SE	0.0500	0.0542	0.0670	0.0953
D	0.0371	0.0439	0.0565	0.0831
CK	0.0386	0.0374	0.0435	0.0606
SN	0.0088	0.0085	0.0136	0.0232
Q	0.0291	0.0271	0.0374	0.0621

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
SI	0.0021	0.0020	0.0018	0.0023
SE	0.0044	0.0039	0.0038	0.0045
D	0.0024	0.0014	0.0017	0.0026
CK	0.0018	0.0023	0.0029	0.0045
SN	0.0075	0.0074	0.0114	0.0177

Delays at 25^{o}C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.2293	0.1763	0.1571	0.1376	4.5130	4.0704	2.0433	1.0159
CK → Q↓	0.2585	0.1490	0.1342	0.1199	3.4095	2.7646	1.3803	0.6926
SN → Q↑	0.0615	0.0761	0.0792	0.0822	2.6363	2.2025	1.1524	0.6104

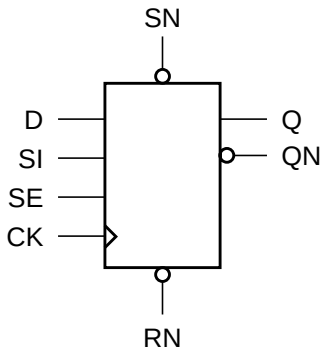
Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
SI	setup↑ → CK	0.1367	0.1406	0.1523	0.1836
	setup↓ → CK	0.3008	0.4102	0.3906	0.4414
	hold↑ → CK	-0.1055	-0.0977	-0.1094	-0.1250
	hold↓ → CK	-0.1836	-0.2461	-0.2422	-0.2969
SE	setup↑ → CK	0.3281	0.4258	0.4102	0.4570
	setup↓ → CK	0.1875	0.4531	0.3281	0.2773
	hold↑ → CK	-0.0977	-0.0820	-0.0977	-0.1211
	hold↓ → CK	-0.0664	-0.1328	-0.1445	-0.1211
D	setup↑ → CK	0.0898	0.1250	0.1328	0.1172
	setup↓ → CK	0.1836	0.4531	0.3320	0.2734
	hold↑ → CK	-0.0664	-0.0820	-0.0898	-0.0703
	hold↓ → CK	-0.0742	-0.2930	-0.1875	-0.1445
CK	minpwh	0.1222	0.1028	0.0882	0.0785
	minpwl	0.1854	0.1708	0.1659	0.1416
SN	minpwl	0.1028	0.1173	0.1513	0.2096
	recovery	-0.0117	0.0469	0.0469	0.0469
	removal	0.1328	0.0938	0.0938	0.0898

Cell Description

The SDFFSR cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low reset (RN) and set (SN). Set (SN) dominates reset (RN).

Logic Symbol



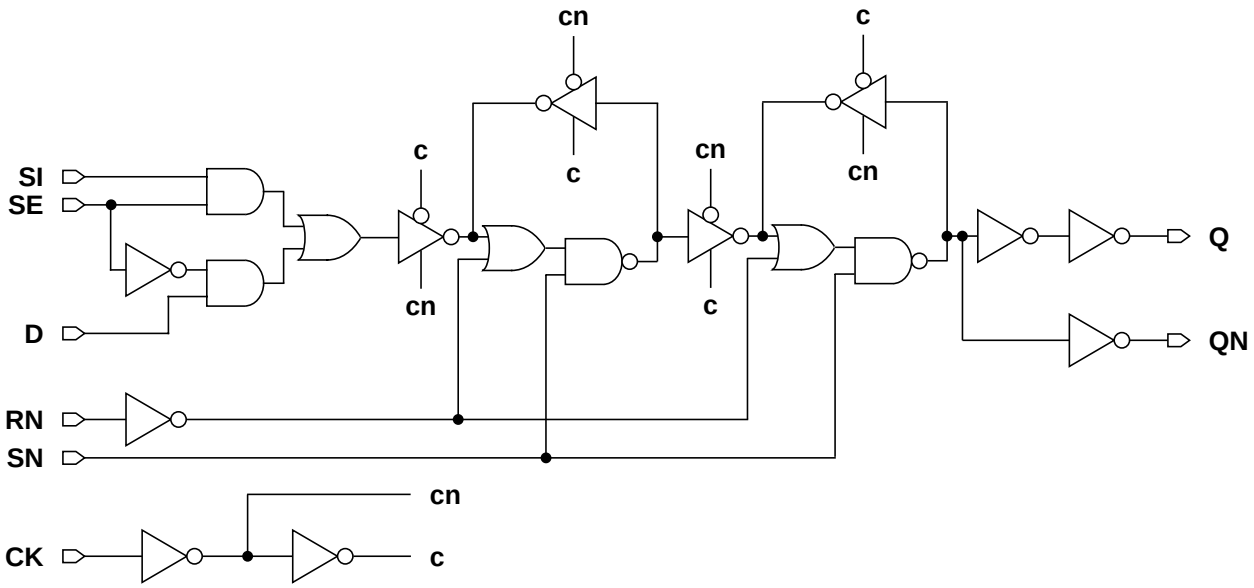
Functions

RN	SN	D	SI	SE	CK	Q[n+1]	QN[n+1]
1	1	1	x	0	↑	1	0
1	1	0	x	0	↑	0	1
1	1	x	x	x	↓	Q[n]	QN[n]
1	1	x	1	1	↑	1	0
1	1	x	0	1	↑	0	1
0	1	x	x	x	x	0	1
1	0	x	x	x	x	1	0
0	0	x	x	x	x	1	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
SDFFSRXL	5.04	17.36
SDFFSRX1	5.04	17.36
SDFFSRX2	5.04	17.36
SDFFSRX4	5.04	22.40

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
SI	0.0384	0.0384	0.0415	0.0575
SE	0.0463	0.0463	0.0497	0.0641
D	0.0331	0.0331	0.0359	0.0502
CK	0.0378	0.0388	0.0401	0.0496
SN	0.0074	0.0082	0.0101	0.0163
RN	0.0173	0.0186	0.0210	0.0335
Q	0.0474	0.0518	0.0766	0.1357

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
SI	0.0020	0.0020	0.0019	0.0020
SE	0.0045	0.0045	0.0047	0.0049
D	0.0019	0.0019	0.0019	0.0025
CK	0.0022	0.0027	0.0028	0.0036
SN	0.0057	0.0062	0.0077	0.0130
RN	0.0026	0.0028	0.0034	0.0051

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.3359	0.3036	0.2981	0.2858	4.4656	3.9780	2.0192	1.0098
CK → Q↓	0.2632	0.2496	0.2392	0.2362	2.4954	2.2563	1.1523	0.5758
SN → Q↑	0.1588	0.1425	0.1394	0.1343	4.4657	3.9779	2.0192	1.0098
SN → Q↓	0.1487	0.1399	0.1410	0.1348	2.4963	2.2565	1.1524	0.5758
RN → Q↓	0.2150	0.2043	0.1938	0.1817	2.4962	2.2565	1.1524	0.5758
CK → QN↑	0.2195	0.2019	0.1820	0.1831	4.4918	3.9853	2.0230	1.0121
CK → QN↓	0.3013	0.2708	0.2579	0.2483	2.7020	2.3065	1.1719	0.5872
SN → QN↑	0.1055	0.0933	0.0845	0.0823	4.5147	3.9945	2.0277	1.0154
SN → QN↓	0.1237	0.1074	0.0985	0.0966	2.5790	2.2766	1.1603	0.5834
RN → QN↑	0.1716	0.1574	0.1373	0.1290	4.5127	3.9939	2.0274	1.0152

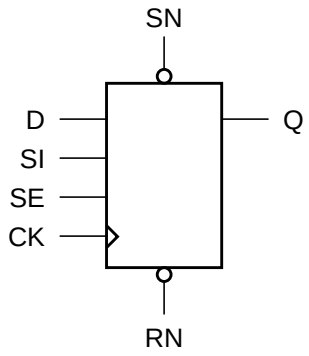
Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
SI	setup↑ → CK	0.1406	0.1484	0.1406	0.1641
	setup↓ → CK	0.2930	0.3047	0.2891	0.3164
	hold↑ → CK	-0.1055	-0.1133	-0.1094	-0.1250
	hold↓ → CK	-0.1875	-0.1992	-0.1875	-0.2109
SE	setup↑ → CK	0.3125	0.3281	0.3086	0.3320
	setup↓ → CK	0.3125	0.3242	0.2773	0.2227
	hold↑ → CK	-0.0938	-0.0977	-0.0977	-0.1172
	hold↓ → CK	-0.1445	-0.1523	-0.1484	-0.1250
D	setup↑ → CK	0.1250	0.1367	0.1250	0.1250
	setup↓ → CK	0.3203	0.3320	0.2773	0.2188
	hold↑ → CK	-0.0938	-0.0977	-0.0938	-0.0938
	hold↓ → CK	-0.2148	-0.2266	-0.1758	-0.1250
CK	minpwh	0.0979	0.0930	0.0930	0.0833
	minpwl	0.1951	0.1756	0.1708	0.1659
SN	minpwl	0.1222	0.1076	0.1076	0.1416
	recovery	0.0000	0.0117	0.0117	0.0078
	removal	0.0859	0.0742	0.0781	0.0820
RN	minpwl	0.1562	0.1513	0.1611	0.2631
	recovery	0.0703	0.0781	0.0586	0.0586
	removal	-0.0469	-0.0547	-0.0391	-0.0312

Cell Description

The SDFFSRHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low reset (RN) and set (SN), and set dominating reset. The cell has a single output (Q) and fast clock-to-out path.

Logic Symbol



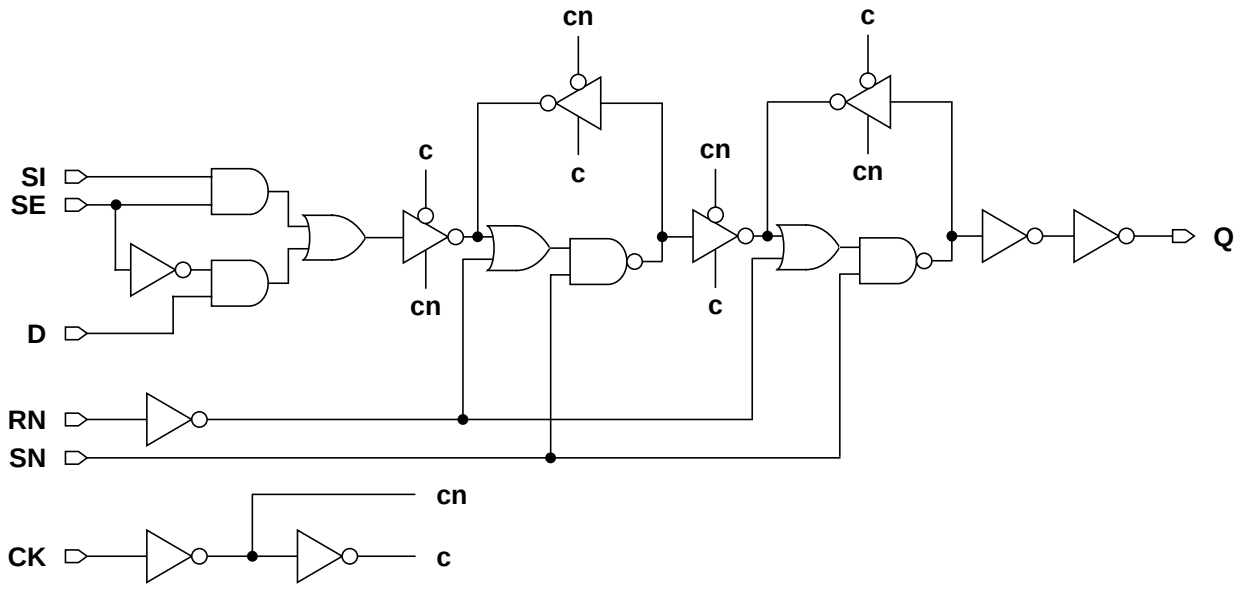
Functions

RN	SN	D	SI	SE	CK	Q[n+1]
1	1	1	x	0	↑	1
1	1	0	x	0	↑	0
1	1	x	x	x	↓	Q[n]
1	1	x	1	1	↑	1
1	1	x	0	1	↑	0
0	1	x	x	x	x	0
1	0	x	x	x	x	1
0	0	x	x	x	x	1

Cell Size

Drive Strength	Height (µm)	Width (µm)
SDFFSRHQXL	5.04	17.36
SDFFSRHQX1	5.04	17.36
SDFFSRHQX2	5.04	22.40
SDFFSRHQX4	5.04	29.68

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
SI	0.0443	0.0494	0.0713	0.1176
SE	0.0519	0.0569	0.0785	0.1184
D	0.0398	0.0450	0.0666	0.0991
CK	0.0398	0.0399	0.0498	0.0709
SN	0.0096	0.0106	0.0153	0.0249
RN	0.0222	0.0262	0.0371	0.0589
Q	0.0323	0.0298	0.0499	0.0791

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
SI	0.0017	0.0017	0.0017	0.0019
SE	0.0050	0.0045	0.0045	0.0052
D	0.0023	0.0015	0.0021	0.0037
CK	0.0020	0.0023	0.0036	0.0050
SN	0.0099	0.0102	0.0153	0.0235
RN	0.0019	0.0032	0.0043	0.0076

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.2307	0.1882	0.1710	0.1586	6.4279	5.8807	2.9167	1.4584
CK → Q↓	0.2270	0.1512	0.1376	0.1243	3.2695	2.7556	1.3760	0.6915
SN → Q↑	0.0856	0.0803	0.0880	0.0861	3.2974	2.5461	1.3226	0.6989
SN → Q↓	0.0395	0.0502	0.0452	0.0373	2.9924	2.4837	1.3167	0.6895
RN → Q↓	0.1594	0.1170	0.0991	0.0855	3.0391	2.4785	1.3138	0.6886

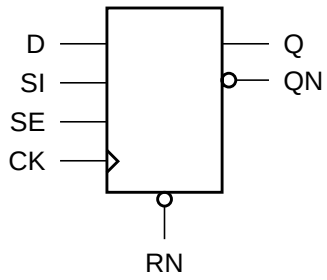
Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
SI	setup↑ → CK	0.1680	0.1719	0.1953	0.2461
	setup↓ → CK	0.3867	0.3789	0.4180	0.5117
	hold↑ → CK	-0.1055	-0.1094	-0.1250	-0.1602
	hold↓ → CK	-0.1836	-0.2109	-0.2461	-0.3516
SE	setup↑ → CK	0.4102	0.4062	0.4375	0.5508
	setup↓ → CK	0.2578	0.3516	0.3008	0.2656
	hold↑ → CK	-0.1016	-0.0938	-0.1172	-0.1562
	hold↓ → CK	-0.0703	-0.1562	-0.1406	-0.1211
D	setup↑ → CK	0.1172	0.1523	0.1562	0.1445
	setup↓ → CK	0.2578	0.3594	0.3008	0.2656
	hold↑ → CK	-0.0664	-0.0938	-0.0898	-0.0742
	hold↓ → CK	-0.0703	-0.1953	-0.1406	-0.1250
CK	minpwh	0.1222	0.1028	0.0930	0.0833
	minpwl	0.1951	0.1854	0.1708	0.1416
SN	minpwl	0.1125	0.1416	0.1805	0.2534
	recovery	0.0469	0.0508	0.0586	0.0586
	removal	0.1289	0.0898	0.0938	0.0938
RN	minpwl	0.2437	0.1805	0.2534	0.4234
	recovery	0.0898	0.0938	0.0938	0.0938
	removal	-0.0195	-0.0352	-0.0156	0.0078

Cell Description

The SDFFTR cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and synchronous active-low reset (RN). Scan enable (SE) dominates reset (RN).

Logic Symbol



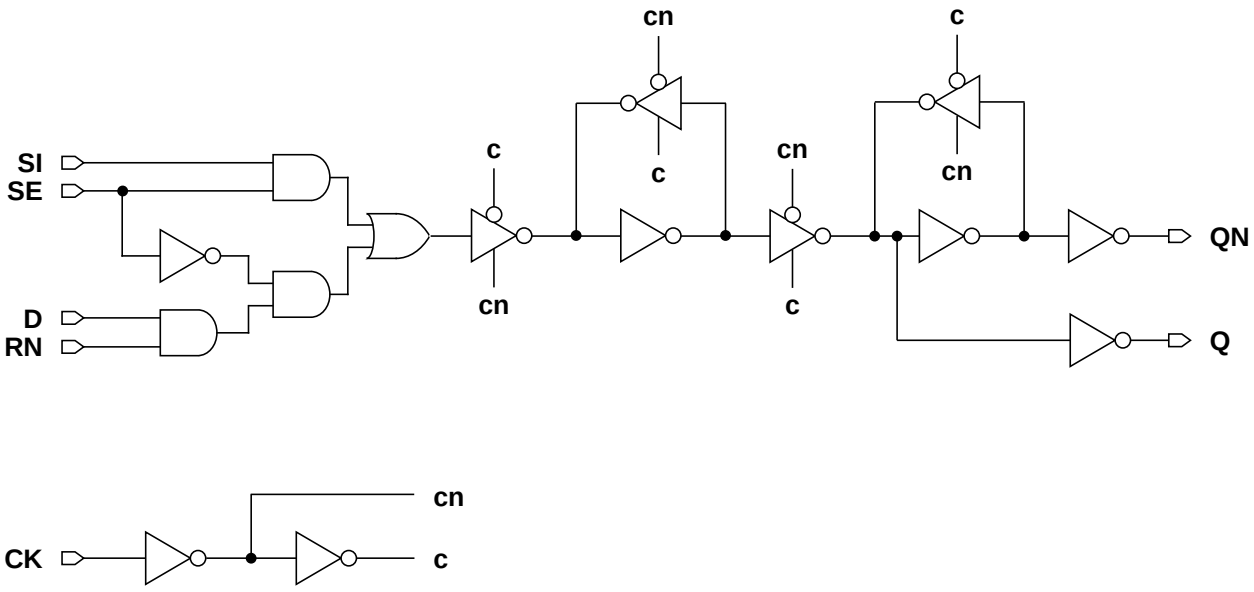
Functions

RN	D	SI	SE	CK	Q[n+1]	QN[n+1]
x	x	0	1	↑	0	1
x	x	1	1	↑	1	0
0	x	x	0	↑	0	1
1	0	x	0	↑	0	1
1	1	x	0	↑	1	0
x	x	x	x	↓	Q[n]	QN[n]

Cell Size

Drive Strength	Height (µm)	Width (µm)
SDFFTRXL	5.04	12.88
SDFFTRX1	5.04	12.88
SDFFTRX2	5.04	15.68
SDFFTRX4	5.04	17.92

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
SI	0.0403	0.0407	0.0515	0.0727
SE	0.0482	0.0488	0.0581	0.0752
D	0.0358	0.0362	0.0453	0.0593
CK	0.0417	0.0430	0.0527	0.0680
RN	0.0394	0.0398	0.0493	0.0658
Q	0.0333	0.0351	0.0623	0.1031

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
SI	0.0024	0.0024	0.0021	0.0024
SE	0.0047	0.0047	0.0044	0.0053
D	0.0017	0.0017	0.0019	0.0023
CK	0.0020	0.0027	0.0035	0.0054
RN	0.0019	0.0019	0.0021	0.0038

Delays at 25^{o}C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.1849	0.1723	0.1674	0.1376	4.4720	3.9810	2.0217	1.0112
CK → Q↓	0.1465	0.1373	0.1275	0.1181	2.5729	2.2845	1.1651	0.5823
CK → QN↑	0.1875	0.1769	0.1721	0.1571	4.4708	3.9802	2.0193	1.0099
CK → QN↓	0.2345	0.2255	0.2263	0.1900	2.5089	2.2621	1.1523	0.5757

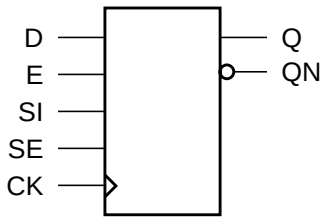
Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
SI	setup↑ → CK	0.1055	0.1094	0.1328	0.1523
	setup↓ → CK	0.2969	0.3125	0.3242	0.3594
	hold↑ → CK	-0.0859	-0.0859	-0.1055	-0.1211
	hold↓ → CK	-0.2070	-0.2266	-0.2305	-0.2734
SE	setup↑ → CK	0.3047	0.3203	0.3359	0.3594
	setup↓ → CK	0.3164	0.3320	0.2734	0.2148
	hold↑ → CK	-0.0664	-0.0742	-0.0898	-0.1133
	hold↓ → CK	-0.1484	-0.1523	-0.1680	-0.1328
D	setup↑ → CK	0.1172	0.1250	0.1406	0.1055
	setup↓ → CK	0.3164	0.3281	0.2773	0.2031
	hold↑ → CK	-0.0977	-0.1016	-0.1133	-0.0820
	hold↓ → CK	-0.2344	-0.2461	-0.1836	-0.1211
CK	minpwh	0.0979	0.0882	0.0882	0.0688
	minpwl	0.2048	0.1805	0.1854	0.1368
RN	setup↑ → CK	0.1211	0.1328	0.1523	0.1133
	setup↓ → CK	0.3594	0.3711	0.3086	0.2344
	hold↑ → CK	-0.1055	-0.1055	-0.1211	-0.0938
	hold↓ → CK	-0.2578	-0.2812	-0.2070	-0.1445

Cell Description

The SEDFF cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and synchronous active-high enable (E).

Logic Symbol



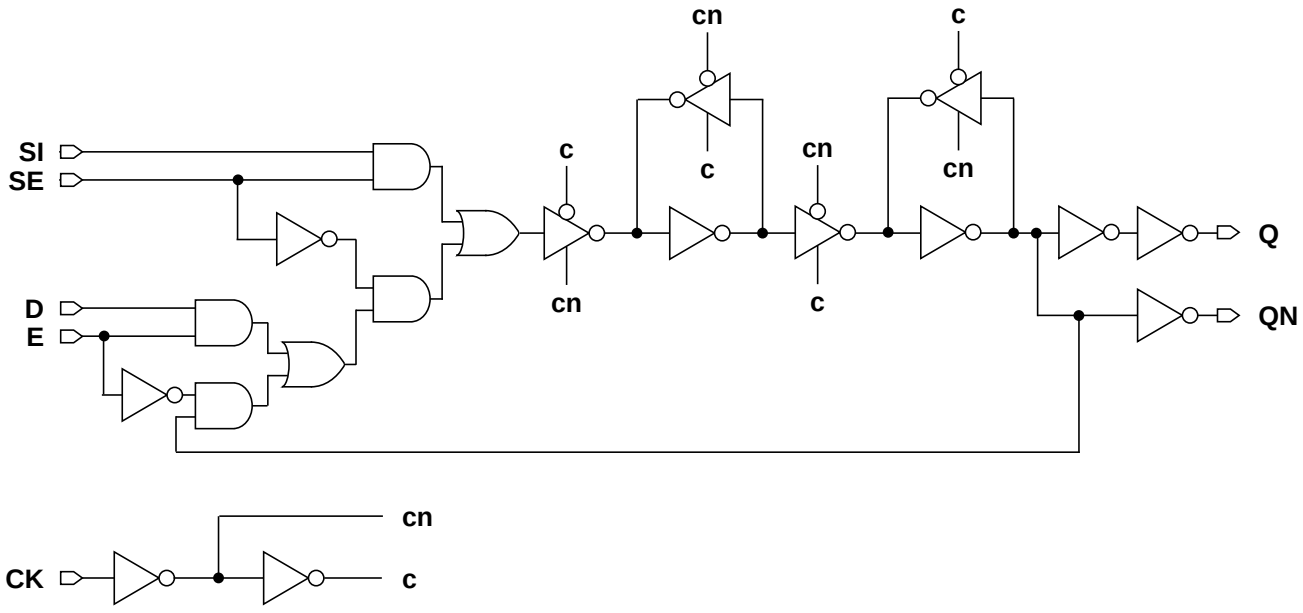
Functions

D	E	SI	SE	CK	Q[n+1]	QN[n+1]
x	x	1	1	↑	1	0
x	x	0	1	↑	0	1
x	0	x	0	↑	Q[n]	QN[n]
0	1	x	0	↑	0	1
1	1	x	0	↑	1	0
x	x	x	x	↓	Q[n]	QN[n]

Cell Size

Drive Strength	Height (µm)	Width (µm)
SEDFFXL	5.04	15.68
SEDFFX1	5.04	15.68
SEDFFX2	5.04	17.92
SEDFFX4	5.04	20.72

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
SI	0.0489	0.0498	0.0608	0.0854
SE	0.0586	0.0596	0.0716	0.0944
D	0.0415	0.0438	0.0536	0.0712
CK	0.0688	0.0741	0.0895	0.1184
E	0.0599	0.0620	0.0719	0.0931
Q	0.0396	0.0419	0.0706	0.1152

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
SI	0.0021	0.0019	0.0022	0.0032
SE	0.0040	0.0040	0.0043	0.0052
D	0.0021	0.0019	0.0021	0.0032
CK	0.0022	0.0028	0.0036	0.0056
E	0.0051	0.0049	0.0052	0.0063

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.1887	0.1735	0.1535	0.1305	4.4726	3.9808	2.0218	1.0113
CK → Q↓	0.1495	0.1365	0.1214	0.1093	2.5885	2.4990	1.1644	0.5863
CK → QN↑	0.2164	0.1919	0.1703	0.1562	4.4772	3.9825	2.0201	1.0103
CK → QN↓	0.2695	0.2498	0.2185	0.1928	2.5766	2.2805	1.1553	0.5817

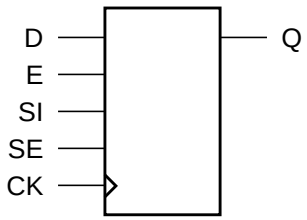
Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
SI	setup↑ → CK	0.1406	0.1367	0.1641	0.1328
	setup↓ → CK	0.2773	0.3828	0.2852	0.2305
	hold↑ → CK	-0.1250	-0.1172	-0.1523	-0.1250
	hold↓ → CK	-0.2656	-0.3906	-0.2734	-0.2148
SE	setup↑ → CK	0.3750	0.4922	0.3750	0.3164
	setup↓ → CK	0.3984	0.5039	0.4062	0.3164
	hold↑ → CK	-0.1016	-0.0977	-0.1211	-0.0977
	hold↓ → CK	-0.1992	-0.1875	-0.2148	-0.1836
D	setup↑ → CK	0.1445	0.1445	0.1719	0.1445
	setup↓ → CK	0.3672	0.4688	0.3750	0.2852
	hold↑ → CK	-0.1250	-0.1172	-0.1406	-0.1094
	hold↓ → CK	-0.2656	-0.3555	-0.2695	-0.1953
CK	minpwh	0.0979	0.0930	0.0833	0.0688
	minpwl	0.2145	0.1854	0.1999	0.1611
E	setup↑ → CK	0.3984	0.5000	0.4102	0.3281
	setup↓ → CK	0.2969	0.4141	0.3008	0.2305
	hold↑ → CK	-0.1328	-0.1328	-0.1562	-0.1250
	hold↓ → CK	-0.1836	-0.1797	-0.2031	-0.1797

Cell Description

The SEDFFHQ cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and synchronous active-high enable (E). The cell has a single output (Q) and fast clock-to-output path.

Logic Symbol



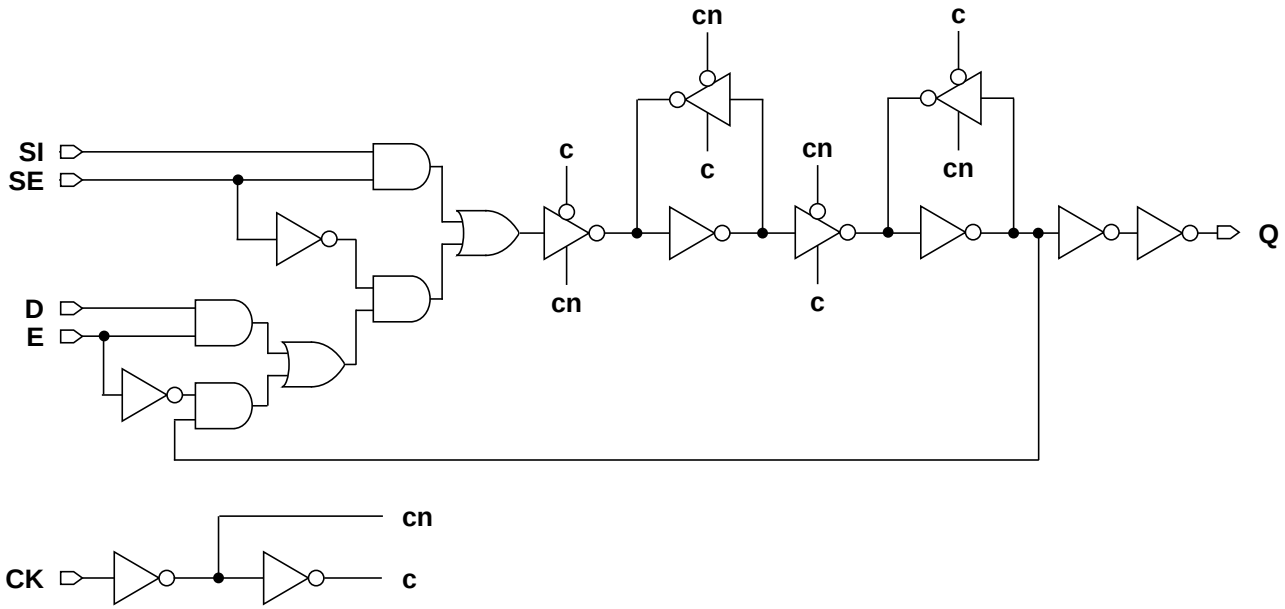
Functions

D	E	SI	SE	CK	Q[n+1]
x	x	1	1	↑	1
x	x	0	1	↑	0
x	0	x	0	↑	Q[n]
0	1	x	0	↑	0
1	1	x	0	↑	1
x	x	x	x	↓	Q[n]

Cell Size

Drive Strength	Height (µm)	Width (µm)
SEDFFHQXL	5.04	18.48
SEDFFHQX1	5.04	19.04
SEDFFHQX2	5.04	20.72
SEDFFHQX4	5.04	22.96

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
SI	0.0480	0.0562	0.0719	0.1040
SE	0.0675	0.0720	0.0895	0.1233
D	0.0674	0.0741	0.0917	0.1258
CK	0.0557	0.0672	0.0913	0.1349
E	0.0877	0.0863	0.1033	0.1351
Q	0.0331	0.0374	0.0534	0.0772

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
SI	0.0018	0.0017	0.0017	0.0017
SE	0.0018	0.0016	0.0017	0.0017
D	0.0024	0.0024	0.0025	0.0025
CK	0.0016	0.0027	0.0035	0.0050
E	0.0019	0.0018	0.0019	0.0019

Delays at 25^{o}C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.2658	0.1536	0.1482	0.1251	4.4819	3.9783	2.0195	1.0099
CK → Q↓	0.3046	0.1866	0.1769	0.1577	2.7470	2.2590	1.1505	0.6022

Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
SI	setup↑ → CK	0.2031	0.2109	0.2227	0.2578
	setup↓ → CK	0.1758	0.1914	0.1953	0.2188
	hold↑ → CK	-0.0820	-0.1094	-0.1172	-0.1523
	hold↓ → CK	-0.1523	-0.1641	-0.1680	-0.1875
SE	setup↑ → CK	0.2656	0.2695	0.2812	0.3164
	setup↓ → CK	0.2383	0.2344	0.2383	0.2617
	hold↑ → CK	-0.1367	-0.1680	-0.1797	-0.2148
	hold↓ → CK	-0.1367	-0.1484	-0.1602	-0.1914
D	setup↑ → CK	0.2852	0.2500	0.2695	0.3008
	setup↓ → CK	0.2852	0.2305	0.2383	0.2617
	hold↑ → CK	-0.1523	-0.1484	-0.1641	-0.1953
	hold↓ → CK	-0.2617	-0.2031	-0.2109	-0.2305
CK	minpwh	0.1271	0.0688	0.0688	0.0590
	minpwl	0.1756	0.1513	0.1513	0.1708
E	setup↑ → CK	0.3438	0.3164	0.3320	0.3633
	setup↓ → CK	0.2930	0.2500	0.2500	0.2617
	hold↑ → CK	-0.2070	-0.2188	-0.2305	-0.2656
	hold↓ → CK	-0.1094	-0.1289	-0.1562	-0.2266

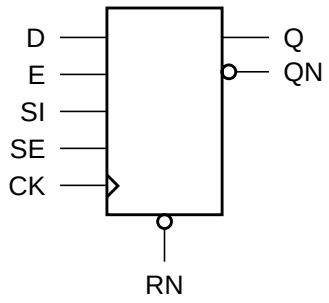
Cell Description

The SEDFFTR cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), synchronous active-high enable (E) and synchronous active low reset (RN). Scan enable (SE) dominates reset (RN) and enable (E).

Functions

RN	D	E	SI	SE	CK	Q[n+1]	QN[n+1]
x	x	x	0	1	↑	0	1
x	x	x	1	1	↑	1	0
1	x	0	x	0	↑	Q[n]	QN[n]
0	x	x	x	0	↑	0	1
1	1	1	x	0	↑	1	0
1	0	1	x	0	↑	0	1
x	x	x	x	x	↓	Q[n]	QN[n]

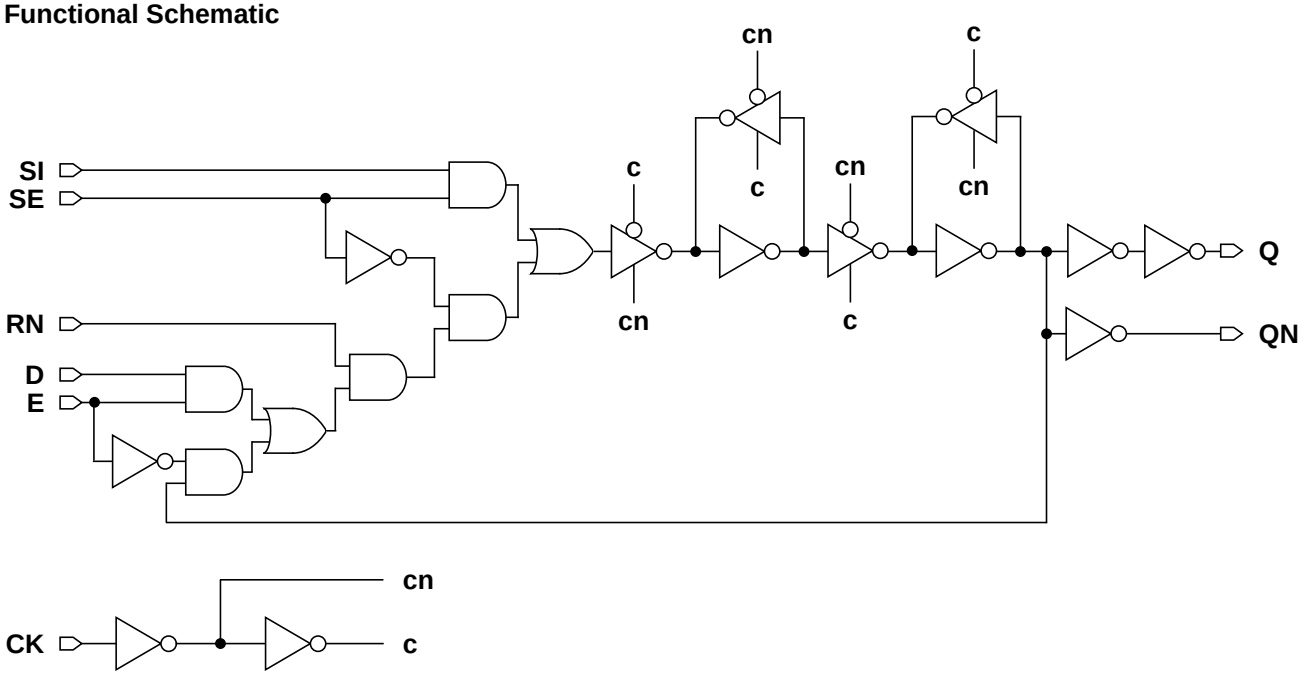
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
SEDFFTRXL	5.04	22.40
SEDFFTRX1	5.04	23.52
SEDFFTRX2	5.04	23.52
SEDFFTRX4	5.04	24.64

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
SI	0.0631	0.0765	0.0794	0.0794
SE	0.0884	0.1001	0.1043	0.1044
D	0.0853	0.1000	0.1037	0.1034
CK	0.0681	0.0906	0.1000	0.1000
E	0.1104	0.1166	0.1195	0.1202
RN	0.0577	0.0723	0.0747	0.0746
Q	0.0496	0.0617	0.0823	0.1261

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
SI	0.0022	0.0022	0.0022	0.0022
SE	0.0041	0.0041	0.0041	0.0041
D	0.0021	0.0033	0.0034	0.0033
CK	0.0021	0.0035	0.0043	0.0043
E	0.0023	0.0024	0.0025	0.0024
RN	0.0029	0.0029	0.0029	0.0029

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.2845	0.1706	0.1757	0.2102	4.4798	3.9789	2.0197	1.0104
CK → Q↓	0.2897	0.1894	0.1830	0.1970	2.6414	2.2581	1.1511	0.5767
CK → QN↑	0.1797	0.1379	0.1306	0.1388	4.4901	3.9811	2.0222	1.0128
CK → QN↓	0.1883	0.1319	0.1371	0.1583	2.7539	2.2952	1.1747	0.5956

Timing Constraints at 25°C, 1.8V, Typical Process

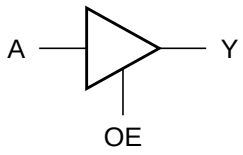
Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
SI	setup↑ → CK	0.2109	0.2578	0.2461	0.2266
	setup↓ → CK	0.1836	0.2031	0.1992	0.2031
	hold↑ → CK	-0.1172	-0.1484	-0.1641	-0.1641
	hold↓ → CK	-0.1680	-0.1758	-0.1797	-0.1797
SE	setup↑ → CK	0.2656	0.3164	0.3086	0.2891
	setup↓ → CK	0.2773	0.3008	0.2891	0.2695
	hold↑ → CK	-0.1680	-0.2109	-0.2148	-0.2148
	hold↓ → CK	-0.1445	-0.1797	-0.1953	-0.1953
D	setup↑ → CK	0.2852	0.2812	0.2734	0.2539
	setup↓ → CK	0.2773	0.2266	0.2266	0.2266
	hold↑ → CK	-0.1758	-0.1719	-0.1836	-0.1836
	hold↓ → CK	-0.2578	-0.2031	-0.2031	-0.2070
CK	minpwh	0.1562	0.0833	0.0930	0.1222
	minpwl	0.1805	0.1708	0.1708	0.1708
E	setup↑ → CK	0.3359	0.3477	0.3359	0.3164
	setup↓ → CK	0.2891	0.2500	0.2461	0.2422
	hold↑ → CK	-0.2344	-0.2461	-0.2500	-0.2500
	hold↓ → CK	-0.1016	-0.0977	-0.1094	-0.1328
RN	setup↑ → CK	0.2031	0.2344	0.2266	0.2070
	setup↓ → CK	0.1758	0.1953	0.1914	0.1914
	hold↑ → CK	-0.0898	-0.1250	-0.1367	-0.1367
	hold↓ → CK	-0.1602	-0.1680	-0.1719	-0.1719

Cell Description

The TBUF cell provides the logical buffer of a single input (A) with an active-high output enable (OE). When the enable is high, the output (Y) is represented by the logic equation:

$Y = A$

Logic Symbol



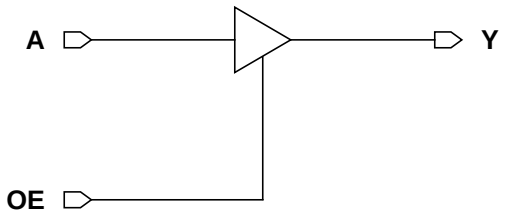
Functions

OE	A	Y
0	x	Z
1	0	0
1	1	1

Cell Size

Drive Strength	Height (µm)	Width (µm)
TBUFXL	5.04	4.48
TBUFX1	5.04	4.48
TBUFX2	5.04	4.48
TBUFX3	5.04	5.04
TBUFX4	5.04	5.60
TBUFX8	5.04	7.28
TBUFX12	5.04	8.96
TBUFX16	5.04	10.64
TBUFX20	5.04	14.00

Functional Schematic



AC Power

Pin	Power (μW/MHz)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A	0.0231	0.0243	0.0328	0.0393	0.0482	0.0914	0.1274	0.1618	0.2099
OE	0.0168	0.0172	0.0221	0.0258	0.0339	0.0655	0.0913	0.1181	0.1501

Pin Capacitance

Pin	Capacitance (pF)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A	0.0022	0.0022	0.0030	0.0038	0.0045	0.0101	0.0133	0.0161	0.0215
OE	0.0040	0.0042	0.0044	0.0041	0.0045	0.0058	0.0081	0.0104	0.0128
Y	0.0021	0.0025	0.0043	0.0045	0.0062	0.0121	0.0161	0.0212	0.0267

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A → Y↑	0.0814	0.0853	0.0913	0.0883	0.0798	0.0773	0.0696	0.0706	0.0709
A → Y↓	0.1220	0.1264	0.1298	0.1199	0.1141	0.1036	0.0968	0.0975	0.0980
OE → Y↑	0.0548	0.0596	0.0664	0.0706	0.0654	0.0634	0.0572	0.0574	0.0585
OE → Y↓	0.0941	0.0954	0.0961	0.0944	0.0940	0.0864	0.0841	0.0819	0.0840

Description	K_{load} (ns/pF)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A → Y↑	4.4822	3.9876	2.0250	1.2977	1.0129	0.5062	0.3276	0.2520	0.2049
A → Y↓	3.7373	2.3184	1.1848	0.7458	0.5920	0.2936	0.1984	0.1495	0.1132
OE → Y↑	4.4757	3.9845	2.0244	1.2974	1.0126	0.5062	0.3275	0.2520	0.2049
OE → Y↓	3.7339	2.3141	1.1819	0.7437	0.5909	0.2932	0.1982	0.1493	0.1130

Cell Description

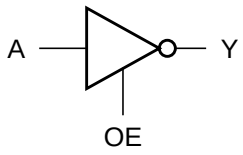
The TBUFI cell provides the logical inversion of a single input (A) with an active-high output enable (OE). When the enable is high, the output (Y) is represented by the logic equation:

$$Y = \overline{A}$$

Functions

OE	A	Y
0	x	Z
1	0	1
1	1	0

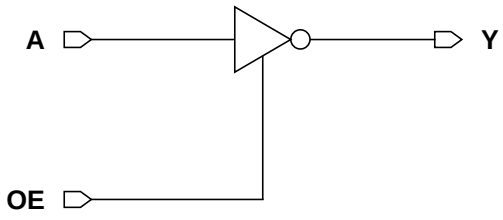
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
TBUFIXL	5.04	2.80
TBUFIX1	5.04	2.80
TBUFIX2	5.04	3.92
TBUFIX3	5.04	6.16
TBUFIX4	5.04	6.16
TBUFIX8	5.04	7.84
TBUFIX12	5.04	10.64
TBUFIX16	5.04	11.76
TBUFIX20	5.04	15.12

Functional Schematic



AC Power

Pin	Power (μW/MHz)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A	0.0204	0.0204	0.0371	0.0447	0.0526	0.0980	0.1450	0.1877	0.2392
OE	0.0138	0.0138	0.0230	0.0271	0.0343	0.0637	0.0962	0.1318	0.1622

Pin Capacitance

Pin	Capacitance (pF)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A	0.0038	0.0038	0.0076	0.0022	0.0022	0.0039	0.0055	0.0069	0.0087
OE	0.0030	0.0030	0.0039	0.0041	0.0041	0.0062	0.0082	0.0102	0.0127
Y	0.0033	0.0033	0.0045	0.0045	0.0055	0.0108	0.0162	0.0215	0.0269

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A → Y↑	0.0527	0.0530	0.0493	0.1443	0.1563	0.1278	0.1235	0.1181	0.1191
A → Y↓	0.0279	0.0282	0.0249	0.1520	0.1477	0.1312	0.1273	0.1251	0.1249
OE → Y↑	0.0573	0.0577	0.0596	0.0707	0.0752	0.0609	0.0586	0.0582	0.0588
OE → Y↓	0.0194	0.0197	0.0167	0.0962	0.0930	0.0881	0.0863	0.0830	0.0840

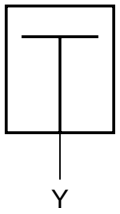
Description	K_{load} (ns/pF)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A → Y↑	5.6081	5.6027	2.8925	1.2895	1.0153	0.5072	0.3275	0.2455	0.1963
A → Y↓	2.7393	2.7315	1.3663	0.7414	0.5917	0.2860	0.1952	0.1459	0.1159
OE → Y↑	5.6168	5.6066	2.8948	1.2886	1.0145	0.5069	0.3273	0.2454	0.1962
OE → Y↓	2.7410	2.7323	1.3664	0.7391	0.5902	0.2856	0.1950	0.1457	0.1157

Cell Description

The TIEHI cell drives the output (Y) to a logic high. The output is driven through diffusion and not tied directly to the power rail to provide some ESD protection. The output (Y) is represented by the logic equation:

$$Y = 1$$

Logic Symbol



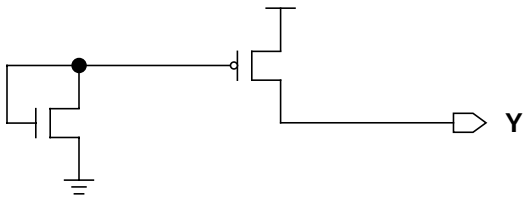
Function

Y
1

Cell Size

Drive Strength	Height (µm)	Width (µm)
TIEHI	5.04	1.68

Functional Schematic

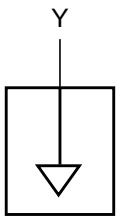


Cell Description

The TIELO cell drives the output (Y) to a logic low. The output is driven through diffusion and not tied directly to the power rail to provide some ESD protection. The output (Y) is represented by the logic equation:

$$Y = 0$$

Logic Symbol



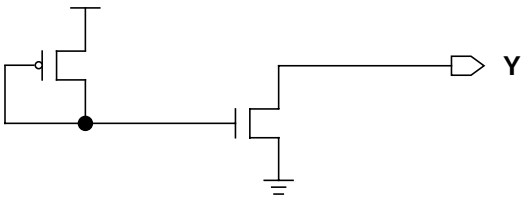
Function

Y
0

Cell Size

Drive Strength	Height (µm)	Width (µm)
TIELO	5.04	1.68

Functional Schematic



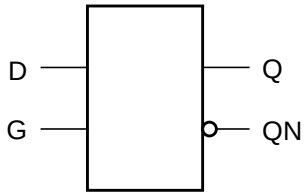
Cell Description

The TLAT cell is an active-high D-type transparent latch. When the enable (G) is high, data is transferred to the outputs (Q, QN).

Functions

G	D	Q[n+1]	QN[n+1]
1	0	0	1
1	1	1	0
0	x	Q[n]	QN[n]

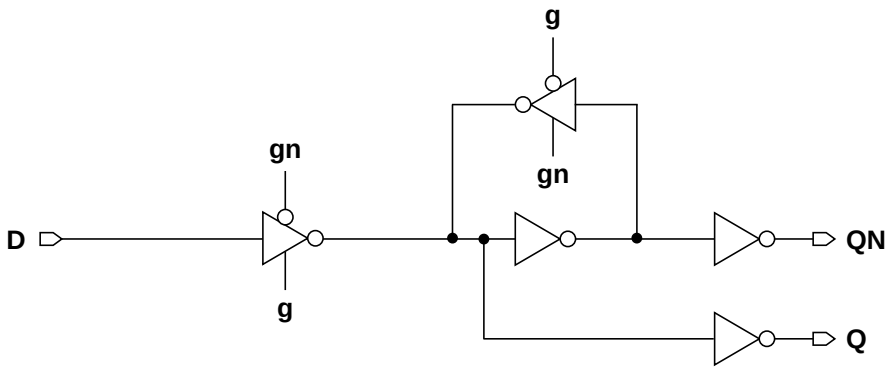
Logic Symbol

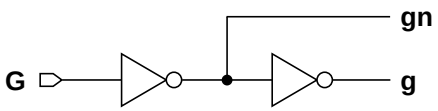


Cell Size

Drive Strength	Height (µm)	Width (µm)
TLATXL	5.04	6.16
TLATX1	5.04	6.16
TLATX2	5.04	7.28
TLATX4	5.04	10.08

Functional Schematic





AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
D	0.0028	0.0050	0.0074	0.0161
G	0.0219	0.0233	0.0279	0.0413
Q	0.0381	0.0388	0.0599	0.1030

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0022	0.0037	0.0051	0.0116
G	0.0022	0.0026	0.0025	0.0036

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
D → Q↑	0.0988	0.0724	0.0707	0.0621	4.3918	3.9822	2.0226	1.0396
D → Q↓	0.1718	0.1209	0.1157	0.1051	2.7450	2.2885	1.2377	0.5583
G → Q↑	0.1812	0.1529	0.1552	0.1358	4.3905	3.9817	2.0224	1.0395
G → Q↓	0.1805	0.1253	0.1281	0.1169	2.7432	2.2879	1.2377	0.5582
D → QN↑	0.2180	0.1633	0.1688	0.1618	4.3664	3.9807	2.0198	1.0386
D → QN↓	0.1544	0.1298	0.1465	0.1296	2.5198	2.2649	1.2292	0.5621
G → QN↑	0.2277	0.1686	0.1820	0.1740	4.3663	3.9808	2.0198	1.0387
G → QN↓	0.2376	0.2110	0.2316	0.2037	2.5197	2.2648	1.2292	0.5621

Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → G	0.0117	-0.0078	-0.0156	-0.0156
	setup↓ → G	0.1250	0.0781	0.0742	0.0625
	hold↑ → G	0.0000	0.0234	0.0273	0.0312
	hold↓ → G	-0.1211	-0.0703	-0.0625	-0.0547
G	minpwh	0.0979	0.0833	0.0833	0.0688

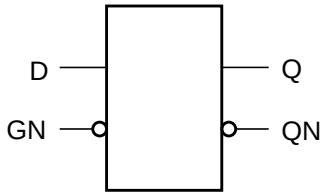
Cell Description

The TLATN cell is an active-low D-type transparent latch. When the enable (GN) is low, data is transferred to the outputs (Q, QN).

Functions

GN	D	Q[n+1]	QN[n+1]
0	0	0	1
0	1	1	0
1	x	Q[n]	QN[n]

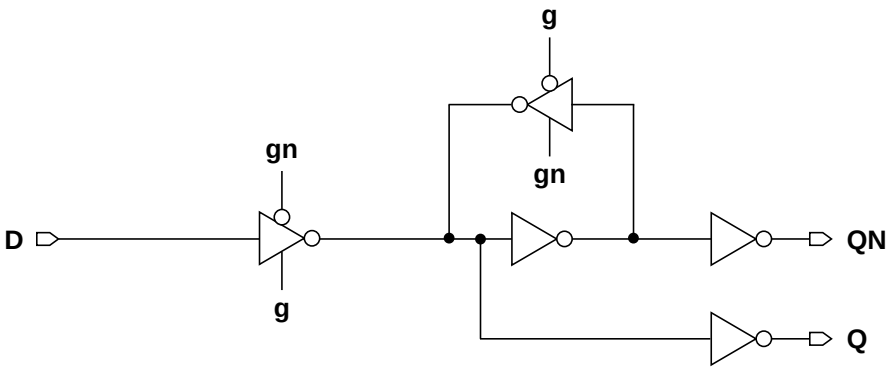
Logic Symbol

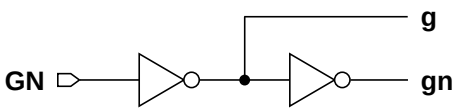


Cell Size

Drive Strength	Height (µm)	Width (µm)
TLATNXL	5.04	6.72
TLATNX1	5.04	6.72
TLATNX2	5.04	7.28
TLATNX4	5.04	10.08

Functional Schematic





AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
D	0.0031	0.0054	0.0075	0.0165
GN	0.0223	0.0278	0.0352	0.0526
Q	0.0396	0.0406	0.0650	0.1063

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0022	0.0037	0.0052	0.0118
GN	0.0022	0.0026	0.0025	0.0037

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
D → Q↑	0.0942	0.0732	0.0713	0.0625	4.3870	3.9825	2.0230	1.0397
D → Q↓	0.1639	0.1212	0.1170	0.1039	2.7164	2.2859	1.1676	0.5579
GN → Q↑	0.1516	0.1202	0.1250	0.1011	4.3868	3.9836	2.0237	1.0400
GN → Q↓	0.2438	0.1974	0.2003	0.1757	2.7165	2.2858	1.1676	0.5578
D → QN↑	0.2126	0.1630	0.1744	0.1614	4.3652	3.9815	2.0199	1.0387
D → QN↓	0.1522	0.1292	0.1498	0.1312	2.5240	2.2650	1.1584	0.5623
GN → QN↑	0.2934	0.2398	0.2580	0.2333	4.3649	3.9814	2.0199	1.0387
GN → QN↓	0.2106	0.1774	0.2052	0.1705	2.5237	2.2651	1.1585	0.5623

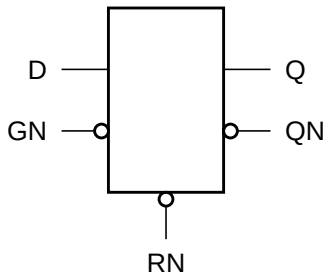
Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → GN	0.0625	0.0469	0.0469	0.0430
	setup↓ → GN	0.0938	0.0508	0.0391	0.0273
	hold↑ → GN	-0.0547	-0.0352	-0.0352	-0.0312
	hold↓ → GN	-0.0781	-0.0273	-0.0234	-0.0156
GN	minpwl	0.1222	0.1028	0.1076	0.0882

Cell Description

The TLATNR cell is an active-low D-type transparent latch with asynchronous active-low reset (RN). When the enable (GN) is low, data is transferred to the outputs (Q, QN).

Logic Symbol



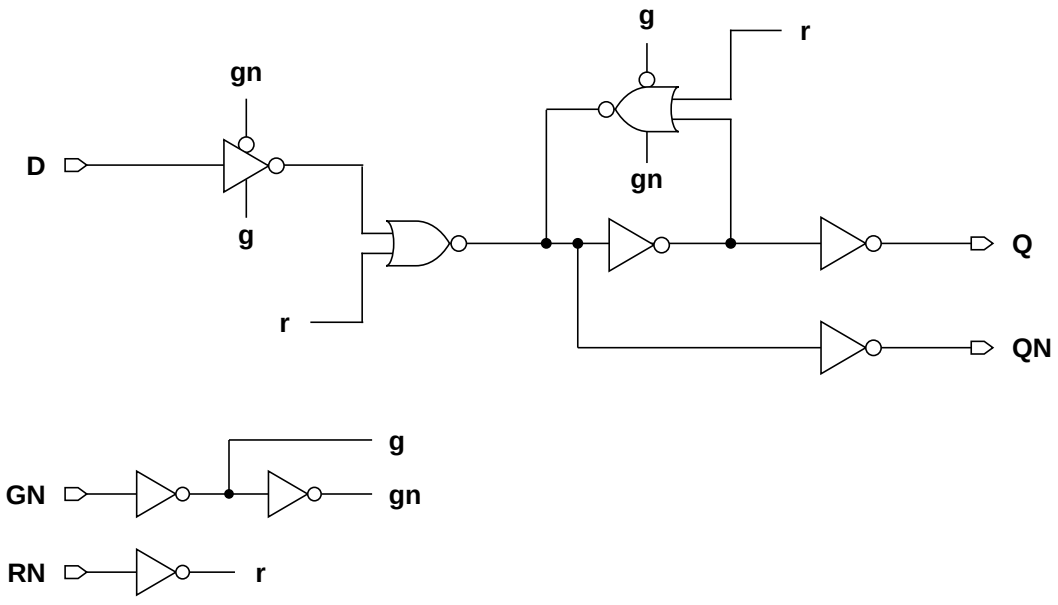
Functions

RN	GN	D	Q[n+1]	QN[n+1]
1	0	0	0	1
1	0	1	1	0
1	1	x	Q[n]	QN[n]
0	x	x	0	1

Cell Size

Drive Strength	Height (µm)	Width (µm)
TLATNRXL	5.04	7.84
TLATNRX1	5.04	7.84
TLATNRX2	5.04	8.40
TLATNRX4	5.04	11.20

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
D	0.0039	0.0039	0.0055	0.0115
GN	0.0274	0.0277	0.0359	0.0570
RN	0.0049	0.0050	0.0056	0.0065
Q	0.0431	0.0439	0.0755	0.1192

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0028	0.0028	0.0043	0.0086
GN	0.0021	0.0021	0.0023	0.0032
RN	0.0043	0.0044	0.0052	0.0066

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
D → Q↑	0.1123	0.1085	0.0989	0.0899	4.3994	3.9933	2.0278	0.9873
D → Q↓	0.1622	0.1737	0.1707	0.1487	2.4851	2.3349	1.1888	0.5665
GN → Q↑	0.1676	0.1642	0.1510	0.1329	4.3991	3.9931	2.0280	0.9877
GN → Q↓	0.2486	0.2597	0.2520	0.2284	2.4846	2.3347	1.1887	0.5664
RN → Q↑	0.1107	0.1069	0.0948	0.0839	4.3993	3.9931	2.0277	0.9873
RN → Q↓	0.1181	0.1259	0.1792	0.2740	2.4215	2.3100	1.2141	0.6269
D → QN↑	0.2145	0.2169	0.2273	0.2046	4.3660	3.9807	2.0196	0.9834
D → QN↓	0.1700	0.1690	0.1757	0.1648	2.3198	2.2688	1.1583	0.5628
GN → QN↑	0.3019	0.3039	0.3093	0.2847	4.3656	3.9806	2.0196	0.9834
GN → QN↓	0.2266	0.2260	0.2289	0.2089	2.3216	2.2696	1.1584	0.5629
RN → QN↑	0.1700	0.1704	0.2360	0.3379	4.3654	3.9803	2.0194	0.9830
RN → QN↓	0.1688	0.1677	0.1719	0.1591	2.3204	2.2689	1.1583	0.5629

Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → GN	0.0781	0.0820	0.0703	0.0664
	setup↓ → GN	0.0898	0.0977	0.0898	0.0586
	hold↑ → GN	-0.0703	-0.0625	-0.0586	-0.0508
	hold↓ → GN	-0.0742	-0.0742	-0.0742	-0.0469
GN	minpwl	0.1368	0.1416	0.1271	0.1125
RN	minpwl	0.1173	0.1222	0.1562	0.2242
	recovery	0.0742	0.0703	0.0625	0.0508

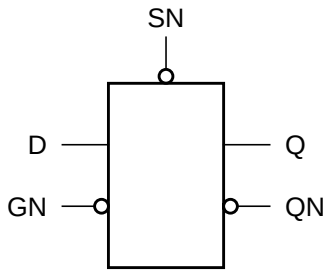
Cell Description

The TLATNS cell is an active-low D-type transparent latch with asynchronous active-low set (SN). When the enable (GN) is low, data is transferred to the outputs (Q, QN).

Functions

SN	GN	D	Q[n+1]	QN[n+1]
1	0	0	0	1
1	0	1	1	0
1	1	x	Q[n]	QN[n]
0	x	x	1	0

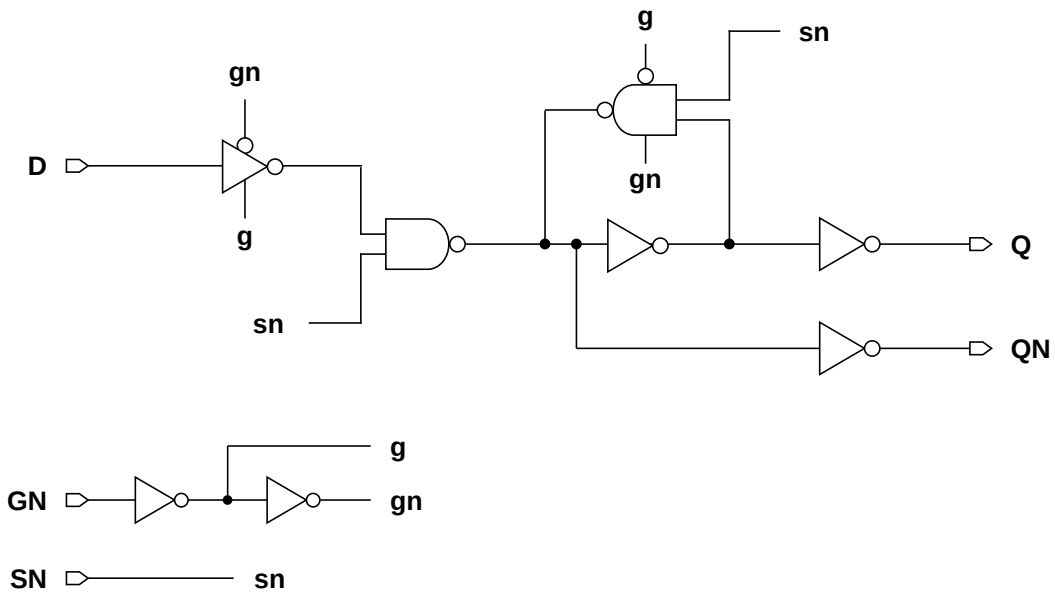
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
TLATNSXL	5.04	9.52
TLATNSX1	5.04	9.52
TLATNSX2	5.04	10.08
TLATNSX4	5.04	12.88

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
D	0.0041	0.0041	0.0069	0.0120
GN	0.0281	0.0294	0.0340	0.0478
SN	0.0155	0.0155	0.0171	0.0236
Q	0.0523	0.0553	0.0816	0.1257

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0029	0.0029	0.0046	0.0083
GN	0.0021	0.0027	0.0028	0.0036
SN	0.0020	0.0020	0.0025	0.0035

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
D → Q↑	0.1148	0.1155	0.1051	0.0968	4.4035	3.9977	2.0283	0.9876
D → Q↓	0.2081	0.2230	0.1905	0.1779	2.8485	2.6140	1.2045	0.5801
GN → Q↑	0.1782	0.1613	0.1479	0.1351	4.4031	3.9982	2.0298	0.9885
GN → Q↓	0.2831	0.2853	0.2555	0.2342	2.8489	2.6144	1.2047	0.5802
SN → Q↑	0.1748	0.1757	0.1996	0.2561	4.3762	3.9859	2.0280	0.9922
SN → Q↓	0.2398	0.2553	0.2134	0.1969	2.8490	2.6142	1.2046	0.5801
D → QN↑	0.2739	0.2783	0.2484	0.2330	4.3649	3.9807	2.0200	0.9834
D → QN↓	0.1905	0.1956	0.1832	0.1703	2.5474	2.2781	1.1583	0.5588
GN → QN↑	0.3503	0.3419	0.3143	0.2898	4.3652	3.9808	2.0201	0.9834
GN → QN↓	0.2554	0.2430	0.2277	0.2100	2.5476	2.2781	1.1584	0.5588
SN → QN↑	0.3062	0.3111	0.2716	0.2521	4.3650	3.9807	2.0200	0.9834
SN → QN↓	0.2494	0.2553	0.2798	0.3359	2.5437	2.2766	1.1585	0.5596

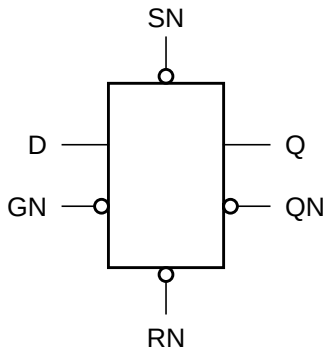
Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → GN	0.0898	0.0977	0.0859	0.0781
	setup↓ → GN	0.1367	0.1523	0.1094	0.0938
	hold↑ → GN	-0.0859	-0.0898	-0.0781	-0.0664
	hold↓ → GN	-0.1016	-0.1094	-0.0781	-0.0703
GN	minpwl	0.1611	0.1465	0.1319	0.1222
SN	minpwl	0.1416	0.1465	0.1562	0.1902
	recovery	0.1641	0.1758	0.1250	0.1055

Cell Description

The TLATNSR cell is an active-low D-type transparent latch with asynchronous active-low set (SN) and reset (RN), and set dominating reset. When the enable (GN) is low, data is transferred to the outputs (Q, QN).

Logic Symbol



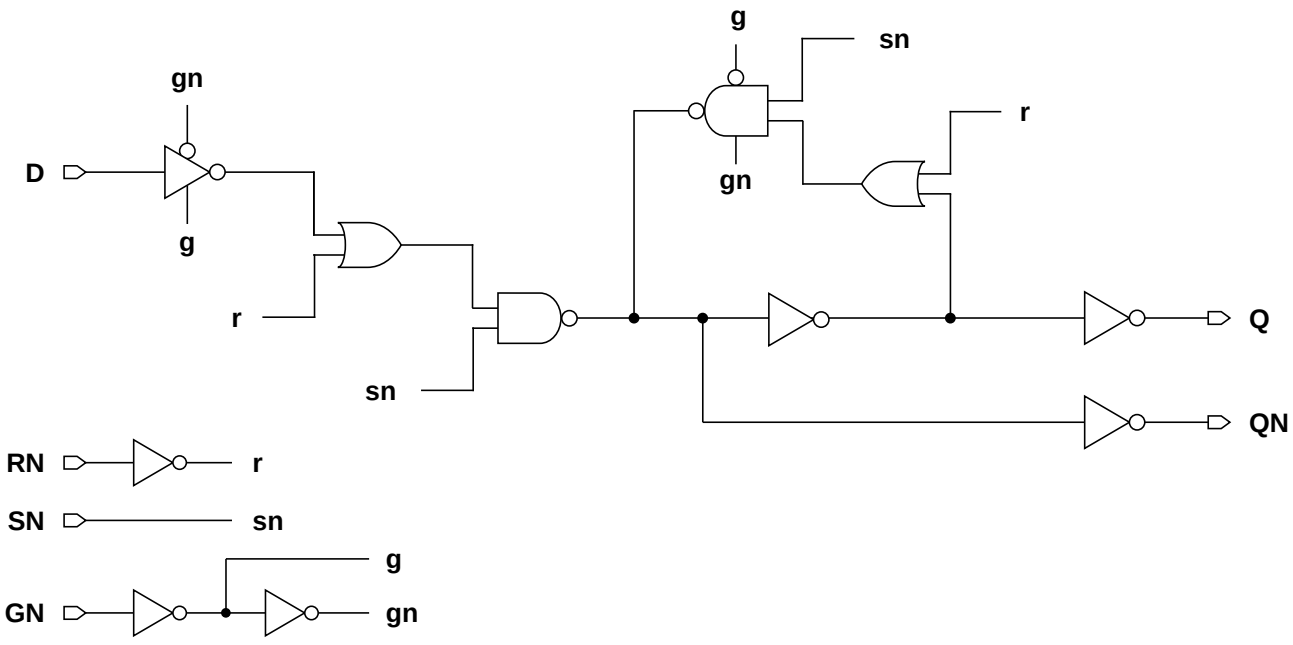
Functions

RN	SN	GN	D	Q[n+1]	QN[n+1]
1	1	0	0	0	1
1	1	0	1	1	0
1	1	1	x	Q[n]	QN[n]
0	1	x	x	0	1
1	0	x	x	1	0
0	0	x	x	1	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
TLATNSRXL	5.04	10.08
TLATNSRX1	5.04	10.08
TLATNSRX2	5.04	11.20
TLATNSRX4	5.04	15.12

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
D	0.0040	0.0040	0.0063	0.0119
GN	0.0286	0.0296	0.0340	0.0606
SN	0.0173	0.0187	0.0239	0.0416
RN	0.0050	0.0055	0.0071	0.0133
Q	0.0556	0.0593	0.0908	0.1595

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0031	0.0031	0.0043	0.0093
GN	0.0021	0.0027	0.0027	0.0037
SN	0.0020	0.0024	0.0036	0.0056
RN	0.0042	0.0044	0.0051	0.0093

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
D → Q↑	0.1416	0.1447	0.1620	0.1367	4.4280	4.0086	2.0375	0.9912
D → Q↓	0.2359	0.2556	0.2370	0.2330	2.9538	2.6695	1.3668	0.6037
GN → Q↑	0.1947	0.1820	0.1937	0.1686	4.4266	4.0084	2.0374	0.9913
GN → Q↓	0.3006	0.3079	0.2934	0.2894	2.9537	2.6696	1.3669	0.6038
SN → Q↑	0.1940	0.1756	0.1483	0.1513	4.3876	3.9899	2.0237	0.9861
SN → Q↓	0.2615	0.2736	0.2514	0.2503	2.9436	2.6649	1.3649	0.6024
RN → Q↑	0.1371	0.1409	0.1573	0.1331	4.4281	4.0086	2.0375	0.9912
RN → Q↓	0.1970	0.1896	0.1907	0.1650	3.0218	2.6427	1.3716	0.5957
D → QN↑	0.3042	0.3090	0.2875	0.2909	4.3638	3.9797	2.0199	0.9834
D → QN↓	0.2185	0.2238	0.2423	0.2142	2.6255	2.2771	1.2906	0.5595
GN → QN↑	0.3702	0.3627	0.3449	0.3481	4.3639	3.9797	2.0200	0.9834
GN → QN↓	0.2730	0.2625	0.2751	0.2468	2.6269	2.2778	1.2907	0.5596
SN → QN↑	0.3296	0.3271	0.3019	0.3078	4.3643	3.9799	2.0201	0.9835
SN → QN↓	0.2697	0.2540	0.2261	0.2272	2.6210	2.2752	1.2894	0.5590
RN → QN↑	0.2645	0.2409	0.2383	0.2187	4.3628	3.9792	2.0204	0.9837
RN → QN↓	0.2144	0.2204	0.2381	0.2108	2.6261	2.2773	1.2906	0.5595

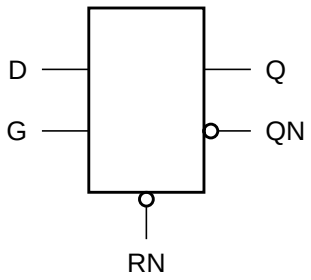
Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → GN	0.1133	0.1250	0.1406	0.1133
	setup↓ → GN	0.1758	0.1875	0.1562	0.1406
	hold↑ → GN	-0.1055	-0.1133	-0.1289	-0.1016
	hold↓ → GN	-0.1367	-0.1484	-0.1211	-0.1172
GN	minpwl	0.1708	0.1611	0.1756	0.1465
SN	minpwl	0.1611	0.1513	0.1222	0.1173
	recovery	0.1953	0.1992	0.1602	0.1523
	removal	-0.1953	-0.1992	-0.1602	-0.1523
RN	minpwl	0.1999	0.1756	0.1659	0.1271
	recovery	0.1094	0.1172	0.1328	0.1055
	removal	-0.1055	-0.1133	-0.1289	-0.1016

Cell Description

The TLATR cell is an active-high D-type transparent latch with asynchronous active-low reset (RN). When the enable (G) is high, data is transferred to the outputs (Q, QN).

Logic Symbol



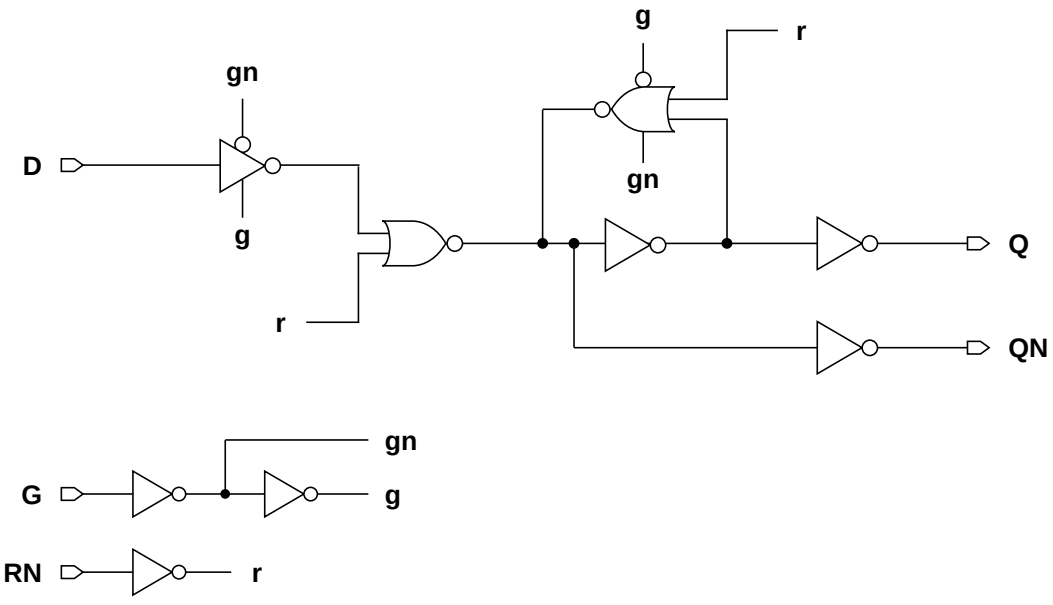
Functions

RN	G	D	Q[n+1]	QN[n+1]
1	1	0	0	1
1	1	1	1	0
1	0	x	Q[n]	QN[n]
0	x	x	0	1

Cell Size

Drive Strength	Height (µm)	Width (µm)
TLATRXL	5.04	7.28
TLATRX1	5.04	7.28
TLATRX2	5.04	8.40
TLATRX4	5.04	10.64

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
D	0.0035	0.0037	0.0056	0.0115
G	0.0284	0.0286	0.0319	0.0511
RN	0.0045	0.0045	0.0056	0.0067
Q	0.0401	0.0419	0.0716	0.1149

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0026	0.0028	0.0044	0.0086
G	0.0021	0.0021	0.0024	0.0033
RN	0.0041	0.0042	0.0052	0.0066

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
D → Q↑	0.1148	0.1131	0.1000	0.0910	4.5052	3.9938	2.0279	1.0140
D → Q↓	0.1788	0.1797	0.1633	0.1481	2.7322	2.3433	1.1854	0.5902
G → Q↑	0.2051	0.2035	0.1881	0.1860	4.5036	3.9933	2.0275	1.0138
G → Q↓	0.1845	0.1864	0.1750	0.1544	2.7299	2.3425	1.1854	0.5915
RN → Q↑	0.1109	0.1090	0.0960	0.0849	4.5051	3.9938	2.0278	1.0140
RN → Q↓	0.1209	0.1283	0.1805	0.2746	2.6296	2.3151	1.2160	0.6494
D → QN↑	0.2287	0.2237	0.2196	0.2029	4.4726	3.9810	2.0197	1.0102
D → QN↓	0.1741	0.1756	0.1766	0.1651	2.5348	2.2716	1.1583	0.5792
G → QN↑	0.2362	0.2323	0.2326	0.2111	4.4724	3.9809	2.0196	1.0102
G → QN↓	0.2654	0.2673	0.2657	0.2607	2.5364	2.2723	1.1584	0.5793
RN → QN↑	0.1710	0.1740	0.2372	0.3357	4.4713	3.9803	2.0194	1.0098
RN → QN↓	0.1706	0.1719	0.1730	0.1591	2.5350	2.2717	1.1583	0.5792

Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → G	0.0273	0.0352	0.0078	0.0000
	setup↓ → G	0.1406	0.1328	0.1172	0.1016
	hold↑ → G	-0.0039	0.0000	0.0117	0.0195
	hold↓ → G	-0.1367	-0.1289	-0.1133	-0.0977
G	minpwh	0.1222	0.1271	0.1076	0.1028
RN	minpwl	0.1222	0.1271	0.1562	0.2242
	recovery	0.0117	0.0117	-0.0078	-0.0195

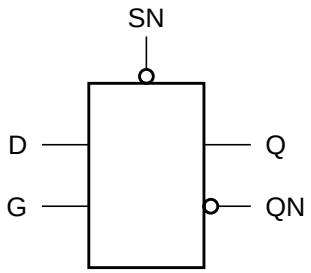
Cell Description

The TLATS cell is an active-high D-type transparent latch with asynchronous active-low set (SN). When the enable (G) is high, data is transferred to the outputs (Q, QN).

Functions

SN	G	D	Q[n+1]	QN[n+1]
1	1	0	0	1
1	1	1	1	0
1	0	x	Q[n]	QN[n]
0	x	x	1	0

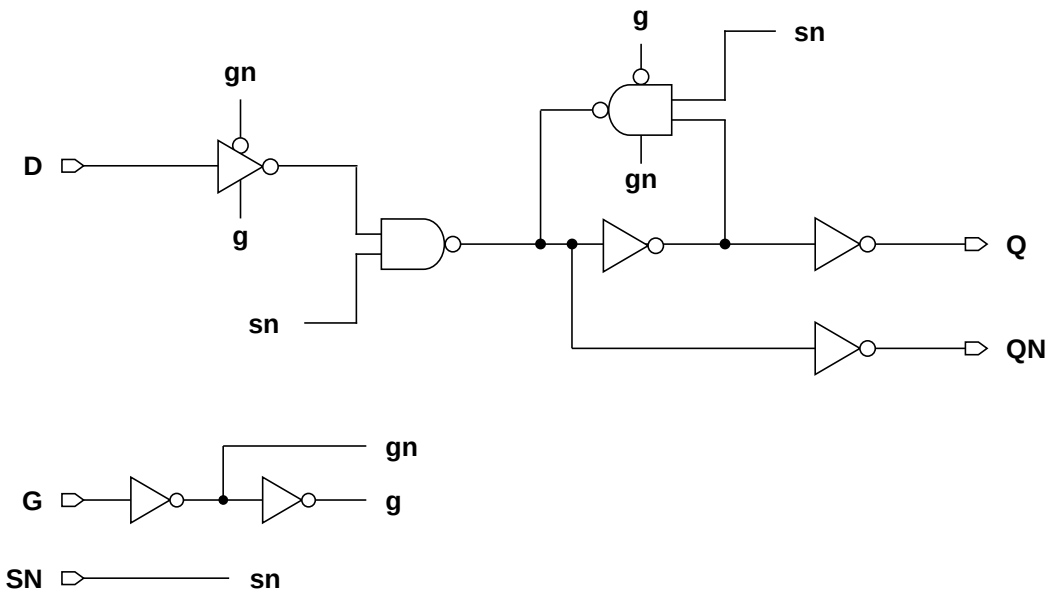
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
TLATSXL	5.04	8.40
TLATSX1	5.04	8.40
TLATSX2	5.04	10.08
TLATSX4	5.04	12.88

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
D	0.0042	0.0044	0.0072	0.0125
G	0.0298	0.0315	0.0325	0.0405
SN	0.0176	0.0176	0.0169	0.0230
Q	0.0473	0.0503	0.0755	0.1165

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0035	0.0036	0.0047	0.0090
G	0.0022	0.0028	0.0028	0.0036
SN	0.0027	0.0027	0.0025	0.0035

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
D → Q↑	0.1119	0.1126	0.1039	0.0880	4.5064	3.9962	2.0279	1.0138
D → Q↓	0.2059	0.2111	0.1894	0.1797	2.8345	2.3924	1.2037	0.6003
G → Q↑	0.2084	0.2002	0.1936	0.1733	4.5047	3.9956	2.0275	1.0136
G → Q↓	0.1973	0.1954	0.1795	0.1667	2.8331	2.3921	1.2031	0.5999
SN → Q↑	0.1712	0.1746	0.2002	0.2583	4.4779	3.9847	2.0281	1.0196
SN → Q↓	0.2353	0.2410	0.2122	0.1978	2.8349	2.3926	1.2038	0.6003
D → QN↑	0.2727	0.2712	0.2478	0.2337	4.4709	3.9809	2.0201	1.0103
D → QN↓	0.1871	0.1935	0.1826	0.1604	2.5500	2.2788	1.1589	0.5789
G → QN↑	0.2653	0.2568	0.2386	0.2210	4.4713	3.9811	2.0202	1.0103
G → QN↓	0.2847	0.2822	0.2732	0.2462	2.5499	2.2789	1.1589	0.5789
SN → QN↑	0.3026	0.3015	0.2709	0.2520	4.4708	3.9809	2.0201	1.0103
SN → QN↓	0.2464	0.2549	0.2812	0.3373	2.5457	2.2774	1.1591	0.5799

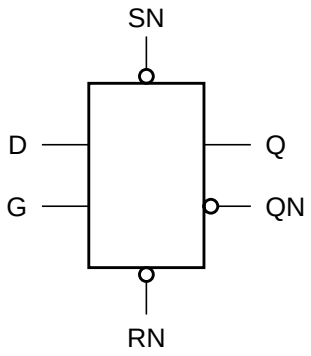
Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → G	0.0078	0.0312	0.0078	-0.0078
	setup↓ → G	0.1641	0.1680	0.1367	0.1250
	hold↑ → G	0.0000	-0.0117	0.0039	0.0195
	hold↓ → G	-0.1562	-0.1562	-0.1289	-0.1172
G	minpwh	0.1125	0.1222	0.1076	0.0930
SN	minpwl	0.1416	0.1465	0.1611	0.1902
	recovery	0.1914	0.1953	0.1602	0.1445

Cell Description

The TLATSR cell is an active-high D-type transparent latch with asynchronous active-low set (SN) and reset (RN), and set dominating reset. When the enable (G) is high, data is transferred to the outputs (Q, QN).

Logic Symbol



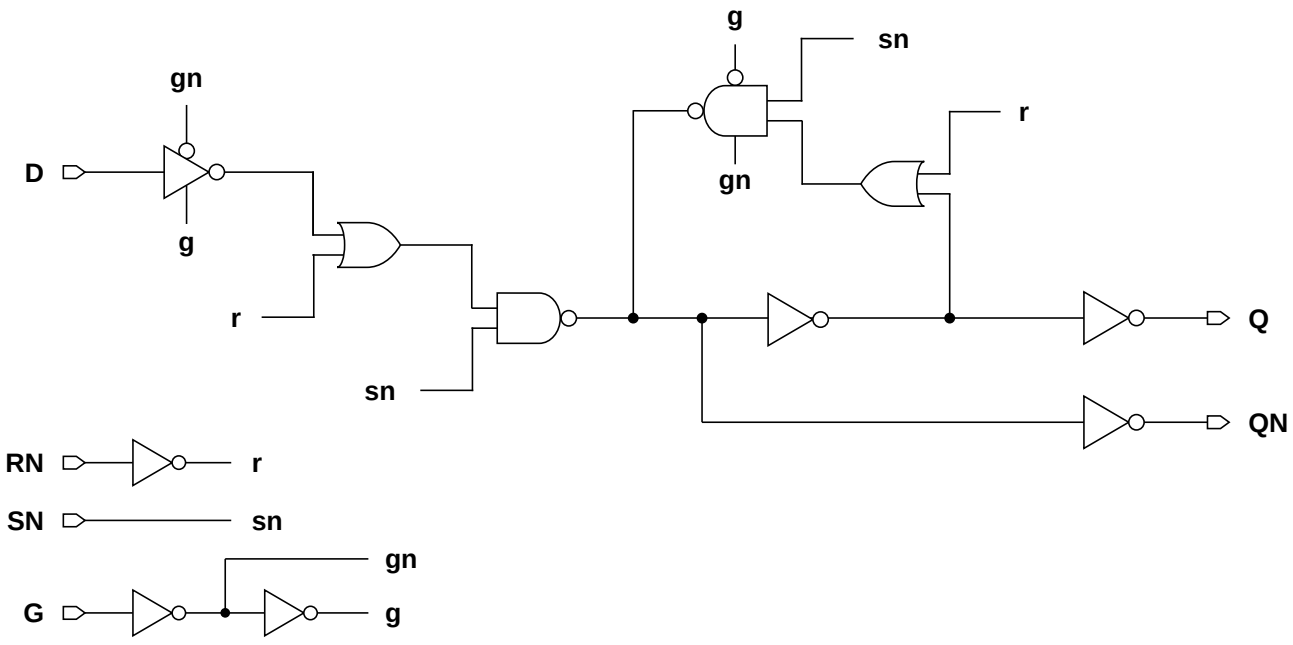
Functions

RN	SN	G	D	Q[n+1]	QN[n+1]
1	1	1	0	0	1
1	1	1	1	1	0
1	1	0	x	Q[n]	QN[n]
0	1	x	x	0	1
1	0	x	x	1	0
0	0	x	x	1	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
TLATSRXL	5.04	10.08
TLATSRX1	5.04	10.08
TLATSRX2	5.04	10.64
TLATSRX4	5.04	14.56

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
D	0.0039	0.0041	0.0059	0.0124
G	0.0312	0.0318	0.0336	0.0490
SN	0.0174	0.0190	0.0247	0.0405
RN	0.0045	0.0048	0.0075	0.0124
Q	0.0549	0.0578	0.0901	0.1445

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0031	0.0032	0.0043	0.0095
G	0.0021	0.0026	0.0027	0.0039
SN	0.0020	0.0025	0.0040	0.0055
RN	0.0040	0.0041	0.0054	0.0090

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
D → Q↑	0.1501	0.1493	0.1500	0.1357	4.5409	4.0081	2.0352	1.0234
D → Q↓	0.2489	0.2581	0.2492	0.2225	3.0060	2.4702	1.2528	0.6228
G → Q↑	0.2343	0.2244	0.2286	0.2038	4.5398	4.0076	2.0350	1.0233
G → Q↓	0.2516	0.2518	0.2440	0.2141	3.0067	2.4706	1.2528	0.6228
SN → Q↑	0.1966	0.1810	0.1494	0.1430	4.4935	3.9890	2.0242	1.0185
SN → Q↓	0.2753	0.2784	0.2612	0.2399	2.9955	2.4658	1.2502	0.6216
RN → Q↑	0.1454	0.1446	0.1457	0.1315	4.5409	4.0081	2.0352	1.0234
RN → Q↓	0.1997	0.2065	0.1739	0.1782	3.0144	2.4716	1.2301	0.6266
D → QN↑	0.3192	0.3158	0.3056	0.2773	4.4688	3.9799	2.0195	1.0158
D → QN↓	0.2261	0.2279	0.2283	0.2115	2.5506	2.2790	1.1595	0.5838
G → QN↑	0.3238	0.3113	0.3016	0.2694	4.4688	3.9799	2.0196	1.0158
G → QN↓	0.3117	0.3044	0.3078	0.2802	2.5522	2.2796	1.1597	0.5839
SN → QN↑	0.3455	0.3363	0.3173	0.2943	4.4692	3.9801	2.0197	1.0158
SN → QN↓	0.2726	0.2595	0.2260	0.2174	2.5430	2.2762	1.1583	0.5833
RN → QN↑	0.2698	0.2624	0.2271	0.2294	4.4659	3.9787	2.0201	1.0160
RN → QN↓	0.2219	0.2237	0.2244	0.2074	2.5509	2.2792	1.1595	0.5839

Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → G	0.0508	0.0781	0.0625	0.0430
	setup↓ → G	0.2031	0.2070	0.1914	0.1641
	hold↑ → G	-0.0273	-0.0430	-0.0352	-0.0195
	hold↓ → G	-0.1953	-0.1953	-0.1797	-0.1523
G	minpwh	0.1416	0.1513	0.1465	0.1173
SN	minpwl	0.1659	0.1562	0.1222	0.1125
	recovery	0.2305	0.2266	0.2031	0.1797
	removal	-0.2266	-0.2227	-0.1992	-0.1758
RN	minpwl	0.2048	0.1951	0.1465	0.1368
	recovery	0.0430	0.0586	0.0469	0.0273
	removal	-0.0391	-0.0547	-0.0430	-0.0234

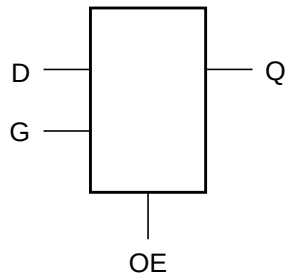
Cell Description

The TTLAT cell is an active-high D-type transparent latch with active-high output enable (OE). When the enable (G) is high and the output enable (OE) is high, data is transferred to the output (Q).

Functions

OE	G	D	Q[n+1]
0	x	x	Z
1	1	0	0
1	1	1	1
1	0	x	Q[n]

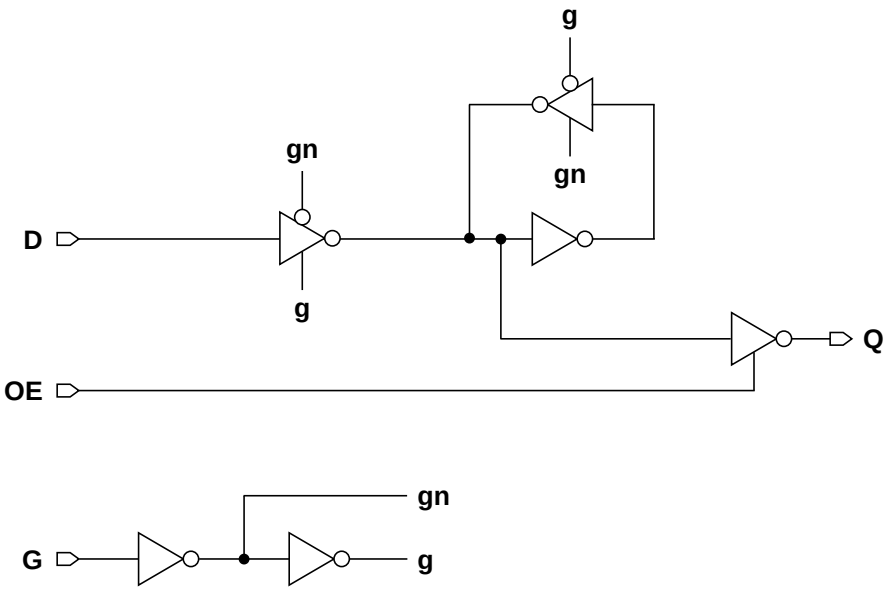
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
TTLATXL	5.04	7.84
TTLATX1	5.04	7.84
TTLATX2	5.04	11.76
TTLATX4	5.04	15.12

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
D	0.0047	0.0072	0.0133	0.0135
G	0.0246	0.0266	0.0389	0.0440
OE	0.0386	0.0600	0.1078	0.1703
Q	0.0373	0.0588	0.1038	0.1642

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0034	0.0050	0.0094	0.0094
G	0.0021	0.0027	0.0036	0.0039
OE	0.0027	0.0032	0.0047	0.0085
Q	0.0021	0.0044	0.0062	0.0112

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
D → Q↑	0.0974	0.0911	0.0922	0.1038	5.9051	2.3839	1.2240	0.6272
D → Q↓	0.1442	0.1320	0.1284	0.1526	4.0035	1.5279	0.7646	0.4062
G → Q↑	0.1777	0.1684	0.1788	0.1878	5.9063	2.3845	1.2243	0.6273
G → Q↓	0.1594	0.1423	0.1413	0.1664	4.0011	1.5271	0.7643	0.4059
OE → Q↑	0.0243	0.0215	0.0176	0.0173	5.8555	2.3501	1.2069	0.6178
OE → Q↓	0.0182	0.0154	0.0126	0.0123	3.9327	1.4897	0.7480	0.3923

Timing Constraints at 25°C, 1.8V, Typical Process

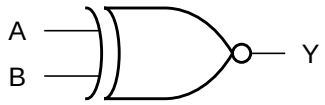
Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → G	-0.0117	-0.0117	-0.0234	-0.0117
	setup↓ → G	0.0820	0.0742	0.0664	0.0859
	hold↑ → G	0.0273	0.0234	0.0352	0.0273
	hold↓ → G	-0.0664	-0.0625	-0.0547	-0.0703
G	minpwh	0.0785	0.0736	0.0785	0.0833

Cell Description

The XNOR2 cell provides a logical EXCLUSIVE NOR of two inputs (A, B). The output (Y) is represented by the logic equation:

$$Y = (A \bullet B) + (\bar{A} \bullet \bar{B})$$

Logic Symbol



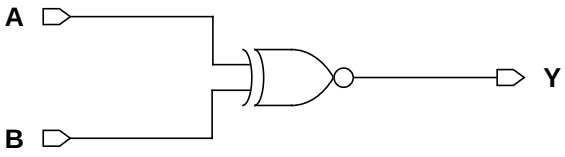
Functions

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Cell Size

Drive Strength	Height (µm)	Width (µm)
XNOR2XL	5.04	5.04
XNOR2X1	5.04	5.04
XNOR2X2	5.04	6.16
XNOR2X4	5.04	10.64

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A	0.0351	0.0354	0.0600	0.1056
B	0.0354	0.0455	0.0890	0.1672

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A	0.0053	0.0050	0.0071	0.0121
B	0.0022	0.0051	0.0102	0.0203

Delays at 25^{o}C, 1.8V, Typical Process

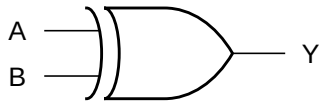
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A → Y↑	0.1077	0.1057	0.1193	0.1018	4.4791	3.9828	2.0206	0.9792
A → Y↓	0.1051	0.1059	0.0938	0.0891	2.6259	2.2991	1.1634	0.5639
B → Y↑	0.1492	0.1113	0.1018	0.0981	4.4820	3.9835	2.0211	0.9794
B → Y↓	0.1535	0.1302	0.1158	0.1115	2.6400	2.3038	1.1668	0.5655

Cell Description

The XOR2 cell provides a logical EXCLUSIVE OR of two inputs (A, B). The output (Y) is represented by the logic equation:

$$Y = (A \bullet \bar{B}) + (\bar{A} \bullet B)$$

Logic Symbol



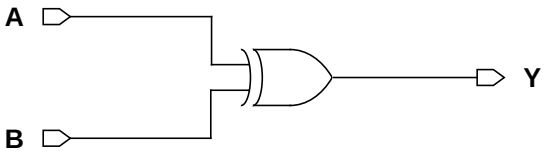
Functions

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
XOR2XL	5.04	5.04
XOR2X1	5.04	5.04
XOR2X2	5.04	6.16
XOR2X4	5.04	10.64

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A	0.0337	0.0335	0.0550	0.0960
B	0.0338	0.0437	0.0842	0.1625

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A	0.0054	0.0051	0.0071	0.0125
B	0.0022	0.0050	0.0103	0.0202

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A → Y↑	0.1075	0.0983	0.1086	0.0898	4.4813	3.9793	2.0190	0.9781
A → Y↓	0.1058	0.1058	0.1033	0.0943	2.6386	2.3039	1.1661	0.5654
B → Y↑	0.1482	0.1116	0.1001	0.0934	4.4808	3.9834	2.0214	0.9792
B → Y↓	0.1546	0.1326	0.1158	0.1140	2.6388	2.3040	1.1660	0.5654

Cell Description

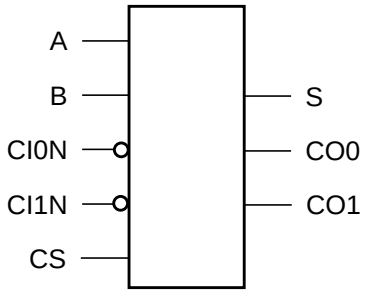
The AFCSHCIN cell provides a carry-select adder function that produces the arithmetic sum (S) and carry-outs (CO0, CO1) of the operands (A, B) with active-low carry-ins (CI0N, CI1N).The three outputs (S, CO0, CO1) are represented by the logic equations:

$$S = CS \bullet (A \oplus B \oplus \overline{CI1N}) + \overline{CS} \bullet (A \oplus B \oplus \overline{CI0N})$$

$$CO0 = (A \bullet B) + (A \bullet \overline{CI0N}) + (B \bullet \overline{CI0N})$$

$$CO1 = (A \bullet B) + (A \bullet \overline{CI1N}) + (B \bullet \overline{CI1N})$$

Logic Symbol



Cell Size

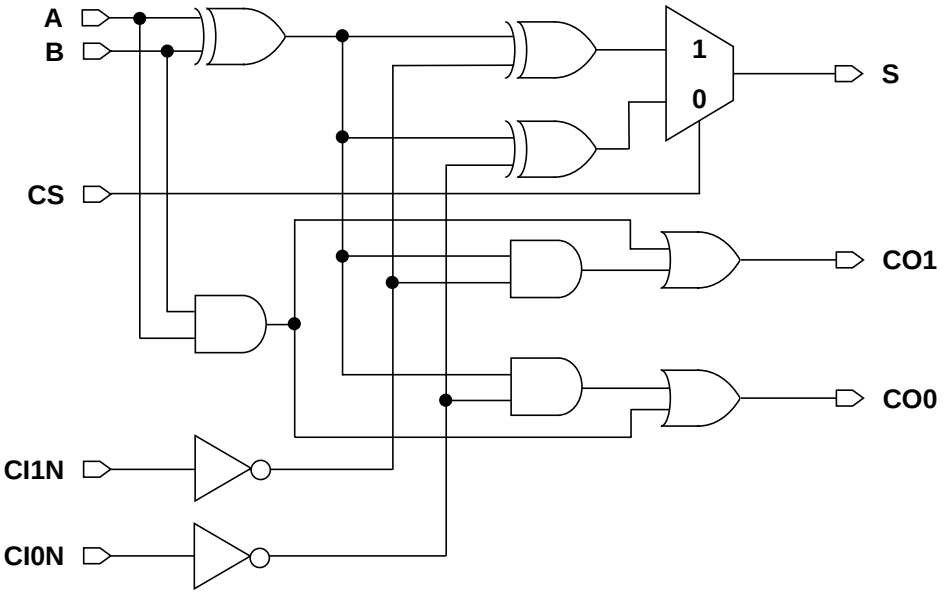
Drive Strength	Height (µm)	Width (µm)
AFCSHCINX2	5.04	31.36
AFCSHCINX4	5.04	35.84

Functions

A	B	CI0N	CI1N	CS	S	CO0	CO1
0	0	0	0	0	1	0	0
0	0	0	0	1	1	0	0
0	0	0	1	0	1	0	0
0	0	0	1	1	0	0	0
0	0	1	0	0	0	0	0
0	0	1	0	1	1	0	0
0	0	1	1	0	0	0	0
0	0	1	1	1	0	0	0
0	1	0	0	0	0	1	1
0	1	0	0	1	0	1	1
0	1	0	1	0	0	1	0
0	1	0	1	1	1	1	0
0	1	1	0	0	1	0	1
0	1	1	0	1	0	0	1
0	1	1	1	0	1	0	0
0	1	1	1	1	1	0	0

A	B	CI0N	CI1N	CS	S	CO0	CO1
1	0	0	0	0	0	1	1
1	0	0	0	1	0	1	1
1	0	0	1	0	0	1	0
1	0	0	1	1	1	1	0
1	0	1	0	0	1	0	1
1	0	1	0	1	0	0	1
1	0	1	1	0	1	0	0
1	0	1	1	1	1	0	0
1	1	0	0	0	1	1	1
1	1	0	0	1	1	1	1
1	1	0	1	0	1	1	1
1	1	0	1	1	0	1	1
1	1	1	0	0	0	1	1
1	1	1	0	1	1	1	1
1	1	1	1	0	0	1	1
1	1	1	1	1	0	1	1

Functional Schematic



AC Power

Pin	Power (µW/MHz)	
	X2	X4
CS	0.0606	0.0596
A	0.3154	0.3544
B	0.2783	0.3218
CI0N	0.1253	0.1524
CI1N	0.1256	0.1511

Pin Capacitance

Pin	Capacitance (pF)	
	X2	X4
CS	0.0052	0.0046
A	0.0063	0.0060
B	0.0135	0.0131
CI0N	0.0075	0.0122
CI1N	0.0074	0.0107

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)		K_{load} (ns/pF	
	X2	X4	X2	X4
CS → S↑	0.1158	0.1213	2.0213	2.0868
CS → S↓	0.1016	0.1098	1.1668	1.2627
A → S↑	0.3681	0.3974	2.0221	2.0873
A → S↓	0.3346	0.3674	1.1688	1.2632
B → S↑	0.2979	0.3244	2.0221	2.0873
B → S↓	0.2830	0.3238	1.1694	1.2635
CI0N → S↑	0.2227	0.2293	2.0221	2.0873
CI0N → S↓	0.2270	0.2294	1.1690	1.2633
CI1N → S↑	0.2004	0.1935	2.0217	2.0871
CI1N → S↓	0.2141	0.2267	1.1670	1.2627
A → CO0↑	0.1810	0.1822	2.4857	2.4970
A → CO0↓	0.2028	0.2245	1.5552	1.3233
B → CO0↑	0.1342	0.1503	2.4257	2.4926
B → CO0↓	0.1498	0.1668	1.5368	1.3133
CI0N → CO0↑	0.0687	0.0519	2.5024	1.2457
CI0N → CO0↓	0.0441	0.0378	1.4981	0.7931
A → CO1↑	0.1822	0.2031	2.5536	2.2049
A → CO1↓	0.2230	0.2516	1.6725	1.3627
B → CO1↑	0.1228	0.1349	2.5776	2.1951
B → CO1↓	0.1516	0.1766	1.6666	1.3546
CI1N → CO1↑	0.0678	0.0578	2.6191	1.3865
CI1N → CO1↓	0.0416	0.0374	1.5027	0.7842

Cell Description

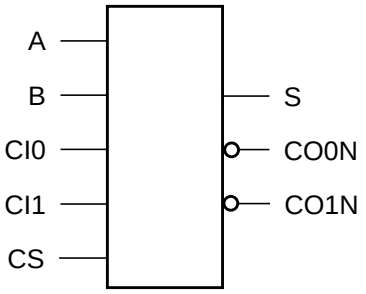
The AFCSHCON cell provides a carry-select adder function that produces the arithmetic sum (S) and active-low carry-outs (CO0N, CO1N) of two operands (A, B) with carry-ins (CI0, CI1). The three outputs (S, CO0N, CO1N) are represented by the logic equations:

$$S = CS \bullet (A \oplus B \oplus CI1) + \overline{CS} \bullet (A \oplus B \oplus CI0)$$

$$CO0N = \overline{(A \bullet B) + (A \bullet CI0) + (B \bullet CI0)}$$

$$CO1N = \overline{(A \bullet B) + (A \bullet CI1) + (B \bullet CI1)}$$

Logic Symbol



Cell Size

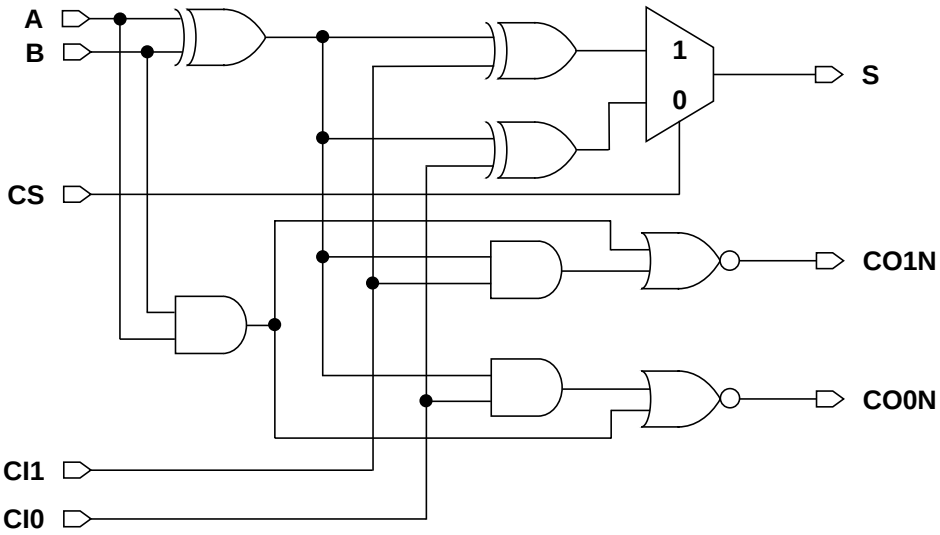
Drive Strength	Height (µm)	Width (µm)
AFCSHCONX2	5.04	32.48
AFCSHCONX4	5.04	35.84

Functions

A	B	CI0	CI1	CS	S	CO0N	CO1N
0	0	0	0	0	0	1	1
0	0	0	0	1	0	1	1
0	0	0	1	0	0	1	1
0	0	0	1	1	1	1	1
0	0	1	0	0	1	1	1
0	0	1	0	1	0	1	1
0	0	1	1	0	1	1	1
0	0	1	1	1	1	1	1
0	1	0	0	0	1	1	1
0	1	0	0	1	1	1	1
0	1	0	1	0	1	1	0
0	1	0	1	1	0	1	0
0	1	1	0	0	0	0	1
0	1	1	0	1	1	0	1
0	1	1	1	0	0	0	0
0	1	1	1	1	0	0	0

A	B	CI0	CI1	CS	S	CO0N	CO1N
1	0	0	0	0	1	1	1
1	0	0	0	1	1	1	1
1	0	0	1	0	1	1	0
1	0	0	1	1	0	1	0
1	0	1	0	0	0	0	1
1	0	1	0	1	1	0	1
1	0	1	1	0	0	0	0
1	0	1	1	1	0	0	0
1	1	0	0	0	0	0	0
1	1	0	0	1	0	0	0
1	1	0	1	0	0	0	0
1	1	0	1	1	1	0	0
1	1	1	0	0	1	0	0
1	1	1	0	1	0	0	0
1	1	1	1	0	1	0	0
1	1	1	1	1	1	0	0

Functional Schematic



AC Power

Pin	Power (µW/MHz)	
	X2	X4
CS	0.0614	0.0592
A	0.3363	0.3350
B	0.3159	0.3182
CI0	0.1498	0.1830
CI1	0.1326	0.1603

Pin Capacitance

Pin	Capacitance (pF)	
	X2	X4
CS	0.0081	0.0079
A	0.0106	0.0103
B	0.0130	0.0128
CI0	0.0106	0.0213
CI1	0.0106	0.0199

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)		K_{load} (ns/pF	
	X2	X4	X2	X4
CS → S↑	0.1164	0.1136	2.0213	2.0185
CS → S↓	0.1027	0.1014	1.1677	1.1506
A → S↑	0.3948	0.3848	2.0222	2.0188
A → S↓	0.3618	0.3415	1.1695	1.1514
B → S↑	0.3548	0.3440	2.0222	2.0188
B → S↓	0.3101	0.3052	1.1701	1.1511
CI0 → S↑	0.2263	0.2136	2.0222	2.0188
CI0 → S↓	0.2246	0.2046	1.1696	1.1512
CI1 → S↑	0.1863	0.1762	2.0216	2.0186
CI1 → S↓	0.1995	0.1815	1.1679	1.1506
A → CO0N↑	0.2003	0.2162	2.5393	2.4089
A → CO0N↓	0.2151	0.2138	1.4893	1.5642
B → CO0N↑	0.1713	0.1856	2.7511	2.4096
B → CO0N↓	0.1790	0.1734	1.4808	1.5642
CI0 → CO0N↑	0.0644	0.0383	2.8126	1.6630
CI0 → CO0N↓	0.0387	0.0299	1.4880	1.1263
A → CO1N↑	0.2175	0.2192	2.5601	2.3933
A → CO1N↓	0.2117	0.2120	1.5243	1.4986
B → CO1N↑	0.1887	0.1889	2.3983	2.3943
B → CO1N↓	0.1725	0.1717	1.5237	1.4985
CI1 → CO1N↑	0.0589	0.0397	2.6055	1.7401
CI1 → CO1N↓	0.0379	0.0280	1.4894	1.1352

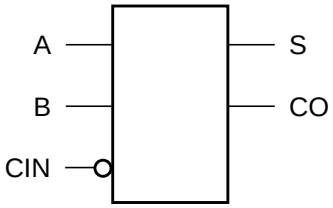
Cell Description

The AFHCIN cell is a full adder that provides the arithmetic sum (S) and carry-out (CO) of two operands (A, B) with active-low carry-in (CIN). The outputs (S, CO) are represented by the logic equations:

$$S = A \oplus B \oplus \overline{CIN}$$

$$CO = (A \bullet B) + (A \bullet \overline{CIN}) + (B \bullet \overline{CIN})$$

Logic Symbol



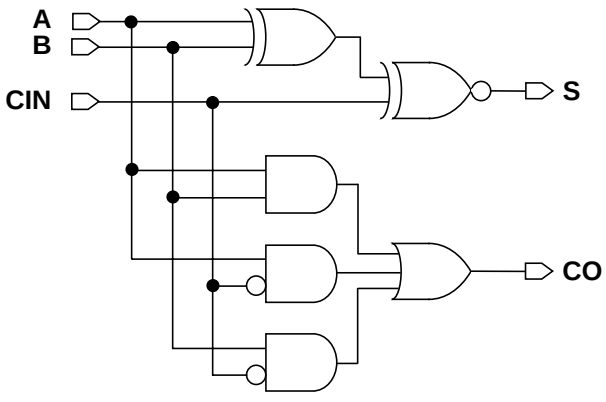
Functions

A	B	CIN	S	CO
0	0	0	1	0
0	0	1	0	0
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	1
1	1	1	0	1

Cell Size

Drive Strength	Height (µm)	Width (µm)
AFHCINX2	5.04	15.12
AFHCINX4	5.04	17.36

Functional Schematic



AC Power

Pin	Power (µW/MHz)	
	X2	X4
A	0.1596	0.1766
B	0.1652	0.1816
CIN	0.1166	0.1647

Pin Capacitance

Pin	Capacitance (pF)	
	X2	X4
A	0.0052	0.0052
B	0.0153	0.0134
CIN	0.0103	0.0205

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)		K_{load} (ns/pF	
	X2	X4	X2	X4
A → S↑	0.2148	0.2252	2.0205	2.0181
A → S↓	0.2541	0.2719	1.1671	1.1509
B → S↑	0.1697	0.1782	2.0218	2.0187
B → S↓	0.1783	0.1898	1.1663	1.1505
CIN → S↑	0.1169	0.0986	2.0215	2.0181
CIN → S↓	0.1280	0.1234	1.1693	1.1518
A → CO↑	0.1466	0.1686	2.6133	2.5375
A → CO↓	0.1782	0.2030	1.6337	1.5305
B → CO↑	0.1035	0.1195	2.6064	2.5316
B → CO↓	0.1324	0.1559	1.6169	1.5247
CIN → CO↑	0.0449	0.0400	2.5035	1.2222
CIN → CO↓	0.0333	0.0327	1.4978	0.7498

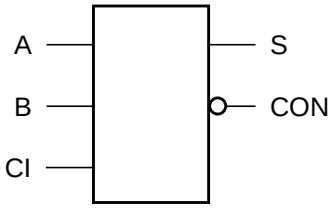
Cell Description

The AFHCON cell is a full adder that provides the arithmetic sum (S) and active-low carry-out (CON) of two operands (A, B) with carry-in (CI). The outputs (S, CON) are represented by the logic equations:

$$S = A \oplus B \oplus CI$$

$$CON = \overline{(A \bullet B) + (A \bullet CI) + (B \bullet CI)}$$

Logic Symbol



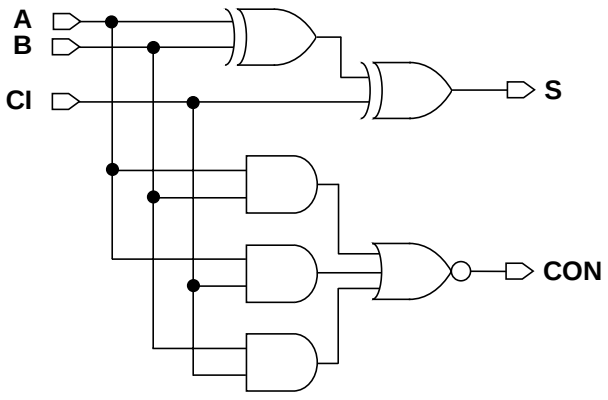
Functions

A	B	CI	S	CON
0	0	0	0	1
0	0	1	1	1
0	1	0	1	1
0	1	1	0	0
1	0	0	1	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
AFHCONX2	5.04	15.12
AFHCONX4	5.04	15.68

Functional Schematic



AC Power

Pin	Power (µW/MHz)	
	X2	X4
A	0.1661	0.1944
B	0.1532	0.1731
CI	0.1086	0.1597

Pin Capacitance

Pin	Capacitance (pF)	
	X2	X4
A	0.0051	0.0051
B	0.0174	0.0175
CI	0.0096	0.0205

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)		K_{load} (ns/pF	
	X2	X4	X2	X4
A → S↑	0.2031	0.2206	2.3242	2.0182
A → S↓	0.2375	0.2528	1.3372	1.1514
B → S↑	0.1325	0.1433	2.3252	2.0185
B → S↓	0.1550	0.1760	1.3360	1.1511
CI → S↑	0.1136	0.1015	2.3239	2.0185
CI → S↓	0.1213	0.1266	1.3372	1.1517
A → CON↑	0.1881	0.2067	2.7331	2.7626
A → CON↓	0.1589	0.1823	1.7238	1.7284
B → CON↑	0.1159	0.1333	2.7709	2.7831
B → CON↓	0.0940	0.1151	1.7429	1.7401
CI → CON↑	0.0577	0.0445	2.6791	1.2317
CI → CON↓	0.0385	0.0310	1.6414	0.7605

Cell Description

The AHHCIN cell is a half adder that provides the arithmetic sum (S) and carry-out (CO) of the input operand (A) with an active-low carry-in (CIN). The outputs (S, CO) are represented by the logic equations:

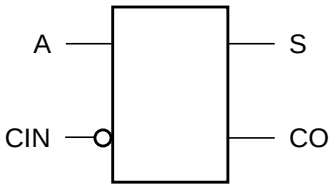
$$S = A \oplus \overline{CIN}$$

$$CO = A \bullet \overline{CIN}$$

Functions

A	CIN	S	CO
0	0	1	0
0	1	0	0
1	0	0	1
1	1	1	0

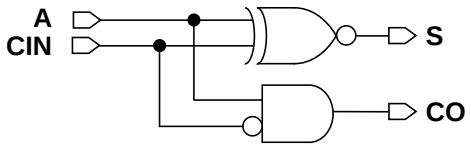
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
AHHCINX2	5.04	7.84
AHHCINX4	5.04	8.40

Functional Schematic



AC Power

Pin	Power (µW/MHz)	
	X2	X4
A	0.0905	0.1064
CIN	0.0740	0.0882

Pin Capacitance

Pin	Capacitance (pF)	
	X2	X4
A	0.0074	0.0096
CIN	0.0149	0.0177

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)		K_{load} (ns/pF	
	X2	X4	X2	X4
A → S↑	0.0709	0.0695	2.6940	2.6995
A → S↓	0.0766	0.0693	1.6017	1.6353
CIN → S↑	0.0421	0.0415	2.6992	2.7016
CIN → S↓	0.0520	0.0495	1.6391	1.6512
A → CO↑	0.0581	0.0539	2.8940	1.9689
A → CO↓	0.0750	0.0604	1.2817	0.7439
CIN → CO↑	0.0406	0.0399	2.8932	1.9686
CIN → CO↓	0.0229	0.0202	1.2756	0.7420

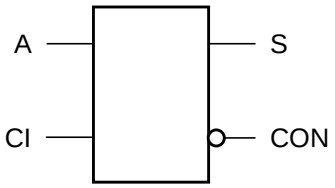
Cell Description

The AHHCON cell is a half adder that provides the arithmetic sum (S) and active-low carry-out (CON) of the input operand (A) with carry-in (CI). The outputs (S, CON) are represented by the logic equations:

$$S = A \oplus CI$$

$$CON = \overline{A \bullet CI}$$

Logic Symbol



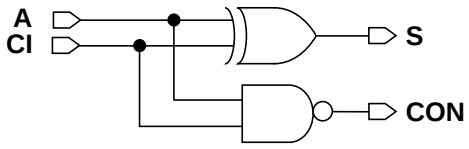
Functions

A	CI	S	CON
0	0	0	1
0	1	1	1
1	0	1	1
1	1	0	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
AHHCONX2	5.04	6.16
AHHCONX4	5.04	7.28

Functional Schematic



AC Power

Pin	Power (µW/MHz)	
	X2	X4
A	0.0931	0.1142
CI	0.0572	0.0722

Pin Capacitance

Pin	Capacitance (pF)	
	X2	X4
A	0.0102	0.0151
CI	0.0149	0.0192

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)		K_{load} (ns/pF	
	X2	X4	X2	X4
A → S↑	0.0772	0.0718	2.4511	2.5041
A → S↓	0.0842	0.0852	1.5184	1.5162
CI → S↑	0.0481	0.0406	2.4431	2.4878
CI → S↓	0.0583	0.0547	1.4883	1.5030
A → CON↑	0.0323	0.0310	2.5461	1.2732
A → CON↓	0.0215	0.0208	1.7781	0.8891
CI → CON↑	0.0270	0.0243	2.5474	1.2735
CI → CON↓	0.0193	0.0175	1.7781	0.8891

Cell Description

The booth encoder block (BENC) cell performs a 2-bit multiplier recoding per a modified Booth's algorithm. Each BENC cell examines 3 bits of the multiplier (M0, M1, M2) and generates the appropriate control signals to adjust the multiplicand for subsequent partial product reduction. The outputs (S, A, X2) are represented by the logic equations:

$$A = M2 + (\overline{M0} \bullet \overline{M1})$$

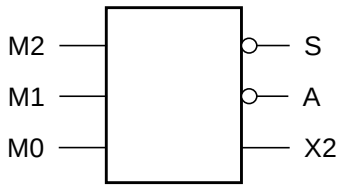
$$S = \overline{M2} + (M0 \bullet M1)$$

$$X2 = \overline{M1 \oplus M0}$$

Functions

M2	M1	M0	X2	A	S
0	0	0	1	1	1
0	0	1	0	0	1
0	1	0	0	0	1
0	1	1	1	0	1
1	0	0	1	1	0
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	1	1	1

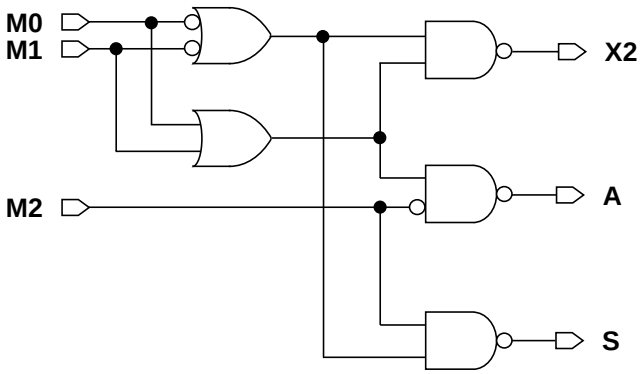
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
BENCX1	5.04	19.60
BENCX2	5.04	25.20
BENCX4	5.04	42.00

Functional Schematic



AC Power

Pin	Power (µW/MHz)		
	X1	X2	X4
M2	0.0717	0.1173	0.2200
M1	0.1408	0.2475	0.4707
M0	0.1547	0.2675	0.4937

Pin Capacitance

Pin	Capacitance (pF)		
	X1	X2	X4
M2	0.0065	0.0088	0.0133
M1	0.0089	0.0133	0.0269
M0	0.0078	0.0123	0.0241

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)			K_{load} (ns/pF)		
	X1	X2	X4	X1	X2	X4
M2 → A↑	0.1708	0.1724	0.1778	1.0160	0.5076	0.2537
M2 → A↓	0.1591	0.1618	0.1804	0.6147	0.3056	0.1526
M1 → A↑	0.1782	0.1753	0.1673	1.0157	0.5074	0.2536
M1 → A↓	0.1467	0.1380	0.1392	0.6155	0.3060	0.1527
M0 → A↑	0.1723	0.1672	0.1584	1.0156	0.5073	0.2536
M0 → A↓	0.1403	0.1311	0.1313	0.6154	0.3059	0.1527
M2 → S↑	0.1520	0.1358	0.1269	1.0154	0.5075	0.2631
M2 → S↓	0.1178	0.1027	0.0976	0.6129	0.3040	0.1516
M1 → S↑	0.2301	0.2166	0.1987	1.0151	0.5073	0.2630
M1 → S↓	0.2379	0.2202	0.2001	0.6140	0.3044	0.1518
M0 → S↑	0.2192	0.1902	0.1770	1.0149	0.5072	0.2629
M0 → S↓	0.2133	0.1768	0.1678	0.6138	0.3042	0.1517
M1 → X2↑	0.1672	0.1521	0.1410	1.0153	0.5128	0.2540
M1 → X2↓	0.1905	0.1785	0.1661	0.6710	0.3268	0.1539
M0 → X2↑	0.2138	0.1776	0.1671	1.0152	0.5128	0.2540
M0 → X2↓	0.2223	0.1850	0.1767	0.6711	0.3267	0.1540

Cell Description

The BMX cell performs the shifting and 2' s complement inversion of the multiplicand bits (M1, M0) based on the recode control signals (X2, A, S) from the booth encoder block cell. The partial product output (PP) is represented by the logic equation:

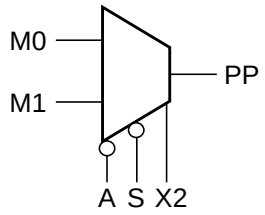
$$PP = X2 \bullet ((M0 \bullet \bar{A}) + (\overline{M0} \bullet \bar{S})) + \overline{X2} \bullet ((M1 \bullet \bar{A}) + (\overline{M1} \bullet \bar{S}))$$

Functions[1]

X2	A	S	M0	M1	PP
0	0	0	x	x	x
0	0	1	x	0	0
0	0	1	x	1	1
0	1	0	x	0	1
0	1	0	x	1	0
0	1	1	x	x	0
1	0	0	x	x	x
1	0	1	0	x	0
1	0	1	1	x	1
1	1	0	0	x	1
1	1	0	1	x	0
1	1	1	x	x	0

[1] Shaded areas represent illegal conditions.

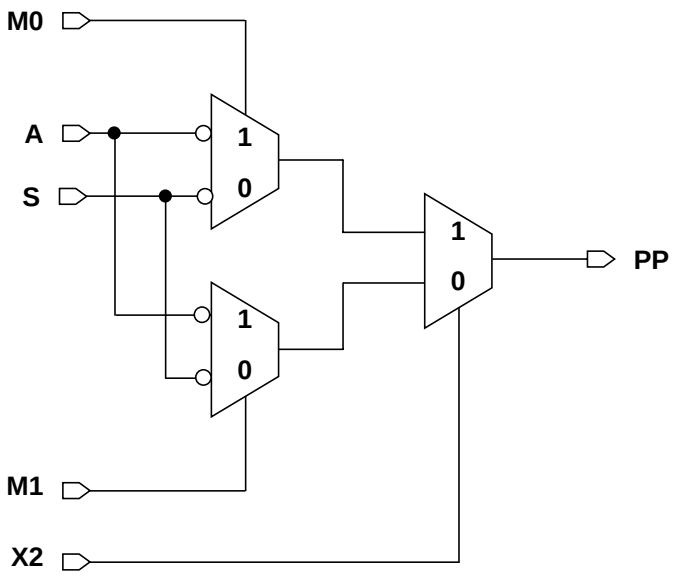
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
BMXX1	5.04	12.32

Functional Schematic



AC Power

Pin	Power (µW/
	X1
X2	0.0361
M0	0.0547
A	0.0558
S	0.0721
M1	0.0473

Pin Capacitance

Pin	Capacitanc
	X1
X2	0.0030
M0	0.0054
A	0.0039
S	0.0038
M1	0.0051

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)	K_{load} (ns/pF
	X1	X1
X2 → PP↑	0.1079	3.9794
X2 → PP↓	0.1031	2.3022
M0 → PP↑	0.1634	3.9830
M0 → PP↓	0.1989	2.3046
A → PP↑	0.1809	3.9830
A → PP↓	0.1788	2.3044
S → PP↑	0.1974	3.9832
S → PP↓	0.1906	2.3049
M1 → PP↑	0.1520	3.9828
M1 → PP↓	0.1814	2.2984

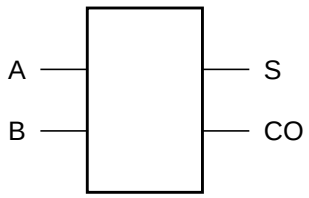
Cell Description

The CMPR22 cell provides the arithmetic sum (S) and carry out (CO) of two operands (A, B). The two outputs (S, CO) are represented by the logic equations:

$S = (\bar{A} \bullet B) + (A \bullet \bar{B})$

$CO = A \bullet B$

Logic Symbol



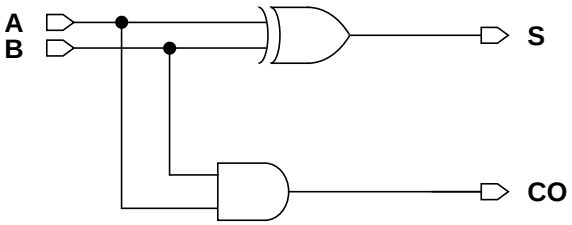
Functions

A	B	S	CO
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Cell Size

Drive Strength	Height (µm)	Width (µm)
CMPR22X1	5.04	7.84

Functional Schematic



AC Power

Pin	Power (µW/
	X1
A	0.0986
B	0.0556

Pin Capacitance

Pin	Capacitance
	X1
A	0.0087
B	0.0077

Delays (25°C, 1.8V, Typical Process)

Description	Intrinsic Delay (ns)	K_{load} (ns/ pF)
	X1	X1
A → S↑	0.0717	2.4708
A → S↓	0.0763	1.5282
B → S↑	0.0474	2.4609
B → S↓	0.0607	1.4658
A → CO↑	0.0724	3.9834
A → CO↓	0.0958	2.4823
B → CO↑	0.0723	3.9834
B → CO↓	0.0904	2.4790

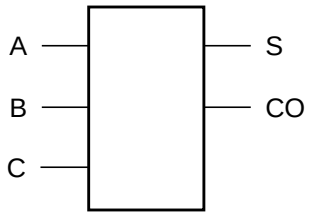
Cell Description

The CMPR32 cell takes in 3 bits of the partial product (A, B, C) and compresses them into 2-bits of partial product (S, CO). The two outputs (S, CO) are represented by the logic equations:

$$S = A \oplus B \oplus C$$

$$CO = (A \bullet B) + (A \bullet C) + (B \bullet C)$$

Logic Symbol



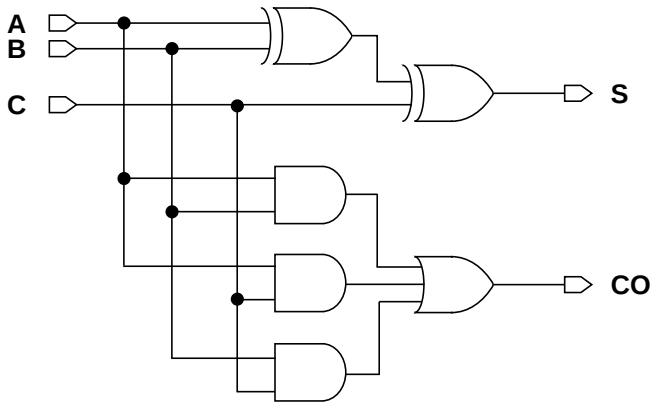
Functions

A	B	C	S	CO
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Cell Size

Drive Strength	Height (µm)	Width (µm)
CMPR32X1	5.04	12.88

Functional Schematic



AC Power

Pin	Power
	X1
A	0.1052
B	0.1365
C	0.0566

Pin Capacitance

Pin	Capacit
	X1
A	0.0058
B	0.0057
C	0.0057

Delays at 25°C, 1.8V, Typical Process

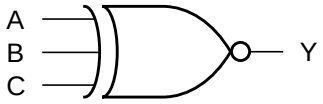
Description	Intrinsic Delay (ns)	K_{load} (ns/pF)
	X1	X1
A → S↑	0.1836	3.9964
A → S↓	0.2420	2.3851
B → S↑	0.2169	3.9971
B → S↓	0.2747	2.3850
C → S↑	0.1430	3.9933
C → S↓	0.1270	2.3962
A → CO↑	0.2216	3.9768
A → CO↓	0.2214	2.3217
B → CO↑	0.2537	3.9764
B → CO↓	0.2414	2.2846
C → CO↑	0.1161	3.9880
C → CO↓	0.1520	2.3376

Cell Description

The XNOR3 cell provides a logical EXCLUSIVE NOR of three inputs (A, B, C). The output (Y) is represented by the following equation:

$$Y = \overline{A \oplus B \oplus C}$$

Logic Symbol



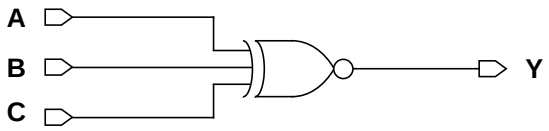
Functions

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
XNOR3X2	5.04	11.20
XNOR3X4	5.04	16.24

Functional Schematic



AC Power

Pin	Power (µW/MHz)	
	X2	X4
A	0.1246	0.2244
B	0.1084	0.1841
C	0.0503	0.0917

Pin Capacitance

Pin	Capacitance (pF)	
	X2	X4
A	0.0054	0.0057
B	0.0126	0.0171
C	0.0043	0.0078

Delays at 25°C, 1.8V, Typical Process

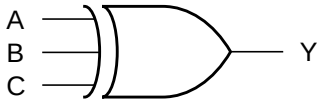
Description	Intrinsic Delay (ns)		K_{load} (ns/pF)	
	X2	X4	X2	X4
A → Y↑	0.2193	0.2271	2.0281	1.0140
A → Y↓	0.2372	0.2487	1.2245	0.6389
B → Y↑	0.1393	0.1648	2.0277	1.0176
B → Y↓	0.1678	0.2055	1.2184	0.6357
C → Y↑	0.1122	0.1196	2.0268	1.0175
C → Y↓	0.1124	0.1334	1.2167	0.6338

Cell Description

The XOR3 cell provides a logical EXCLUSIVE OR of three inputs (A, B, C). The output (Y) is represented by the following equation:

$$Y = A \oplus B \oplus C$$

Logic Symbol



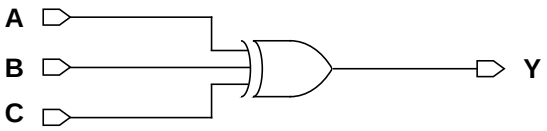
Functions

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Cell Size

Drive Strength	Height (µm)	Width (µm)
XOR3X2	5.04	11.20
XOR3X4	5.04	16.80

Functional Schematic



AC Power

Pin	Power (µW/MHz)	
	X2	X4
A	0.1269	0.2157
B	0.1121	0.1782
C	0.0499	0.0909

Pin Capacitance

Pin	Capacitance (pF)	
	X2	X4
A	0.0055	0.0055
B	0.0127	0.0178
C	0.0072	0.0136

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)		K_{load} (ns/pF)	
	X2	X4	X2	X4
A → Y↑	0.2253	0.2266	2.0286	1.0139
A → Y↓	0.2390	0.2443	1.2266	0.6388
B → Y↑	0.1404	0.1611	2.0284	1.0174
B → Y↓	0.1713	0.1987	1.2189	0.6345
C → Y↑	0.1134	0.1182	2.0276	1.0172
C → Y↓	0.1140	0.1296	1.2141	0.6334

Cell Description

The CMPR42 cell takes in 4 bits of the partial product (A, B, C, D) and compresses them into 2-bits of partial product (S, CO). The cell requires an intermediate carry-in input (ICI) from the n-1 compressor and an intermediate carry-out output (CO) to the n+1 compressor. The CMPR42 cell also contains an internal sum IS. The internal sum IS, carry-in output (ICO), and the two outputs (S, CO) are represented by the logic equations:

$$IS = A \oplus B \oplus C$$

$$ICO = (A \bullet B) + (A \bullet C) + (B \bullet C)$$

$$S = IS \oplus D \oplus ICI$$

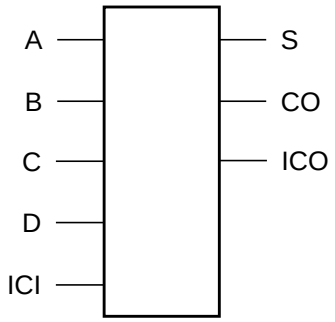
$$CO = (IS \bullet D) + (IS \bullet ICI) + (D \bullet ICI)$$

Functions

A	B	C	IS	ICO
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

IS	D	ICI	S	CO
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

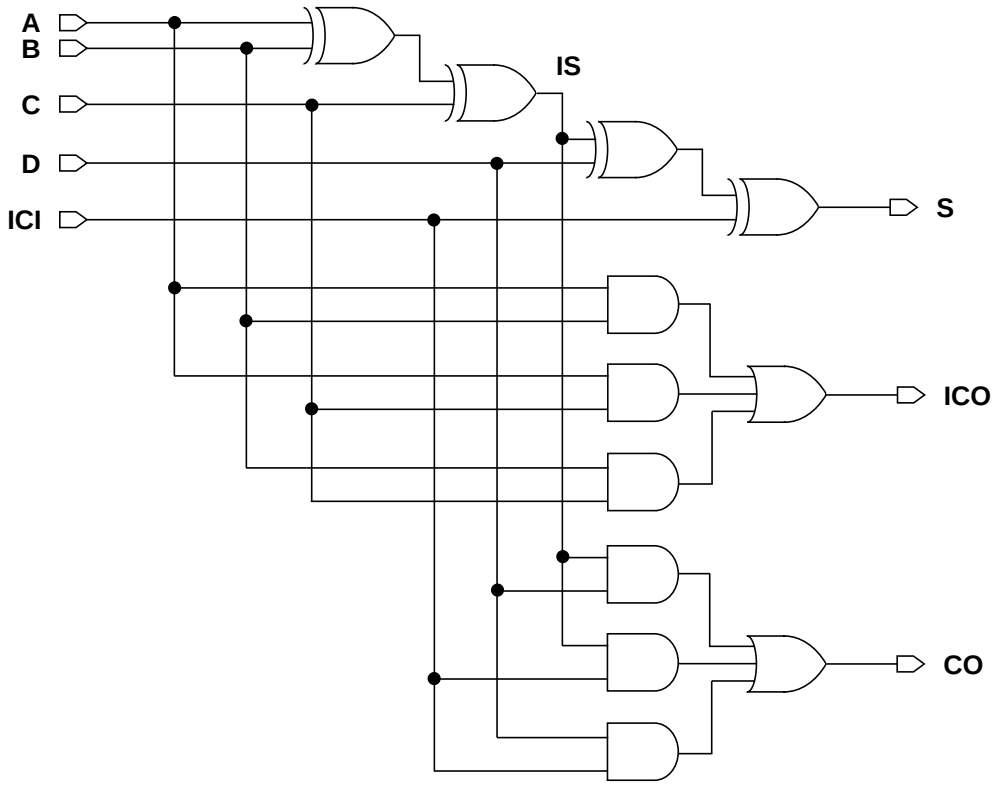
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
CMPR42X1	5.04	23.52
CMPR42X2	5.04	24.08

Functional Schematic



AC Power

Pin	Power (µW/MHz)	
	X1	X2
A	0.1694	0.2579
B	0.1640	0.2498
C	0.1533	0.2332
D	0.1247	0.1869
ICI	0.0628	0.1022

Pin Capacitance

Pin	Capacitance (pF)	
	X1	X2
A	0.0088	0.0133
B	0.0093	0.0133
C	0.0082	0.0112
D	0.0059	0.0078
ICI	0.0033	0.0051

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)		K_{load} (ns/pF)	
	X1	X2	X1	X2
A → S↑	0.4131	0.3987	3.9869	2.0231
A → S↓	0.5028	0.4737	2.2955	1.1631
B → S↑	0.3496	0.3287	3.9870	2.0231
B → S↓	0.4393	0.4036	2.2954	1.1631
C → S↑	0.3157	0.3009	3.9863	2.0229
C → S↓	0.4063	0.3769	2.2955	1.1632
D → S↑	0.2771	0.2617	3.9813	2.0209
D → S↓	0.3321	0.3090	2.2954	1.1631
ICI → S↑	0.1532	0.1421	3.9857	2.0223
ICI → S↓	0.1782	0.1600	2.2967	1.1636
A → ICO↑	0.0790	0.0792	3.9858	2.0238
A → ICO↓	0.1440	0.1300	2.2968	1.1654
B → ICO↑	0.0782	0.0809	3.9873	2.0240
B → ICO↓	0.1357	0.1251	2.2970	1.1654
C → ICO↑	0.0687	0.0664	3.9841	2.0219
C → ICO↓	0.1157	0.1079	2.2982	1.1689
A → CO↑	0.4008	0.3875	3.9835	2.0221
A → CO↓	0.4675	0.4493	2.2811	1.1613
B → CO↑	0.3504	0.3392	3.9835	2.0221
B → CO↓	0.4170	0.4010	2.2811	1.1614
C → CO↑	0.3104	0.2973	3.9834	2.0220
C → CO↓	0.3405	0.3251	2.2811	1.1614
D → CO↑	0.2611	0.2414	3.9798	2.0205
D → CO↓	0.2555	0.2412	2.2701	1.1584
ICI → CO↑	0.0869	0.0828	3.9864	2.0228
ICI → CO↓	0.1232	0.1154	2.3055	1.1715

Cell Description

The RF1R1W register file cell is an active-high D-type transparent latch with an active-high tri-state output. The output (RB) is inverted.

Functions for Write Operations

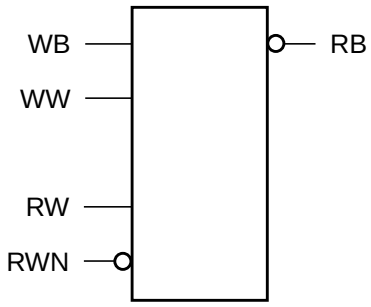
WW	WB	q[n+1]
0	0	0
0	1	q[n]
0	0	q[n]
0	1	q[n]
1	0	0
1	1	1
1	0	q[n]
1	1	1

Functions for Read Operations[1]

RW	RWN	q	RB
0	0	0	1
0	0	1	Hi-Z
0	1	0	Hi-Z
0	1	1	Hi-Z
1	0	0	1
1	0	1	0
1	1	0	Hi-Z
1	1	1	0

[1] Shaded areas represent operations that are legal only during RW/RWN transitions.

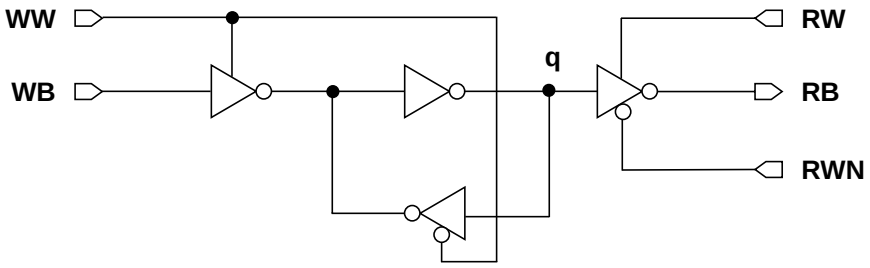
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
RF1R1WX2	5.04	6.16

Functional Schematic



AC Power

Pin	Power (µW/MHz)
	X2
WW	0.0308
WB	0.0319
RW	0.0045
RB	0.0216

Pin Capacitance

Pin	Capacitance (pF)
	X2
WW	0.0054
WB	0.0023
RW	0.0025
RWN	0.0016
RB	0.0070

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)	K_{load} (ns/pF)
	X2	X2
WW → RB↑	0.2112	3.9379
WW → RB↓	0.1311	1.7576
WB → RB↑	0.1927	3.9380
WB → RB↓	0.1433	1.7576
RW → RB↑	0.0271	3.9363
RW → RB↓	0.0115	1.7558

Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)
		X2
WW	minpwh	0.0688
WB	setup↑ → WW	0.0820
	setup↓ → WW	0.0977
	hold↑ → WW	-0.0703
	hold↓ → WW	-0.0898

Cell Description

The RF2R1W register file cell is an active-high D-type transparent latch with two independently controlled, active-high tri-state outputs. The cell has two read ports and one write port. The outputs (R1B, R2B) are inverted.

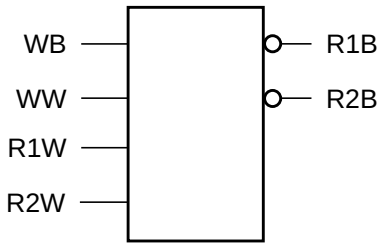
Functions for Write Operations

WW	WB	q[n+1]
0	0	q[n]
0	1	q[n]
1	0	0
1	1	1

Functions for Read Operations

R1W/ R2W	q	R1B/ R2B
0	0	Hi-Z
0	1	Hi-Z
1	0	1
1	1	0

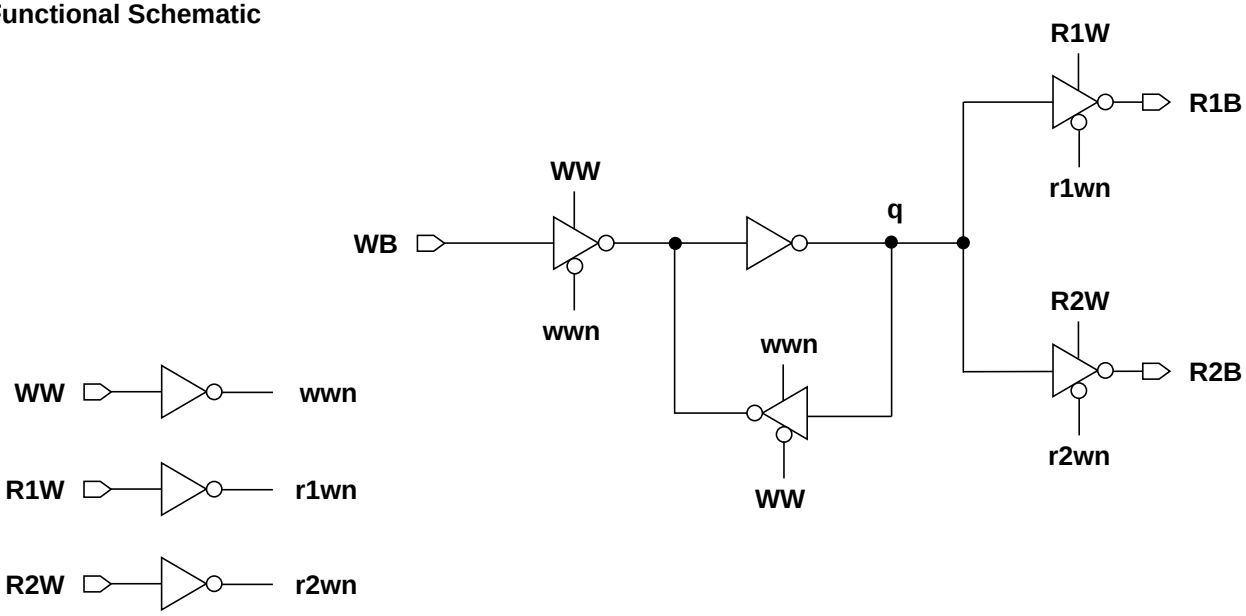
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
RF2R1WX2	5.04	9.52

Functional Schematic



AC Power

Pin	Power (µW/MHz)
	X2
WB	0.0432
WW	0.0139
R1W	0.0102
R2W	0.0102
R1B	0.0816

Pin Capacitance

Pin	Capacitance (pF)
	X2
WB	0.0024
WW	0.0043
R1W	0.0032
R2W	0.0041
R1B	0.0044
R2B	0.0042

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)	K_{load} (ns/pF)
	X2	X2
WB → R1B↑	0.2215	3.9385
WB → R1B↓	0.1731	1.7623
WW → R1B↑	0.2367	3.9385
WW → R1B↓	0.1615	1.7623
R1W → R1B↑	0.0538	3.9343
R1W → R1B↓	0.0146	1.7528
WB → R2B↑	0.2213	3.9390
WB → R2B↓	0.1727	1.7624
WW → R2B↑	0.2364	3.9389
WW → R2B↓	0.1611	1.7624
R2W → R2B↑	0.0535	3.9343
R2W → R2B↓	0.0142	1.7529

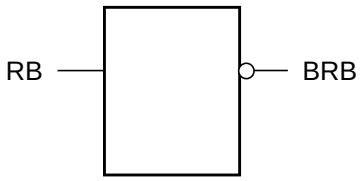
Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)
		X2
WB	setup↑ → WW	0.0938
	setup↓ → WW	0.1094
	hold↑ → WW	-0.0820
	hold↓ → WW	-0.0938
WW	minpwh	0.0833

Cell Description

The RFRD output buffer has a "keeper" function that holds the input and output ports at the present level when the input (RB) is in a state of high-impedance.

Logic Symbol



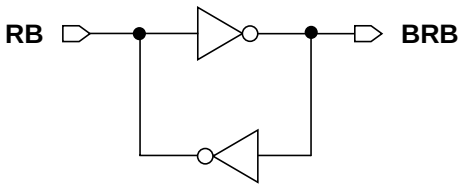
Functions

RB	BRB
0	1
1	0
Hi-Z	Keep

Cell Size

Drive Strength	Height (µm)	Width (µm)
RFRDX1	5.04	3.36
RFRDX2	5.04	3.36
RFRDX4	5.04	3.92

Functional Schematic



AC Power

Pin	Power (µW/MHz)		
	X1	X2	X4
RB	0.0302	0.0388	0.0537

Pin Capacitance

Pin	Capacitance (pF)		
	X1	X2	X4
RB	0.0811	0.0855	0.0892

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)			K_{load} (ns/pF)		
	X1	X2	X4	X1	X2	X4
RB → BRB↑	0.0457	0.0332	0.0250	3.9812	2.0193	1.0094
RB → BRB↓	0.0288	0.0204	0.0152	2.2326	1.1390	0.5695