Generation of .LEF File

- Do the following in the directory where your standard cells(hw5) are located
- The following are the files to be copied
- cp /sw/CDS/TANNER/stream.map
- Create a sub-directory in the present directory and name it as "tech"
- cp /sw/CDS/TANNER/tech/*.* to the tech directory

Unfortunately the abstract view created in Virtuoso does not include some important information required by Silicon Ensemble, so this intermediate step helps in moving the design between programs.

Abstract generator comes as a part of the Silicon Ensemble package. As such, it cannot directly read ICFB library databases. We need to export the standard cell library to Stream (GDS) format, then re-import the GDS file in Abstract Generator.

Next slide explains " Exporting to GDS format"

Checklist:

You should be having "stream.map" and "/tech/tech.dpux" before you go to the next slide

Exporting to GDS Format

- To export to GDS format from ICFB:
- Go to the **CIW**.
- Click on *File -> Export -> Stream*...
- In the **Virtuoso Stream Out** form, enter the following information:

Run Directory: .(just a dot meaning current directory)

Library Name: <your standard_cells library name>

Top Cell Name: (leave blank)

View Name: layout

Output File: <example : "STD.gds">

• Then, click on the User-Defined Data button. A new form, the Stream-Out User-Defined Data form will appear.

-			Virtu	oso® Stream Out
ок	Cancel	Defaults	Apply	Help
User-Def	ined Data	And Optic	ins	User-Defined Data Options
Template	File	Load	Save	Ĭ.
				Library Browser
Run Direc	tory			.1
Library Na	ame			Štandard_cells
Top Cell N	lame			Ĭ.
View Nam	ne			layout
Output				Stream DB ASCII Dump
Output Fil	le			STD. gdsj
Scale UU	/DBU			0.00100000
Units				micron millimeter mil
Process N	lice Value	0-20		

Figure 1

Exporting to GDS Format

- In the Stream Out User-Defined Data form, enter "stream.map" for the Layer Map Table. Then, click on OK.
- The text file **stream.map** tells ICFB which layers correspond to which GDS numbers. When we re-import the GDS file back into Abstract Generator, we are going to use the same Layer Map file.
- Refer to Fig : 2 (next slide) for the **Stream Out User-Defined Data** form.

📕 Stream Out User-Defined Data	×
OK Cancel Defaults Apply	Help
Convert Pin to	🔶 geometry 🐟 text 🐟 drop
Pin Text Map Table	ļ.
Keep pin information as attribute number	<u>dï</u>
Cell Name Map Table	<u>I.</u>
Layer Map Table	stream.map
Text Font Map Table	ļ
User-Defined Property Mapping File	<u>I.</u>
User-Defined Property Separator	
User-Defined SKILL File	ļ.

Figure 2 : Stream Out User-defined data

Exporting to GDS Format

- Now, back in the Virtuoso Stream Out Form (Figure 1), click on the Options button. A new form, the Stream Out Options form will appear (Figure 3).
- In the Stream Out Options form, select "No Merge" for the "Convert PCells to Geometry" field. This flattens out any parametric cells in the cell library (For the I/O Pad Cells). Then, click on OK.
- Click on **OK** in the **Virtuoso Stream Out** form. A *GDS* file (STD.*gds)* containing the standard cell library will be generated.



Figure 3: Stream Out Options Form

Using Abstract Generator to create LEF file

- To start up Abstract Generator:
- Go to the directory where your standard cells are located and type :

abstract -- tech ./ tech &

• This will bring up the abstract generator screen. First, we need to import the *GDS* file containing our standard cell layouts, that we exported from ICFB previously.

🗶 Abstract - [I	no current lib	rary]						_ 🗆 ×
File Bins (Cells Flow							Help
80								
Bin	Cells	Cell	Layout	Logical	Pins	Extract	Abstract	Verify
Core	0							
IO	0							
Corner	0							
Block	0							
Ignore	0							

Figure 4: Abstract Generator's Main Window

- In the main window, click on *File -> Technology*...
- After a few moments, the Technology File Editor should appear. Click on Library path on the left column, then give "some library name" and "Path" on the top row. (refer Figure 5, next slide)



Figure 5: Abstract Generator's tech

• Click on Layers on the left column, then click on Mapping on the top row. (refer Figure 6, next slide)

-	Te	chnology	File Editor——./1	tech/tech.dpux 🛛 🖓 🗌
File Edit Help				
Categories	efine Elect	ronic D	isplay Mapp [.]	ing
Library Path				
Layers	Gds Number	Gds Type	Layer	Purpose GDS
Inter Layers	1 25	0	cc y	▼]drawing ▼A
Vias	2 47	0	cc y	▼drawing ▼ Map
Via Rules	3 48	0	cc	drawing
Routing Rules	4 55	0	cc y	drawing Add
Global	5 49	0	metal1 '	▼ drawing ▼
	6 232	0	metal1 ·	▼pin ▼ Delete
	7 51	0	metal2	▼ drawing ▼
	8 233	0	metal2	▼pin ▼
	9 62	0	metal3 ·	▼ drawing ▼
1	0 234	0	metal3 ·	▼pin ▼

Figure 6

- You should see all the numbers which means already the stream.map had been loaded
- Click File -> Save and then Close the window

- In the main window, click on *File -> Library*.
- If you have more than one design library, you will have to choose a design library to be your current working library.
- You should see the figure 4 again with no changes

- Click on *File -> Import -> Stream(GDSII)*
- The **Import** form will appear (you may have to resize it after it appears).

💥 Import Layout	_ 🗆 ×
GDSII Filenames:	
	Browse
Map GDSII names:	No Mapping
	OK Cancel Help

- Click on the **Browse** button. A browse form will appear (Figure 7, next slide)
- The GDS file we are looking for is STD.*gds*.
- Navigate through the browser to get to that file.
- Double-click on the file STD.*gds*.
- Back in the Import window, click on OK.

_	Import	Layout	•
	GDSII Filenames:		
	/home/balash/651/lef/STD.gds		Browse
P	Map GDSII names:	No Mapping 🖃	
[Default Bin:	Core 💻	
		OK Cancel	Help .

Figure 7: Browse Import Layout File Form

• After a few moments, the standard cell layouts contained in *std.gds* will be imported into abstract generator. Notice that the **Core** bin now has "number of cells you have got ".

Viewing Cell Layout

- In the main window, click on the **Core** bin once. You should see that beside each cell, there is a green tick mark in the **Layout** column. This means there is a valid layout view for each cell.
- Under Cell, your cell names will be listed

—			Abstract – chandra	- 🗆
File Bins	Cells Flo	W		Help
V				
Bin	Cells	Cell	Layoot Logical Pins Extract Abstract Veri	fy
Core	7	FILL		
IO	0	INV		
Corner	0	INV_1	\checkmark	
Block	0	INV_2		
Ignore	6	NAND2	\checkmark	
		NAND2_1	\checkmark	
		NAND2_2		

Abstract Generation - Overview

- There are three main steps in generating abstracts – generating the *Pins* view, the *Extract* view and finally the *Abstract* view.
- The *Pins* step maps text labels to metal layers, designating certain metal blocks as pins (all pin information is lost during GDS export, so we need to re-instate that information).
- The *Extract* step merges metal blocks under the same net into one single net we will not be using this function since we want our pins to be specifically 3x3 lambda sized pins. It also changes any *metal.pin* layer into *metal.net*.

Abstract Generation - Overview

- The *Abstract* step copies the pin (net) information from the *Extract* step, and generated blockages for the metal and via layers (or any other layer that you specify). These blockages will tell the placeand-route tool (namely Silicon Ensemble) which parts of the standard cell to avoid routing over with certain layers.
- The resulting *Abstract* view contains only *net* and *blockage* information.
- An *LEF* file will then be generated, using the *Abstract* view of the standard cells.

- Since all the standard cells are alike, we can process them all at once.
- Select all the cells.
- Click on *Flow -> Pins*. The **Pins** form will appear.
- Enter the fields as shown in Figure 8. The next slide after that will explain what the entries mean.

_		Running step Pins for the selected cell(s)	
Г	-Sten	Map Text Boundary	
	◆ Pins	Map text labels to pins: ((text drawing) (metal1 pin) (metal1 drawing) (met al2 pin) (metal2 drawing)) Power pin names (regular expressions):	
	Bin	VDD VDD! vdd vdd! VCC VCC! vcc vcc! Ground pin names (regular expressions): VSS VSS! vss vss! GND GND! and and!	
	◆ Core	Output pin names (regular expressions): Out	
		Run Cancel Help	

Figure 8: Pins Form (Map Tab)

- Map Text Label to Pins: Notice we have entered "((text drawing) (metal1 pin) (metal1 drawing) (metal 2 pin) (metal 2 drawing))" for this field.
- This tells Abgen to map any text in *text.drawing* to *metal1.pin* shapes if there are any *metal1.pin* shapes overlapping the text.
- If there aren't any *metal1.pin* shapes overlapping the text, then map the text to any overlapping *metal1.drawing* shapes.
- This works for us because all our text labels are either located over *metal1.pin* shapes (for our regular pins), or over *metal1.drawing* shapes (for our vdd/gnd pins).

• We have entered "**Out**" for the output pin names. In case of Inverter output pin named is "Out". List the Output pin names that you have in your standard cell

• In the exported LEF file, these pins will have "output" as their direction.

- The *Pins* step also generates Place-and-Route Boundaries (PR Boundaries) for each cell.
- Click on the **Boundary** tab. The **Pins** form will change to that of figure 9 (next slide).
- Choose "always" for the Create Boundary field.
- Fill in the values for "Adjust Boundary By" according to that shown in figure 9.

Running step Pins for the selected cell(s)

	Create boundary:	always
	Using geometry on layers:	
	metal1 metal2 metal3 via vi	a2 poly
	Adjust Boundary By	
	Left:	-0.6
	Right:	-0.6
ī	Тор:	-0.9
	Bottom:	-0.9
	Fix Boundary To	
	Left:	r
	Right:	
	Тор:	
	Bottom:	

- 🗆 ×

Figure 9: Pins Form (Boundary Tab)

- Now, click on **Run**. Abgen will take a few moments to generate *Pins* views for the selected standard cells.
- After Abgen is done, you will see an exclamation mark beside each selected cell, in the **Pins** column. An exclamation mark means that there was a warning (not an error) in the generation of that view.
- To see what the warning was, click on a standard cell (e.g. click on *any cell*). Then, click on *Cells* > *Report*.

-	-			Abstract – char	ndra			-	
	File Bins	Cells Flo	W					Hel	р
			⊠ ∞ Ľ 🗸						
	Bin	Cells	Cell	Layout	Logical Pins	Extract	Abstract	Verify	
	Core	7	FILL						
	IO	0	INV						
	Corner	0	INV_1						
	Block	0	INV_2						
	Ignore	6	NAND2						
			NAND2_1						
			NAND2_2						

Abstract Generation – Extract Step

- In the main window, select all the standard cells
- Click on *Flow -> Extract*. The *Extract* form will appear.
- Click once on the Extract Signal Nets box to deselect it.
- Then, click on the **Power** tab to bring up the Power Net menu. Click once on the **Extract Power Nets** box to **de-select** it.
- Click on **Run**. This will run *Extract* on all the cells.
- To view the *Extract* view of a cell, select that cell, then click on *Cells -> Edit -> Extract*.

Step	Signal Power Antenna	
💠 Pins	Extract signal nets	
🔶 Extract	Extract through layers:	
	metal1 metal2 metal3 via via2	
	Extract through weak layers:	
		,
	Restrict pins to layers:	
	metal1 metal2 metal3 via via2	
Di		
BIN	Extract Limitations	
 Core 	Maximum depth: 20	
	Maximum distance:	
	Minimum width:	
	Create Must Connect Pins If Required	
	Only on terminals named:	

Figure 10: Extract Form (Signal Tab)

ep	Signal Powe	er Antenna	
าร	Extract por	wer nets	
tract	Extract throug	jh layers:	
	metall metal	2 metal3 via via2	
	Restrict pins t	to layers:	
	metall metal	2 metal3 via via2	
	Future et Linsite	4i	
		luons	1 00
	Maximum dep	un: anco:	20
	Minimum widt	ance.	
		41.	

Figure 11: Extract Form (Power Tab)



Abstract Generation – Abstract Step

- In the main window, select all the standard cells *FILL, INV,INV_1,INV_2, NAND2, NAND2_1,NAND2_2 (given as example here)*
- Under the Blockage tab, make sure that "metal1 metal2 metal3 via via2" is entered for the "Create detailed blockages on layers" field.
- Under the **Site** tab, enter "core" for the site name.
- Click on **Run**. This will generate abstracts for the aforementioned cells.

Running step Abstract for the selected cell(s)

ſ		1	1								
-Step	Adjust	Blockage	Site	Overlap	Grids						
🔷 Pins	Create	detailed bloc	kages o	n layers:							
♦ Extract	metal1 metal2 metal3 via via2										
• restaut											
	Create	shrinkwrap I	blockage	s on layers:							
	- Shrink	-Wrap									
	Numbe	er of min wid	th tracks								
Bin											
Core	Numbe	er of microns	:								
		ndow	und com	o louor nino	-						
	Distan	ce w cui aro	unu sam	e iayer pins	•						
	Distan	ce to cut aro	und nins	on laver be	low:						
			ana pino	on ayor bo							
				(1					
				Run	Cancel	Help					

Figure 12: Abstract Form (Blockage Tab)

- 🗆 X

Running step Abstract for the selected cell(s)												
Step	Adjust	Blockage	Site	Overlap	Grids							
 ◇ Pins ◇ Extract ◆ Abstract 	Site Na	ame:			core							
Bin Core												

Figure 13: Abstract Form (Site Tab)

Abstract Generation – Abstract Step

- Notice that there are exclamation marks in the **Abstract** column of the cells, in the main window.
- Select a cell (e.g. *INV*), then click on *Cells* > *Report*.
- The report for the *Abstract* step warns us that the **vdd** and **gnd** terminals have no pins on the Metal1-Metal2 routing grid.
- The warning can be safely ignored.



Abstract Generation – Verify Step

- In the main window, select all the standard cells
- Click on **Run**.
- Check out the next picture for results

_				Abstract – STD1				· 🗆
F	ile Bins	Cells Flo	W					Help
	0		8 📾 🗳 💞					
	Bin	Cells	Cell	Layout Logical	Pins	Extract	Abstract	Verify
	Core	7	FILL					ļ
1	IO	0	INV					
(Corner	0	INV_1					
	Block	0	INV_2					1 (C
	Ignore	9	NAND2					1 (I (I (I (I (I (I (I (I (I (
			NAND2_1					1 (I (I (I (I (I (I (I (I (I (
			NAND2_2					1 I I I I I I I I I I I I I I I I I I I
Ī.								_

Figure 14: Verify Form

A Note about Warnings

- Warnings do not equal errors!
- Whenever you encounter a warning (or even an 'info' line), check its validity, and compare it with what you know about the standard cells.
- If the warning is something that you know about, and you know that it is okay, then you can safely ignore the warning.
- Of course if there is genuine concern about the warning you should go back to your previous steps and fix whatever is causing the warning before proceeding.

Cell Orientation

- All the cells in the **core** bin should have abstract views by now.
- Select all the standard cells (exclude the Pad cells).
- Click on *Cells -> Cell Properties*
- Change property **symmetry** to **X**, then click on **Apply** (refer figure 32, next slide).
- Click on **OK** to close the form.
- Having a symmetry of X means the cells can only be flipped about the X-axis.

X	Cell Properties			
	Change property	symmetry — t	0 X	- Apply
	Cell	Bin	class	symmetry
	DFFSRX1	Core	CORE	X
	FILL	Core	CORE	X
	FILL2	Core	CORE	X
	INVX1	Core	CORE	X
	NAND2X1	Core	CORE	X
	NOR2X1	Core	CORE	X
	TIEHI	Core	CORE	X
	TIELO	Core	CORE	X
			ок Са	ncel Help

Figure 15: Cell Properties Form

Extracting to LEF Format

- In the main window, click on *File -> Export* -> *LEF*.
- The Export LEF form will appear.
- Click on the **Browse** button, and save the LEF file as 'abstract.*lef*'.(Any name)
- Set "LEF Units " to be 100.
- Click on **OK** in the **Export LEF** form.

	Export LEF	· 🗆
LEF Filename:		
abstract.lef		Browse
LEF Units:	100 -	
LEF Version:	5.3 💻	
Export LEF for Bin:	A11 —	
🖾 Export Antenna LE	=	
Antenna LEF Filename		
antenna.let		
	OK Cancel	Не1р

Figure 16: Export LEF Form

Modify the following in LEF file

- Pico "abstract.lef"
- Scroll down till you see the following and change its value from 18.00 to 24.00 (Check out next slide)

-	_									axe					· 🔲
*	~/	651/hw	6/Sta	andaro	d_cel	ls.1	ef								
	love	Search	Insert	Delete	Нер	Misc	Font	Window	Buffer	Show	File	Quit	\sim	 	
		ARULE AYER I DIRE AYER I DIRE DIRE	TURN2 metal: CTION metal: CTION 2	GENE 2 ; HORI: 2 ; VERT	RATE ZONT ICAL	AL ; ;									
	VIARULE TURN3 GENERATE LAYER metal3 ; DIRECTION HORIZONTAL ; LAYER metal3 ; DIRECTION VERTICAL ; END TURN3														
	SIT	TE CO CLAS SYMM SIZE COP	re S ETRY e	CO Y 2.	RE ; ; 400	BY 1	8.00	0 ;(Ch	ange	18.00	o, t	o 24.000)			
	SIT	TE CO CLAS SYMM SIZE COM	rner S ETRY her	PA R9 30	D ; O Y O.OO	; 0 by	300	.000;							

Figure 17: Change in the LEF file