A CCSDS-Based Communication System for a Single Chip On-Board Computer

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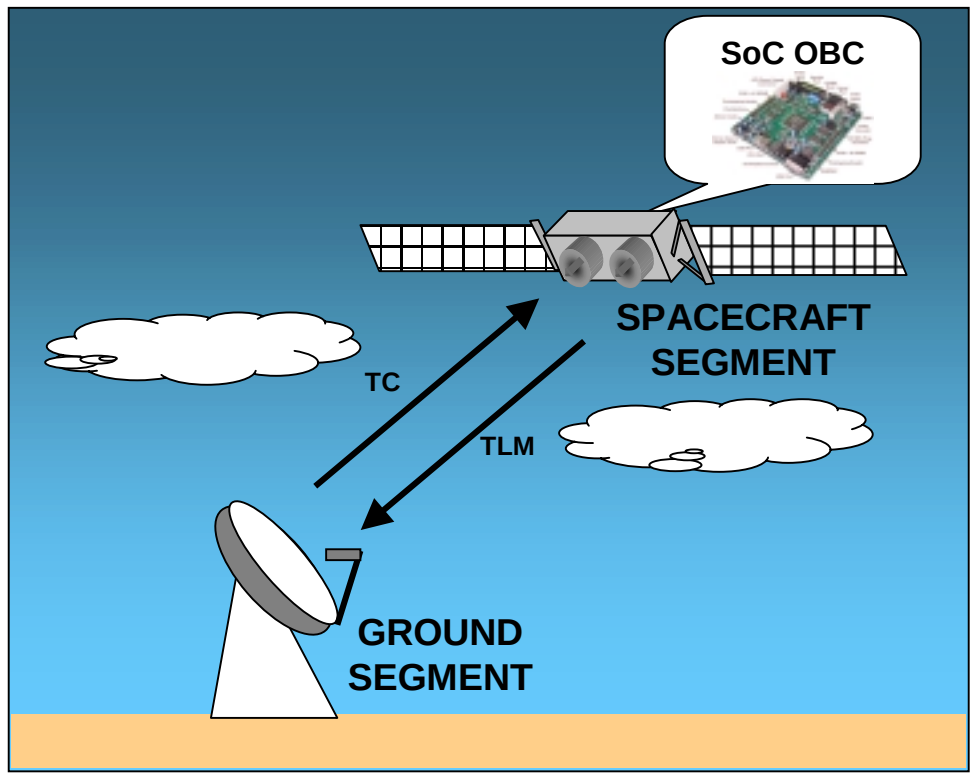
Outline

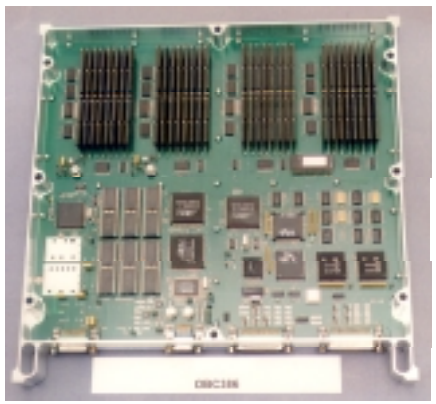
- Introduction
- SoC Research
- System Level Integration
- CCSDS Software Package
- Simulation Experiment
- Conclusions

Objectives

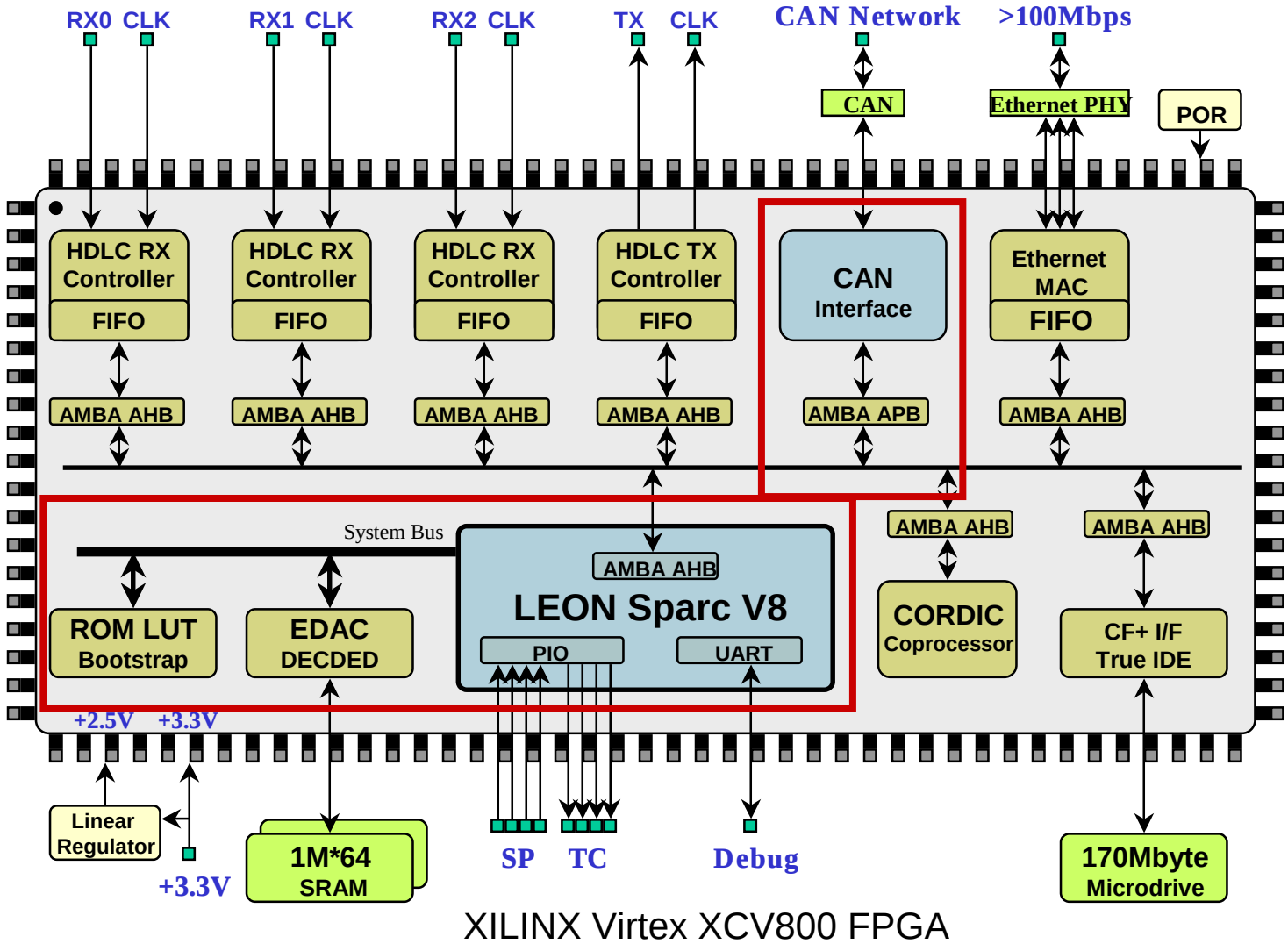
- To implement a ***simplified yet* RELIABLE Consultative Committee of Space Data Systems (CCSDS) *TLM & TC*** space communication system satisfying the needs of a single chip on-board computer (OBC) of a small satellite.
- To simulate the operation of the software on a single-chip OBC prototype.



SoC Research

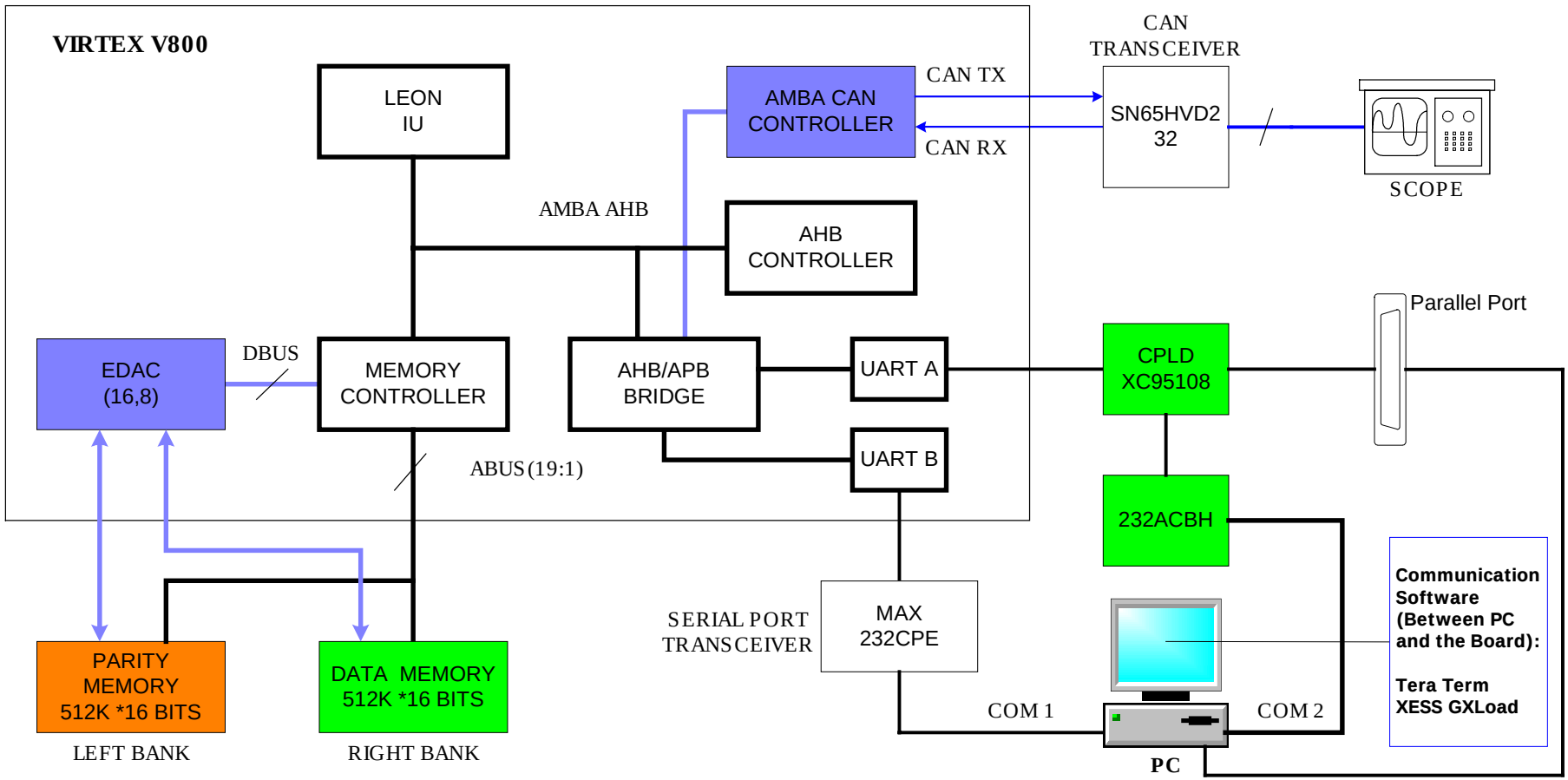


Surrey Satellite Technology (SSTL) On-Board Computer (OBC)



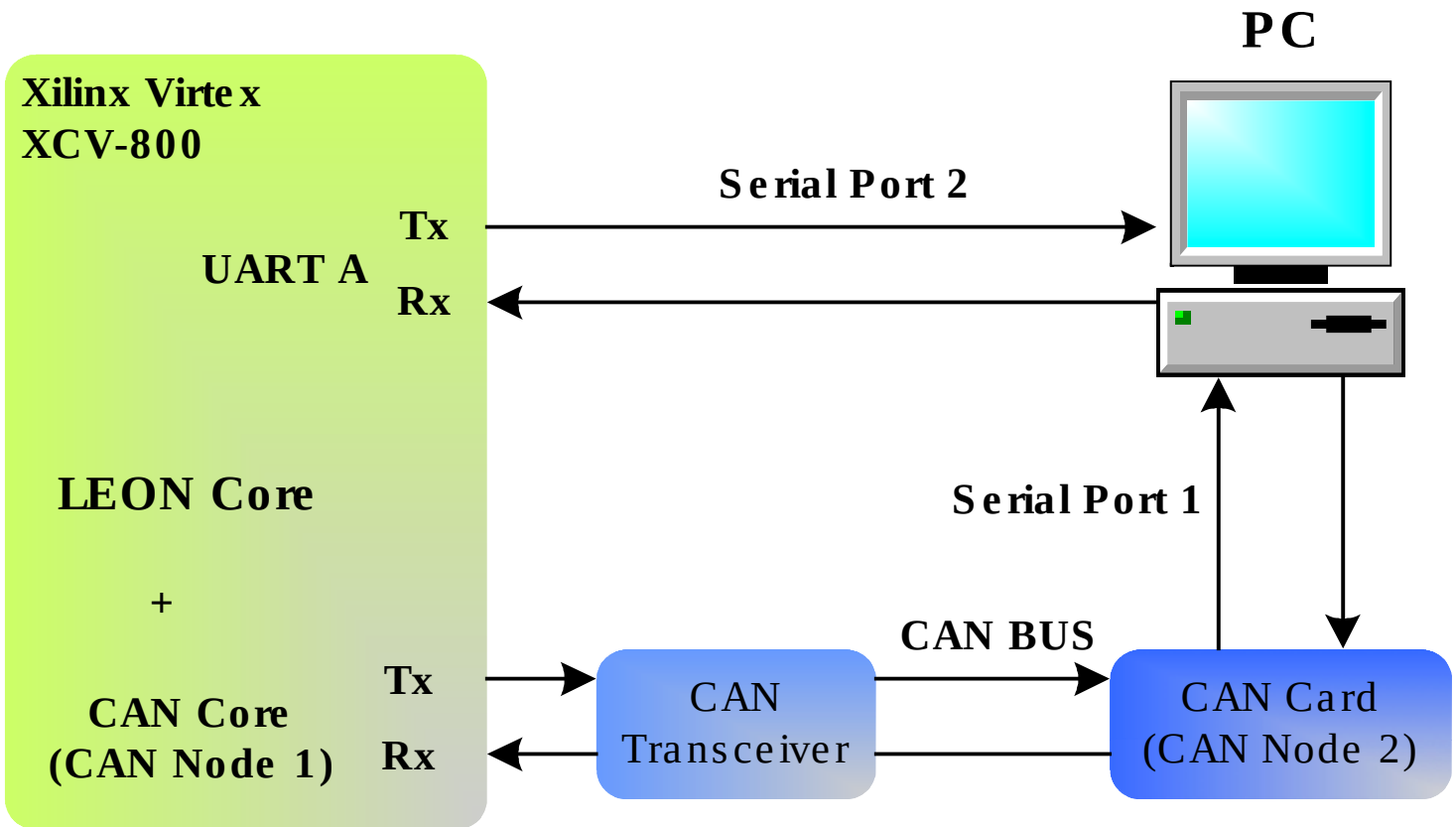
XILINX Virtex XCV800 FPGA

Integration of CAN, EDAC and LEON Processor IP Cores



CAN IP Core - CAN Card

Communication under the Control of the LEON Processor



CAN Core:

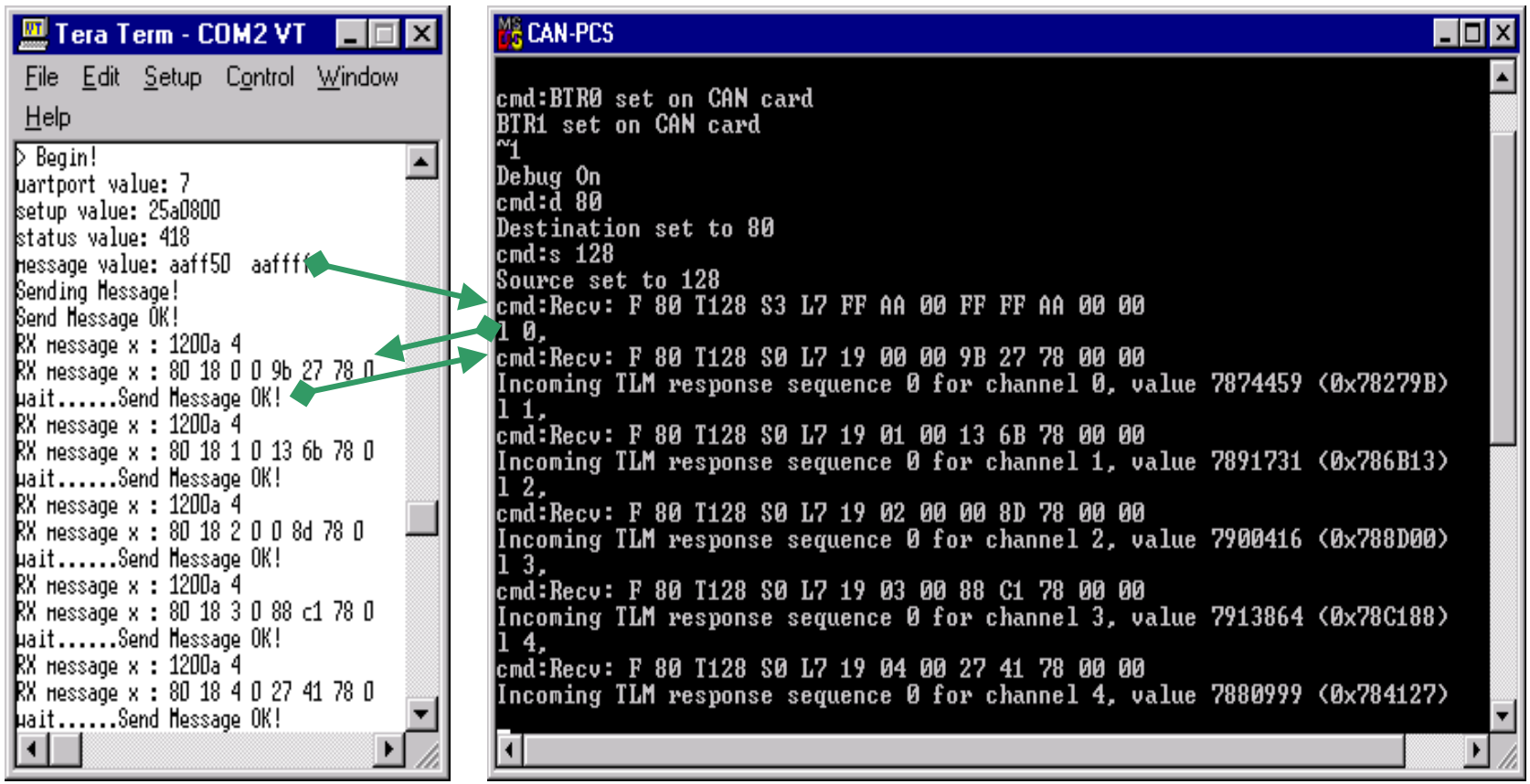
- System Frequency: 25 MHz
- Baud Rate: 312,500 bps

CAN Card:

- System Frequency: 14.7456 MHz
- Baud Rate: 307,197 bps

CAN IP Core - CAN Card

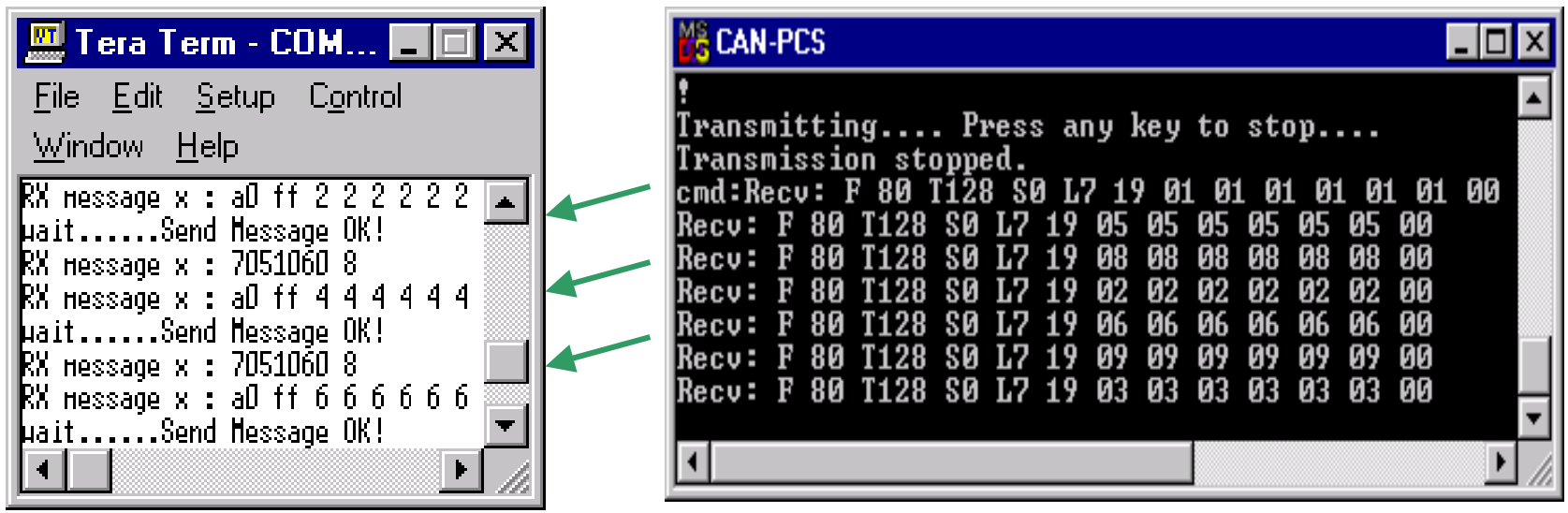
Data Transmission



CAN IP core **CAN Card**

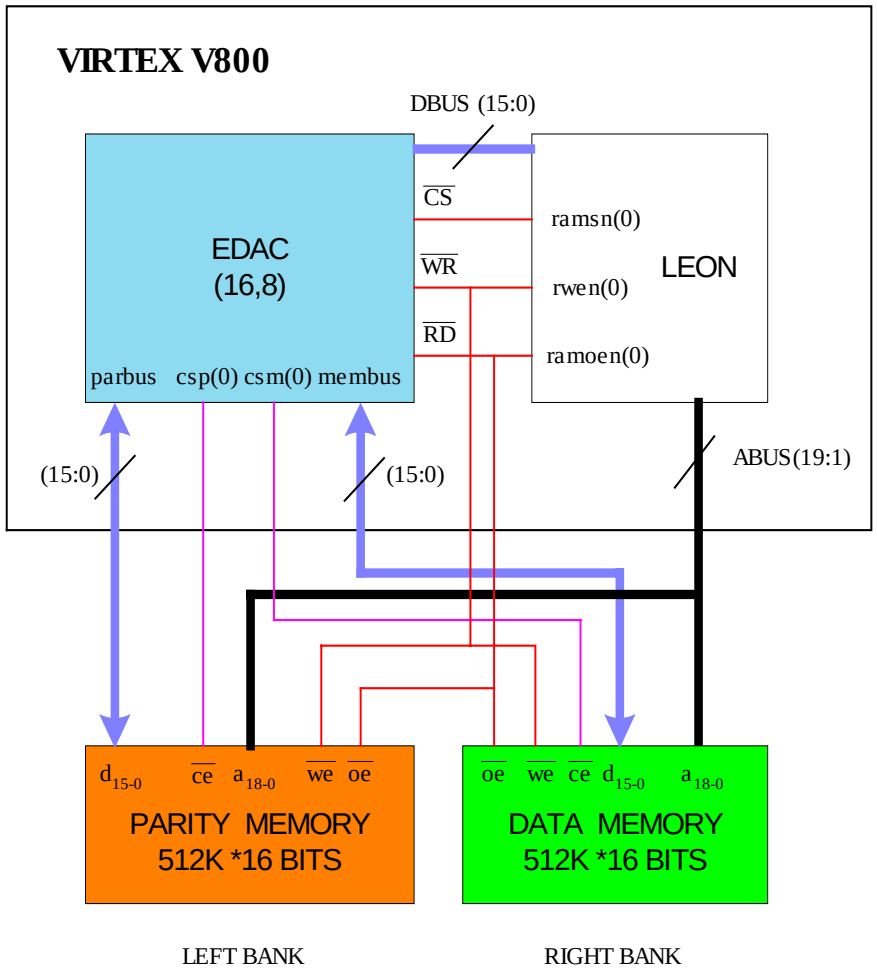
CAN IP Core - CAN Card

High Speed Transmit Test

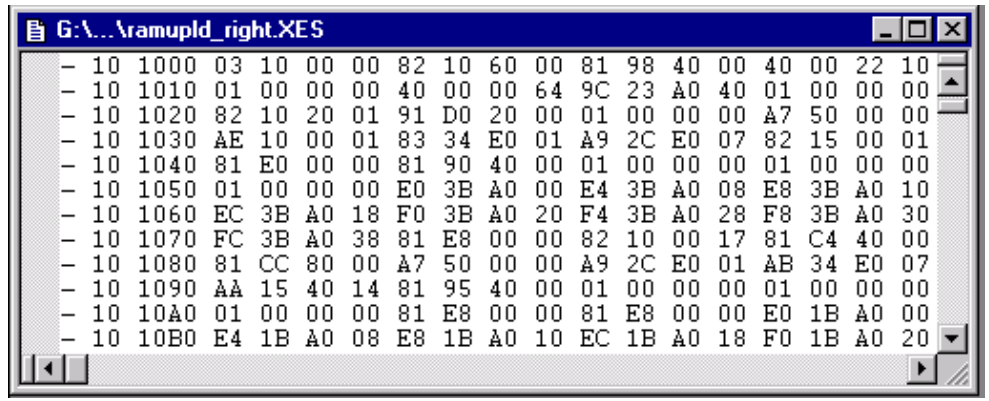


CAN IP Core **CAN Card**

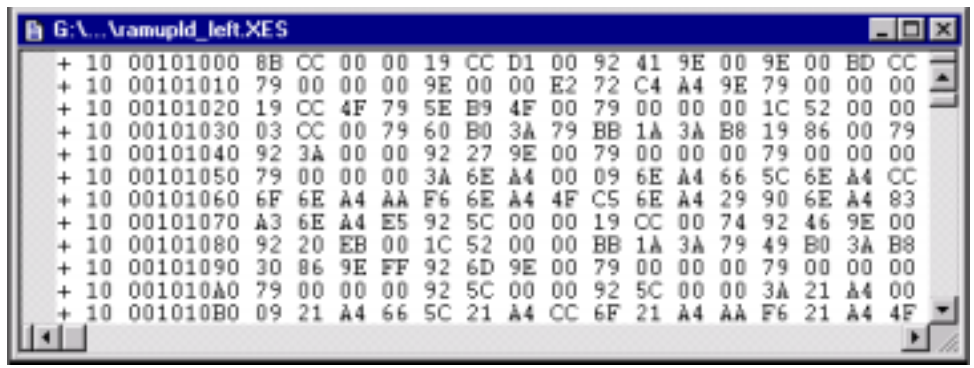
Integration of an EDAC IP Core and the LEON Processor



The EDAC core is integrated with LEON through the system bus.

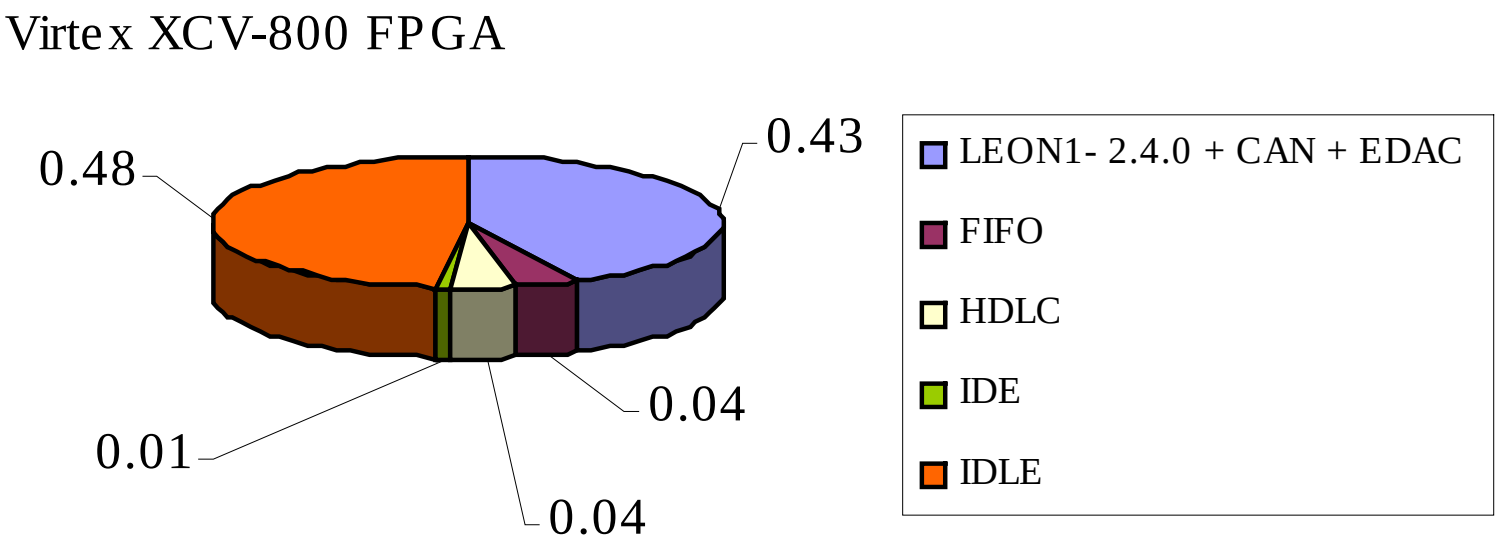


Data Memory – Right Bank



Parity Memory – Left Bank

Synthesis Results
Based on Xilinx Virtex V800



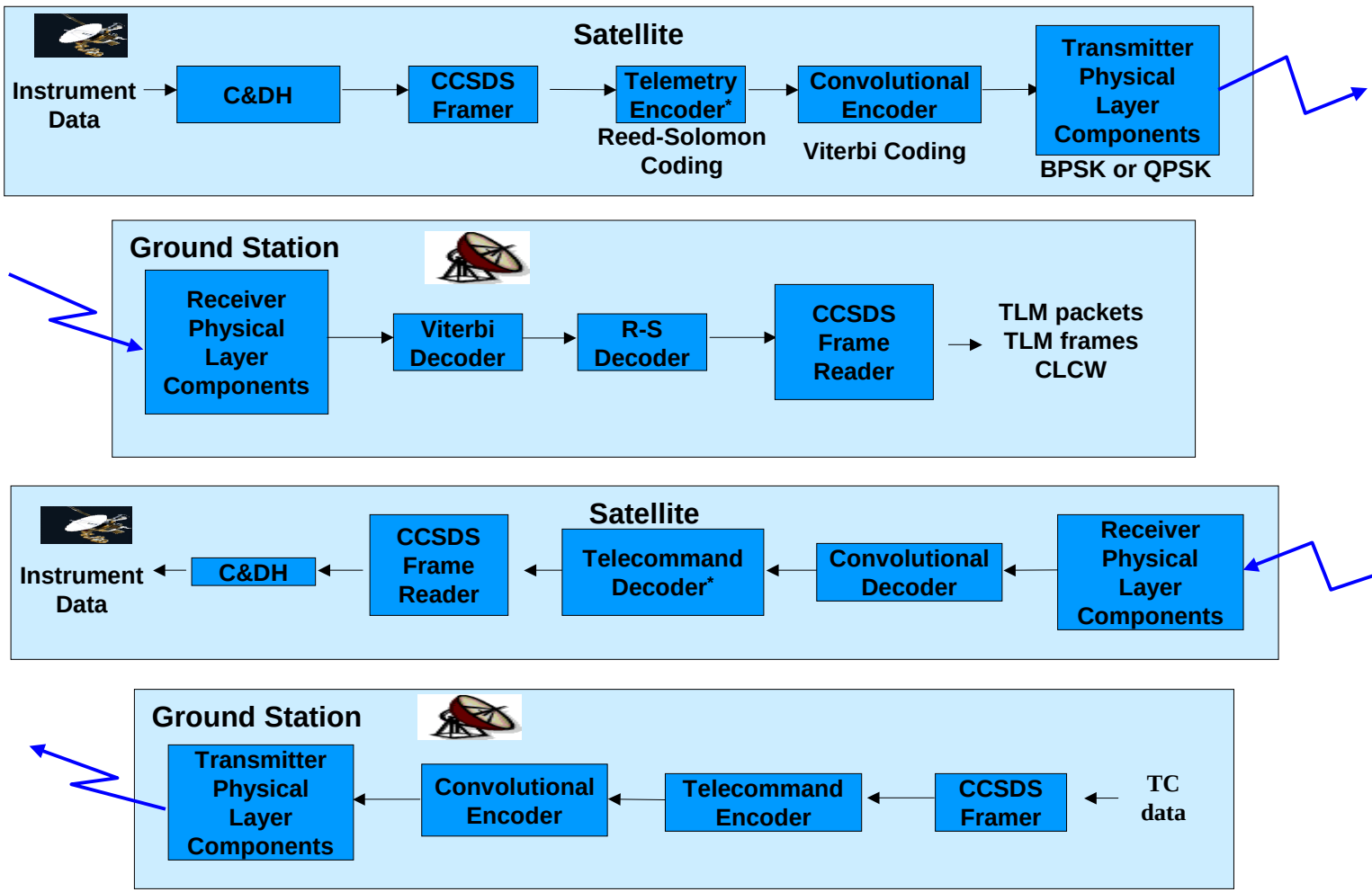
- Synthesis Tool: Synplify 6.0 +
- LEON + CAN + EDAC => 43% of XCV800

Why CCSDS?

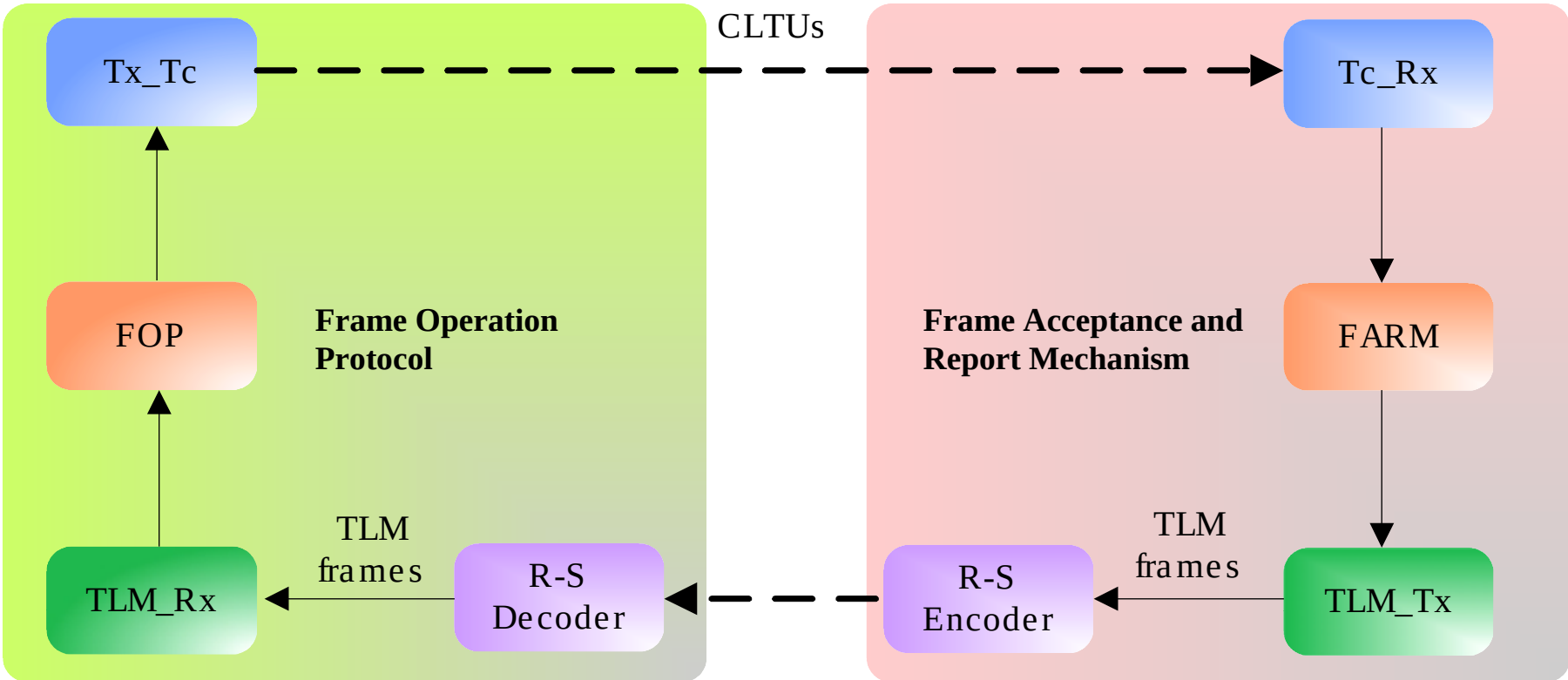
- Standard space industry communication protocol.
- Employed on numerous missions ranging from relatively simple low earth missions to deep space probes.
- Could lead to spacecraft interoperability, re-usable systems and mission cross support – not just for in-house missions but across the CCSDS space agencies members.

CCSDS = Cross Support &Interoperability+STANDARD

CCSDS TC & TLM Data Flow



CCSDS Software Package Structure & Interfaces

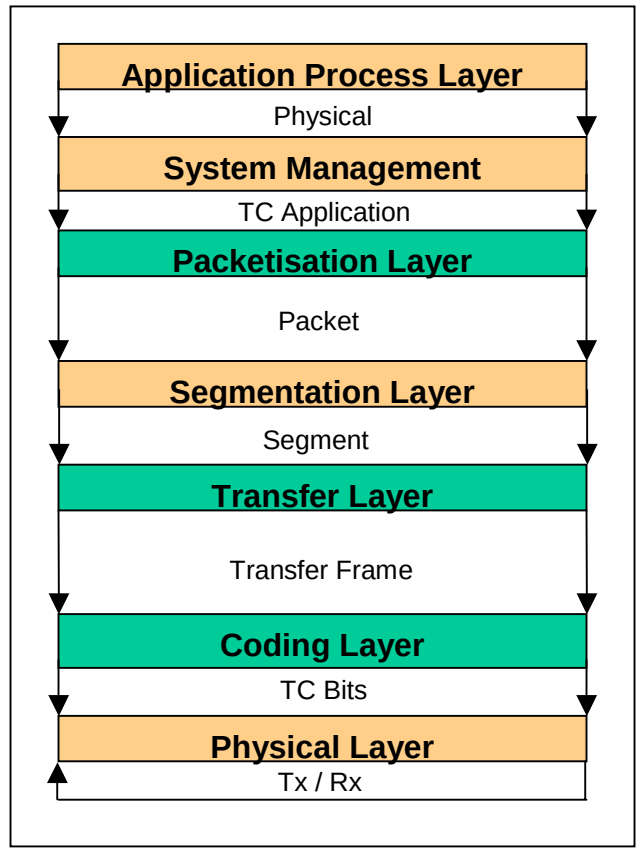


- A simplified software implementation of the CCSDS TLM and TC Command Operation Protocol (COP-1) based on FARM and FOP.
- Both the FARM and FOP systems contain the minimal CCSDS requirements to provide a reliable CCSDS communication system.
- The Reed-Solomon Encoder and Decoder are based on a C code, written by Phil Karn, KA9Q

CCSDS Software Package

- FARM Software Subsystem:
  - Produces the TC frame acceptance for the spacecraft.
  - Develops TC report mechanisms to the FOP via CLCWs (inside TLM frames).
- FOP Software Subsystem:
  - Processes the CLCWs (TLM frame).
  - Transmits or retransmits the TC frames back to the FARM.
- TLM Coding Subsystem:
  - Reed-Solomon Encoder/Decoder.
  - (255, 223) Reed-Solomon Code, E = 16.
  - Field generator polynomial:

    $$F(x) = x^8 + x^7 + x^2 + x + 1.$$
  - Symbol Interleaving: 1.



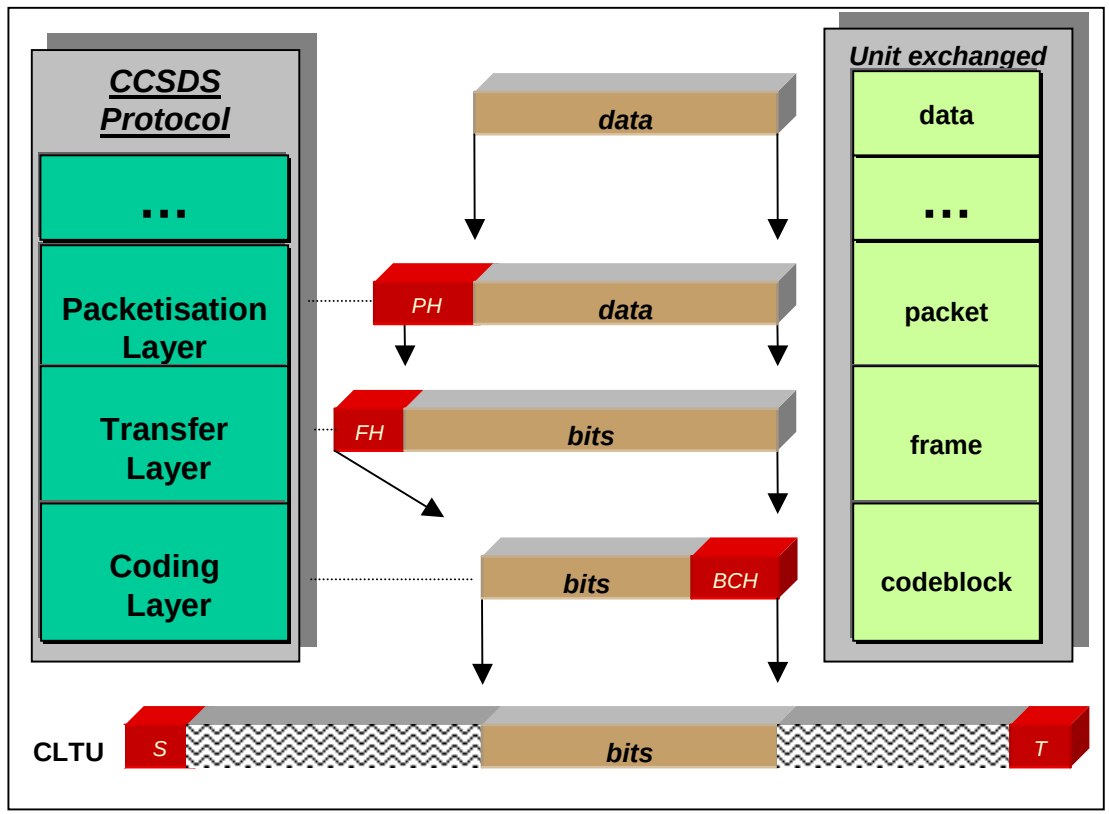
CCSDS Software - TC

CCSDS TC Frame Transmitter:

- Formats the TC packets of length 275 bytes.
- Formats the TC frames of length 280 bytes.
- Calculates the error detection code (BCH).
- Insets the TC packets into the TC frames.
- Inserts the TC frames into Codeblocks.
- Formats the CLTUs.
- Inserts the Codeblocks into the CLTUs.

CCSDS TC Frame Receiver:

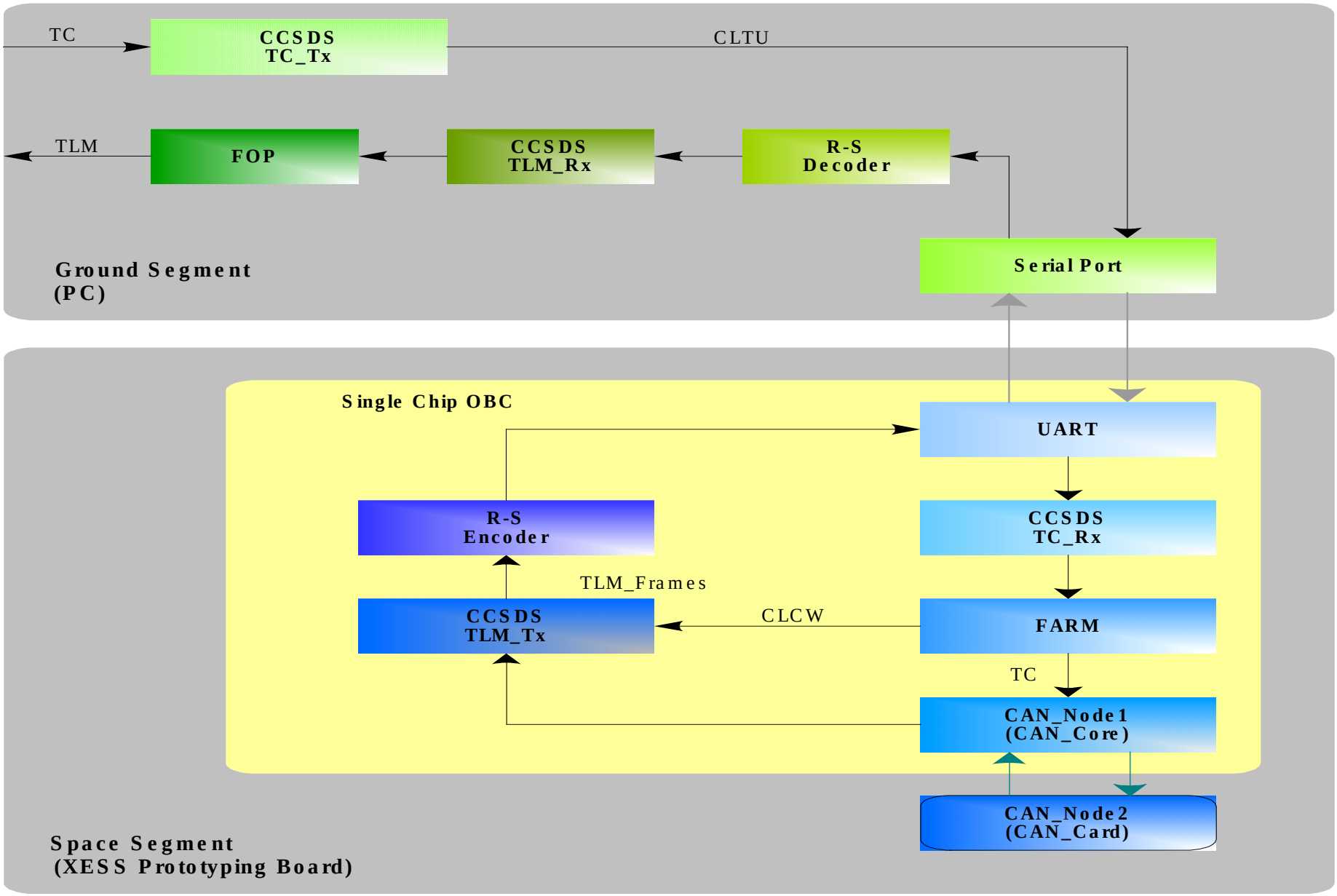
- Subtracts the Codeblocks from the CLTUs.
- Subtracts the TC frames from the Codeblocks.
- Decodes (BCH) the TC frames and TC packets.



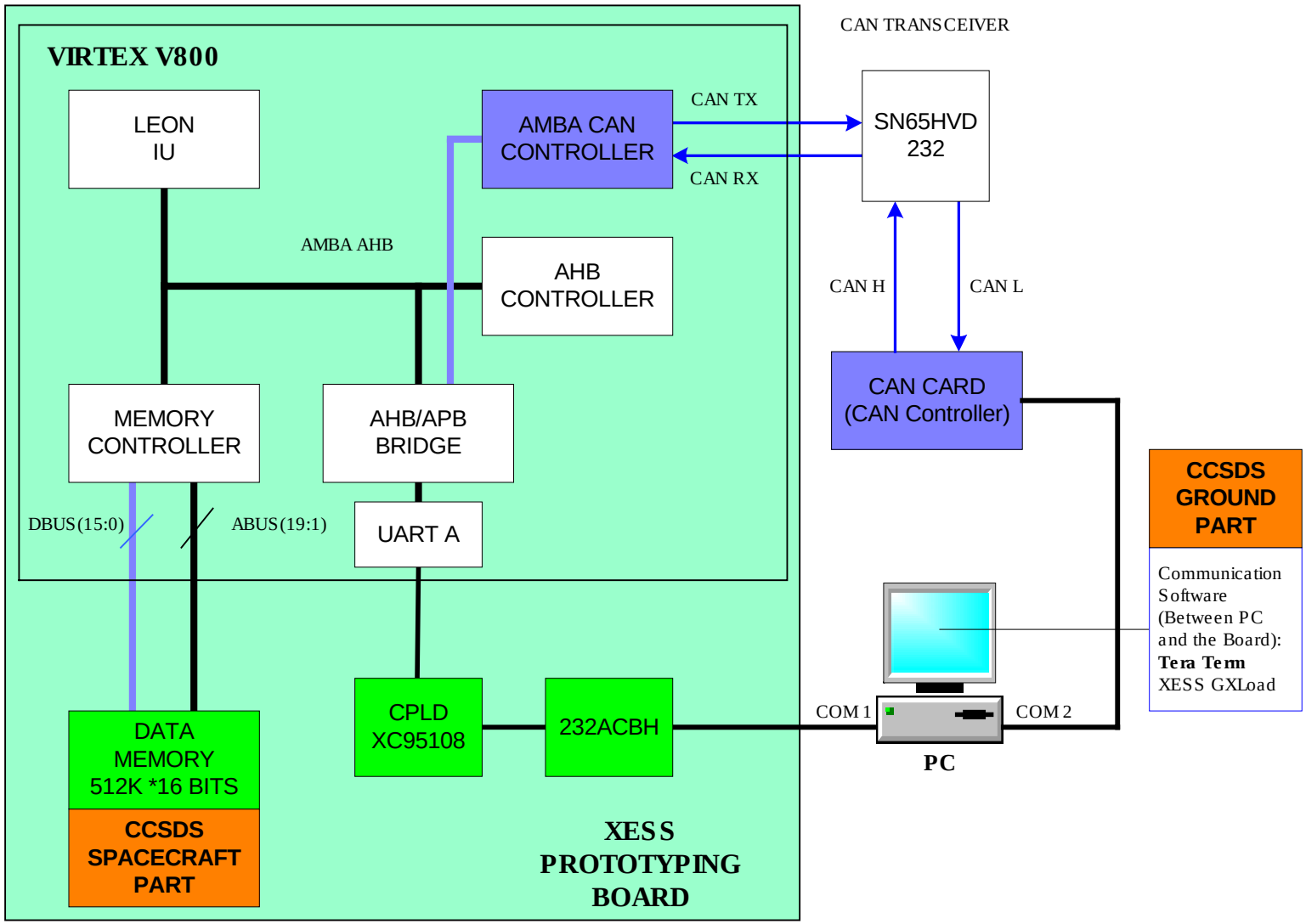
CCSDS Software - TLM

- CCSDS TLM Frame Transmitter (CCSDS TLM_Tx):
  - Formats the TLM packet of length 256 byte.
  - Formats the TLM frame of length 268 bytes.
  - Calculates the CRC of length 2 bytes (included in TLM Frame).
  - Inserts the TLM packets into the TLM frames.
  - Formats the Attached Synchronous Marker (ASM)
  - Transmits the full CCSDS TLM frame.
- CCSDS TLM Frame Receiver (CCSDS TLM_Rx):
  - Decodes the TLM frames (checks the CRC).
  - Subtracts the TLM packets from the TLM frames.
  - Inserts the TLM packet into buffer for future HL usage.

Simulation Scheme

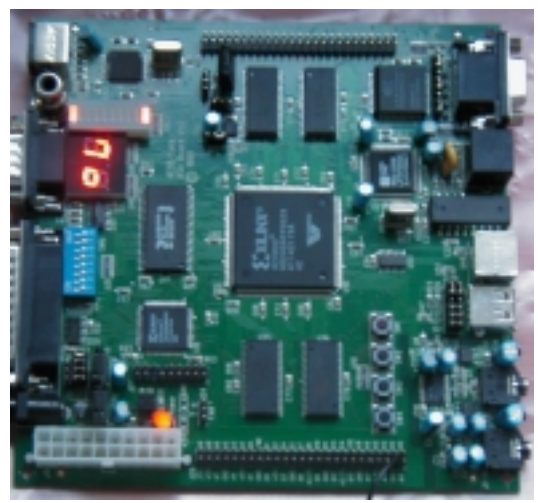


Experimental Setup



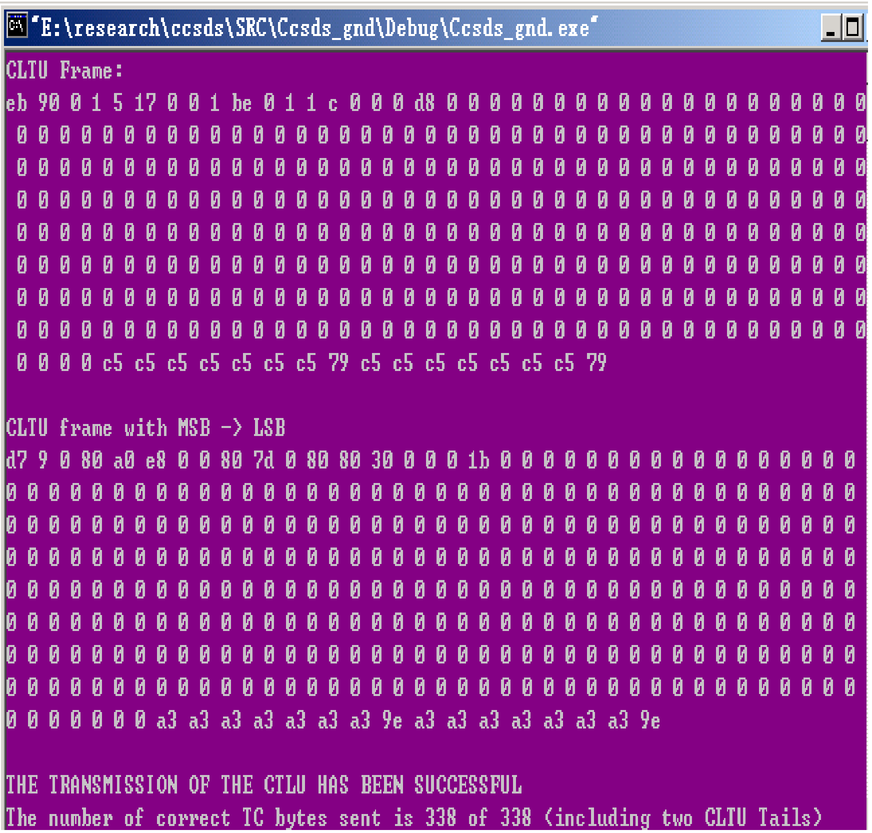
Experimental Setup - Details

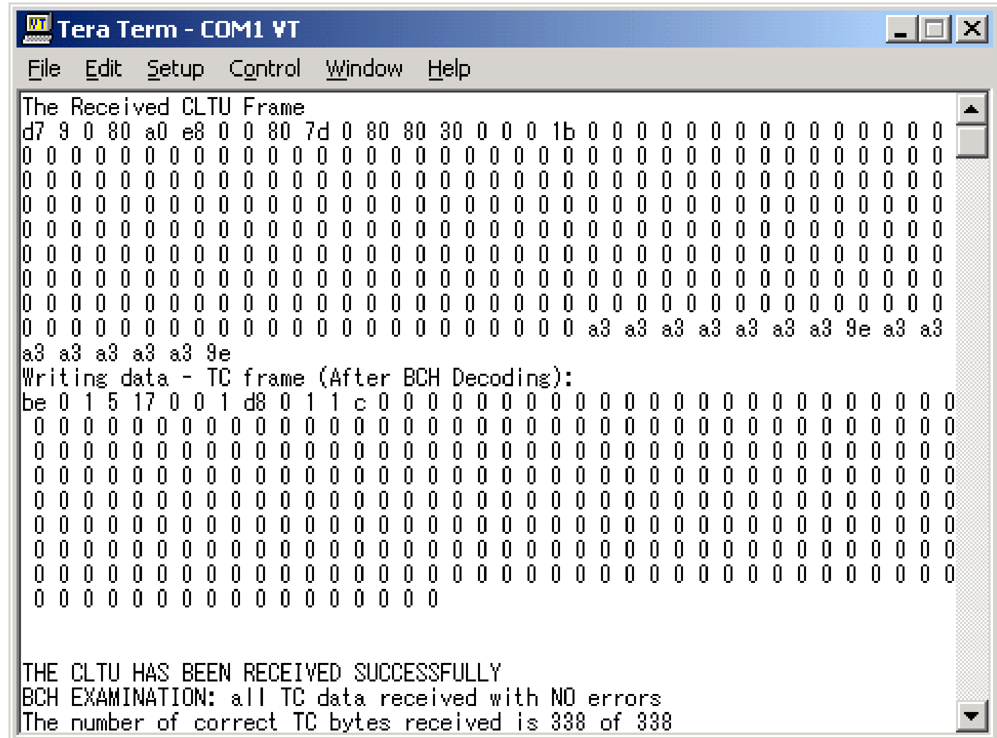
- Processor - LEON 2-1.0.2a VHDL IP core (SPARC V8) (ESA)
  - Working Frequency – 25 MHz
  - UART Baud Rate – 38,400 bps
  - Internal S-Record Boot Loader
- On-Board Network (Node 1) - HurriCANe VHDL IP core (ESA)
  - Baud Rate: 312,500 bps
- EDAC – EDAC VHDL IP core (SSTL)
  - Double-bit correcting Quasi-Cyclic (16,8) shortened EDAC code
- Prototyping Board - XESS XSV800 (Xilinx Virtex 800 FPGAs)
  - Up to 100 MHz programmable oscillator
  - 16M Bits SRAM (Two banks - 512K x 16)
  - 16M Bits flash RAM
- On-Board Application Program – S-Record File
  - 160K Bytes (CCSDS_SC Software Package)



Simulation Results

Transmission of a CLTU TC Frame from TC_Tx to TC_Rx

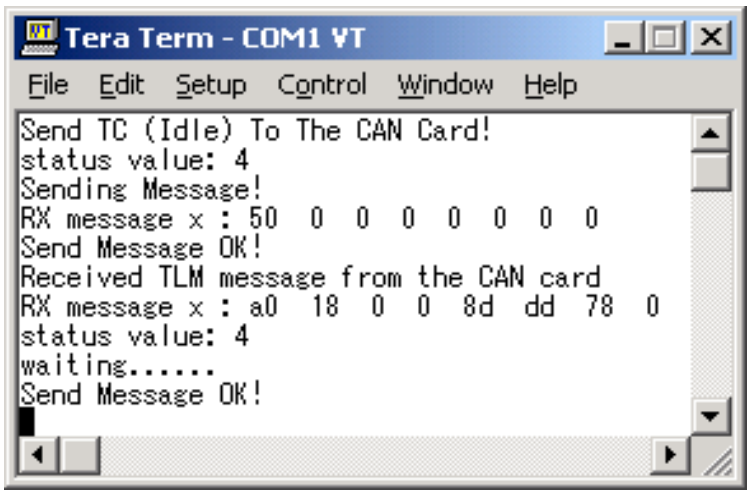


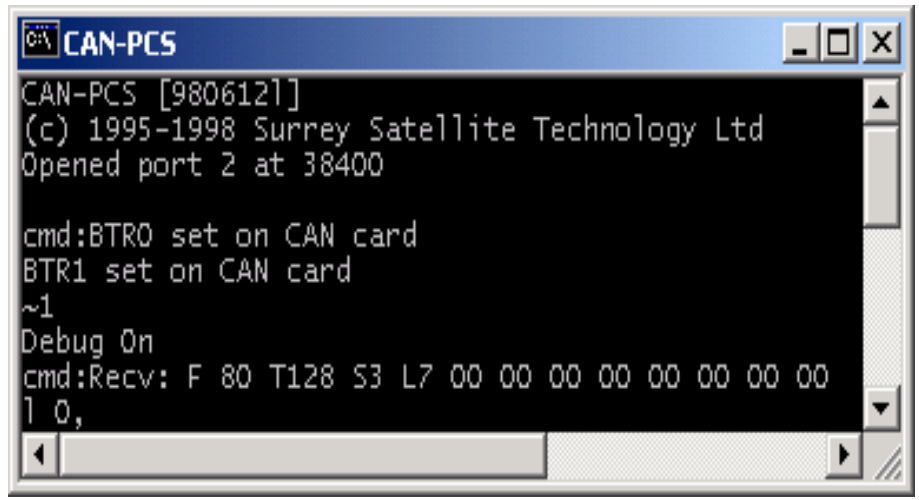


Ground Segment (PC) → Spacecraft Segment (OBC)

Simulation Results

Transmission of TC & TLM between the CAN Core and the CAN Card

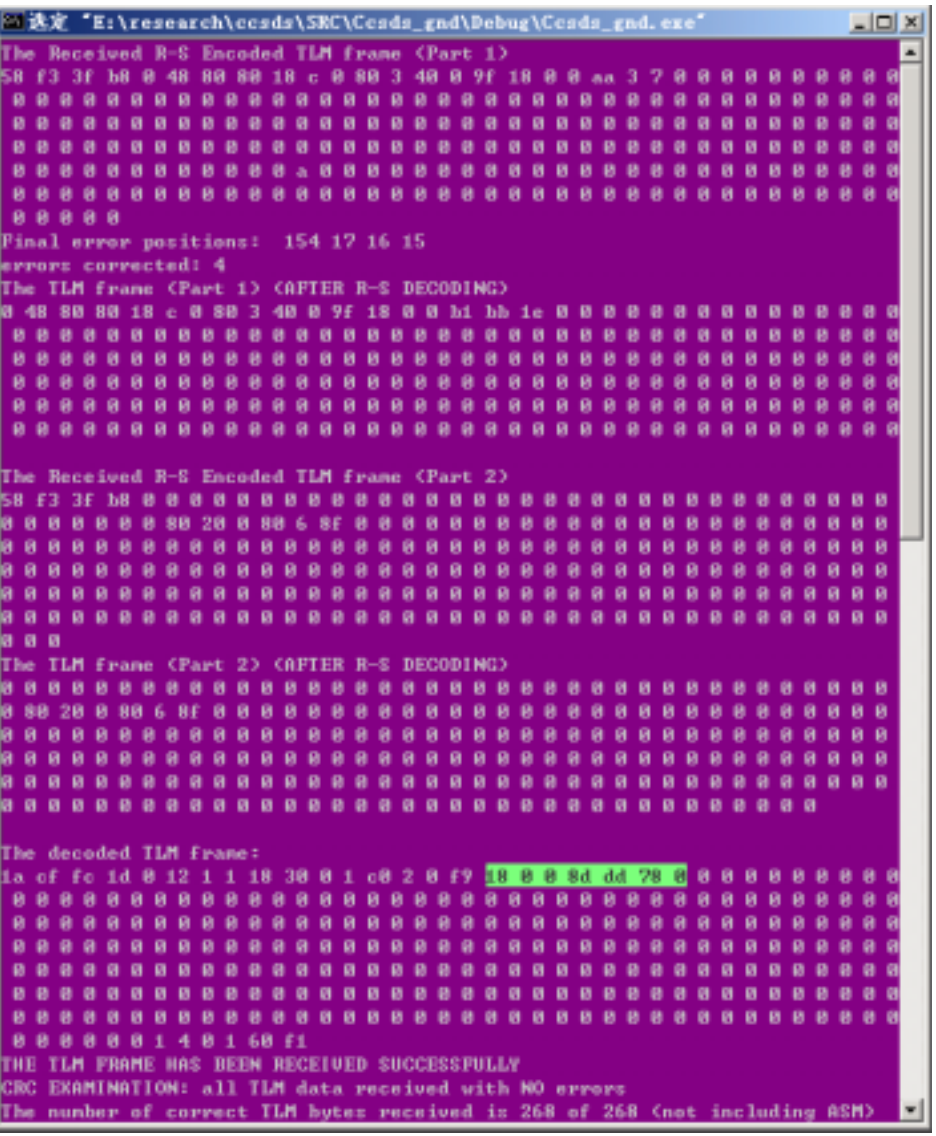


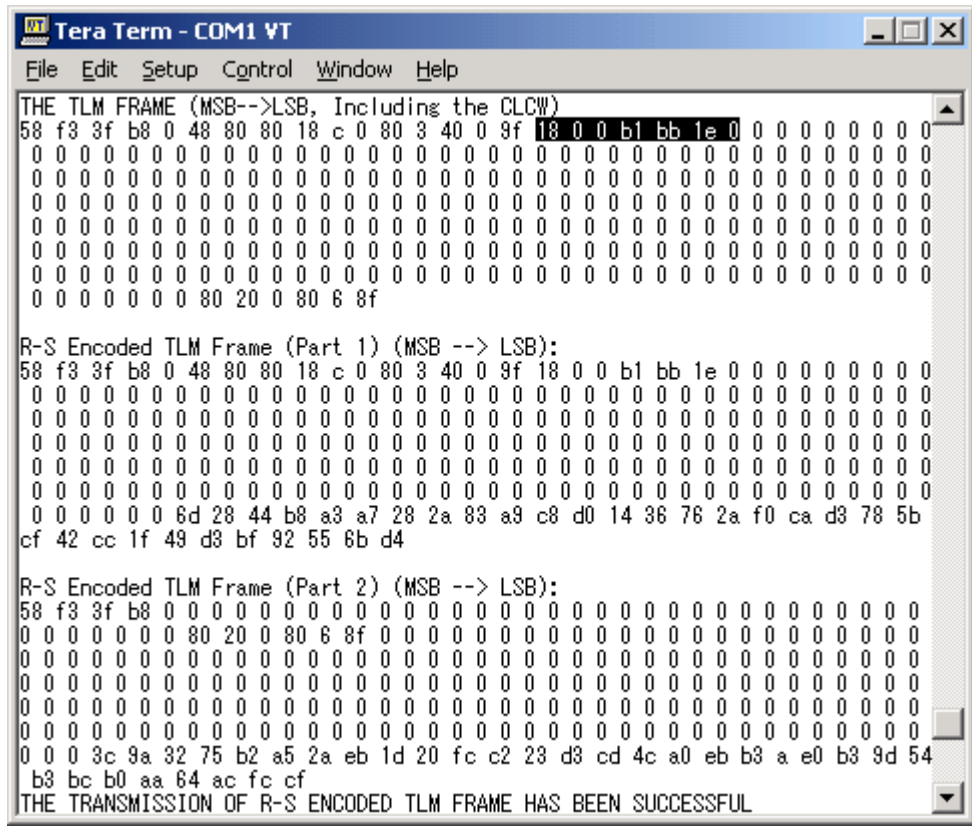


CAN IP Core - CAN Node 1 (OBC) ⟺ CAN Card - CAN Node 2 (Payload)

Simulation Results

Transmission of a TLM Frame from TLM_Tx to TLM_Rx





Ground Segment (PC) ⟸ Spacecraft Segment (OBC)

Conclusions

- A simplified, yet reliable, standalone software implementation of the CCSDS protocol has been developed.
- The CCSDS software package features a modular structure which can facilitate easy expansions of functionality to suit specific mission requirements.
- The software imposes minimal memory footprint and performance requirements on the OBC.
- The functionality of the package has been verified via simulation using a single-chip OBC subsystem prototyped in a high density FPGA.
- The CCSDS software supported by a single-chip OBC and a thin-layer hardware interface can provide a cost effective and flexible communication solution for low-cost small satellites.
- The availability of a communication system, specifically designed to meet the needs of a single-chip OBC, will facilitate further research in miniaturisation of small satellites.