



A CCSDS-Based Communication System for a Single Chip On-Board Computer

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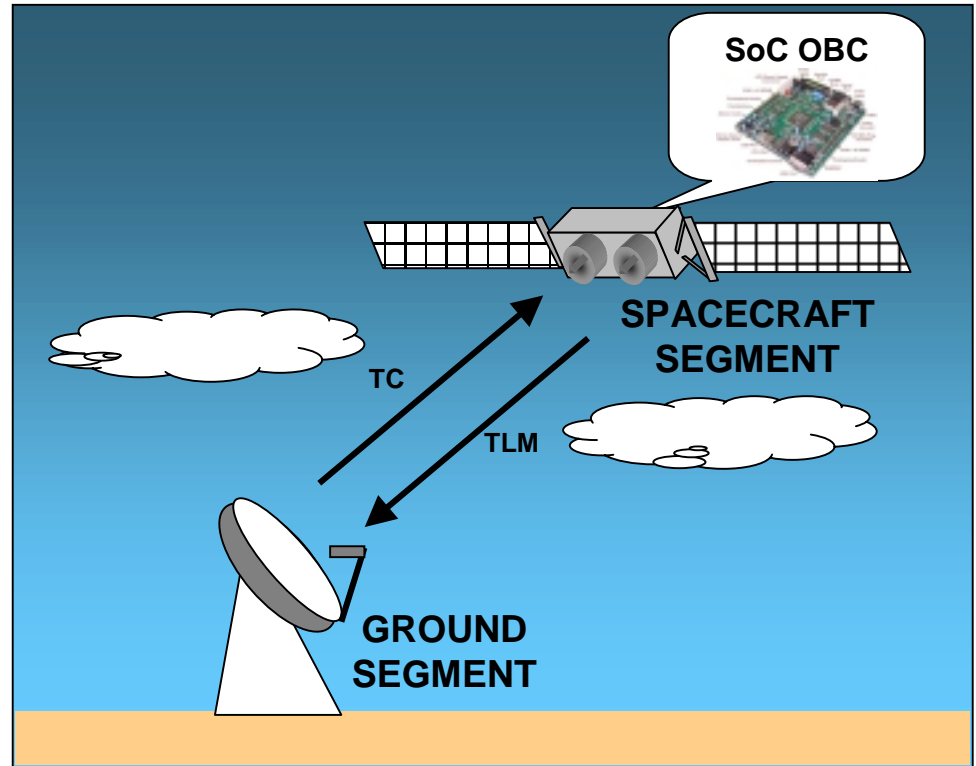
Outline

- Introduction
- SoC Research
- System Level Integration
- CCSDS Software Package
- Simulation Experiment
- Conclusions



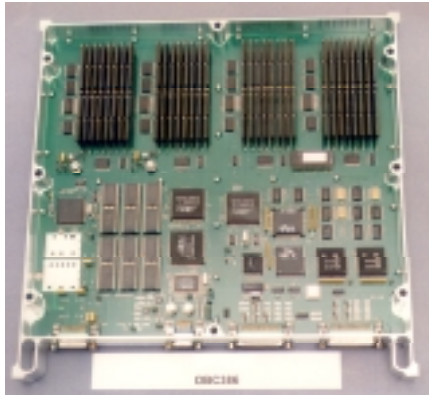
Objectives

- To implement a *simplified yet RELIABLE Consultative Committee of Space Data Systems (CCSDS) TLM & TC* space communication system satisfying the needs of a single chip on-board computer (OBC) of a small satellite.
- To simulate the operation of the software on a single-chip OBC prototype.

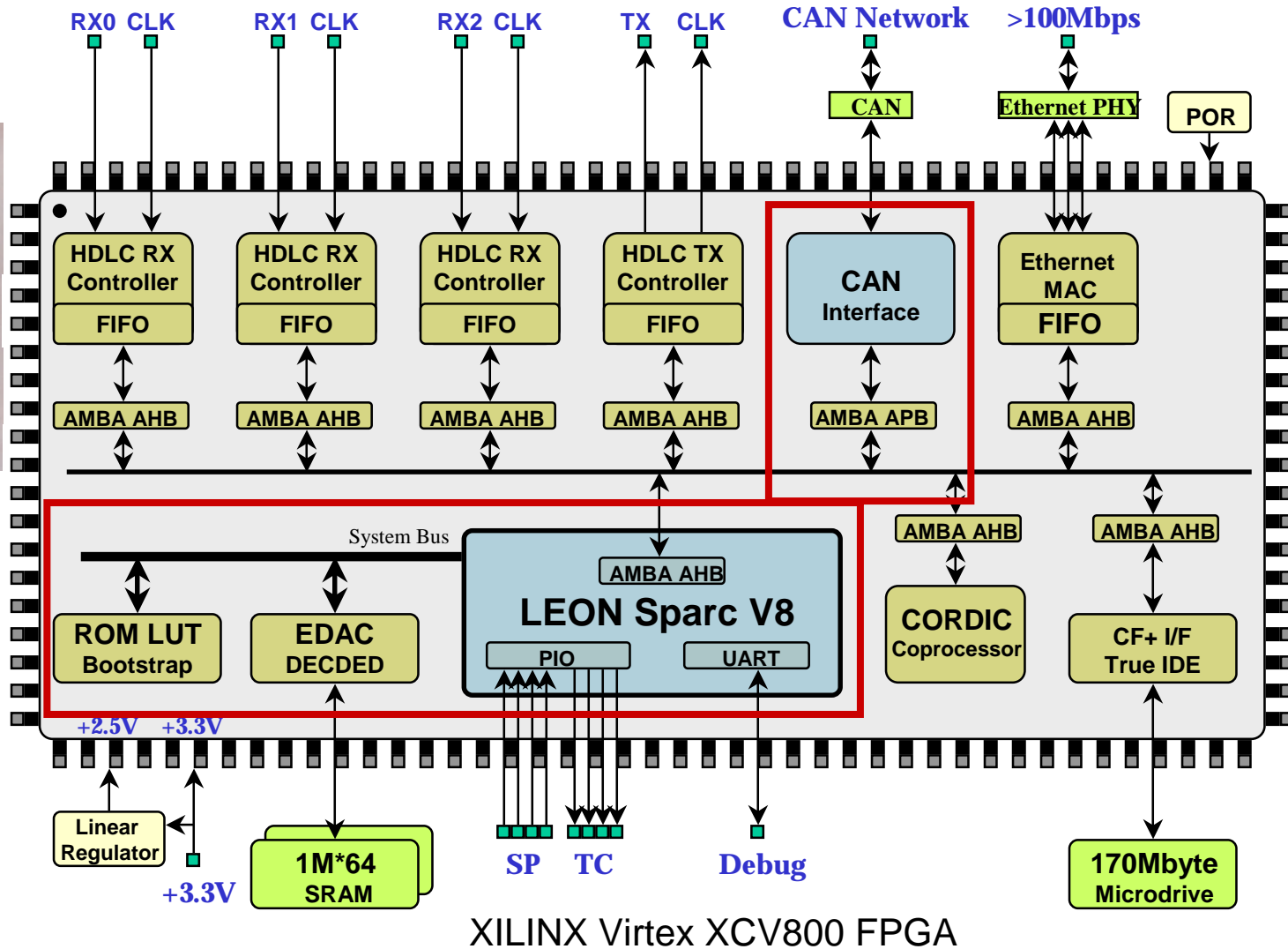




SoC Research

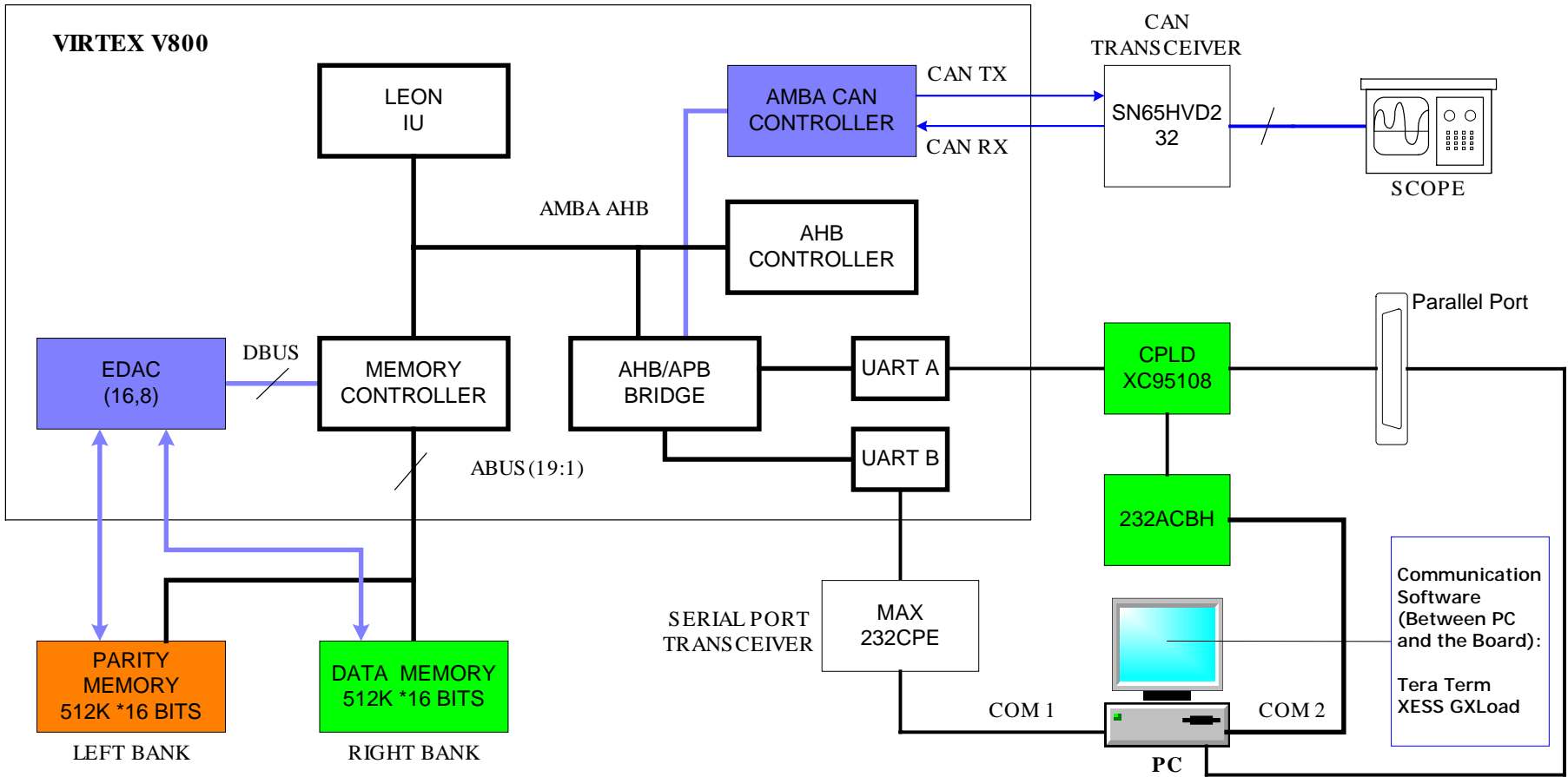


Surrey Satellite Technology (SSTL) On-Board Computer (OBC)





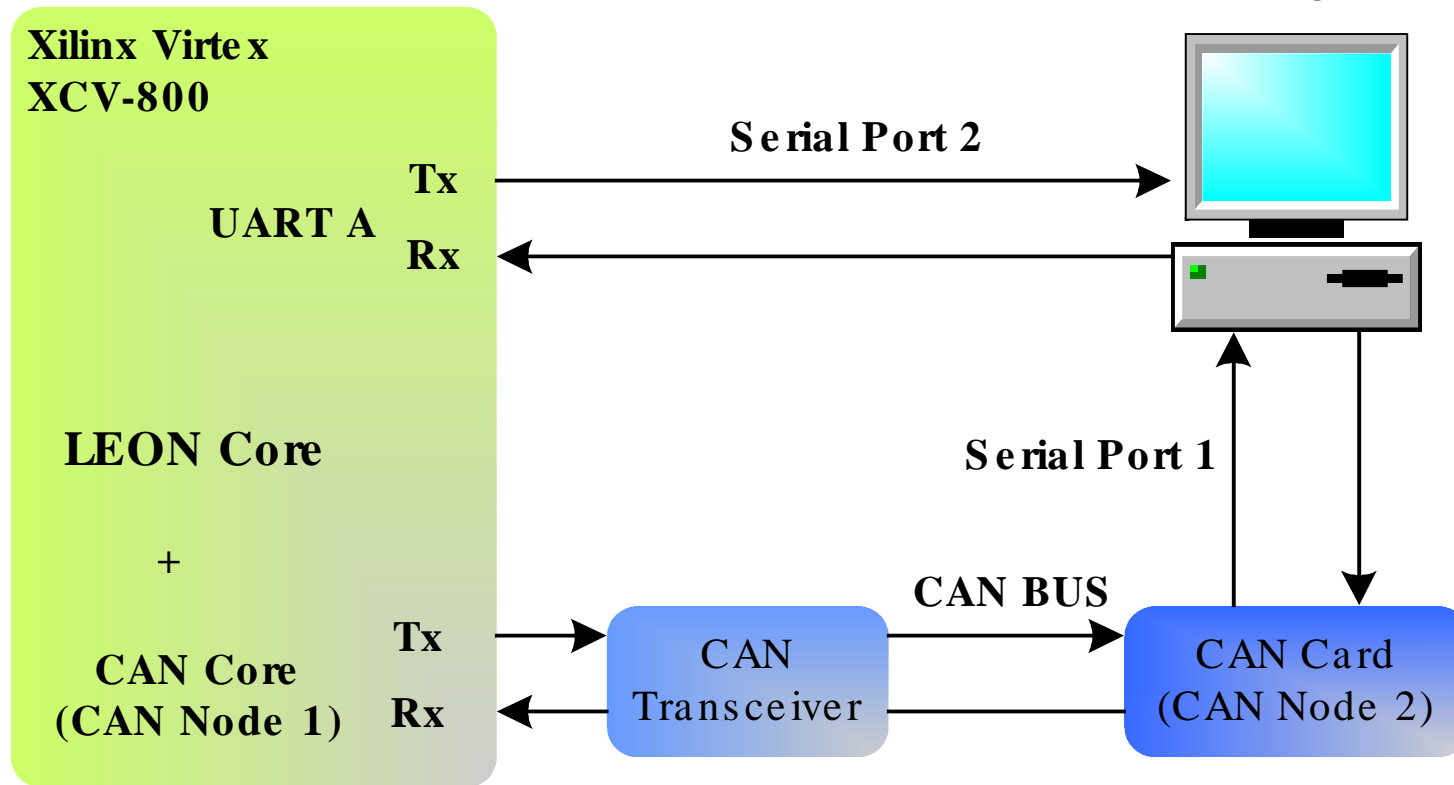
Integration of CAN, EDAC and LEON Processor IP Cores





CAN IP Core - CAN Card

Communication under the Control of the LEON Processor



CAN Core:

- System Frequency: 25 MHz
- Baud Rate: 312,500 bps

CAN Card:

- System Frequency: 14.7456 MHz
- Baud Rate: 307,197 bps



CAN IP Core - CAN Card

Data Transmission

```

Tera Term - COM2 VT
File Edit Setup Control Window
Help
> Begin!
uartport value: 7
setup value: 25a0800
status value: 418
message value: aaff50 aaffff
Sending Message!
Send Message OK!
RX message x : 1200a 4
RX message x : 80 18 0 0 9b 27 78 0
wait.....Send Message OK!
RX message x : 1200a 4
RX message x : 80 18 1 0 13 6b 78 0
wait.....Send Message OK!
RX message x : 1200a 4
RX message x : 80 18 2 0 0 8d 78 0
wait.....Send Message OK!
RX message x : 1200a 4
RX message x : 80 18 3 0 88 c1 78 0
wait.....Send Message OK!
RX message x : 1200a 4
RX message x : 80 18 4 0 27 41 78 0
wait.....Send Message OK!
  
```

CAN IP core

```

CAN-PCS
cmd:BTR0 set on CAN card
BTR1 set on CAN card
^1
Debug On
cmd:d 80
Destination set to 80
cmd:s 128
Source set to 128
cmd:Recv: F 80 T128 S3 L7 FF AA 00 FF FF AA 00 00
l 0,
cmd:Recv: F 80 T128 S0 L7 19 00 00 9B 27 78 00 00
Incoming TLM response sequence 0 for channel 0, value 7874459 (0x78279B)
l 1,
cmd:Recv: F 80 T128 S0 L7 19 01 00 00 13 6B 78 00 00
Incoming TLM response sequence 0 for channel 1, value 7891731 (0x786B13)
l 2,
cmd:Recv: F 80 T128 S0 L7 19 02 00 00 8D 78 00 00
Incoming TLM response sequence 0 for channel 2, value 7900416 (0x788D00)
l 3,
cmd:Recv: F 80 T128 S0 L7 19 03 00 00 88 C1 78 00 00
Incoming TLM response sequence 0 for channel 3, value 7913864 (0x78C188)
l 4,
cmd:Recv: F 80 T128 S0 L7 19 04 00 00 27 41 78 00 00
Incoming TLM response sequence 0 for channel 4, value 7880999 (0x784127)
  
```

CAN Card



CAN IP Core - CAN Card

High Speed Transmit Test

```
Tera Term - COM...  
File Edit Setup Control  
Window Help  
RX message x : a0 ff 2 2 2 2 2 2  
wait.....Send Message OK!  
RX message x : 7051060 8  
RX message x : a0 ff 4 4 4 4 4 4  
wait.....Send Message OK!  
RX message x : 7051060 8  
RX message x : a0 ff 6 6 6 6 6 6  
wait.....Send Message OK!
```

CAN IP Core

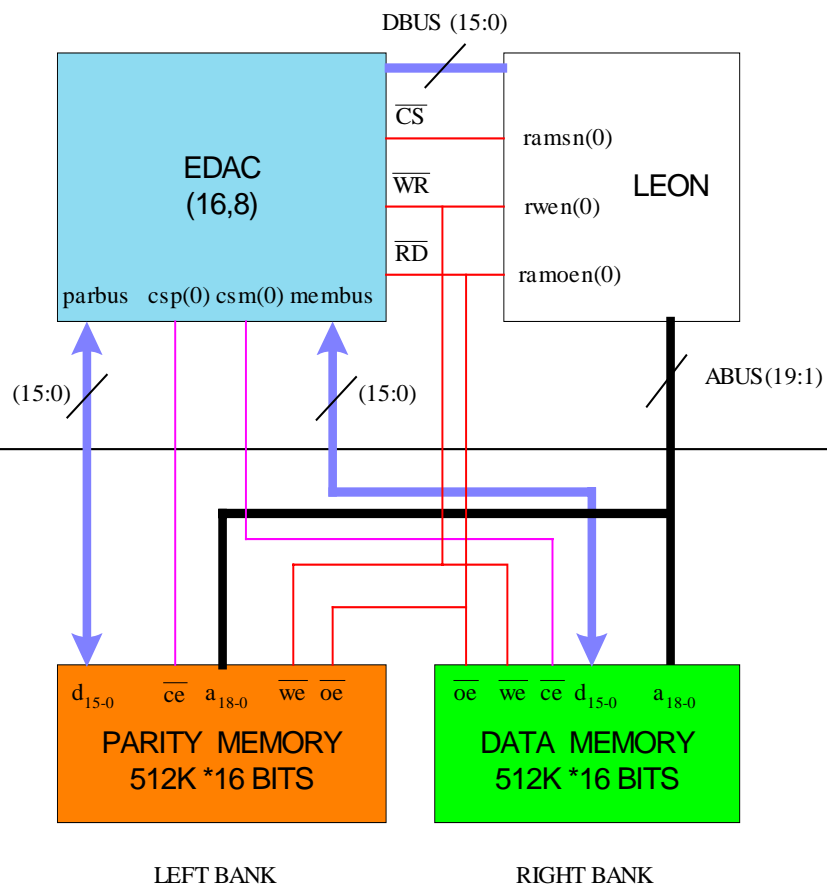
```
MS-DOS CAN-PCS  
?  
Transmitting.... Press any key to stop....  
Transmission stopped.  
cmd:Recv: F 80 T128 S0 L7 19 01 01 01 01 01 01 00  
Recv: F 80 T128 S0 L7 19 05 05 05 05 05 05 00  
Recv: F 80 T128 S0 L7 19 08 08 08 08 08 08 00  
Recv: F 80 T128 S0 L7 19 02 02 02 02 02 02 00  
Recv: F 80 T128 S0 L7 19 06 06 06 06 06 06 00  
Recv: F 80 T128 S0 L7 19 09 09 09 09 09 09 00  
Recv: F 80 T128 S0 L7 19 03 03 03 03 03 03 00
```

CAN Card



Integration of an EDAC IP Core and the LEON Processor

VIRTEX V800



The EDAC core is integrated with LEON through the system bus.

```

G:\...ramupld_right.XES
- 10 1000 03 10 00 00 82 10 60 00 81 98 40 00 40 00 22 10
- 10 1010 01 00 00 00 40 00 00 64 9C 23 A0 40 01 00 00 00
- 10 1020 82 10 20 01 91 D0 20 00 01 00 00 00 A7 50 00 00
- 10 1030 AE 10 00 01 83 34 E0 01 A9 2C E0 07 82 15 00 01
- 10 1040 81 E0 00 00 81 90 40 00 01 00 00 00 01 00 00 00
- 10 1050 01 00 00 00 E0 3B A0 00 E4 3B A0 08 E8 3B A0 10
- 10 1060 EC 3B A0 18 F0 3B A0 20 F4 3B A0 28 F8 3B A0 30
- 10 1070 FC 3B A0 38 81 E8 00 00 82 10 00 17 81 C4 40 00
- 10 1080 81 CC 80 00 A7 50 00 00 A9 2C E0 01 AB 34 E0 07
- 10 1090 AA 15 40 14 81 95 40 00 01 00 00 00 01 00 00 00
- 10 10A0 01 00 00 00 81 E8 00 00 81 E8 00 00 E0 1B A0 00
- 10 10B0 E4 1B A0 08 E8 1B A0 10 EC 1B A0 18 F0 1B A0 20

```

Data Memory – Right Bank

```

G:\...ramupld_left.XES
+ 10 00101000 8B CC 00 00 19 CC D1 00 92 41 9E 00 9E 00 BD CC
+ 10 00101010 79 00 00 00 9E 00 00 E2 72 C4 A4 9E 79 00 00 00
+ 10 00101020 19 CC 4F 79 5E B9 4F 00 79 00 00 00 1C 52 00 00
+ 10 00101030 03 CC 00 79 60 B0 3A 79 BB 1A 3A B8 19 86 00 79
+ 10 00101040 92 3A 00 00 92 27 9E 00 79 00 00 00 79 00 00 00
+ 10 00101050 79 00 00 00 3A 6E A4 00 09 6E A4 66 5C 6E A4 CC
+ 10 00101060 6F 6E A4 AA F6 6E A4 4F C5 6E A4 29 90 6E A4 83
+ 10 00101070 A3 6E A4 E5 92 5C 00 00 19 CC 00 74 92 46 9E 00
+ 10 00101080 92 20 EB 00 1C 52 00 00 BB 1A 3A 79 49 B0 3A B8
+ 10 00101090 30 86 9E FF 92 6D 9E 00 79 00 00 00 79 00 00 00
+ 10 001010A0 79 00 00 00 92 5C 00 00 92 5C 00 00 3A 21 A4 00
+ 10 001010B0 09 21 A4 66 5C 21 A4 CC 6F 21 A4 AA F6 21 A4 4F

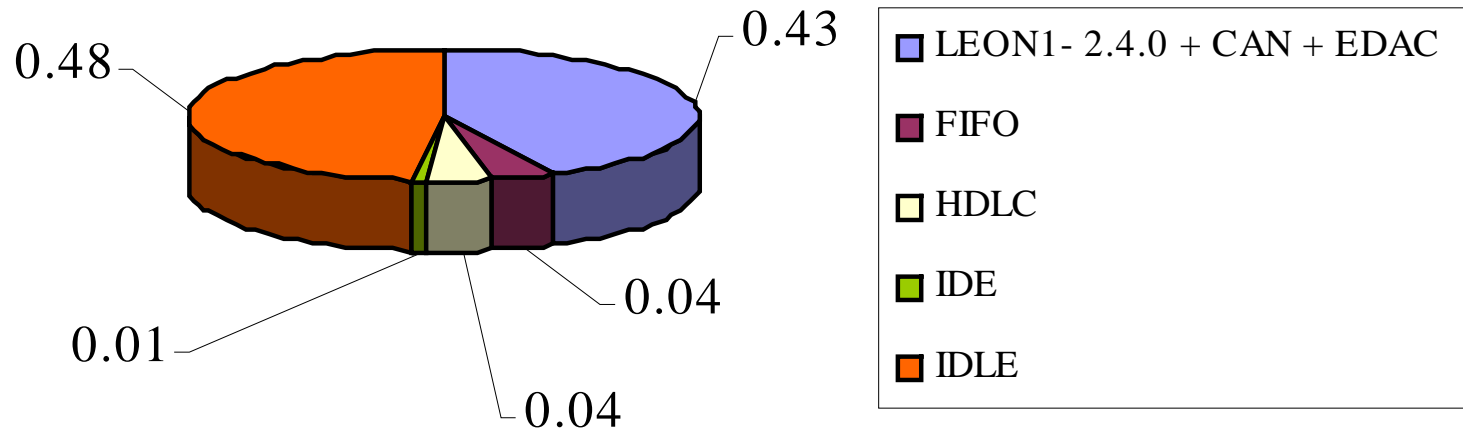
```

Parity Memory – Left Bank



Synthesis Results Based on Xilinx Virtex V800

Virtex XCV-800 FPGA



- Synthesis Tool: Synplify 6.0 +
- LEON + CAN + EDAC => 43% of XCV800



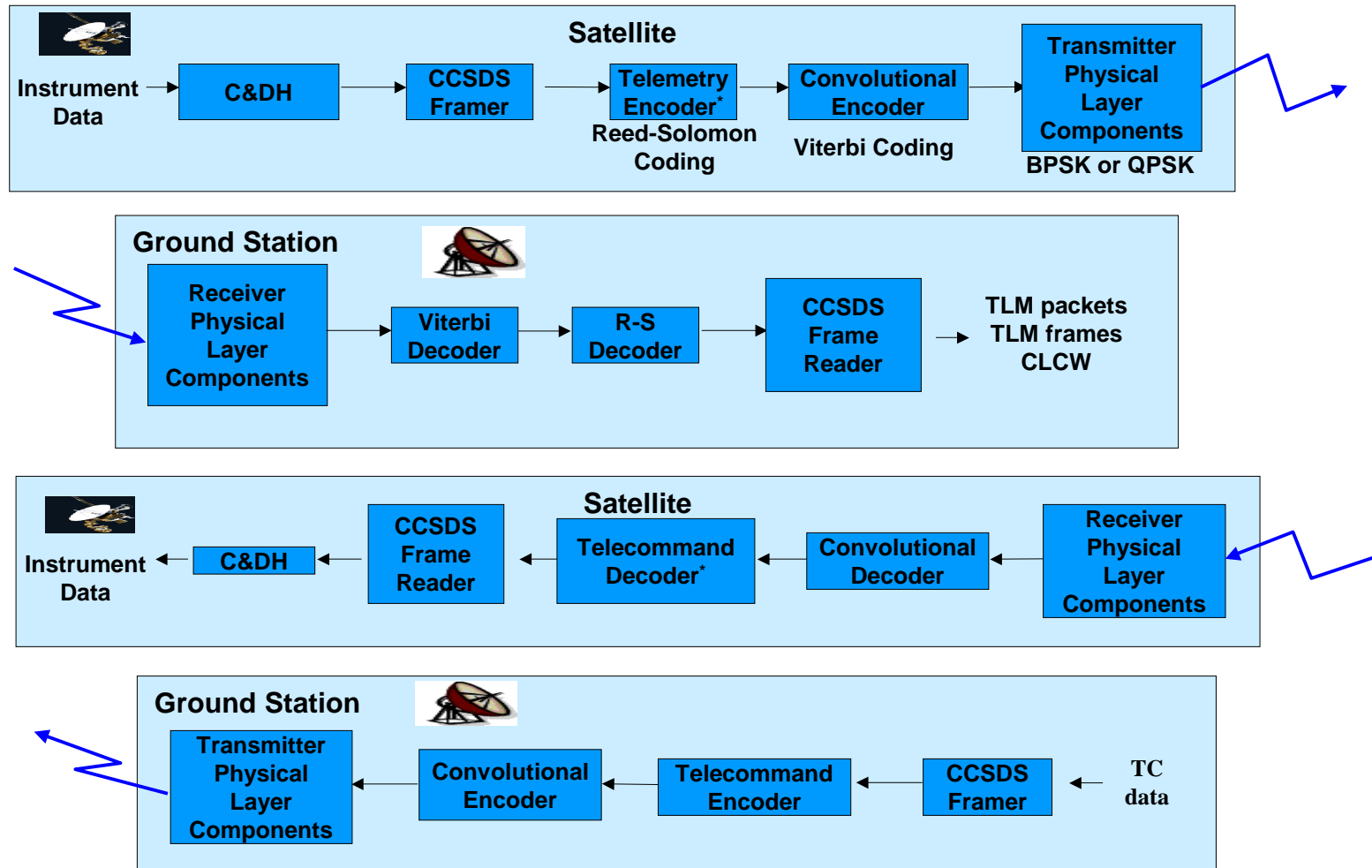
Why CCSDS?

- ❑ Standard space industry communication protocol.
- ❑ Employed on numerous missions ranging from relatively simple low earth missions to deep space probes.
- ❑ Could lead to spacecraft interoperability, re-usable systems and mission cross support – not just for in-house missions but across the CCSDS space agencies members.

CCSDS = Cross Support & Interoperability + STANDARD

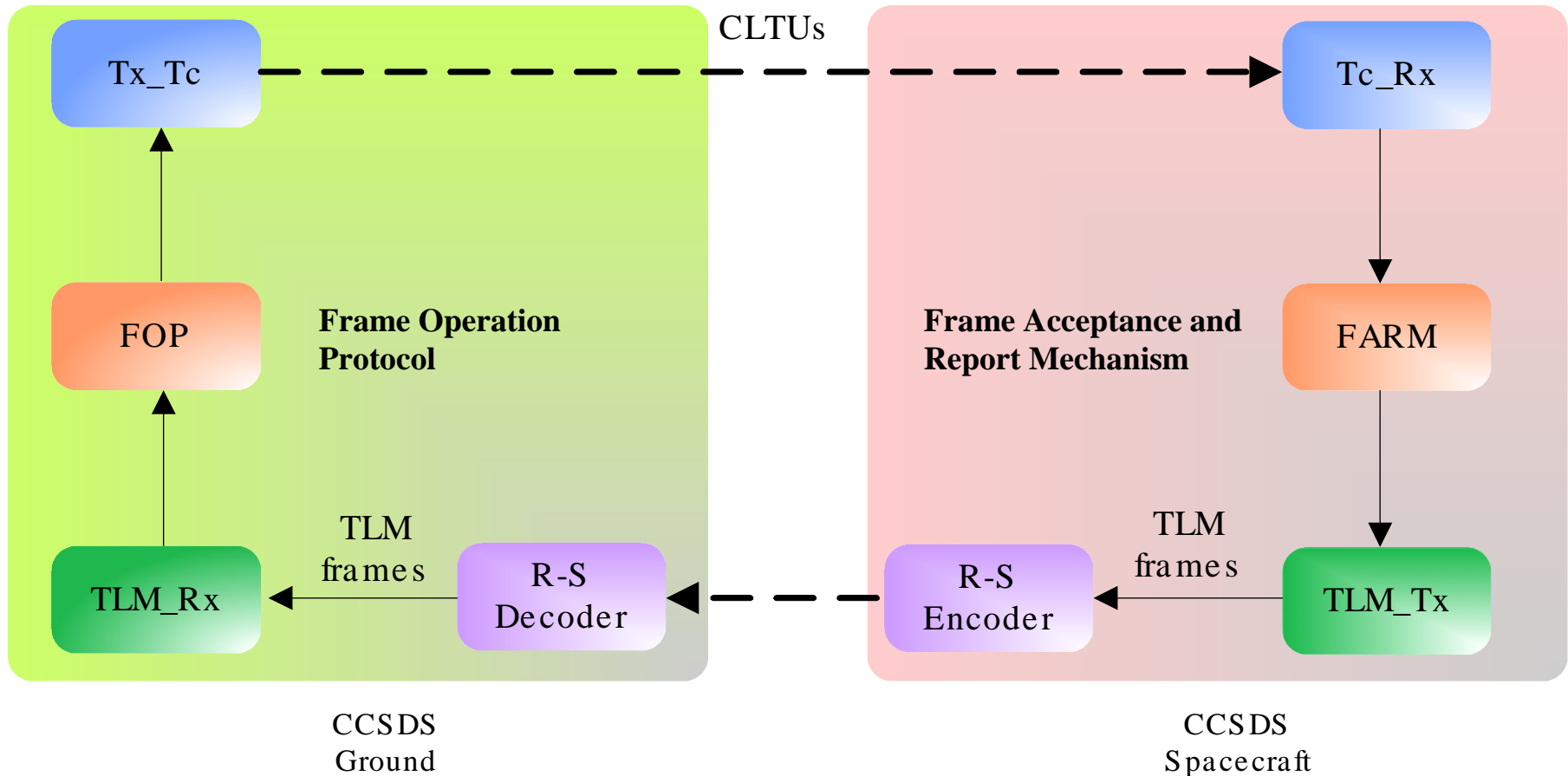


CCSDS TC & TLM Data Flow





CCSDS Software Package Structure & Interfaces

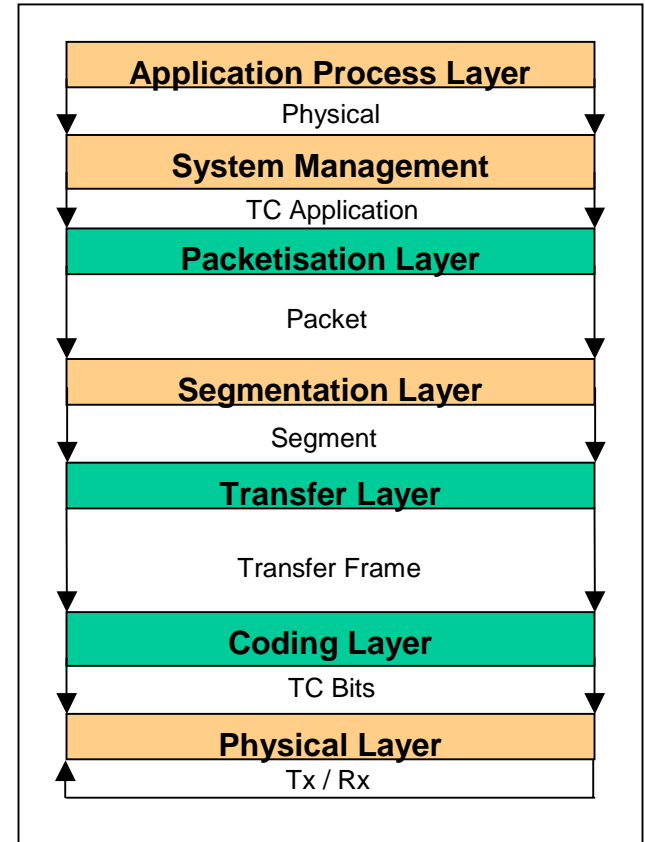


- A simplified software implementation of the CCSDS TLM and TC Command Operation Protocol (COP-1) based on FARM and FOP.
- Both the FARM and FOP systems contain the minimal CCSDS requirements to provide a reliable CCSDS communication system.
- The Reed-Solomon Encoder and Decoder are based on a C code, written by Phil Karn, KA9Q



CCSDS Software Package

- ❑ **FARM** Software Subsystem:
 - Produces the TC frame acceptance for the spacecraft.
 - Develops TC report mechanisms to the FOP via CLCWs (inside TLM frames).
- ❑ **FOP** Software Subsystem:
 - Processes the CLCWs (TLM frame).
 - Transmits or retransmits the TC frames back to the FARM.
- ❑ **TLM Coding** Subsystem:
 - Reed-Solomon Encoder/Decoder.
 - (255, 223) Reed-Solomon Code, E = 16.
 - Field generator polynomial:
$$F(x) = x^8 + x^7 + x^2 + x + 1.$$
 - Symbol Interleaving: 1.





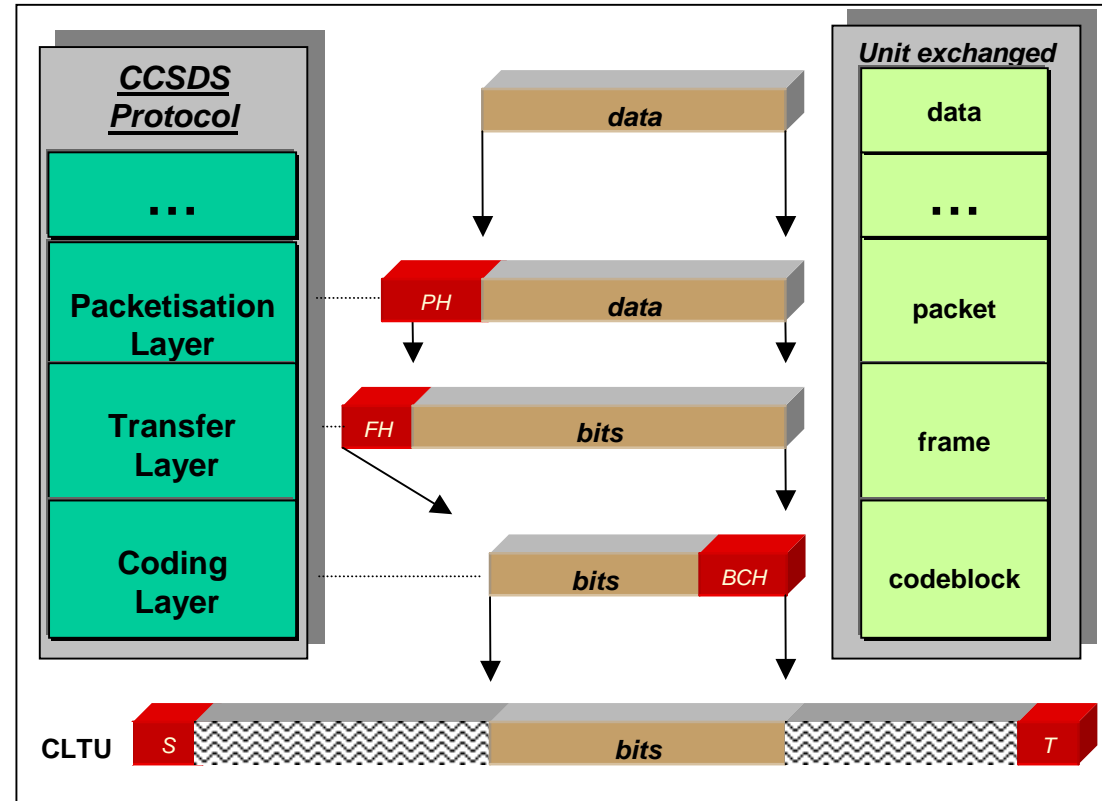
CCSDS Software - TC

CCSDS TC Frame Transmitter:

- Formats the TC packets of length 275 bytes.
- Formats the TC frames of length 280 bytes.
- Calculates the error detection code (BCH).
- Inserts the TC packets into the TC frames.
- Inserts the TC frames into Codeblocks.
- Formats the CLTUs.
- Inserts the Codeblocks into the CLTUs.

CCSDS TC Frame Receiver:

- Subtracts the Codeblocks from the CLTUs.
- Subtracts the TC frames from the Codeblocks.
- Decodes (BCH) the TC frames and TC packets.





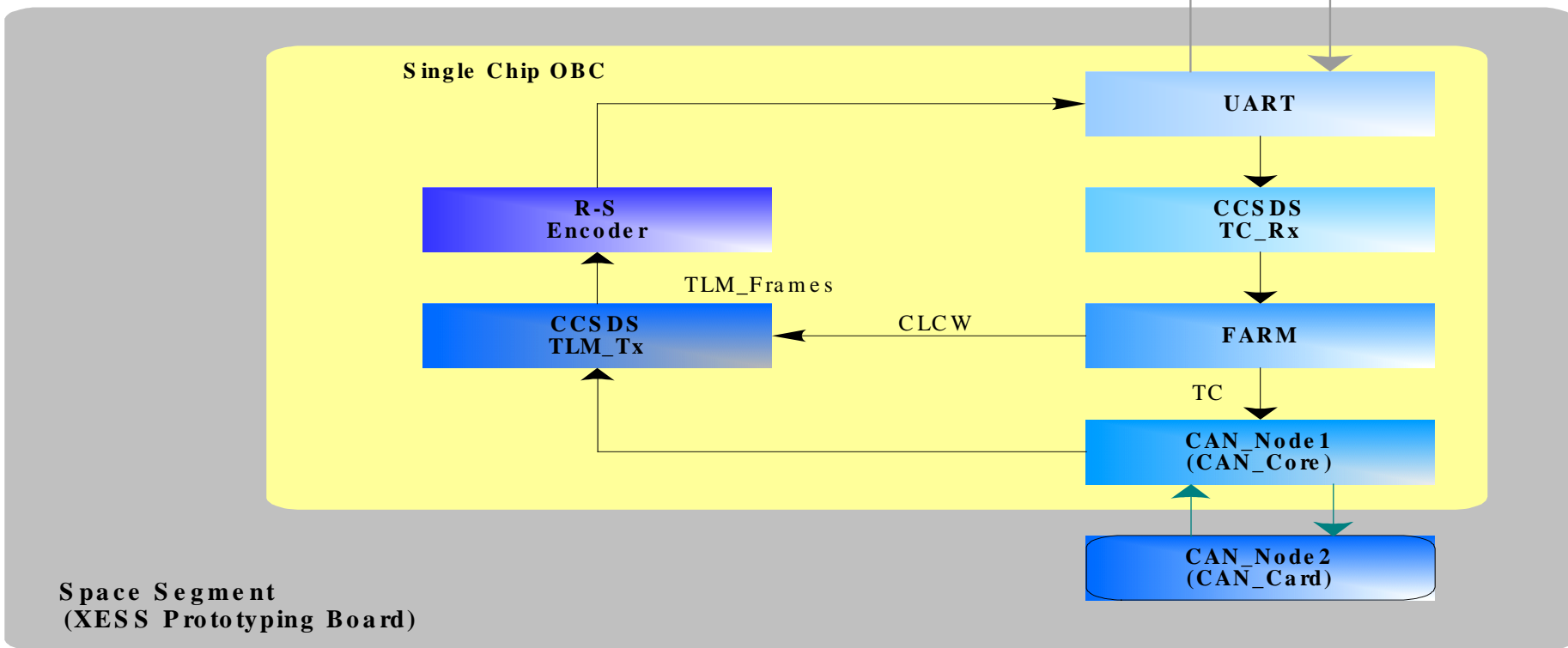
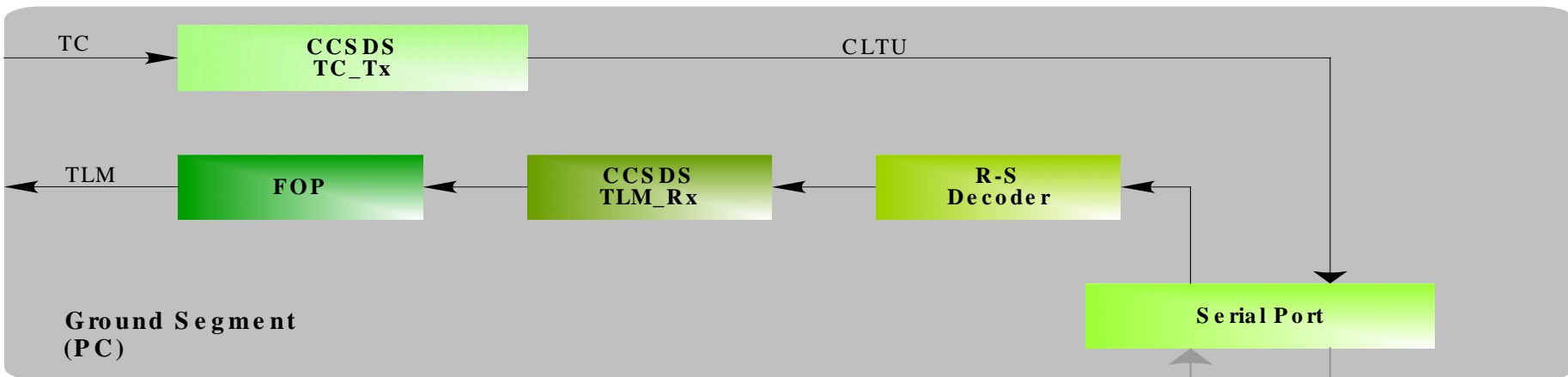
CCSDS Software - TLM

- ❑ **CCSDS TLM Frame Transmitter (CCSDS TLM_Tx):**
 - Formats the TLM packet of length 256 byte.
 - Formats the TLM frame of length 268 bytes.
 - Calculates the CRC of length 2 bytes (included in TLM Frame).
 - Inserts the TLM packets into the TLM frames.
 - Formats the Attached Synchronous Marker (ASM)
 - Transmits the full CCSDS TLM frame.

- ❑ **CCSDS TLM Frame Receiver (CCSDS TLM_Rx):**
 - Decodes the TLM frames (checks the CRC).
 - Subtracts the TLM packets from the TLM frames.
 - Inserts the TLM packet into buffer for future HL usage.

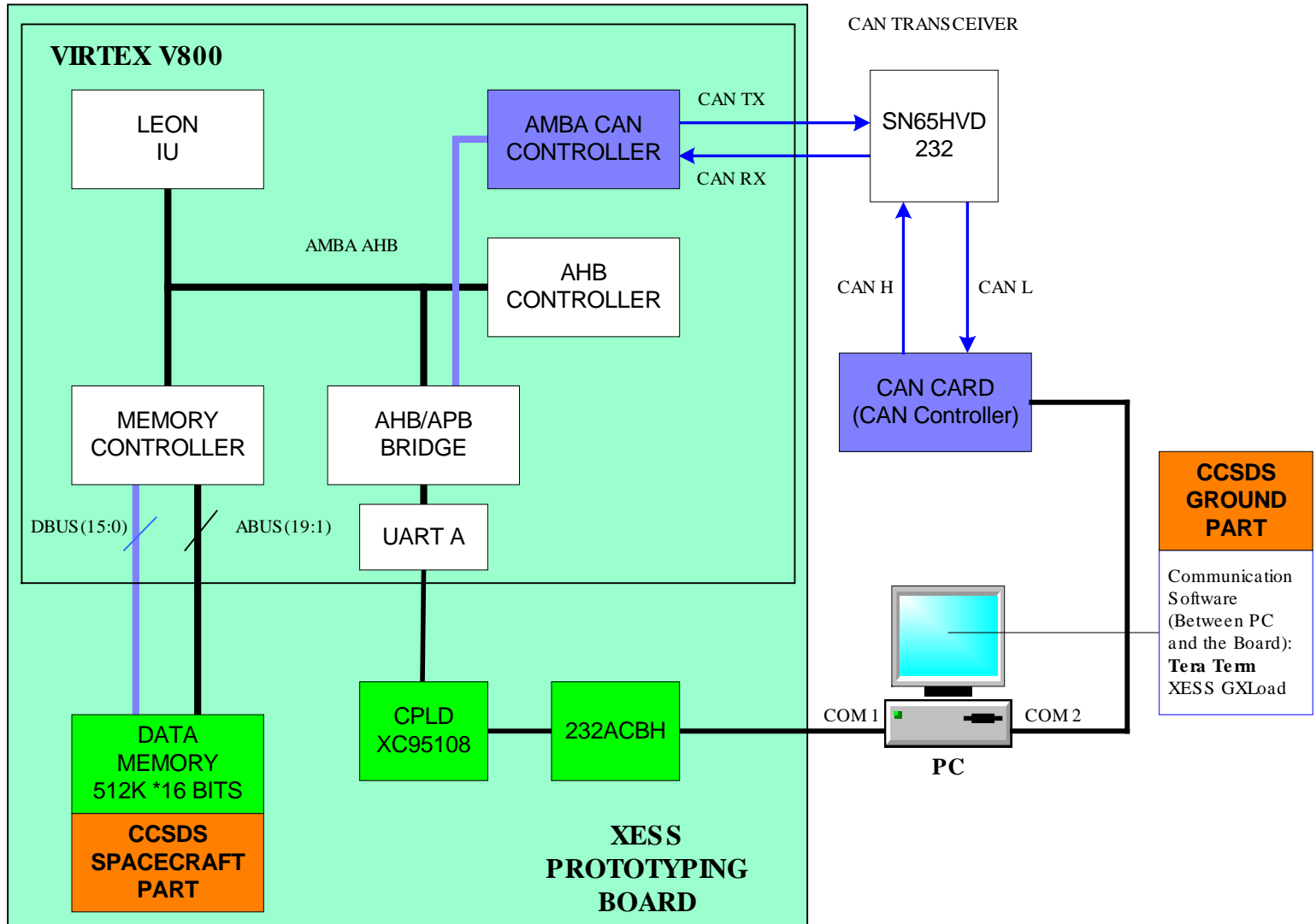


Simulation Scheme





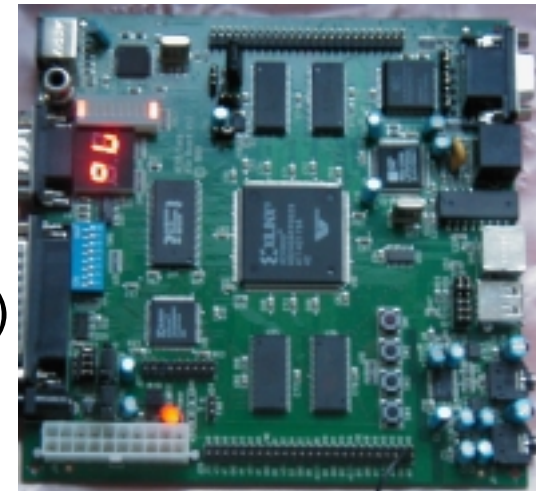
Experimental Setup





Experimental Setup - Details

- ❑ Processor - [LEON 2-1.0.2a VHDL IP](#) core (SPARC V8) (ESA)
 - Working Frequency – 25 MHz
 - UART Baud Rate – 38,400 bps
 - Internal S-Record Boot Loader
- ❑ On-Board Network (Node 1) - [HurriCANE VHDL IP](#) core (ESA)
 - Baud Rate: 312,500 bps
- ❑ EDAC – EDAC VHDL IP core (SSTL)
 - Double-bit correcting Quasi-Cyclic (16,8) shortened EDAC code
- ❑ Prototyping Board - [XESS XSV800](#) (Xilinx Virtex 800 FPGAs)
 - Up to 100 MHz programmable oscillator
 - 16M Bits SRAM (Two banks - 512K x 16)
 - 16M Bits flash RAM
- ❑ On-Board Application Program – S-Record File
 - 160K Bytes (CCSDS_SC Software Package)





Simulation Results

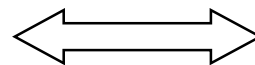
Transmission of TC & TLM between the CAN Core and the CAN Card

```
Tera Term - COM1 VT
File Edit Setup Control Window Help
Send TC (Idle) To The CAN Card!
status value: 4
Sending Message!
RX message x : 50 0 0 0 0 0 0 0
Send Message OK!
Received TLM message from the CAN card
RX message x : a0 18 0 0 8d dd 78 0
status value: 4
waiting.....
Send Message OK!
```

```
CAN-PCS
CAN-PCS [9806121]
(c) 1995-1998 Surrey Satellite Technology Ltd
Opened port 2 at 38400

cmd:BTR0 set on CAN card
BTR1 set on CAN card
~1
Debug On
cmd:Recv: F 80 T128 S3 L7 00 00 00 00 00 00 00
1 0,
```

CAN IP Core - CAN Node 1
(OBC)



CAN Card - CAN Node 2
(Payload)



Conclusions

- ❑ A simplified, yet reliable, standalone software implementation of the CCSDS protocol has been developed.
- ❑ The CCSDS software package features a modular structure which can facilitate easy expansions of functionality to suit specific mission requirements.
- ❑ The software imposes minimal memory footprint and performance requirements on the OBC.
- ❑ The functionality of the package has been verified via simulation using a single-chip OBC subsystem prototyped in a high density FPGA.
- ❑ The CCSDS software supported by a single-chip OBC and a thin-layer hardware interface can provide a cost effective and flexible communication solution for low-cost small satellites.
- ❑ The availability of a communication system, specifically designed to meet the needs of a single-chip OBC, will facilitate further research in miniaturisation of small satellites.