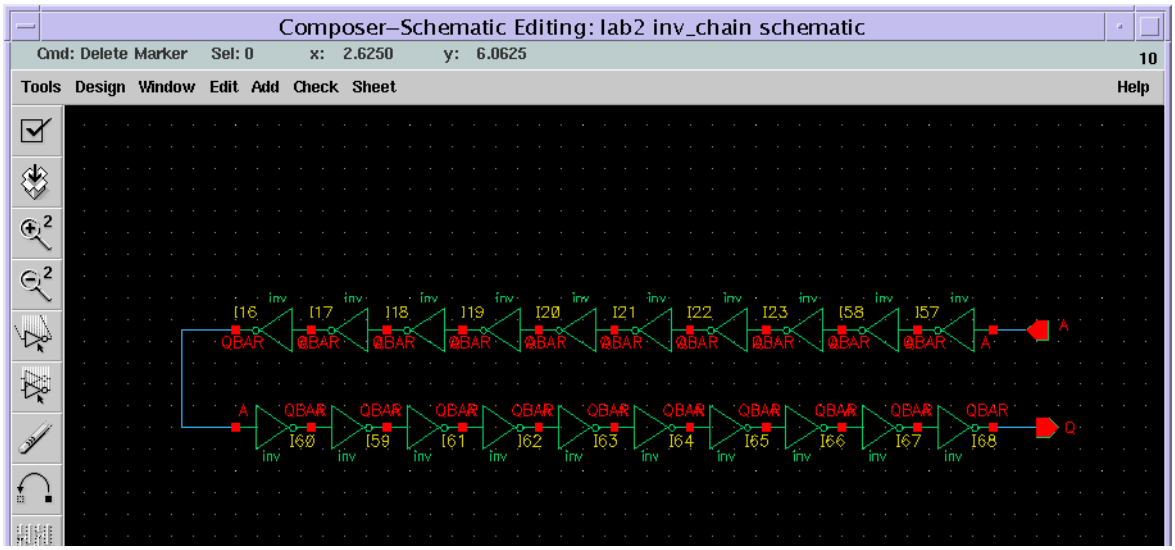
Using Silicon Ensemble with your own standard cell(s).

Lund 010320

1. Preparing a design for Silicon Ensemble.

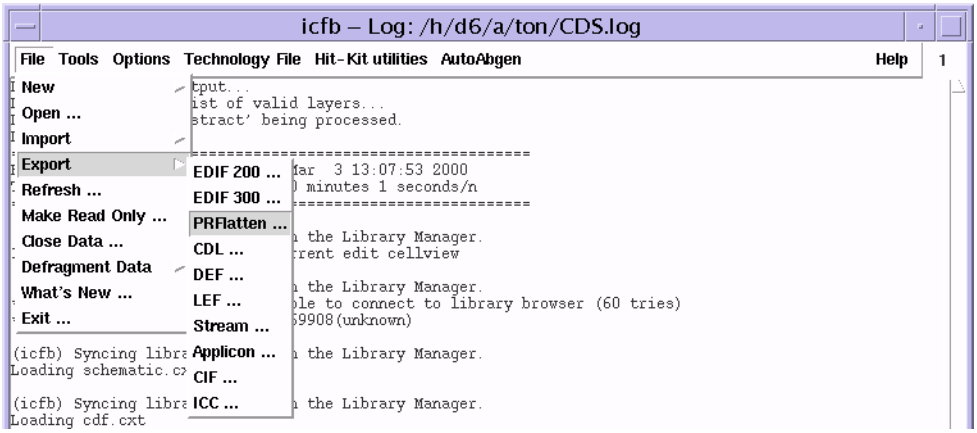
In a large standard cell design, placement of cells and drawing the connections between cells manually is probably too time consuming work. For designs consisting of perhaps thousands of gates, manual placement and routing will be almost impossible. Instead, a place and route tool is used. In this tutorial, a small design block is made using the place and route tool “Silicon Ensemble”.

Create a new schematic and name it “inv_chain”. Place an even number of inverters to form a chain (in this example 20 inverters are used) and name the input and output to the chain “A” and “Q”.

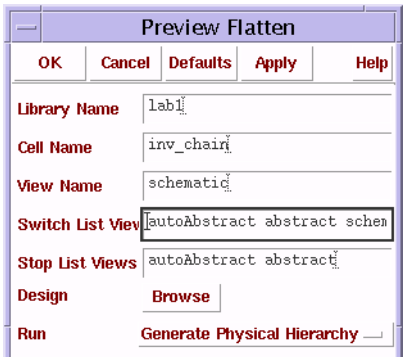


Do Check and Save [X].
The schematic now describes a netlist for the inverter chain. For a more complicated design it is now appropriate to perform a simulation (analog or digital) the analog simulation is done as for the single inverter and is therefore not covered in this tutorial.

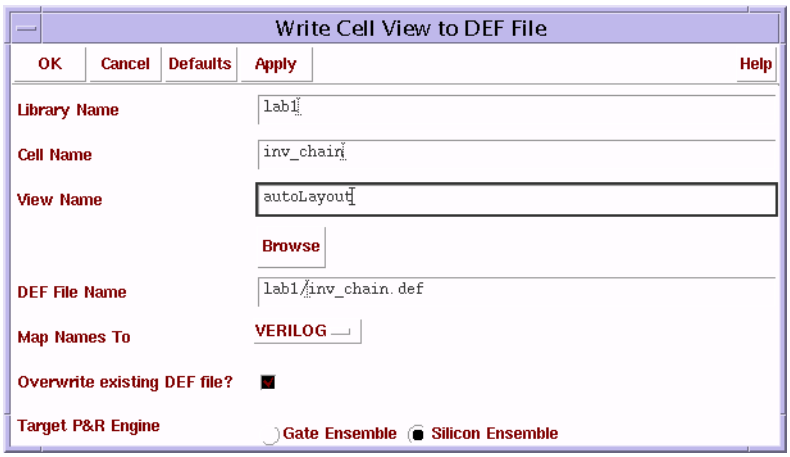
In the icfb-window, select File-Export-PRFlatten.



Fill in the fields in the “Preview Flatten-form” as below and press OK



In the icfb-window, select File-Export-DEF.
Fill in the fields in the “Write Cell View to DEF File -form” as below and press OK



A file inv_chain.def containing a netlist describing the inverter chain is now created. This netlist is used in Silicon Ensemble to describe the design. Some small adjustments must however be made in the .DEF-file.
Go to a xterm-window where Cadence has been initialized, go to directory lab1 and write:
$AMS_DIR/defpul inv_chain.def
A new file inv_cain_mod.def is now created.
If all steps are performed correctly, place & route of the inverter chain can now be performed in Silicon Ensemble.

2. Starting up Silicon Ensemble.

Go to your cadence work directory(~/cadence/digic01)
Since your disk quota probably is not large enough to run Silicon Ensemble, a working directory in the /tmp-area is created. As a consequence of this, you must stay at the same workstation during the whole design process.
In the xterm-window:

```
> mkdir -p /var/tmp/e9xyz/SE
> ln -s /var/tmp/e9xyz/SE
> cd SE
> $AMS_DIR/build_se_dir
> inittde dig01 nostart
> seultra &
```

Silicon Ensemble now opens.

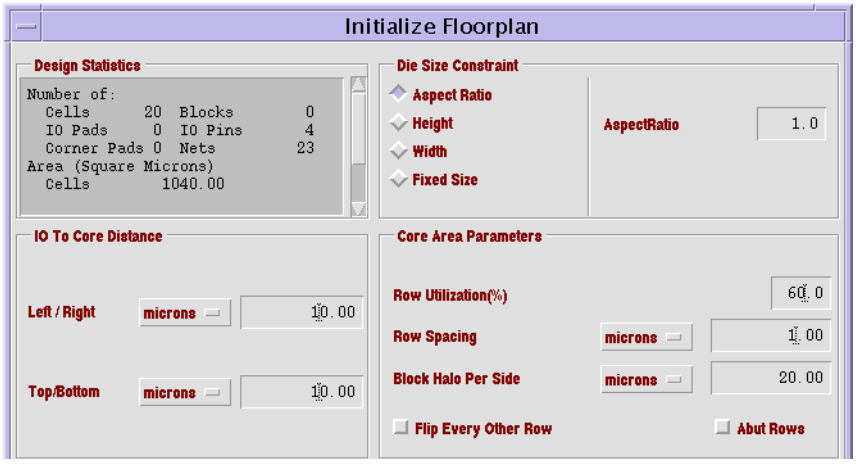
3. Initializing Silicon Ensemble.

Open a xterm-window.
Open the file “lefdefin.mac” from the “SE” directory and fill in the correct search paths to your .lef and .def -files.
Write “exec lefdefin.mac;” At the bottom line of the Silicon Ensemble-window.

4. Initializing the Floorplan.

Select Floorplan-Initialize Floorplan.

Fill in the fields as below and click OK.

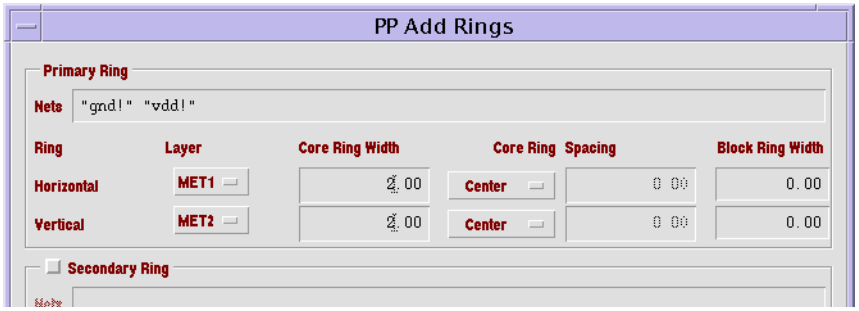


5. Placement.

Select Place-IOs
Click OK in the next window.
Select Place-Cells.
Click OK in the next window.
After a while all cells are placed out.

6. Power routing.

Next, select Route-Plan Power.
In the Plan Power-window, select Add Rings. Change Core Ring Width to 2 and click OK.



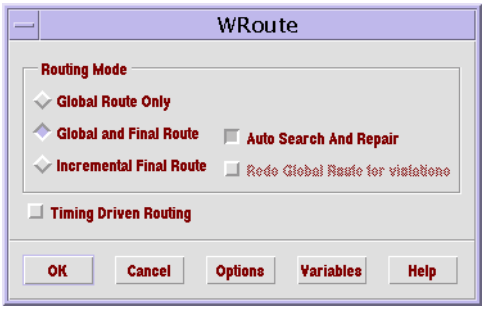
Close the Plan Power-window.
Select Route Connect Ring.

Click OK in the next window.

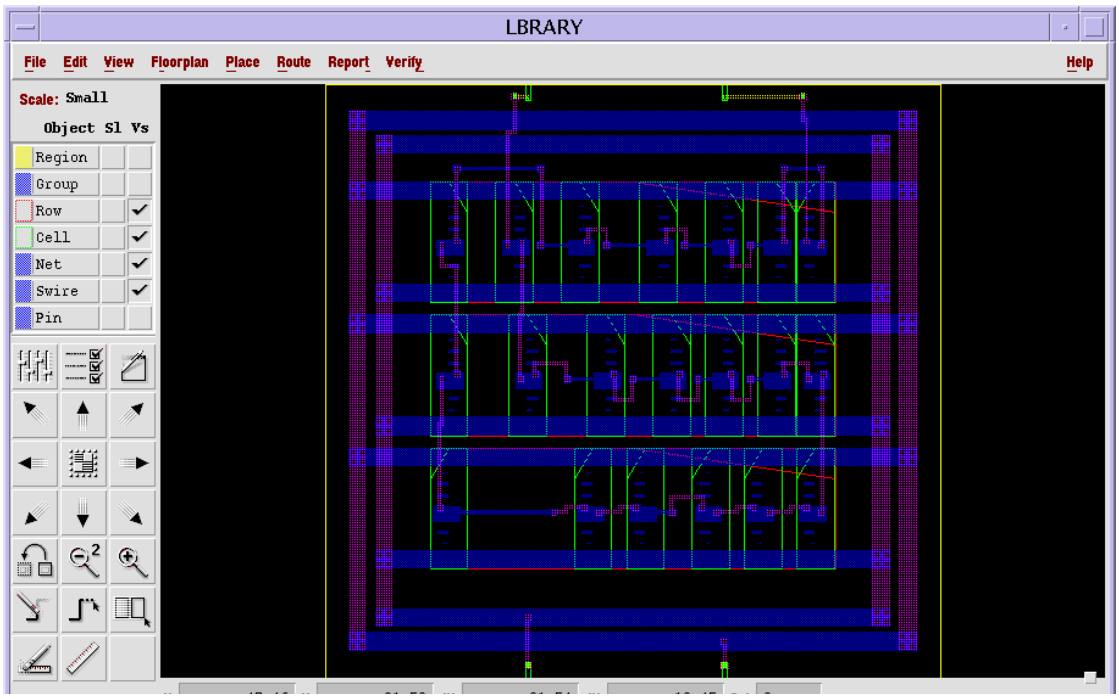
7. Global and Final Routing.

Select Route-WRoute.

Select the options as below and click OK.



After a while, the routing is ready.



Take a moment to investigate the routed circuit. Discuss it with a teacher.

8. Exporting the design.

The design can now be exported using the .def format.
Select File-Export-DEF

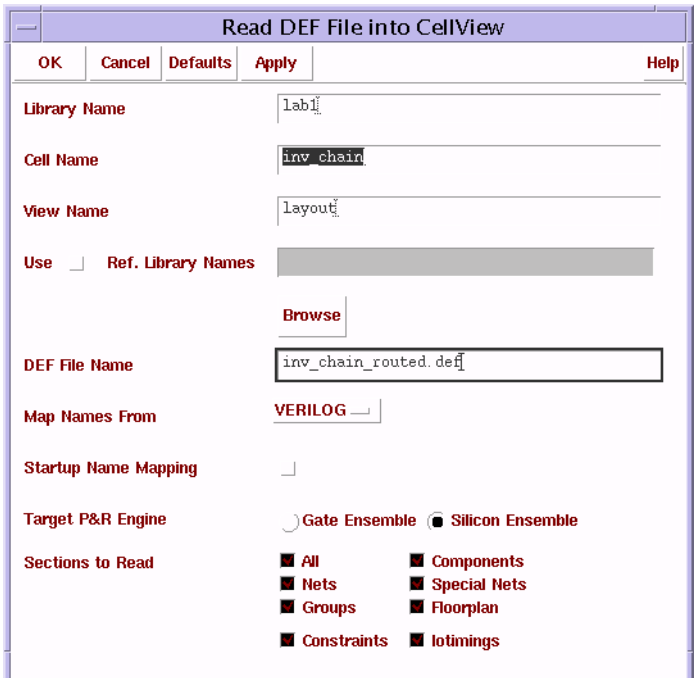
Export the design as inv_chain_routed.def

Copy inv_chain_routed.def to your cadence directory in a xterm window.

9. Importing the design to a layout window.

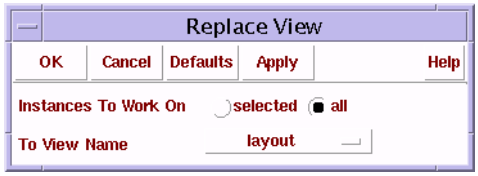
In the icfb-window, select File-Import-DEF.

Fill in the form as below and click OK.

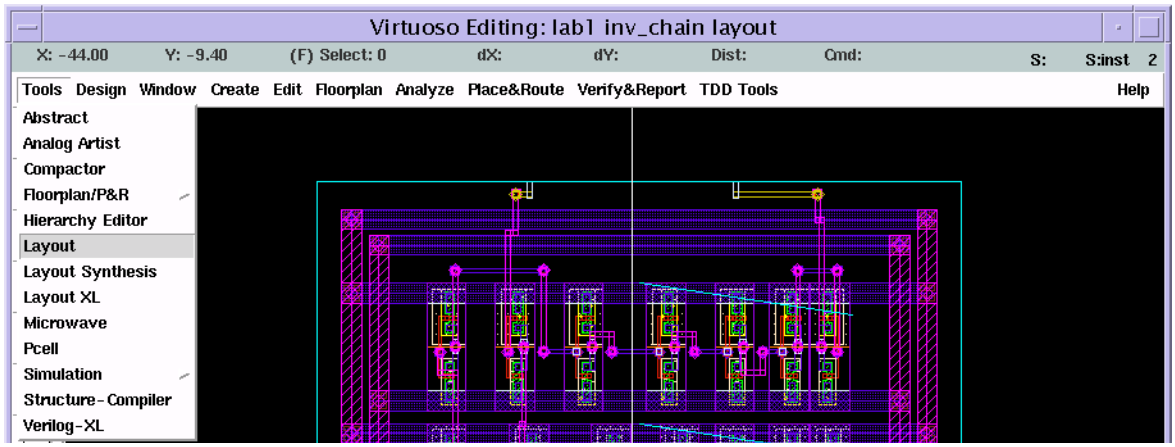


Open the layout view.
Select Floorplan-Replace view.

Select the “all“ option and click OK.



Change tool by selecting Tools-Layout.



10. Checking the design.

DRC , LVS and post-layout simulation can now be made as in the previous tutorial.
Note: There might be an extra “|” added before each pin name. To get the LVS to pass, those must be removed.