Using Silicon Ensemble with your own standard cell(s).



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1. Preparing a design for Silicon Ensemble.

In a large standard cell design, placement of cells and drawing the connections between cells manually is probably too time consuming work. For designs consisting of perhaps thousands of gates, manual placement and routing will be almost impossible. Instead, a place and route tool is used. In this tutorial, a small design block is made using the place and route tool "Silicon Ensemble".

Create a new schematic and name it "inv_chain". Place an even number of inverters to form a chain (in this example 20 inverters are used) and name the input and output to the chain "A" and "Q".



Do Check and Save [X].

The schematic now describes a netlist for the inverter chain. For a more complicated design it is now appropriate to perform a simulation (analog or digital) the analog simulation is done as for the single inverter and is therefore not covered in this tutorial.

In the icfb-window, select File-Export-PRFlatten.

	icfb – Log: /h/d6/a/ton/CDS.log		- [
File Tools Options Technology Fil	e Hit-Kit utilities AutoAbgen	Help	1	I
I New tput I Open ist of valid stract' bein	d layers ng processed.		-	
I Import				
Refresh EDIF 200	far 3 13:07:53 2000) minutes 1 seconds/n			
Make Read Only PRFlatten	the Library Manager			
Defragment Data	rent edit cellview			
What's New LEF	h the Library Manager. Le to connect to library browser (60 tries)			
Exit Stream	9908 (unknown)			
Loading schematic.c? CIF	I CHE LIDIATY MANAGEL.			
(icfb) Syncing libra ICC Loading cdf.cxt	the Library Manager.			

Fill in the fields in the "Preview Flatten-form" as below and press OK

- Preview Flatten								
OK Cancel Defaults Apply Help								
Library N	ame 1	ab1į́						
Cell Name inv_chain								
View Nan	View Name schematic							
Switch Li	Switch List View							
Stop List	Views a	utoAbstra	ct abstr:	actį				
Design	E	Browse						
Run	Ge	enerate Phy	ysical Hier	rarchy				

In the icfb-window, select File-Export-DEF. Fill in the fields in the "Write Cell View to DEF File -form" as below and press OK

_			Write Cell View to DEF File			
ок	Cancel	Defaults	Apply	p		
Library N	lame		labl	-		
Cell Nam	e		inv_chair <u>í</u>			
View Nar	ne		autoLayout			
			Browse			
DEF File	Name		lab1/jinv_chain.def			
Map Nan	nes To		VERILOG			
Overwrit	æ existing	DEF file?	•			
Target P	&R Engine) Gate Ensemble 间 Silicon Ensemble			

A file inv_chain.def containing a netlist describing the inverter chain is now created. This netlist is used in Silicon Ensemble to describe the design. Some small adjustments must however be made in the .DEF-file.

Go to a xterm-window where Cadence has been initialized, go to directory lab1 and write: \$AMS_DIR/defpul inv_chain.def

A new file inv_cain_mod.def is now created.

If all steps are performed correctly, place & route of the inverter chain can now be performed in Silicon Ensemble.

2. Starting up Silicon Ensemble.

Go to your cadence work directory(~/cadence/digic01)

Since your disk quota probably is not large enough to run Silicon Ensemble, a working directory in the /tmp-area is created. As a consequence of this, you must stay at the same workstation during the whole design process.

In the xterm-window:

- > mkdir -p /var/tmp/e9xyz/SE
- > ln -s /var/tmp/e9xyz/SE
- > cd SE
- > \$AMS_DIR/build_se_dir
- > inittde dig01 nostart

```
> seultra &
```

Silicon Ensemble now opens.

3. Initializing Silicon Ensemble.

Open a xterm-window.

Open the file "lefdefin.mac" from the "SE" directory and fill in the correct search paths to your .lef and .def -files.

Write "exec lefdefin.mac;" At the bottom line of the Silicon Ensemble-window.

4. Initializing the Floorplan.

Select Floorplan-Initialize Floorplan.

Fill in the fields as below and click OK.

-	Initialize Floorplan		
Design Statistics Number of: Cells 20 Blocks 0 IO Pads 0 IO Pins 4 Corner Pads 0 Nets 23 Area (Square Microns) Cells 1040.00	Die Size Constraint	AspectRatio	1.0
IO To Core Distance	Core Area Parameters		
Left / Right microns 📼 🗌	ŭ0.00 Row Utilization(%)		60 <u>,</u> 0
	Row Spacing	microns 🗆	1 <u>.</u> 00
Top/Bottom microns -	Ŭ. 00 Block Halo Per Side	microns 💷 2	0.00
	Flip Every Other Row	🔟 Abut Ro	WS

5. Placement.

Select Place-IOs Click OK in the next window. Select Place-Cells. Click OK in the next window. After a while all cells are placed out.

6. Power routing.

Next, select Route-Plan Power.

In the Plan Power-window, select Add Rings. Change Core Ring Width to 2 and click OK.

-		PP Add	l Rings		
Primary Rin	ıg				
Nets "gnd	!" "vdd!"				
Ring	Layer	Core Ring Width	Core Ring Spaci	ng	Block Ring Width
Horizontal	MET1 🖃	Ž. 00	Center 🔤	0 00	0.00
Vertical	MET2 🔤	Ž. 00	Center -	0 00	0.00
Seconda	ary Ring				
64A300					

Close the Plan Power-window. Select Route Connect Ring.

Click OK in the next window.

7. Global and Final Routing.

Select Route-WRoute.

Select the options as below and click OK.

	WRoute
Routing Mode Global Route Only Global and Final Route Incremental Final Route	Auto Search And Repair Redo Global Hauto tor visitationo
Timing Driven Routing	
OK Cancel	Options Variables Help

After a while, the routing is ready.

_								LBRARY	
<u>File</u>	dit <u>v</u>	iew	Floorplan	Place	Route	Report	Verify	<u>L</u>	elp
Scale: S	Small							31ba	
Obj	ect S	l Vs	-						
Regi	on								
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4									

Take a moment to investigate the routed circuit. Discuss it with a teacher.

8. Exporting the design.

The design can now be exported using the .def format. Select File-Export-DEF

Export the design as inv_chain_routed.def

		Expo	ort DEF	I
)EF File Name			
iı	nv_chain_r	outed.d	lef	Browse
4	All 🔷	Logical	🔷 Physic	cal
	Cells		🗐 Modificat	ions
	Nets		🗆 Constrair	nte
	Special Nets		🗐 External	Pins
	Vias		🗐 Scan Cha	ún
	Groups		💷 Layout M	odifications
	History		🔟 Aliases	
	ОКС	ancel	Variables	Help

Copy inv_chain_routed.def to your cadence directory in a xterm window.

9. Importing the design to a layout window.

In the icfb-window, select File-Import-DEF.

Fill in the form as below and click OK.

— Rea	d DEF File into CellView	
OK Cancel Defaults A	/abb/A	Help
Library Name	labl	
Cell Name	inv_chain	
View Name	layout	
Use 🔄 Ref. Library Names		
	Browse	
DEF File Name	inv_chain_routed.def	
Map Names From	VERILOG	
Startup Name Mapping		
Target P&R Engine) Gate Ensemble (Silicon Ensemble	
Sections to Read	AllComponentsNetsSpecial NetsGroupsFloorplanConstraintsI otimings	

Open the layout view. Select Floorplan-Replace view.

Select the "all" option and click OK.

- Replace View								
ок	Cancel	Defaults	Apply	Help				
Instance	Instances To Work Onselected (e all							
To View	Name		layout					

Change tool by selecting Tools-Layout.

	Virtuoso	Editing: lab1 inv	_chain layout		• 🗆
X: -44.00 Y: -9.40	(F) Select: 0	dX: dY:	Dist: Cm	d: S:	S:inst 2
Tools Design Window Creat	te Edit Floorplan Analyze	Place&Route Verify8	Report TDD Tools		Help
Abstract					
Analog Artist					
Compactor					
Floorplan/P&R -		.	₽ ₽		
Hierarchy Editor					
Layout					
Layout Synthesis		•	•		
Layout XL					
Microwave					
Pcell					
Simulation -					
Structure-Compiler					
Verilog-XL					

10. Checking the design.

DRC , LVS and post-layout simulation can now be made as in the previous tutorial. Note: There might be an extra "|" added before each pin name. To get the LVS to pass, those must be removed.