



ModelSim® SE User's Manual

Software Version 6.5b

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Table of Contents

Chapter 1

Introduction	43
Tool Structure and Flow	43
Simulation Task Overview	44
Basic Steps for Simulation	46
Step 1 — Collecting Files and Mapping Libraries	46
Step 2 — Compiling the Design (vlog, vcom, socom)	48
Step 3 — Loading the Design for Simulation	48
Step 4 — Simulating the Design	49
Step 5 — Debugging the Design	49
Modes of Operation	50
Command Line Mode	50
Batch Mode	51
What is an "Object"	52
Graphic Interface Overview	52
Standards Supported	52
Assumptions	53
Text Conventions	53
Installation Directory Pathnames	54
Where to Find Our Documentation	54
Mentor Graphics Support	55
Additional Support	55

Chapter 2

Graphical User Interface	57
Design Object Icons and Their Meaning	59
Setting Fonts	59
Using the Find and Filter Functions	60
Using the Find Options Popup Menu	63
User-Defined Radices	63
Using the radix define Command	64
Saving and Reloading Formats and Content	66
Main Window	66
Elements of the Main Window	66
Rearranging the Main Window	72
Common Windows	73
Navigating in the Main Window	74
Main Window Toolbar	74
Processes Window	92
Displaying the Processes Window	94
Viewing Data in the Processes Window	94
Post-Processing Mode	98

Create Textual Process Report	99
Call Stack Window	100
Class Tree Window	101
Displaying the Class Tree Window	102
GUI Elements of the Class Tree Window	102
Class Graph Window	103
Displaying the Class Graph Window	104
GUI Elements of the Class Graph Window	105
Windows Containing Code Coverage Data	105
Coverage Details Window	106
Current Exclusions Window	108
Dataflow Window	109
FSM List Window	110
GUI Elements of the FSM List Window	110
FSM Viewer Window	111
FSM Viewer Window Tasks	112
GUI Elements of the FSM Viewer Window	113
Instance Coverage Window	115
List Window	116
Displaying the List Window	117
Viewing Data in the List Window	117
GUI Elements of the List Window	118
Locals Window	120
Displaying the Locals Window	120
Viewing Data in the Locals Window	121
GUI Elements of the Locals Window	121
Memory and Memory Data Windows	122
Associative Arrays in Verilog/SystemVerilog	124
Viewing Single and Multidimensional Memories	124
Viewing Packed Arrays	125
Viewing Memory Contents	125
Direct Address Navigation	125
Splitting the Memory Contents Window	125
Missed Coverage Windows	126
Objects Window	127
Filtering the Objects List	128
Filtering by Name	128
Filtering by Signal Type	129
Toggle Coverage in the Objects Window	129
Profiling Windows	131
Profiling Window Columns	131
Source Window	132
Opening Source Files	134
Displaying Multiple Source Files	134
Dragging and Dropping Objects into the Wave and List Windows	135
Setting your Context by Navigating Source Files	135
Coverage Data in the Source Window	138
Debugging with Source Annotation	141
Accessing Textual Dataflow Information	143

Table of Contents

Using Language Templates.	144
Setting File-Line Breakpoints with the GUI.	147
Adding File-Line Breakpoints with the bp Command	148
Modifying File-Line Breakpoints	148
Checking Object Values and Descriptions	150
Marking Lines with Bookmarks	150
Performing Incremental Search for Specific Code	151
Customizing the Source Window	151
Structure Window	152
Structure Window Tasks.	153
GUI Elements of the Structure Window.	154
Code Coverage in Structure Window	159
Verification Browser Window.	159
Controlling the Verification Browser Columns	160
Saving Verification Browser Column and Filter Settings	161
GUI Elements of the Verification Browser Window	161
Transcript Window	162
Displaying the Transcript Window.	163
Viewing Data in the Transcript Window	163
Transcript Window Tasks.	163
GUI Elements of the Transcript Window	164
Message Viewer Window	165
Watch Window	171
Adding Objects to the Watch Window.	172
Expanding Objects to Show Individual Bits.	172
Grouping and Ungrouping Objects.	173
Saving and Reloading Format Files	174
Wave Window	174
Wave Window Panes	175
Objects You Can View in the Wave Window	181
Wave Window Toolbar.	182

Chapter 3

Protecting Your Source Code	183
Usage Models for Protecting Verilog Source Code.	183
Delivering IP Code with Undefined Macros	184
Delivering IP Code with Vendor-Defined Macros	186
Delivering Protected Verilog IP with `protect	189
Usage Models for Protecting VHDL Source Code	192
Using ModelSim Default Encryption for VHDL	192
User-Selected Encryption for VHDL	194
Using raw Encryption for VHDL	195
Encrypting Several Parts of a VHDL Source File	196
Using Portable Encryption for Multiple Simulators	198
Protecting Source Code Using -nodebug.	199
Encryption and Encoding Methods	200
Creating an Encryption Envelope	201
Protection Expressions	204

Using Public Encryption Keys.	205
Using the Mentor Graphics Public Encryption Key	205
Compiling a Design with +protect.	207
Chapter 4	
Optimizing Designs with vopt	209
Optimization Flows	209
Three-Step Flow	209
Two-Step Flow	212
Optimizing Parameters and Generics.	212
Optimizing Portions of your Design	214
Simulating Designs with Several Different Test Benches	214
Alternate Optimization Flows	215
Simulating Designs with Read-Only Libraries.	215
Creating an Environment for Optimized and Unoptimized Flows.	216
Preserving Design Visibility with the Learn Flow	216
Description of Learn Flow Control Files	218
Controlling Optimization from the GUI	218
Optimization Considerations for Verilog Designs.	219
Design Object Visibility for Designs with PLI.	219
Performing Optimization on Designs Containing SDF	220
Reporting on Gate-Level Optimizations.	221
Using Pre-Compiled Libraries	222
Event Order and Optimized Designs	222
Timing Checks in Optimized Designs	222
Chapter 5	
Projects.	223
What are Projects?	223
What are the Benefits of Projects?	223
Project Conversion Between Versions	224
Getting Started with Projects	224
Step 1 — Creating a New Project.	225
Step 2 — Adding Items to the Project	226
Step 3 — Compiling the Files.	227
Step 4 — Simulating a Design	230
Other Basic Project Operations.	232
The Project Window	232
Sorting the List	233
Creating a Simulation Configuration.	233
Optimization Configurations	235
Organizing Projects with Folders.	235
Adding a Folder	235
Specifying File Properties and Project Settings.	237
File Compilation Properties	237
Project Settings	239
Accessing Projects from the Command Line.	240

Chapter 6

Design Libraries	241
Design Library Overview	241
Design Unit Information	241
Working Library Versus Resource Libraries	241
Archives	242
Working with Design Libraries	242
Creating a Library	243
Managing Library Contents	243
Assigning a Logical Name to a Design Library	245
Moving a Library	246
Setting Up Libraries for Group Use	246
Specifying Resource Libraries	247
Verilog Resource Libraries	247
VHDL Resource Libraries	247
Predefined Libraries	248
Alternate IEEE Libraries Supplied	248
Rebuilding Supplied Libraries	248
Regenerating Your Design Libraries	249
Maintaining 32- and 64-bit Versions in the Same Library	250
Importing FPGA Libraries	250
Protecting Source Code	251

Chapter 7

VHDL Simulation	253
Basic VHDL Usage	253
Compilation and Simulation of VHDL	253
Creating a Design Library for VHDL	253
Compiling a VHDL Design—the vcom Command	254
Simulating a VHDL Design	256
Differences Between Versions of VHDL	257
Foreign Language Interface	259
Simulator Resolution Limit for VHDL	260
Default Binding	260
Delta Delays	261
Using the TextIO Package	264
Syntax for File Declaration	264
Using STD_INPUT and STD_OUTPUT Within ModelSim	265
TextIO Implementation Issues	265
Writing Strings and Aggregates	265
Reading and Writing Hexadecimal Numbers	266
Dangling Pointers	267
The ENDLINE Function	267
The ENDFILE Function	267
Using Alternative Input/Output Files	267
Flushing the TEXTIO Buffer	268
Providing Stimulus	268
VITAL Usage and Compliance	268

VITAL Source Code	268
VITAL 1995 and 2000 Packages	269
VITAL Compliance	269
Compiling and Simulating with Accelerated VITAL Packages	270
Compiler Options for VITAL Optimization	271
VHDL Utilities Package (util)	271
get_resolution	271
init_signal_driver()	272
init_signal_spy()	272
signal_force()	272
signal_release()	273
to_real()	273
to_time()	274
Modeling Memory	274
Examples of Different Memory Models	275
Affecting Performance by Cancelling Scheduled Events	284
Chapter 8	
Verilog and SystemVerilog Simulation	285
Standards, Nomenclature, and Conventions	285
Basic Verilog Usage	286
Verilog Compilation	287
Creating a Working Library	287
Invoking the Verilog Compiler	287
Incremental Compilation	289
Library Usage	292
SystemVerilog Multi-File Compilation	293
Verilog-XL Compatible Compiler Arguments	295
Verilog-XL uselib Compiler Directive	295
Verilog Configurations	298
Verilog Generate Statements	299
Initializing Registers and Memories	300
Verilog Simulation	302
Simulator Resolution Limit (Verilog)	303
Event Ordering in Verilog Designs	306
Debugging Event Order Issues	309
Debugging Signal Segmentation Violations	311
Negative Timing Checks	313
Verilog-XL Compatible Simulator Arguments	322
Using Escaped Identifiers	322
Cell Libraries	324
SDF Timing Annotation	324
Delay Modes	324
System Tasks and Functions	325
IEEE Std 1364 System Tasks and Functions	326
SystemVerilog System Tasks and Functions	328
System Tasks and Functions Specific to the Tool	329
Verilog-XL Compatible System Tasks and Functions	333

Table of Contents

Compiler Directives	336
IEEE Std 1364 Compiler Directives	337
Compiler Directives for vlog	337
Verilog-XL Compatible Compiler Directives	339
Sparse Memory Modeling	340
Manually Marking Sparse Memories	340
Automatically Enabling Sparse Memories	341
Combining Automatic and Manual Modes	341
Priority of Sparse Memories	341
Determining Which Memories Were Implemented as Sparse	341
Verilog PLI/VPI and SystemVerilog DPI	342
Standards, Nomenclature, and Conventions	343

Chapter 9

SystemC Simulation 345

Supported Platforms and Compiler Versions	345
Building gcc with Custom Configuration Options	346
Usage Flow for SystemC-Only Designs	347
Binding to Verilog or SystemVerilog Designs	348
Limitations of Bind Support for SystemC	348
Compiling SystemC Files	348
Creating a Design Library for SystemC	348
Invoking the SystemC Compiler	349
Compiling Optimized and/or Debug Code	349
Specifying an Alternate g++ Installation	350
Maintaining Portability Between OSCI and the Simulator	350
Switching Platforms and Compilation	351
Using sccom in Addition to the Raw C++ Compiler	351
Compiling Changed Files Only (Incremental Compilation)	352
Issues with C++ Templates	354
Linking the Compiled Source	363
Simulating SystemC Designs	363
Loading the Design	363
Running Simulation	364
SystemC Time Unit and Simulator Resolution	364
Initialization and Cleanup of SystemC State-Based Code	366
Debugging the Design	367
Viewable SystemC Types	367
Viewable SystemC Objects	368
Waveform Compare with SystemC	369
Debugging Source-Level Code	369
SystemC Object and Type Display	373
Support for Globals and Statics	373
Support for Aggregates	374
SystemC Dynamic Module Array	375
Viewing FIFOs	375
Viewing SystemC Memories	376
Properly Recognizing Derived Module Class Pointers	376

Custom Debugging of SystemC Channels and Variables.	378
Modifying SystemC Source Code	383
Code Modification Examples	384
Using sc_main as Top Level.	386
Differences Between the Simulator and OSCI	389
Fixed-Point Types.	390
Algorithmic C Datatype Support	391
Support for cin	391
OSCI 2.2 Feature Implementation Details.	392
Support for OSCI TLM Library	392
Phase Callback	392
Accessing Command-Line Arguments.	392
sc_stop Behavior.	393
Construction Parameters for SystemC Types	393
Troubleshooting SystemC Errors.	395
Unexplained Behaviors During Loading or Runtime.	395
Errors During Loading	396
Chapter 10	
Mixed-Language Simulation	401
Basic Mixed-Language Flow.	401
Separate Compilers with Common Design Libraries	402
Using Hierarchical References	402
Using SystemVerilog bind Construct in Mixed-Language Designs	403
Syntax of bind Statement	404
What Can Be Bound	404
Mapping of Types.	405
Using SV Bind With or Without vopt	406
Binding to VHDL Enumerated Types	406
Binding to a VHDL Instance	408
Limitations to Bind Support for SystemC	412
Optimizing Mixed Designs	412
Simulator Resolution Limit	412
Runtime Modeling Semantics	413
Hierarchical References to SystemVerilog.	413
Hierarchical References In Mixed HDL and SystemC Designs.	413
Signal Connections Between Mixed HDL and SystemC Designs	415
Mapping Data Types	416
Verilog and SystemVerilog to VHDL Mappings	416
VHDL To Verilog and SystemVerilog Mappings	420
Verilog or SystemVerilog and SystemC Signal Interaction And Mappings	422
VHDL and SystemC Signal Interaction And Mappings.	431
VHDL Instantiating Verilog or SystemVerilog.	437
Verilog/SystemVerilog Instantiation Criteria Within VHDL.	438
Component Declaration for VHDL Instantiating Verilog	438
vgencomp Component Declaration when VHDL Instantiates Verilog	439
Modules with Bidirectional Pass Switches.	440
Modules with Unnamed Ports.	440

Table of Contents

Verilog or SystemVerilog Instantiating VHDL	441
VHDL Instantiation Criteria Within Verilog	441
Entity and Architecture Names and Escaped Identifiers	442
Named Port Associations	442
Generic Associations	443
SDF Annotation	443
Sharing User-Defined Types	443
SystemC Instantiating Verilog or SystemVerilog	448
Verilog Instantiation Criteria Within SystemC	448
SystemC Foreign Module (Verilog) Declaration	449
Parameter Support for SystemC Instantiating Verilog	450
Verilog or SystemVerilog Instantiating SystemC	455
SystemC Instantiation Criteria for Verilog	455
Exporting SystemC Modules for Verilog	455
Parameter Support for Verilog Instantiating SystemC	456
SystemC Instantiating VHDL	458
VHDL Instantiation Criteria Within SystemC	458
SystemC Foreign Module (VHDL) Declaration	459
Generic Support for SystemC Instantiating VHDL	460
VHDL Instantiating SystemC	465
SystemC Instantiation Criteria for VHDL	465
Component Declaration for VHDL Instantiating SystemC	465
vgencomp Component Declaration when VHDL Instantiates SystemC	466
Exporting SystemC Modules for VHDL	466
Generic Support for VHDL Instantiating SystemC	467
SystemC Procedural Interface to SystemVerilog	467
Definition of Terms	467
SystemC DPI Usage Flow	468
SystemC Import Functions	468
Calling SystemVerilog Export Tasks / Functions from SystemC	472
SystemC Data Type Support in SystemVerilog DPI	472
SystemC Function Prototype Header File (sc_dpiheader.h)	475
Support for Multiple SystemVerilog Libraries	475
SystemC DPI Usage Example	476
Chapter 11	
Advanced Simulation Techniques	479
Checkpointing and Restoring Simulations	479
Checkpoint File Contents	479
Controlling Checkpoint File Compression	480
The Difference Between Checkpoint/Restore and Restart	480
Using Macros with Restart and Checkpoint/Restore	480
Checkpointing Foreign C Code That Works with Heap Memory	481
Checkpointing a Running Simulation	481
Simulating with an Elaboration File	482
Why an Elaboration File?	483
Elaboration File Flow	483
Creating an Elaboration File	483

Loading an Elaboration File	484
Modifying Stimulus	485
Using With the PLI or FLI	485
Chapter 12	
Recording and Viewing Transactions.....	487
Transaction Background	487
What is a Transaction?	488
About the Source Code for Transactions	488
About Transaction Streams.....	489
Viewing Transactions in the GUI	491
Transactions Viewing Commonalities	491
Viewing Transaction Objects in the Structure Window.....	493
Viewing Transactions in the Wave Window	493
Viewing a Transaction in the List Window	500
Viewing a Transaction in the Objects Window	501
Debugging with Tcl	502
Transaction Recording Flow	502
Transaction Recording Guidelines.....	505
Names of Streams and Substreams.....	506
Stream Logging.....	506
Transaction UIDs	507
Attribute Type.....	507
Multiple Uses of the Same Attribute	508
Anonymous Attributes	508
Relationships in Transactions	508
The Life-cycle of a Transaction	508
Transaction Handles and Memory Leaks	509
Transaction Recording Procedures	510
Recording Transactions in Verilog.....	510
Recording Transactions in SystemC.....	513
SCV Limitations	520
CLI Debugging Command Reference	521
Verilog API System Task Reference.....	521
\$add_attribute	521
\$add_relation.....	522
\$begin_transaction	523
\$create_transaction_stream.....	524
\$end_transaction.....	525
\$free_transaction.....	526
Chapter 13	
Recording Simulation Results With Datasets.....	529
Saving a Simulation to a WLF File	530
WLF File Parameter Overview.....	531
Limiting the WLF File Size	532
Opening Datasets	533
Viewing Dataset Structure.....	534

Table of Contents

Structure Tab Columns	535
Managing Multiple Datasets	535
GUI	535
Command Line	536
Restricting the Dataset Prefix Display	537
Saving at Intervals with Dataset Snapshot	537
Collapsing Time and Delta Steps	538
Virtual Objects	539
Virtual Signals	540
Virtual Functions	541
Virtual Regions	542
Virtual Types	542
Chapter 14	
Waveform Analysis.....	543
Objects You Can View	543
Wave Window Overview.....	544
Wave Window Panes	544
List Window Overview	546
Adding Objects to the Wave or List Window	546
Adding Objects with Drag and Drop	547
Adding Objects with Menu Selections	547
Adding Objects with a Command.....	547
Adding Objects with a Window Format File	547
Measuring Time with Cursors in the Wave Window	548
Cursor and Timeline Toolbox.....	548
Working with Cursors.....	550
Understanding Cursor Behavior	551
Jumping to a Signal Transition	552
Linking Cursors	552
Setting Time Markers in the List Window	553
Working with Markers	554
Expanded Time in the Wave and List Windows	554
Expanded Time Terminology	554
Recording Expanded Time Information	555
Viewing Expanded Time Information in the Wave Window	556
Selecting the Expanded Time Display Mode	559
Switching Between Time Modes	561
Expanding and Collapsing Simulation Time	561
Expanded Time Viewing in the List Window	562
Zooming the Wave Window Display	564
Zooming with the Menu, Toolbar and Mouse	564
Saving Zoom Range and Scroll Position with Bookmarks.....	565
Searching in the Wave and List Windows.....	566
Finding Signal Names.....	567
Searching for Values or Transitions	567
Using the Expression Builder for Expression Searches	568
Formatting the Wave Window.....	571

Setting Wave Window Display Preferences	571
Formatting Objects in the Wave Window	574
Dividing the Wave Window	575
Splitting Wave Window Panes	577
Wave Groups	578
Creating a Wave Group	579
Deleting or Ungrouping a Wave Group	580
Adding Items to an Existing Wave Group	581
Removing Items from an Existing Wave Group	581
Miscellaneous Wave Group Features	581
Formatting the List Window	582
Setting List Window Display Properties	582
Formatting Objects in the List Window	582
Saving the Window Format	584
Printing and Saving Waveforms in the Wave window	585
Saving a .eps Waveform File and Printing in UNIX	585
Printing from the Wave Window on Windows Platforms	586
Printer Page Setup	586
Saving List Window Data to a File	586
Viewing SystemVerilog Class Objects	586
Combining Objects into Buses	589
Creating a Virtual Signal	590
Configuring New Line Triggering in the List Window	591
Using Gating Expressions to Control Triggering	593
Sampling Signals at a Clock Change	594
Miscellaneous Tasks	595
Examining Waveform Values	595
Displaying Drivers of the Selected Waveform	595
Sorting a Group of Objects in the Wave Window	595
Creating and Managing Breakpoints	595
Signal Breakpoints	596
File-Line Breakpoints	598
Saving and Restoring Breakpoints	599
Waveform Compare	600
Mixed-Language Waveform Compare Support	600
Three Options for Setting up a Comparison	601
Setting Up a Comparison with the GUI	602
Starting a Waveform Comparison	602
Adding Signals, Regions, and Clocks	604
Specifying the Comparison Method	605
Setting Compare Options	607
Viewing Differences in the Wave Window	608
Viewing Differences in the List Window	611
Viewing Differences in Textual Format	611
Saving and Reloading Comparison Results	612
Comparing Hierarchical and Flattened Designs	612

Chapter 15

Debugging with the Dataflow Window	615
Dataflow Window Overview	615
Dataflow Usage Flow	616
Post-Simulation Debug Flow Details	616
Common Tasks for Dataflow Debugging	618
Adding Objects to the Dataflow Window	618
Exploring the Connectivity of the Design	618
Exploring Designs with the Embedded Wave Viewer	620
Tracing Events (Causality)	621
Tracing the Source of an Unknown State (StX)	622
Finding Objects by Name in the Dataflow Window	624
Automatically Tracing All Paths Between Two Nets	624
Dataflow Concepts	626
Symbol Mapping	626
Current vs. Post-Simulation Command Output	628
Dataflow Window Graphic Interface Reference	628
What Can I View in the Dataflow Window?	628
How is the Dataflow Window Linked to Other Windows?	629
How Can I Print and Save the Display?	629
How Do I Configure Window Options?	631
How Do I Zoom and Pan the Display?	632

Chapter 16

Code Coverage	635
Overview of Code Coverage Types	636
Language and Datatype Support	636
Usage Flow for Code Coverage Collection	636
Specifying Coverage Types for Collection	637
Enabling Simulation for Code Coverage Collection	638
Saving Code Coverage in the UCDB	639
Code Coverage in the UCDB	641
Code Coverage in the Graphic Interface	641
Understanding Unexpected Coverage Results	643
Code Coverage Types	644
Statement Coverage	644
Branch Coverage	644
Condition and Expression Coverage	645
Toggle Coverage	651
Finite State Machine Coverage	656
Coverage Exclusions	656
What Objects can be Excluded?	656
Auto Exclusions	656
Excluding Objects from Coverage	657
Toggle Exclusion Management	662
Exclude Nodes from Toggle Coverage	664
FSM Coverage Exclusions	665
Saving and Recalling Exclusions	667

Coverage Reports.....	669
Using the coverage report Command.....	669
Using the toggle report Command.....	670
Using the Coverage Report Dialog.....	671
Setting a Default Coverage Reporting Mode.....	672
XML Output.....	673
HTML Output.....	673
Coverage Reporting on a Specific Test.....	673
Notes on Coverage and Optimization.....	674
Customizing Optimization Level for Coverage Runs.....	674
Interaction of Optimization and Coverage Arguments.....	675
Chapter 17	
Finite State Machines.....	677
FSM Recognition.....	677
Unsupported FSM Design Styles.....	678
FSM Design Style Examples.....	678
FSM Coverage.....	681
FSM Multi-State Transitions.....	681
Collecting FSM Coverage Metrics.....	682
Reporting Coverage Metrics for FSMs.....	684
Viewing FSM Information in the GUI.....	685
FSM Coverage Metrics Available in the GUI.....	686
Advanced Command Arguments for FSMs.....	688
Recognized FSM Note.....	688
FSM Recognition Info Note.....	689
FSM Coverage Text Report.....	691
Chapter 18	
Verification Management.....	693
Verification Management Overview.....	693
What is the Unified Coverage Database?.....	695
Coverage and Simulator Use Modes.....	695
Coverage View Mode and the UCDB.....	696
Running Tests and Collecting Data.....	696
Collecting and Saving Coverage Data.....	696
Rerunning Tests and Executing Commands.....	698
Merging Coverage Test Data.....	701
Ranking Coverage Test Data.....	704
About the Merge Algorithm.....	705
Merge Usage Scenarios.....	707
Viewing and Analyzing Verification Data.....	708
Understanding the Test Data in the UCDB.....	709
Storing User Attributes in UCDB.....	711
Viewing Test Data in the GUI.....	711
Generating HTML Coverage Reports.....	714
Retrieving Test Attribute Record Content.....	716

Table of Contents

Chapter 19

C Debug	717
Supported Platforms and gdb Versions	717
Running C Debug on Windows Platforms	718
Setting Up C Debug	718
Running C Debug from a DO File	719
Setting Breakpoints	719
Stepping in C Debug	721
Debugging Active or Suspended Threads	722
Known Problems With Stepping in C Debug	722
Quitting C Debug	723
Finding Function Entry Points with Auto Find bp	723
Identifying All Registered Function Calls	723
Enabling Auto Step Mode	724
Auto Find bp Versus Auto Step Mode	725
Debugging Functions During Elaboration	726
FLI Functions in Initialization Mode	727
PLI Functions in Initialization Mode	727
VPI Functions in Initialization Mode	729
Completing Design Load	729
Debugging Functions when Quitting Simulation	729
C Debug Command Reference	730

Chapter 20

Profiling Performance and Memory Use	733
Introducing Performance and Memory Profiling	733
Statistical Sampling Profiler	734
Memory Allocation Profiler	734
Getting Started with the Profiler	734
Enabling the Memory Allocation Profiler	734
Enabling the Statistical Sampling Profiler	736
Collecting Memory Allocation and Performance Data	736
Running the Profiler on Windows with PLI/VPI Code	737
Interpreting Profiler Data	737
Viewing Profiler Results	737
Ranked Window	738
Design Units Window	738
Calltree Window	739
Structural Window	740
Viewing Profile Details	741
Integration with Source Windows	743
Analyzing C Code Performance	744
Reporting Profiler Results	745
Capacity Analysis	747
Enabling or Disabling Capacity Analysis	748
Levels of Capacity Analysis	750
Obtaining a Graphical Interface (GUI) Display	751
Writing a Text-Based Report	753

Chapter 21	
Signal Spy	757
Designed for Test Benches	758
SignalSpy Supported Types	758
disable_signal_spy	759
enable_signal_spy	761
init_signal_driver	763
init_signal_spy	767
signal_force	771
signal_release	775
Chapter 22	
Monitoring Simulations with JobSpy	779
Basic JobSpy Flow	779
Starting the JobSpy Daemon	780
Running JobSpy from the Command Line	781
Simulation Commands Available to JobSpy	781
Example Session	782
Running the JobSpy GUI	783
Starting Job Manager	783
Invoking Simulation Commands in Job Manager	783
View Commands and Pathnames	784
Viewing Results During Active Simulation	785
Viewing Waveforms from the Command Line	785
Licensing and Job Suspension	786
Checkpointing Jobs	786
Connecting to Load-Sharing Software	787
Checkpointing with Load-Sharing Software	787
Chapter 23	
Generating Stimulus with Waveform Editor	789
Getting Started with the Waveform Editor	789
Using Waveform Editor Prior to Loading a Design	789
Using Waveform Editor After Loading a Design	790
Creating Waveforms from Patterns	791
Creating Waveforms with Wave Create Command	792
Editing Waveforms	793
Selecting Parts of the Waveform	794
Stretching and Moving Edges	796
Simulating Directly from Waveform Editor	796
Exporting Waveforms to a Stimulus File	796
Driving Simulation with the Saved Stimulus File	797
Signal Mapping and Importing EVCD Files	798
Using Waveform Compare with Created Waveforms	798
Saving the Waveform Editor Commands	799

Chapter 24

Standard Delay Format (SDF) Timing Annotation.....	801
Specifying SDF Files for Simulation.....	801
Instance Specification.....	802
SDF Specification with the GUI.....	802
Errors and Warnings.....	803
Compiling SDF Files.....	803
Simulating with Compiled SDF Files.....	803
Using \$sdf_annotate() with Compiled SDF.....	804
VHDL VITAL SDF.....	804
SDF to VHDL Generic Matching.....	804
Resolving Errors.....	805
Verilog SDF.....	805
\$sdf_annotate.....	806
SDF to Verilog Construct Matching.....	807
Optional Edge Specifications.....	810
Optional Conditions.....	811
Rounded Timing Values.....	812
SDF for Mixed VHDL and Verilog Designs.....	812
Interconnect Delays.....	812
Disabling Timing Checks.....	813
Troubleshooting.....	814
Specifying the Wrong Instance.....	814
Matching a Single Timing Check.....	814
Mistaking a Component or Module Name for an Instance Label.....	815
Forgetting to Specify the Instance.....	815

Chapter 25

Value Change Dump (VCD) Files.....	817
Creating a VCD File.....	817
Four-State VCD File.....	817
Extended VCD File.....	818
Case Sensitivity.....	818
Checkpoint/Restore and Writing VCD Files.....	818
Using Extended VCD as Stimulus.....	819
Simulating with Input Values from a VCD File.....	819
Replacing Instances with Output Values from a VCD File.....	820
VCD Commands and VCD Tasks.....	822
Using VCD Commands with SystemC.....	823
Compressing Files with VCD Tasks.....	824
VCD File from Source to Output.....	824
VHDL Source Code.....	824
VCD Simulator Commands.....	824
VCD Output.....	826
VCD to WLF.....	827
Capturing Port Driver Data.....	827
Driver States.....	827
Driver Strength.....	828

Identifier Code	828
Resolving Values	829
Chapter 26	
Tcl and Macros (DO Files).....	833
Tcl Features	833
Tcl References	833
Tcl Commands.....	833
Tcl Command Syntax	834
If Command Syntax	837
set Command Syntax	837
Command Substitution	838
Command Separator	839
Multiple-Line Commands.....	839
Evaluation Order.....	839
Tcl Relational Expression Evaluation.....	839
Variable Substitution	840
System Commands	840
Simulator State Variables	841
Referencing Simulator State Variables.....	842
Special Considerations for the now Variable	842
List Processing.....	843
Reading Variable Values From the INI File	843
Simulator Tcl Commands	844
Simulator Tcl Time Commands.....	844
Conversions.....	845
Relations	845
Arithmetic.....	846
Tcl Examples	846
Macros (DO Files).....	848
Creating DO Files.....	848
Using Parameters with DO Files.....	849
Deleting a File from a .do Script.....	849
Making Macro Parameters Optional.....	850
Useful Commands for Handling Breakpoints and Errors.....	851
Error Action in DO Files.....	852
The Tcl Debugger	852
Starting the Debugger.....	853
How it Works	853
The Chooser	853
The Debugger	854
Breakpoints.....	856
Configuration	857
TclPro Debugger	857
Chapter A	
modelsim.ini Variables.....	859
Organization of the modelsim.ini File.....	859

Table of Contents

Making Changes to the modelsim.ini File	860
Changing the modelsim.ini Read-Only Attribute	860
The Runtime Options Dialog	860
Editing modelsim.ini Variables	864
Overriding the Default Initialization File	864
Variables	865
AcceptLowerCasePragmaOnly	865
AmsStandard	865
AssertFile	866
AssertionDebug	866
AssertionFailAction	866
AssertionFailEnable	867
AssertionFailLimit	867
AssertionFailLocalVarLog	867
AssertionFailLog	868
AssertionPassEnable	868
AssertionPassLimit	868
AssertionPassLog	868
AutoExclusionsDisable	869
BindAtCompile	869
BreakOnAssertion	869
CheckPlusargs	870
CheckpointCompressMode	870
CheckSynthesis	871
CommandHistory	871
ConcurrentFileLimit	871
CoverageSub	872
CoverCells	872
CoverCountAll	872
CoverExcludeDefault	873
CoverFEC	873
CoverMaxFECRows	873
CoverMaxUDPRows	874
CoverOpt	874
CoverRespectHandL	875
CoverShortCircuit	875
CppOptions	875
CppPath	876
DatasetSeparator	876
DefaultForceKind	876
DefaultRadix	877
DefaultRestartOptions	878
DelayFileOpen	878
displaymsgmode	879
DpiOutOfTheBlue	879
DumpportsCollapse	880
error	880
ErrorFile	881
Explicit	881

fatal	881
FsmResetTrans	882
FsmSingle	882
FsmXAssign	883
GenerateFormat	883
GenerateLoopIterationMax	883
GenerateRecursionDepthMax	884
GenerousIdentifierParsing	884
GlobalSharedObjectsList	884
Hazard	885
ieee	885
IgnoreError	885
IgnoreFailure	885
IgnoreNote	886
IgnoreVitalErrors	886
IgnoreWarning	887
ImmediateContinuousAssign	887
IterationLimit	887
LibrarySearchPath	888
License	888
MaxReportRhsCrossProducts	889
MessageFormat	889
MessageFormatBreak	890
MessageFormatBreakLine	890
MessageFormatError	890
MessageFormatFail	891
MessageFormatFatal	891
MessageFormatNote	891
MessageFormatWarning	892
modelsim_lib	892
msgmode	892
MultiFileCompilationUnit	893
NoAutoSDFCCompile	893
NoCaseStaticError	893
NoDebug	894
NoIndexCheck	894
NoOthersStaticError	894
NoRangeCheck	895
note	895
NoVital	895
NoVitalCheck	896
NumericStdNoWarnings	896
OnFinish	897
OnFinishPendingAssert	897
Optimize_1164	898
PathSeparator	898
PedanticErrors	898
PliCompatDefault	899
PrintSimStats	900

Table of Contents

PrintSVPackageLoadingAttribute.	900
Protect	901
Quiet	901
RequireConfigForAllDefaultBinding	901
Resolution	902
RunLength.	902
ScalarOpts	903
SccomLogfile	903
SccomVerbose	903
ScEnableScSignalWriteCheck	904
ScMainFinishOnQuit	904
ScMainStackSize	904
ScShowIeeeDeprecationWarnings	905
ScTimeUnit.	905
ScvPhaseRelationName	905
Show_BadOptionWarning	905
Show_Lint.	906
Show_source.	906
Show_VitalChecksWarnings	906
Show_Warning1	907
Show_Warning2	907
Show_Warning3	907
Show_Warning4	907
Show_Warning5	908
ShowConstantImmediateAsserts	908
ShowFunctions	908
ShowUnassociatedScNameWarning.	909
ShowUndebuggableScTypeWarning	909
ShutdownFile	909
SignalSpyPathSeparator	910
SparseMemThreshold	910
Startup	910
std	911
std_developerskit	911
StdArithNoWarnings	911
suppress.	912
sv_std	912
SVFileExtensions	912
Svlog	913
synopsys	913
ToggleCountLimit	913
ToggleFixedSizeArray	914
ToggleMaxFixedSizeArray.	914
ToggleMaxIntValues	914
ToggleMaxRealValues	915
ToggleNoIntegers	915
TogglePackedAsVec.	916
ToggleVlogEnumBits	916
ToggleVlogIntegers	916

ToggleVlogReal	917
ToggleWidthLimit	917
TranscriptFile	917
UCDBFilename	918
UnbufferedOutput	918
UpCase	918
UserTimeUnit	919
UseScv	919
verilog	919
Veriuser	920
VHDL93	920
vital2000	920
vlog95compat	921
VoptAutoSDFCompile	921
VoptFlow	921
WarnConstantChange	922
warning	922
WaveSignalNameWidth	923
WLFCacheSize	923
WLFCollapseMode	923
WLFCompress	924
WLFDeleteOnQuit	924
WLFFileName	925
WLFIndex	925
WLFOptimize	925
WLFSaveAllRegions	926
WLFsimCacheSize	926
WLFSizeLimit	927
WLFTimeLimit	927
WLFUseThreads	928
ZeroIn	928
ZeroInOptions	928
Commonly Used modelsim.ini Variables	929
Common Environment Variables	929
Hierarchical Library Mapping	929
Creating a Transcript File	930
Using a Startup File	930
Turning Off Assertion Messages	930
Turning off Warnings from Arithmetic Packages	931
Force Command Defaults	931
Restart Command Defaults	931
VHDL Standard	931
Opening VHDL Files	932
Appendix B	
Location Mapping	933
Referencing Source Files with Location Maps	933
Using Location Mapping	933

Table of Contents

Pathname Syntax	934
How Location Mapping Works	934
Mapping with TCL Variables	934
Appendix C	
Error and Warning Messages	935
Message System	935
Message Format	935
Getting More Information	936
Changing Message Severity Level	936
Suppressing Warning Messages	936
Suppressing VCOM Warning Messages	936
Suppressing VLOG Warning Messages	937
Suppressing VOPT Warning Messages	937
Suppressing VSIM Warning Messages	938
Exit Codes	938
Miscellaneous Messages	940
scom Error Messages	943
Enforcing Strict 1076 Compliance	945
Appendix D	
Verilog Interfaces to C	947
Implementation Information	947
g++ Compiler Support for use with Interfaces	949
Registering PLI Applications	949
Registering VPI Applications	951
Registering DPI Applications	952
DPI Use Flow	953
Integrating Export Wrappers into an Import Shared Object	955
When Your DPI Export Function is Not Getting Called	956
Troubleshooting a Missing DPI Import Function	956
DPI and the qverilog Command	956
Simplified Import of Library Functions	957
Use Model for Locked Work Libraries	958
DPI Arguments of Parameterized Datatypes	959
Making Verilog Function Calls from non-DPI C Models	959
Calling C/C++ Functions Defined in PLI Shared Objects from DPI Code	959
Compiling and Linking C Applications for Interfaces	960
For all UNIX Platforms	960
Windows Platforms — C	961
32-bit Linux Platform — C	962
64-bit Linux for IA64 Platform — C	963
64-bit Linux for Opteron/Athlon 64 and EM64T Platforms — C	963
32-bit Solaris UltraSPARC Platform — C	964
32-bit Solaris x86 Platform — C	964
64-bit Solaris UltraSPARC Platform — C	964
64-bit Solaris x86 Platform — C	964
Compiling and Linking C++ Applications for Interfaces	965

Windows Platforms — C++	966
32-bit Linux Platform — C++	967
64-bit Linux for IA64 Platform — C++	967
64-bit Linux for Opteron/Athlon 64 and EM64T Platforms — C++	967
32-bit Solaris UltraSPARC Platform — C++	968
32-bit Solaris x86 Platform — C++	968
64-bit Solaris UltraSPARC Platform — C++	968
64-bit Solaris x86 Platform — C++	969
Specifying Application Files to Load	969
PLI and VPI File loading	969
DPI File Loading	970
Loading Shared Objects with Global Symbol Visibility	970
PLI Example	970
VPI Example	971
DPI Example	972
The PLI Callback reason Argument	973
The sizetf Callback Function	974
PLI Object Handles	975
Third Party PLI Applications	975
Support for VHDL Objects	976
IEEE Std 1364 ACC Routines	977
IEEE Std 1364 TF Routines	979
SystemVerilog DPI Access Routines	979
Verilog-XL Compatible Routines	980
64-bit Support for PLI	980
Using 64-bit ModelSim with 32-bit Applications	980
PLI/VPI Tracing	980
The Purpose of Tracing Files	981
Invoking a Trace	981
Checkpointing and Interface Code	982
Checkpointing Code that Works with Heap Memory	982
Debugging Interface Application Code	982
Appendix E	
Command and Keyboard Shortcuts	985
Command Shortcuts	985
Command History Shortcuts	985
Main and Source Window Mouse and Keyboard Shortcuts	986
List Window Keyboard Shortcuts	989
Wave Window Mouse and Keyboard Shortcuts	989
Appendix F	
Setting GUI Preferences	993
Customizing the Simulator GUI Layout	993
Layouts and Modes of Operation	993
Custom Layouts	993
Automatic Saving of Layouts	995
Resetting Layouts to Their Defaults	995

Table of Contents

Simulator GUI Preferences	995
Setting Preference Variables from the GUI	995
Setting Preference Variables from the Command Line	998
Saving GUI Preferences	998
The modelsim.tcl File	998
Appendix G	
System Initialization	1001
Files Accessed During Startup	1001
Initialization Sequence	1001
Environment Variables	1004
Environment Variable Expansion	1004
Setting Environment Variables	1004
Creating Environment Variables in Windows	1009
Referencing Environment Variables	1010
Removing Temp Files (VSOUT)	1011
Appendix H	
Logic Modeling Hardware Models	1013
VHDL Hardware Model Interface	1013
Creating Foreign Architectures with hm_entity	1014
Hardware Model Vector Ports	1016
Hardware Model Commands	1017
Appendix I	
Logic Modeling SmartModels	1019
VHDL SmartModel Interface	1019
Creating Foreign Architectures with sm_entity	1020
SmartModel Vector Ports	1023
Command Channel	1024
SmartModel Windows	1025
Memory Arrays	1026
Verilog SmartModel Interface	1027
Linking the LMTV Interface to the Simulator	1027
Index	
Third-Party Information	
End-User License Agreement	

List of Examples

Example 2-1. Using the radix define Command	64
Example 2-2. Using radix define to Specify Color	65
Example 3-1. Encryption Envelope Contains Verilog IP Code to be Protected	202
Example 3-2. Encryption Envelope Contains `include Compiler Directives	203
Example 3-3. Using the Mentor Graphics Public Encryption Key in Verilog/SystemVerilog	206
Example 3-4. Results After Compiling with vlog +protect.	207
Example 7-1. Memory Model Using VHDL87 and VHDL93 Architectures	276
Example 7-2. Conversions Package.	278
Example 7-3. Memory Model Using VHDL02 Architecture	280
Example 8-1. Invocation of the Verilog Compiler	287
Example 8-2. Incremental Compilation Example	290
Example 8-3. Sub-Modules with Common Names	293
Example 9-1. Generating SCV Extensions for a Structure	358
Example 9-2. Generating SCV Extensions for a Class without Friend (Private Data Not Generated).	358
Example 9-3. Generating SCV Extensions for a Class with Friend (Private Data Generated)	359
Example 9-4. Generating SCV Extensions for an Enumerated Type	360
Example 9-5. User-Defined Constraint	360
Example 9-6. Use of mti_set_typename	377
Example 9-7. Using the Custom Interface on Different Objects.	380
Example 9-8. Converting sc_main to a Module	384
Example 9-9. Using sc_main and Signal Assignments	385
Example 9-10. Using an SCV Transaction Database	386
Example 9-11. Simple SystemC-only sc_main().	386
Example 10-1. Binding with -cname and -mfcu Arguments.	410
Example 10-2. SystemC Instantiating Verilog - 1.	449
Example 10-3. SystemC Instantiating Verilog - 2.	450
Example 10-4. Sample Foreign Module Declaration, with Constructor Arguments for Parameters 451	
Example 10-5. Passing Parameters as Constructor Arguments - 1	451
Example 10-6. SystemC Instantiating Verilog, Passing Integer Parameters as Template Arguments	453
Example 10-7. Passing Integer Parameters as Template Arguments and Non-integer Parameters as Constructor Arguments	454
Example 10-8. Verilog/SystemVerilog Instantiating SystemC, Parameter Information. . . .	456
Example 10-9. SystemC Design Instantiating a VHDL Design Unit	460
Example 10-10. SystemC Instantiating VHDL, Generic Information.	461
Example 10-11. Passing Parameters as Constructor Arguments - 2	461
Example 10-12. SystemC Instantiating VHDL, Passing Integer Generics as Template Arguments	

462

Example 10-13. Passing Integer Generics as Template Arguments and Non-integer Generics as Constructor Arguments	463
Example 10-14. Global Import Function Registration	468
Example 10-15. SystemVerilog Global Import Declaration	469
Example 10-16. Usage of scSetScopeByName and scGetScopeName	471
Example 12-1. Transactions in List Window	500
Example 12-2. Verilog API Code Example.	513
Example 12-3. SCV Initialization and WLF Database Creation	514
Example 12-4. SCV API Code Example	519
Example 16-1. FEC-based Expression Coverage Example	647
Example 16-2. UDP Condition Truth Table	648
Example 16-3. Vectors in UDP Condition Truth Table	649
Example 16-4. Expression UDP Truth Table	650
Example 16-5. Creating Coverage Exclusions with a .do File	662
Example 16-6. Excluding, Merging and Reporting on Several Runs	668
Example 16-7. Reporting Coverage Data from the Command Line	669
Example 17-1. Verilog Single-State Variable FSM	678
Example 17-2. VHDL Single-State Variable FSM	679
Example 17-3. Verilog Current-State Variable with a Single Next-State Variable FSM	679
Example 17-4. VHDL Current-State Variable and Single Next-State Variable FSM.	680
Example 25-1. Verilog Counter.	819
Example 25-2. VHDL Adder.	819
Example 25-3. Mixed-HDL Design.	820
Example 25-4. Replacing Instances.	821
Example 25-5. VCD Output from vcd dumpports.	831
Example 26-1. Tcl while Loop	846
Example 26-2. Tcl for Command	846
Example 26-3. Tcl foreach Command.	846
Example 26-4. Tcl break Command	847
Example 26-5. Tcl continue Command	847
Example 26-6. Access and Transfer System Information	847
Example 26-7. Tcl Used to Specify Compiler Arguments	848
Example 26-8. Tcl Used to Specify Compiler Arguments—Enhanced	848
Example 26-9. Specifying Files to Compile With argc Macro	850
Example 26-10. Specifying Compiler Arguments With Macro	850
Example 26-11. Specifying Compiler Arguments With Macro—Enhanced.	850
Example D-1. VPI Application Registration	951
Example F-1. Configure Window Layouts Dialog Box	995

List of Figures

Figure 1-1. Tool Structure and Flow	44
Figure 2-1. Graphical User Interface	57
Figure 2-2. Find Mode	60
Figure 2-3. Filter Mode	60
Figure 2-4. Find Options Popup Menu	63
Figure 2-5. User-Defined Radix “States” in the Wave Window	65
Figure 2-6. User-Defined Radix “States” in the List Window	65
Figure 2-7. Main Window of the GUI	67
Figure 2-8. Main Window — Menu Bar	68
Figure 2-9. Main Window — Toolbar Frame	68
Figure 2-10. Main Window — Toolbar	69
Figure 2-11. GUI Windows	69
Figure 2-12. GUI Tab Group	70
Figure 2-13. Wave Window Panes	71
Figure 2-14. Main Window Status Bar	71
Figure 2-15. Window Header Handle	72
Figure 2-16. Tab Handle	73
Figure 2-17. Window Undock Button	73
Figure 2-18. Column Layout Toolbar	75
Figure 2-19. Compile Toolbar	76
Figure 2-20. Coverage Toolbar	76
Figure 2-21. Dataflow Toolbar	78
Figure 2-22. FSM Toolbar	78
Figure 2-23. Help Toolbar	79
Figure 2-24. Layout Toolbar	80
Figure 2-25. Memory Toolbar	80
Figure 2-26. Mode Toolbar	80
Figure 2-27. Process Toolbar	81
Figure 2-28. Profile Toolbar	82
Figure 2-29. NAME Toolbar	83
Figure 2-30. Simulate Toolbar	83
Figure 2-31. Source Toolbar	85
Figure 2-32. Standard Toolbar	86
Figure 2-33. Wave Toolbar	87
Figure 2-34. Wave Bookmark Toolbar	87
Figure 2-35. Wave Compare Toolbar	88
Figure 2-36. Wave Cursor Toolbar	89
Figure 2-37. Wave Edit Toolbar	90
Figure 2-38. Wave Expand Time Toolbar	91
Figure 2-39. Zoom Toolbar	92

List of Figures

Figure 2-40. Processes (Active) Window	93
Figure 2-41. Process Toolbar	93
Figure 2-42. Processes (In Region) Window	93
Figure 2-43. Selecting Show Full Path from Process Menu	96
Figure 2-44. Process Display Options Dialog	97
Figure 2-45. Column Heading Changes When States are Filtered	98
Figure 2-46. Set Next Active RMB Menu Selection	99
Figure 2-47. Next Active Process Displayed in Order Column	99
Figure 2-48. Sample Process Report in the Transcript Window	100
Figure 2-49. Call Stack Window	100
Figure 2-50. Class Tree Window	101
Figure 2-51. Class Graph Window	104
Figure 2-52. Windows that Show Code Coverage Data	106
Figure 2-53. Coverage Details Window Showing Condition Truth Table	107
Figure 2-54. Coverage Details Window Showing Toggle Details	107
Figure 2-55. Coverage Details Window Showing Information from Source Window	108
Figure 2-56. Current Exclusions Window	108
Figure 2-57. Dataflow Window	109
Figure 2-58. FSM List Window	110
Figure 2-59. FSM Viewer Window	112
Figure 2-60. Instance Coverage Window	115
Figure 2-61. Filter Instance List Dialog	116
Figure 2-62. List Window	117
Figure 2-63. Locals Window	120
Figure 2-64. Change Selected Variable Dialog Box	122
Figure 2-65. Memory and Memory Data Windows	123
Figure 2-66. Split Screen View of Memory Contents	126
Figure 2-67. Missed Coverage Window	126
Figure 2-68. Missed Branches Window	127
Figure 2-69. Objects Window	128
Figure 2-70. Objects Filter	128
Figure 2-71. Filtering the Objects List by Name	129
Figure 2-72. Objects Window - Toggle Coverage	130
Figure 2-73. Source Window Showing Language Templates	134
Figure 2-74. Displaying Multiple Source Files	135
Figure 2-75. Setting Context from Source Files	136
Figure 2-76. Coverage in Source Window	139
Figure 2-77. Source Annotation Example	142
Figure 2-78. Popup Menu Choices for Textual Dataflow Information	143
Figure 2-79. Window Shows all Signal Drivers	143
Figure 2-80. Window Shows all Signal Readers	144
Figure 2-81. Language Templates	145
Figure 2-82. Create New Design Wizard	145
Figure 2-83. Inserting Module Statement from Verilog Language Template	146
Figure 2-84. Language Template Context Menus	146

Figure 2-85. Breakpoint in the Source Window	147
Figure 2-86. Modifying Existing Breakpoints	149
Figure 2-87. Source Window with Find Toolbar	151
Figure 2-88. Preferences Dialog for Customizing Source Window	152
Figure 2-89. Structure Window	153
Figure 2-90. Code Coverage Data in the Structure Window	159
Figure 2-91. Browser Tab	160
Figure 2-92. Transcript Window with Find Toolbar	164
Figure 2-93. Message Viewer Window	167
Figure 2-94. Message Viewer Filter Dialog Box	170
Figure 2-95. Watch Window	171
Figure 2-96. Scrollable Hierarchical Display	172
Figure 2-97. Expanded Array	173
Figure 2-98. Grouping Objects in the Watch Window	174
Figure 2-99. Pathnames Pane	175
Figure 2-100. Values Pane	176
Figure 2-101. Waveform Pane	176
Figure 2-102. Analog Sidebar Toolbox	177
Figure 2-103. Cursor Pane	178
Figure 2-104. Toolbox for Cursors and Timeline	178
Figure 2-105. Editing Grid and Timeline Properties	179
Figure 2-106. Cursor Properties Dialog	180
Figure 2-107. Wave Window - Message Bar	180
Figure 3-1. vencrypt Usage Flow	185
Figure 3-2. Delivering IP Code with Vendor-Defined Macros	187
Figure 3-3. Delivering IP with `protect Compiler Directives	189
Figure 5-1. Create Project Dialog	225
Figure 5-2. Project Window Detail	225
Figure 5-3. Add items to the Project Dialog	226
Figure 5-4. Create Project File Dialog	227
Figure 5-5. Add file to Project Dialog	227
Figure 5-6. Right-click Compile Menu in Project Window	228
Figure 5-7. Click Plus Sign to Show Design Hierarchy	228
Figure 5-8. Setting Compile Order	229
Figure 5-9. Grouping Files	230
Figure 5-10. Start Simulation Dialog	231
Figure 5-11. Structure Window with Projects	231
Figure 5-12. Project Window Overview	232
Figure 5-13. Add Simulation Configuration Dialog	234
Figure 5-14. Simulation Configuration in the Project Window	235
Figure 5-15. Add Folder Dialog	236
Figure 5-16. Specifying a Project Folder	236
Figure 5-17. Project Compiler Settings Dialog	237
Figure 5-18. Specifying File Properties	238
Figure 5-19. Project Settings Dialog	239

List of Figures

Figure 6-1. Creating a New Library.	243
Figure 6-2. Design Unit Information in the Workspace	244
Figure 6-3. Edit Library Mapping Dialog	245
Figure 6-4. Import Library Wizard	251
Figure 7-1. VHDL Delta Delay Process	262
Figure 8-1. Fatal Signal Segmentation Violation (SIGSEGV)	312
Figure 8-2. Current Process Where Error Occurred	312
Figure 8-3. Blue Arrow Indicates Where Code Stopped Executing	312
Figure 8-4. null Values in the Locals Window	313
Figure 9-1. SystemC Objects in GUI.	364
Figure 9-2. Breakpoint in SystemC Source	370
Figure 9-3. Setting the Allow lib step Function.	371
Figure 9-4. SystemC Objects and Processes	373
Figure 9-5. Aggregates in Wave Window	375
Figure 12-1. Transaction Anatomy in Wave Window.	490
Figure 12-2. Transaction Stream in Wave Window	492
Figure 12-3. Viewing Transactions and Attributes	494
Figure 12-4. Overlapping Parallel Transactions	494
Figure 12-5. Transaction in Wave Window - Viewing	495
Figure 12-6. Selected Transaction	496
Figure 12-7. Transaction in Wave Window - Customizing.	497
Figure 12-8. Transaction Stream Properties	498
Figure 12-9. Changing Appearance of Attributes	499
Figure 12-10. Transactions in Objects Window	501
Figure 12-11. Recording Transactions.	503
Figure 13-1. Displaying Two Datasets in the Wave Window	530
Figure 13-2. Open Dataset Dialog Box	533
Figure 13-3. Structure Tabs	534
Figure 13-4. The Dataset Browser.	535
Figure 13-5. Dataset Snapshot Dialog	538
Figure 13-6. Virtual Objects Indicated by Orange Diamond.	540
Figure 14-1. Wave Window Object Pathnames Pane	544
Figure 14-2. Wave Window Object Values Pane	545
Figure 14-3. Wave Window Waveform Pane	545
Figure 14-4. Wave Window Cursor Pane	545
Figure 14-5. Wave Window Messages Bar	546
Figure 14-6. Tabular Format of the List Window	546
Figure 14-7. Original Names of Wave Window Cursors	548
Figure 14-8. Cursor and Timeline Toolbox	548
Figure 14-9. Grid and Timeline Properties	549
Figure 14-10. Cursor Properties Dialog Box	550
Figure 14-11. Find Previous and Next Transition Icons	552
Figure 14-12. Cursor Linking Menu	552
Figure 14-13. Configure Cursor Links Dialog.	553
Figure 14-14. Time Markers in the List Window	553

Figure 14-15. Waveform Pane with Collapsed Event and Delta Time	557
Figure 14-16. Waveform Pane with Expanded Time at a Specific Time	557
Figure 14-17. Waveform Pane with Event Not Logged	558
Figure 14-18. Waveform Pane with Expanded Time Over a Time Range	558
Figure 14-19. List Window After write list -delta none Option is Used	562
Figure 14-20. List Window After write list -delta collapse Option is Used	563
Figure 14-21. List Window After write list -delta all Option is Used	563
Figure 14-22. List Window After write list -event Option is Used	564
Figure 14-23. Bookmark Properties Dialog	566
Figure 14-24. Find Signals by Name or Value	567
Figure 14-25. Wave Signal Search Dialog	568
Figure 14-26. Expression Builder Dialog Box	569
Figure 14-27. Selecting Signals for Expression Builder	570
Figure 14-28. Display Tab of the Wave Window Preferences Dialog Box	572
Figure 14-29. Grid & Timeline Tab of Wave Window Preferences Dialog Box	573
Figure 14-30. Clock Cycles in Timeline of Wave Window	574
Figure 14-31. Changing Signal Radix	574
Figure 14-32. Separate Signals with Wave Window Dividers	576
Figure 14-33. Splitting Wave Window Panes	578
Figure 14-34. Wave groups denoted by red diamond	579
Figure 14-35. Modifying List Window Display Properties	582
Figure 14-36. List Signal Properties Dialog	583
Figure 14-37. Changing the Radix in the List Window	584
Figure 14-38. Save Format Dialog	585
Figure 14-39. Class Objects in the Wave Window	587
Figure 14-40. Class Waveforms	588
Figure 14-41. Class Information Popup	588
Figure 14-42. Waveforms for Class Instances	589
Figure 14-43. Signals Combined to Create Virtual Bus	590
Figure 14-44. Virtual Expression Builder	590
Figure 14-45. Line Triggering in the List Window	591
Figure 14-46. Setting Trigger Properties	592
Figure 14-47. Trigger Gating Using Expression Builder	593
Figure 14-48. Modifying the Breakpoints Dialog	597
Figure 14-49. Signal Breakpoint Dialog	597
Figure 14-50. Breakpoints in the Source Window	598
Figure 14-51. File Breakpoint Dialog Box	599
Figure 14-52. Waveform Comparison Wizard	601
Figure 14-53. Start Comparison Dialog	603
Figure 14-54. Compare Tab in the Workspace Pane	603
Figure 14-55. Structure Browser	604
Figure 14-56. Add Comparison by Region Dialog	605
Figure 14-57. Comparison Methods Tab	606
Figure 14-58. Adding a Clock for a Clocked Comparison	607
Figure 14-59. Waveform Comparison Options	608

List of Figures

Figure 14-60. Viewing Waveform Differences in the Wave Window	609
Figure 14-61. Waveform Difference Details and Markers	610
Figure 14-62. Waveform Differences in the List Window	611
Figure 14-63. Reloading and Redisplaying Compare Differences	612
Figure 15-1. The Dataflow Window	615
Figure 15-2. Dataflow Debugging Usage Flow	616
Figure 15-3. Green Highlighting Shows Your Path Through the Design	620
Figure 15-4. Wave Viewer Displays Inputs and Outputs of Selected Process	621
Figure 15-5. Unknown States Shown as Red Lines in Wave Window	623
Figure 15-6. Dataflow: Point-to-Point Tracing	625
Figure 15-7. The Print Postscript Dialog	630
Figure 15-8. The Print Dialog	630
Figure 15-9. The Dataflow Page Setup Dialog	631
Figure 15-10. Configuring Dataflow Options	632
Figure 16-1. Enabling Code Coverage in the Start Simulation Dialog	639
Figure 16-2. Coverage Data is Shown in Window Tabs	642
Figure 16-3. Toggle Coverage Data in the Objects Window	655
Figure 16-4. Sample Toggle Report	671
Figure 16-5. Coverage Report Text Dialog	672
Figure 18-1. Verification of a Design	694
Figure 18-2. Command Setup Dialog Box	700
Figure 18-3. File Merge Dialog	702
Figure 18-4. Test Data in Verification Browser Window	712
Figure 18-5. HTML Coverage Report	715
Figure 19-1. Specifying Path in C Debug setup Dialog	719
Figure 19-2. Setting Breakpoints in Source Code	721
Figure 19-3. Right Click Pop-up Menu on Breakpoint	721
Figure 19-4. Simulation Stopped at Breakpoint on PLI Task	724
Figure 19-5. Stepping into Next File	725
Figure 19-6. Function Pointer to Foreign Architecture	726
Figure 19-7. Highlighted Line in Associated File	727
Figure 19-8. Stop on quit Button in Dialog	730
Figure 20-1. Status Bar: Profile Samples	736
Figure 20-2. Ranked Window	738
Figure 20-3. Design Units Window	739
Figure 20-4. Calltree Window	740
Figure 20-5. Structural Window	741
Figure 20-6. Profile Details Window: Function Usage	742
Figure 20-7. Profile Details Window: Instance Usage	742
Figure 20-8. Profile Details Window: Callers and Callees	743
Figure 20-9. Accessing Source from Profile Views	744
Figure 20-10. Profile Report Example	746
Figure 20-11. Profile Report Dialog Box	747
Figure 20-12. Example of Memory Data in the Capacity Tab	752
Figure 20-13. Displaying Capacity Objects in the Wave Window	753

Figure 22-1. JobSpy Job Manager	784
Figure 22-2. Job Manager View Waveform	785
Figure 23-1. Waveform Editor: Library Window	790
Figure 23-2. Opening Waveform Editor from Structure or Objects Windows	791
Figure 23-3. Create Pattern Wizard	792
Figure 23-4. Wave Edit Toolbar	793
Figure 23-5. Manipulating Waveforms with the Wave Edit Toolbar and Cursors	795
Figure 23-6. Export Waveform Dialog	797
Figure 23-7. Evcd Import Dialog	798
Figure 24-1. SDF Tab in Start Simulation Dialog	802
Figure 26-1. TDebug Choose Dialog	854
Figure 26-2. Tcl Debugger for vsim	855
Figure 26-3. Setting a Breakpoint in the Debugger	856
Figure 26-4. Variables Dialog Box	857
Figure A-1. Runtime Options Dialog: Defaults Tab	861
Figure A-2. Runtime Options Dialog Box: Assertions Tab	862
Figure A-3. Runtime Options Dialog Box: WLF Files Tab	863
Figure D-1. DPI Use Flow Diagram	954
Figure F-1. Save Current Window Layout Dialog Box	994
Figure F-2. Change Text Fonts for Selected Windows	997
Figure F-3. Making Global Font Changes	997

List of Tables

Table 1-1. Simulation Tasks	45
Table 1-2. Use Modes	50
Table 1-3. Definition of Object by Language	52
Table 1-4. Text Conventions	53
Table 1-5. Documentation List	54
Table 2-1. GUI Windows	57
Table 2-2. Design Object Icons	59
Table 2-3. Icon Shapes and Design Object Types	59
Table 2-4. Graphic Elements of Find Toolbar in Find Mode	61
Table 2-5. Windows That Provide a Filter Mode	62
Table 2-6. Graphic Elements of Search Bar in Filter Mode	62
Table 2-7. Information Displayed in Status Bar	72
Table 2-8. Change Column Toolbar Buttons	75
Table 2-9. Compile Toolbar Buttons	76
Table 2-10. Coverage Toolbar Buttons	77
Table 2-11. Dataflow Toolbar Buttons	78
Table 2-12. FSM Toolbar Buttons	79
Table 2-13. Help Toolbar Buttons	79
Table 2-14. Layout Toolbar Buttons	80
Table 2-15. Memory Toolbar Buttons	80
Table 2-16. Mode Toolbar Buttons	81
Table 2-17. Process Toolbar Buttons	81
Table 2-18. Profile Toolbar Buttons	82
Table 2-19. Schematic Toolbar Buttons	83
Table 2-20. Simulate Toolbar Buttons	83
Table 2-21. Source Toolbar Buttons	85
Table 2-22. Standard Toolbar Buttons	86
Table 2-23. Wave Toolbar Buttons	87
Table 2-24. Wave Bookmark Toolbar Buttons	88
Table 2-25. Wave Compare Toolbar Buttons	88
Table 2-26. Wave Cursor Toolbar Buttons	89
Table 2-27. Wave Edit Toolbar Buttons	90
Table 2-28. Wave Expand Time Toolbar Buttons	91
Table 2-29. Zoom Toolbar Buttons	92
Table 2-30. Class Tree Window Icons	102
Table 2-31. Windows that Show Code Coverage Data	106
Table 2-32. FSM List Window Columns	111
Table 2-33. FSM List Window Popup Menu	111
Table 2-34. FSM Viewer Window — Graphical Elements	113
Table 2-35. FSM View Window Popup Menu	114

Table 2-36. FSM View Menu	115
Table 2-37. Memories	123
Table 2-38. Toggle Coverage Columns in the Objects Window	130
Table 2-39. Source Window Code Coverage Indicators	140
Table 2-40. Columns in the Structure Window	155
Table 2-41. Verification Browser Icons	160
Table 2-42. Message Viewer Tasks	167
Table 2-43. Analog Sidebar Icons	177
Table 2-44. Icons and Actions	178
Table 3-1. Compile Options for the -nodebug Compiling	199
Table 8-1. Example Modules—With and Without Timescale Directive	304
Table 8-2. Evaluation 1 of always Statements	307
Table 8-3. Evaluation 2 of always Statement	308
Table 8-4. IEEE Std 1364 System Tasks and Functions - 1	326
Table 8-5. IEEE Std 1364 System Tasks and Functions - 2	326
Table 8-6. IEEE Std 1364 System Tasks	327
Table 8-7. IEEE Std 1364 File I/O Tasks	327
Table 8-8. SystemVerilog System Tasks and Functions - 1	328
Table 8-9. SystemVerilog System Tasks and Functions - 2	328
Table 8-10. SystemVerilog System Tasks and Functions - 4	329
Table 8-11. Tool-Specific Verilog System Tasks and Functions	329
Table 9-1. Supported Platforms for SystemC	345
Table 9-2. Custom gcc Platform Requirements	346
Table 9-3. Generated Extensions for Each Object Type	356
Table 9-4. Time Unit and Simulator Resolution	365
Table 9-5. Viewable SystemC Objects	368
Table 9-6. Mixed-language Compares	369
Table 9-7. Simple Conversion - sc_main to Module	384
Table 9-8. Using sc_main and Signal Assignments	385
Table 9-9. Modifications Using SCV Transaction Database	386
Table 10-1. VHDL Types Mapped To SystemVerilog Port Vectors	407
Table 10-2. SystemVerilog-to-VHDL Data Types Mapping	416
Table 10-3. Verilog Parameter to VHDL Mapping	418
Table 10-4. Allowed VHDL Types for Verilog Ports	418
Table 10-5. Verilog States Mapped to std_logic and bit	419
Table 10-6. VHDL to SystemVerilog Data Types Mapping	420
Table 10-7. VHDL Generics to Verilog Mapping	421
Table 10-8. Mapping VHDL bit to Verilog States	422
Table 10-9. Mapping VHDL std_logic Type to Verilog States	422
Table 10-10. Channel and Port Type Mapping	423
Table 10-11. Data Type Mapping – SystemC to Verilog or SystemVerilog	424
Table 10-12. Data Type Mapping – Verilog or SystemVerilog to SystemC	427
Table 10-13. Mapping Verilog Port Directions to SystemC	429
Table 10-14. Mapping Verilog States to SystemC States	430
Table 10-15. Mapping SystemC bool to Verilog States	431

List of Tables

Table 10-16. Mapping SystemC sc_bit to Verilog States	431
Table 10-17. Mapping SystemC sc_logic to Verilog States	431
Table 10-18. SystemC Port Type Mapping	432
Table 10-19. Mapping Between SystemC sc_signal and VHDL Types	433
Table 10-20. Mapping VHDL Port Directions to SystemC	436
Table 10-21. Mapping VHDL std_logic States to SystemC States	436
Table 10-22. Mapping SystemC bool to VHDL Boolean States	437
Table 10-23. Mapping SystemC sc_bit to VHDL bit	437
Table 10-24. Mapping SystemC sc_logic to VHDL std_logic	437
Table 10-25. Mapping Literals from VHDL to SystemVerilog	444
Table 10-26. Supported Types Inside VHDL Records	444
Table 10-27. Supported Types Inside SystemVerilog Structure	446
Table 10-28. SystemC Types as Represented in SystemVerilog	473
Table 11-1. Checkpoint and Restore Commands	479
Table 12-1. System Tasks and API for Recording Transactions	504
Table 13-1. WLF File Parameters	531
Table 13-2. Structure Tab Columns	535
Table 13-3. vsim Arguments for Collapsing Time and Delta Steps	539
Table 14-1. Cursor and Timeline Toolbox Icons and Actions	548
Table 14-2. Actions for Cursors	550
Table 14-3. Actions for Time Markers	554
Table 14-4. Recording Delta and Event Time Information	555
Table 14-5. Menu Selections for Expanded Time Display Modes	560
Table 14-6. Actions for Bookmarks	565
Table 14-7. Actions for Dividers	577
Table 14-8. Triggering Options	592
Table 14-9. Mixed-Language Waveform Compares	600
Table 15-1. Icon and Menu Selections for Exploring Design Connectivity	619
Table 15-2. Dataflow Window Links to Other Windows and Panes	629
Table 16-1. Coverage Windows	642
Table 16-2. Condition UDP Truth Table for Line 180	648
Table 16-3. Condition UDP Truth Table for Line 38	649
Table 16-4. Expression UDP Truth Table for line 236	650
Table 17-1. Commands Used for FSM Coverage Collection	682
Table 17-2. Commands Used to Capture FSM Debug Information	685
Table 17-3. FSM Coverage Columns	687
Table 17-4. Additional FSM-Related Arguments	688
Table 17-5. Recognized FSM Note Parameters	689
Table 17-6. FSM Recognition Info Note Parameters	689
Table 18-1. Coverage Modes	695
Table 18-2. Predefined Fields in UCDB Test Attribute Record	709
Table 19-1. Supported Platforms and gdb Versions	718
Table 19-2. Simulation Stepping Options in C Debug	721
Table 19-3. Command Reference for C Debug	730
Table 20-1. How to Enable and View Capacity Analysis	749

Table 21-1. Signal Spy Reference Comparison	757
Table 22-1. SIMulation Commands You can Issue from JobSpy	781
Table 23-1. Signal Attributes in Create Pattern Wizard	792
Table 23-2. Waveform Editing Commands	793
Table 23-3. Selecting Parts of the Waveform	794
Table 23-4. Wave Editor Mouse/Keyboard Shortcuts	796
Table 23-5. Formats for Saving Waveforms	797
Table 23-6. Examples for Loading a Stimulus File	797
Table 24-1. Matching SDF to VHDL Generics	804
Table 24-2. Matching SDF IOPATH to Verilog	807
Table 24-3. Matching SDF INTERCONNECT and PORT to Verilog	807
Table 24-4. Matching SDF PATHPULSE and GLOBALPATHPULSE to Verilog	808
Table 24-5. Matching SDF DEVICE to Verilog	808
Table 24-6. Matching SDF SETUP to Verilog	808
Table 24-7. Matching SDF HOLD to Verilog	808
Table 24-8. Matching SDF SETUPHOLD to Verilog	809
Table 24-9. Matching SDF RECOVERY to Verilog	809
Table 24-10. Matching SDF REMOVAL to Verilog	809
Table 24-11. Matching SDF RECREM to Verilog	809
Table 24-12. Matching SDF SKEW to Verilog	809
Table 24-13. Matching SDF WIDTH to Verilog	810
Table 24-14. Matching SDF PERIOD to Verilog	810
Table 24-15. Matching SDF NOCHANGE to Verilog	810
Table 24-16. Matching Verilog Timing Checks to SDF SETUP	810
Table 24-17. SDF Data May Be More Accurate Than Model	811
Table 24-18. Matching Explicit Verilog Edge Transitions to Verilog	811
Table 24-19. SDF Timing Check Conditions	811
Table 24-20. SDF Path Delay Conditions	812
Table 24-21. Disabling Timing Checks	813
Table 25-1. VCD Commands and SystemTasks	822
Table 25-2. VCD Dumpport Commands and System Tasks	822
Table 25-3. VCD Commands and System Tasks for Multiple VCD Files	822
Table 25-4. SystemC Types	823
Table 25-5. Driver States	827
Table 25-6. State When Direction is Unknown	827
Table 25-7. Driver Strength	828
Table 25-8. Values for file_format Argument	830
Table 25-9. Sample Driver Data	831
Table 26-1. Changes to ModelSim Commands	834
Table 26-2. Tcl Backslash Sequences	836
Table 26-3. Tcl List Commands	843
Table 26-4. Simulator-Specific Tcl Commands	844
Table 26-5. Tcl Time Conversion Commands	845
Table 26-6. Tcl Time Relation Commands	845
Table 26-7. Tcl Time Arithmetic Commands	846

List of Tables

Table 26-8. Commands for Handling Breakpoints and Errors in Macros	851
Table 26-9. Tcl Debug States	856
Table A-1. Runtime Option Dialog: Defaults Tab Contents	861
Table A-2. Runtime Option Dialog: Assertions Tab Contents	862
Table A-3. Runtime Option Dialog: WLF Files Tab Contents	863
Table A-4. Commands for Overriding the Default Initialization File	864
Table A-5. License Variable: License Options	888
Table A-6. MessageFormat Variable: Accepted Values	889
Table C-1. Severity Level Types	935
Table C-2. Exit Codes	938
Table D-1. VPI Compatibility Considerations	948
Table D-2. vsim Arguments for DPI Application	970
Table D-3. Supported VHDL Objects	976
Table D-4. Supported ACC Routines	977
Table D-5. Supported TF Routines	979
Table D-6. Values for <action> Argument	981
Table E-1. Command History Shortcuts	985
Table E-2. Mouse Shortcuts	986
Table E-3. Keyboard Shortcuts	986
Table E-4. List Window Keyboard Shortcuts	989
Table E-5. Wave Window Mouse Shortcuts	989
Table E-6. Wave Window Keyboard Shortcuts	990
Table F-1. Predefined GUI Layouts	993
Table F-2. Global Fonts	997
Table G-1. Files Accessed During Startup	1001
Table G-2. Add Library Mappings to modelsim.ini File	1010

Chapter 1

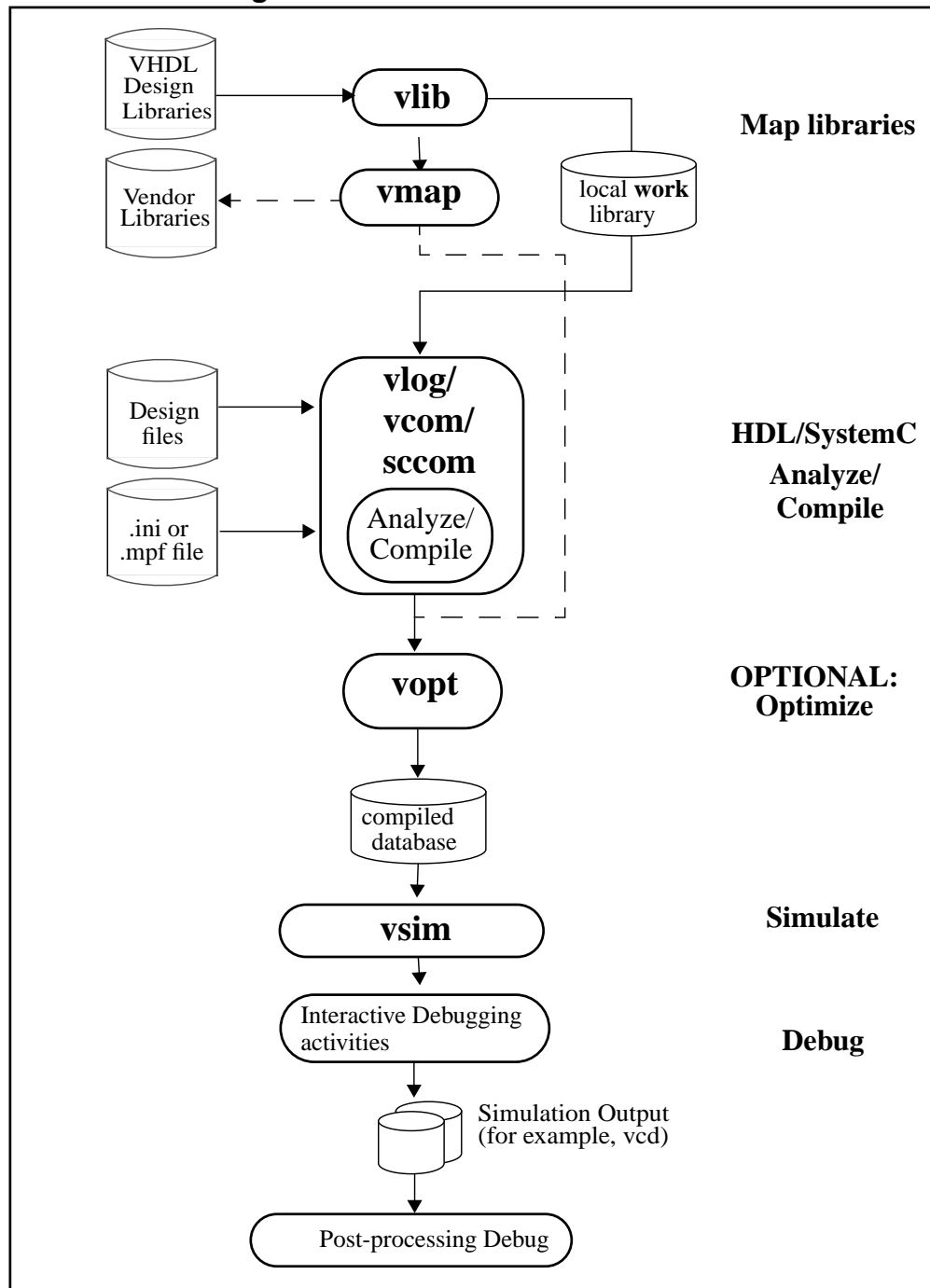
Introduction

This documentation was written for UNIX, Linux, and Microsoft Windows users. Not all versions of ModelSim are supported on all platforms. Contact your Mentor Graphics sales representative for details.

Tool Structure and Flow

The diagram below illustrates the structure of the ModelSim tool, and the flow of that tool as it is used to verify a design.

Figure 1-1. Tool Structure and Flow



Simulation Task Overview

The following table provides a reference for the tasks required for compiling, optimizing, loading, and simulating a design in ModelSim.

Table 1-1. Simulation Tasks







Task	Example Command Line Entry	GUI Menu Pull-down	GUI Icons
Step 1: Map libraries	vlib <library_name> vmmap work <library_name>	1. File > New > Project 2. Enter library name 3. Add design files to project	N/A
Step 2: Compile the design	vlog file1.v file2.v ... (Verilog) vcom file1.vhd file2.vhd ... (VHDL) sccom <top> (SystemC) sccom -link <top>	Compile > Compile or Compile > Compile All	Compile or Compile All icons:  
Step 3: Optimize the design (OPTIONAL)	Optimized when voptflow = 1 in modelsim.ini file (default setting for version 6.2 and later.	To disable optimizations: 1. Simulate > Start Simulation 2. Deselect Enable Optimization button To set optimization options: 1. Simulate > Design Optimization 2. Set desired optimizations	N/A
Step 4: Load the design into the simulator	vsim <top> or vsim <opt_name>	1. Simulate > Start Simulation 2. Click on top design module or optimized design unit name 3. Click OK This action loads the design for simulation.	Simulate icon: 
Step 5: Run the simulation	run step	Simulate > Run	Run , or Run continue , or Run -all icons:   

Table 1-1. Simulation Tasks

Task	Example Command Line Entry	GUI Menu Pull-down	GUI Icons
Step 6: Debug the design Note: Design optimization in step 3 limits debugging visibility	Common debugging commands: bp describe drivers examine force log show	N/A	N/A

Basic Steps for Simulation

This section provides further detail related to each step in the process of simulating your design using ModelSim.

Step 1 — Collecting Files and Mapping Libraries

Files needed to run ModelSim on your design:

- design files (VHDL, Verilog, and/or SystemC), including stimulus for the design
- libraries, both working and resource
- modelsim.ini (automatically created by the library mapping command)

Providing Stimulus to the Design

You can provide stimulus to your design in several ways:

- Language based test bench
- Tcl-based ModelSim interactive command, [force](#)
- VCD files / commands

See [Creating a VCD File](#) and [Using Extended VCD as Stimulus](#)

- 3rd party test bench generation tools

What is a Library?

A library is a location where data to be used for simulation is stored. Libraries are ModelSim's way of managing the creation of data before it is needed for use in simulation. It also serves as a way to streamline simulation invocation. Instead of compiling all design data each and every

time you simulate, ModelSim uses binary pre-compiled data from these libraries. So, if you make a changes to a single Verilog module, only that module is recompiled, rather than all modules in the design.

Working and Resource Libraries

Design libraries can be used in two ways: 1) as a local working library that contains the compiled version of your design; 2) as a resource library. The contents of your working library will change as you update your design and recompile. A resource library is typically unchanging, and serves as a parts source for your design. Examples of resource libraries might be: shared information within your group, vendor libraries, packages, or previously compiled elements of your own working design. You can create your own resource libraries, or they may be supplied by another design team or a third party (for example, a silicon vendor).

For more information on resource libraries and working libraries, see [Working Library Versus Resource Libraries](#), [Managing Library Contents](#), [Working with Design Libraries](#), and [Specifying Resource Libraries](#).

Creating the Logical Library (vlib)

Before you can compile your source files, you must create a library in which to store the compilation results. You can create the logical library using the GUI, using **File > New > Library** (see [Creating a Library](#)), or you can use the `vlib` command. For example, the command:

```
vlib work
```

creates a library named **work**. By default, compilation results are stored in the **work** library.

Mapping the Logical Work to the Physical Work Directory (vmap)

VHDL uses logical library names that can be mapped to ModelSim library directories. If libraries are not mapped properly, and you invoke your simulation, necessary components will not be loaded and simulation will fail. Similarly, compilation can also depend on proper library mapping.

By default, ModelSim can find libraries in your current directory (assuming they have the right name), but for it to find libraries located elsewhere, you need to map a logical library name to the pathname of the library.

You can use the GUI ([Library Mappings with the GUI](#)), a command ([Library Mapping from the Command Line](#)), or a project ([Getting Started with Projects](#)) to assign a logical name to a design library.

The format for command line entry is:

```
vmap <logical_name> <directory_pathname>
```

This command sets the mapping between a logical library name and a directory.

Step 2 — Compiling the Design (vlog, vcom, sccom)

Designs are compiled with one of the three language compilers.

Compiling Verilog (vlog)

ModelSim's compiler for the Verilog modules in your design is [vlog](#). Verilog files may be compiled in any order, as they are not order dependent. See [Verilog Compilation](#) for details.

Compiling VHDL (vcom)

ModelSim's compiler for VHDL design units is [vcom](#). VHDL files must be compiled according to the design requirements of the design. Projects may assist you in determining the compile order: for more information, see [Auto-Generating Compile Order](#). See [Compilation and Simulation of VHDL](#) for details on VHDL compilation.

Compiling SystemC (sccom)

ModelSim's compiler for SystemC design units is [sccom](#), and is used only if you have SystemC components in your design. See [Compiling SystemC Files](#) for details.

Step 3 — Loading the Design for Simulation

vsim topLevelModule

Your design is ready for simulation after it has been compiled. You may then invoke [vsim](#) with the names of the top-level modules (many designs contain only one top-level module). For example, if your top-level modules are "testbench" and "globals", then invoke the simulator as follows:

```
vsim testbench globals
```

After the simulator loads the top-level modules, it iteratively loads the instantiated modules and UDPs in the design hierarchy, linking the design together by connecting the ports and resolving hierarchical references.

You can optionally optimize the design with [vopt](#). For more information on optimization, see [Optimizing Designs with vopt](#).

Using SDF

You can incorporate actual delay values to the simulation by applying SDF back-annotation files to the design. For more information on how SDF is used in the design, see [Specifying SDF Files for Simulation](#).

Step 4 — Simulating the Design

Once the design has been successfully loaded, the simulation time is set to zero, and you must enter a **run** command to begin simulation. For more information, see [Verilog and SystemVerilog Simulation](#), [SystemC Simulation](#), and [VHDL Simulation](#).

The basic simulator commands are:

- [add wave](#)
- [force](#)
- [bp](#)
- [run](#)
- [step](#)

Step 5 — Debugging the Design

Numerous tools and windows useful in debugging your design are available from the ModelSim GUI. In addition, several basic simulation commands are available from the command line to assist you in debugging your design:

- [describe](#)
- [drivers](#)
- [examine](#)
- [force](#)
- [log](#)
- [checkpoint](#)
- [restore](#)
- [show](#)

Modes of Operation

Many users run ModelSim interactively—pushing buttons and/or pulling down menus in a series of windows in the GUI (graphical user interface). But there are really three modes of ModelSim operation, the characteristics of which are outlined in the following table.:

Table 1-2. Use Modes

ModelSim use mode	Characteristics	How ModelSim is invoked
GUI	interactive; has graphical windows, push-buttons, menus, and a command line in the transcript. Default mode	via a desktop icon or from the OS command shell prompt. Example: <code>OS> vsim</code>
Command-line	interactive command line; no GUI	with -c argument at the OS command prompt. Example: <code>OS> vsim -c</code>
Batch	non-interactive batch script; no windows or interactive command line	at OS command shell prompt using "here document" technique or redirection of standard input. Example: <code>C:\ vsim vfiles.v <infile >outfile</code>

The ModelSim User's Manual focuses primarily on the GUI mode of operation. However, this section provides an introduction to the Command-line and Batch modes.

A command is available to help batch users access commands not available for use in batch mode. See the [batch_mode](#) command for more details.

Command Line Mode

In command line mode ModelSim executes any startup command specified by the [Startup](#) variable in the *modelsim.ini* file. If `vsim` is invoked with the **-do "command_string"** option, a DO file (macro) is called. A DO file executed in this manner will override any startup command in the *modelsim.ini* file.

During simulation a transcript file is created containing any messages to stdout. A transcript file created in command line mode may be used as a DO file if you invoke the [transcript on](#) command after the design loads (see the example below). The [transcript on](#) command writes all of the commands you invoke to the transcript file. For example, the following series of commands results in a transcript file that can be used for command input if *top* is re-simulated (remove the **quit -f** command from the transcript file if you want to remain in the simulator).

```
vsim -c top
```

library and design loading messages... then execute:

```
transcript on
force clk 1 50, 0 100 -repeat 100
run 500
run @5000
quit -f
```

Rename transcript files that you intend to use as DO files. They will be overwritten the next time you run **vsim** if you don't rename them. Also, simulator messages are already commented out, but any messages generated from your design (and subsequently written to the transcript file) will cause the simulator to pause. A transcript file that contains only valid simulator commands will work fine; comment out anything else with a "#".

Stand-alone tools pick up project settings in command line mode if they are invoked in the project's root directory. If invoked outside the project directory, stand-alone tools pick up project settings only if you set the **MODELSIM** environment variable to the path to the project file (*<Project_Root_Dir>/<Project_Name>.mpf*).

Basic Command Line Editing and Navigation

While in command line mode you can use basic command line editing and navigation techniques similar to other command line environments, such as:

- History navigation — use the up and down arrows to select commands you have already used.
- Command line editing — use the left and right arrows to edit your current command line.
- Filename completion — use the Tab key to expand filenames.

Batch Mode

Batch mode is an operational mode that provides neither an interactive command line nor interactive windows. In a Windows environment, **vsim** is run from a Windows command prompt and standard input and output are redirected to and from files.

In a UNIX environment, **vsim** can be invoked in batch mode by redirecting standard input using the “here-document” technique.

Here is an example of the "here-document" technique:

```
vsim top <<!
log -r *
run 100
do test.do
quit -f
!
```

Here is an example of a batch mode simulation using redirection of std input and output:

```
vsim counter < yourfile > outfile
```

where "yourfile" is a script containing various ModelSim commands.

You can use the CTRL-C keyboard interrupt to break batch simulation in UNIX and Windows environments.

What is an "Object"

Because ModelSim works with so many languages (SystemC, Verilog, VHDL, SystemVerilog,), an "object" refers to any valid design element in those languages. The word "object" is used whenever a specific language reference is not needed. Depending on the context, "object" can refer to any of the following:

Table 1-3. Definition of Object by Language

Language	An object can be
VHDL	block statement, component instantiation, constant, generate statement, generic, package, signal, alias, or variable
Verilog	function, module instantiation, named fork, named begin, net, task, register, or variable
SystemVerilog	In addition to those listed above for Verilog: class, package, program, interface, array, directive, property, or sequence
SystemC	module, channel, port, variable, or aggregate
PSL	property, sequence, directive, or endpoint

Graphic Interface Overview

While your operating system interface provides the window-management frame, ModelSim controls all internal-window features including menus, buttons, and scroll bars. Because ModelSim's graphic interface is based on Tcl/TK, you also have the tools to build your own simulation environment. Preference variables and configuration commands (see [modelsim.ini Variables](#) for details) give you control over the use and placement of windows, menus, menu options, and buttons. See [Tcl and Macros \(DO Files\)](#) for more information on Tcl.

Standards Supported

ModelSim VHDL implements the VHDL language as defined by IEEE Standards 1076-1987, 1076-1993, and 1076-2002. ModelSim also supports the 1164-1993 *Standard Multivalued Logic System for VHDL Interoperability*, and the 1076.2-1996 *Standard VHDL Mathematical Packages* standards. Any design developed with ModelSim will be compatible with any other VHDL system that is compliant with the 1076 specifications.

ModelSim Verilog implements the Verilog language as defined by the IEEE Std 1364-1995 and 1364-2005. ModelSim Verilog also supports a partial implementation of SystemVerilog 1800-2005 (see `<install_dir>/docs/technotes/sysvlog.note` for implementation details). Both PLI (Programming Language Interface) and VCD (Value Change Dump) are supported for ModelSim users.

In addition, all products support SDF 1.0 through 4.0 (except the NETDELAY statement), VITAL 2.2b, VITAL'95 – IEEE 1076.4-1995, and VITAL 2000 – IEEE 1076.4-2000.

ModelSim implements the SystemC language based on the Open SystemC Initiative (OSCI) SystemC 2.2 reference simulator.

Assumptions

We assume that you are familiar with the use of your operating system and its graphical interface.

We also assume that you have a working knowledge of the design languages. Although ModelSim is an excellent tool to use while learning HDL concepts and practices, this document is not written to support that goal.

Finally, we assume that you have worked the appropriate lessons in the *ModelSim Tutorial* and are familiar with the basic functionality of ModelSim. The *ModelSim Tutorial* is available from the ModelSim **Help** menu.

Text Conventions

Text conventions used in this manual include:

Table 1-4. Text Conventions

Text Type	Description
<i>italic text</i>	provides emphasis and sets off filenames, pathnames, and design unit names
bold text	indicates commands, command options, menu choices, package and library logical names, as well as variables, dialog box selections, and language keywords
monospace type	monospace type is used for program and command examples
The right angle (>)	is used to connect menu choices when traversing menus as in: File > Quit

Table 1-4. Text Conventions

Text Type	Description
path separators	examples will show either UNIX or Windows path separators - use separators appropriate for your operating system when trying the examples
UPPER CASE	denotes file types used by ModelSim (such as, DO, WLF, INI, MPF, PDF, and so forth.)

Installation Directory Pathnames

When referring to installation paths, this manual uses “<installDir>” as a generic representation of the installation directory for all versions of ModelSim. The actual installation directory on your system may contain version information.

Where to Find Our Documentation

Table 1-5. Documentation List

Document	Format	How to get it
<i>Installation & Licensing Guide</i>	PDF	Help > PDF Bookcase
	HTML and PDF	Help > InfoHub
<i>Quick Guide</i> (command and feature quick-reference)	PDF	Help > PDF Bookcase and Help > InfoHub
<i>Tutorial</i>	PDF	Help > PDF Bookcase
	HTML and PDF	Help > InfoHub
<i>User’s Manual</i>	PDF	Help > PDF Bookcase
	HTML and PDF	Help > InfoHub
<i>Reference Manual</i>	PDF	Help > PDF Bookcase
	HTML and PDF	Help > InfoHub
<i>Foreign Language Interface Manual</i>	PDF	Help > PDF Bookcase
	HTML	Help > InfoHub
Std_DevelopersKit User’s Manual	PDF	www.model.com/support/documentation/BOOK/sdk_um.pdf The Standard Developer’s Kit is for use with Mentor Graphics QuickHDL.

Table 1-5. Documentation List

Document	Format	How to get it
Command Help	ASCII	type help [command name] at the prompt in the Transcript pane
Error message help	ASCII	type verror <msgNum> at the Transcript or shell prompt
Tcl Man Pages (Tcl manual)	HTML	select Help > Tcl Man Pages , or find <i>contents.htm</i> in <code>\modeltech\docs\tcl_help_html</code>
Technotes	HTML	available from the support site

Mentor Graphics Support

Mentor Graphics software support includes software enhancements, technical support, access to comprehensive online services with SupportNet, and the optional On-Site Mentoring service. For details, see:

<http://supportnet.mentor.com/about/>

If you have questions about this software release, please log in to SupportNet. You may search thousands of technical solutions, view documentation, or open a Service Request online at:

<http://supportnet.mentor.com/>

If your site is under current support and you do not have a SupportNet login, you may easily register for SupportNet by filling out the short form at:

<http://supportnet.mentor.com/user/register.cfm>

All customer support contact information can be found on our web site at:

<http://supportnet.mentor.com/contacts/supportcenters/>

Additional Support

Online and email technical support options, maintenance renewal, and links to international support contacts:

<http://www.model.com/support>

Access to the most current version of ModelSim:

<http://www.model.com/downloads/>

Place your name on our list for email notification of news and updates:

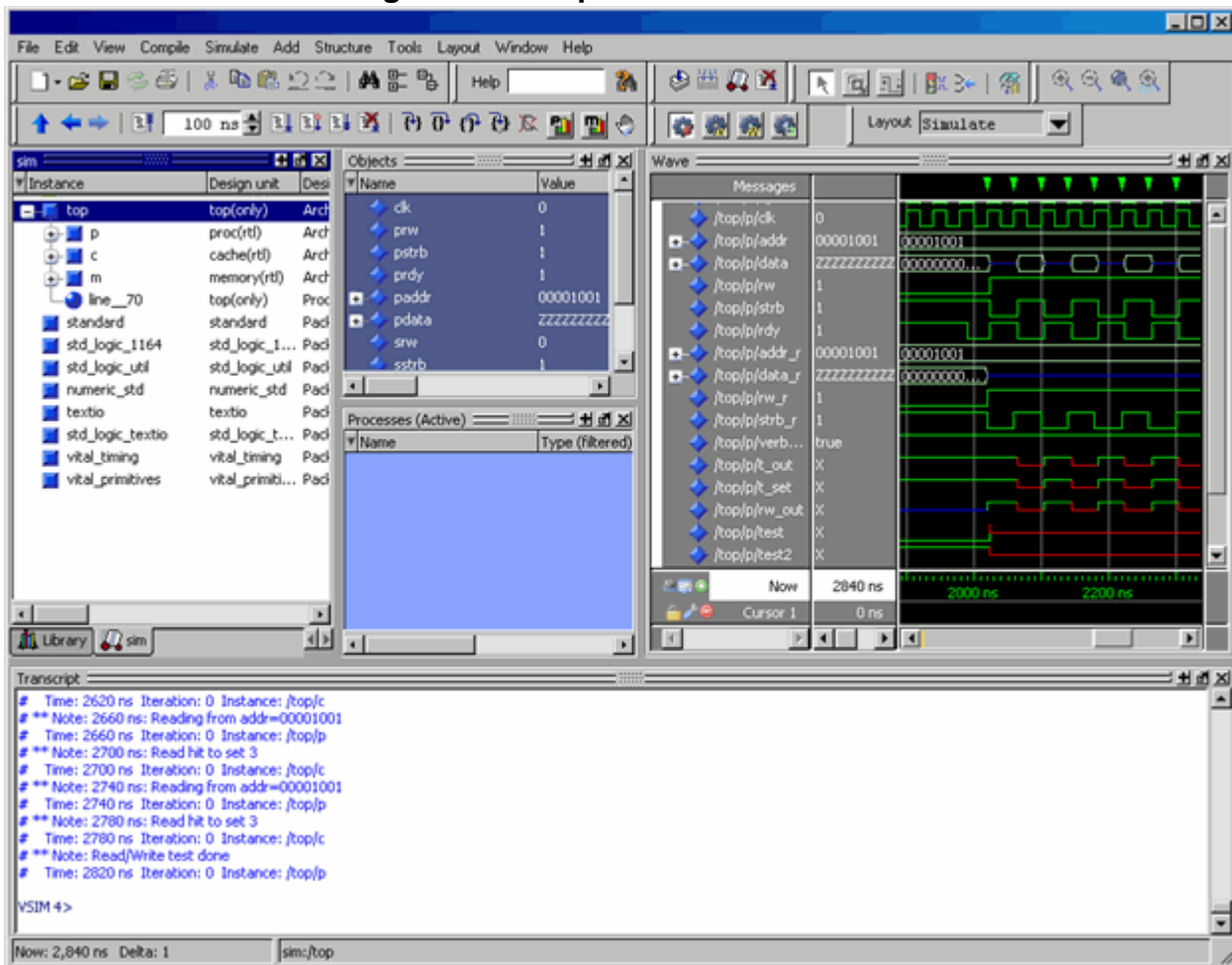
http://www.model.com/resources/resources_newsletter.asp

Chapter 2

Graphical User Interface

ModelSim's graphical user interface (GUI) consists of various windows that give access to parts of your design and numerous debugging tools. All windows display within the ModelSim Main window.

Figure 2-1. Graphical User Interface



The following table summarizes all of the available windows.

Table 2-1. GUI Windows

Window name	Description	More details
Main	central GUI access point	Main Window

Table 2-1. GUI Windows

Window name	Description	More details
Process	displays all processes that are scheduled to run during the current simulation cycle	Processes Window
Class Browsers	displays interactive relationships of SystemVerilog classes	Class Tree Window Class Graph Window
Code coverage	a collection of windows that display code coverage data	Windows Containing Code Coverage Data
Dataflow	displays "physical" connectivity and lets you trace events (causality)	Dataflow Window
List	shows waveform data in a tabular format	List Window
Locals	displays data objects that are immediately visible at the current execution point of the selected process	Locals Window
Memory	windows that show memories and their contents	Memory and Memory Data Windows
Watch	displays signal or variable values at the current simulation time	Watch Window
Objects	displays all declared data objects in the current scope	Objects Window
Profile	windows that display performance and memory profiling data	Profiling Windows
Source	a text editor for viewing and editing files: HDL, SystemC, DO. and so forth.	Source Window
Verification Management	displays information about your UCDB test bench	Verification Browser Window
Transcript	keeps a running history of commands and messages and provides a command-line interface	Transcript Window
Wave	displays waveforms	Wave Window

The windows are customizable in that you can position and size them as you see fit, and ModelSim will remember your settings upon subsequent invocations. You can restore ModelSim windows and panes to their original settings by selecting Layout > Reset in the menu bar.

Design Object Icons and Their Meaning







The color and shape of icons convey information about the language and type of a design object. [Table 2-2](#) shows the icon colors and the languages they indicate.

Table 2-2. Design Object Icons

Icon color	Design Language
light blue	Verilog or SystemVerilog
dark blue	VHDL
green	SystemC
orange	virtual object

Here is a list of icon shapes and the design object types they indicate:

Table 2-3. Icon Shapes and Design Object Types

Icon shape	Example	Design Object Type
Square		any scope (VHDL block, Verilog named block, SC module, class, interface, task, function, and so forth.)
Circle		process
Diamond		valued object (signals, nets, registers, SystemC channel, and so forth.)
Caution Sign		comparison object
Diamond with red dot		an editable waveform created with the waveform editor
Star		transaction; The color of the star for each transaction depends on the language of the region in which the transaction stream occurs: dark blue for VHDL, light blue for Verilog and SystemVerilog, green for SystemC.

Setting Fonts

You may need to adjust font settings to accommodate the aspect ratios of wide screen and double screen displays or to handle launching ModelSim from an X-session.

Font Scaling

To change font scaling, select the Transcript window, then **Transcript > Adjust Font Scaling**. You will need a ruler to complete the instructions in the lower right corner of the dialog. When you have entered the pixel and inches information, click OK to close the dialog. Then, restart

ModelSim to see the change. This is a one time setting; you should not need to set it again unless you change display resolution or the hardware (monitor or video card). The font scaling applies to Windows and UNIX operating systems. On UNIX systems, the font scaling is stored based on the \$DISPLAY environment variable.

Using the Find and Filter Functions

Finding and/or filtering capabilities are available for most windows. The filtering function is denoted by a “Contains” field (Figure 2-3).

Figure 2-2. Find Mode



Figure 2-3. Filter Mode




For windows that support both find (Figure 2-2) and filter modes (Figure 2-3), you can toggle between the two modes by doing any one of the following:

- Use the **Ctrl-M** hotkey.
- Click the “Find” or “Contains” words in the toolbar.
- Select the mode from the Find Options popup menu (see [Using the Find Options Popup Menu](#)).

The last selected mode is remembered between sessions.

A “Find” toolbar will appear along the bottom edge of the active window when you do any one of the following:

- Select **Edit > Find** in the menu bar.
- Click the **Find** icon in the toolbar. 
- Right-click anywhere in the active window and select **Find** from the popup menu.
- Press **Ctrl-F** on your Windows keyboard.

All of the above actions are toggles - repeat the action and the Find toolbar will close.

There is a simple history mechanism to allow saving search strings for later use. The keyboard shortcuts to support this are:

- Ctrl -S — save current search text into history list
- Ctrl-P — retrieve previous search text

- Ctrl-N — retrieve next search text









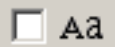


Other hotkey actions include:

- Esc — closes the Find toolbar
- Enter (Windows) or Return (UNIX or Linux) — initiates a “Find Next” action
- Ctrl-T — search while typing (default is on)

The search entry field turns red if no matches are found.

The graphic elements associated with the Find toolbar are shown in [Table 2-4](#).

Table 2-4. Graphic Elements of Find Toolbar in Find Mode

Graphic Element	Action
 Find	opens the find toolbar in the active window
 Close	closes the find toolbar
 Find entry field	allows entry of find parameters
 Find Options	opens the Find Options popup menu
 Clear Entry Field	clears the entry field
 Execute Search	initiates the search
 Toggle Search Direction	toggles search direction upward or downward through the active window
 Find All Matches; Bookmark All Matches (for Source window only)	highlights every occurrence of the find item; for the Source window only, places a blue flag (bookmark) at every occurrence of the find item
<input type="checkbox"/>  Match Case	search must match the case of the text entered in the Find field
<input type="checkbox"/>  Exact (whole word)	searches for whole words that match those entered in the Find field
<input type="checkbox"/>  Regular Expression	searches for a regular expression

To remove bookmarks from the Source window, select **Source > Clear Bookmarks** from the menu bar when the Source window is active.

Using the Filter Mode



The filter mode allows you to filter information in the following windows:

Table 2-5. Windows That Provide a Filter Mode

Coverage, Assertions, and Cover Directives
Memory
Objects
Process
Structure and File Windows
Class Tree
Message Viewer
Verification Test Browser and Tracker

By entering a string in the “Contains” text entry box, you can filter the view of the selected window down to the specific information you are looking for.

Table 2-6. Graphic Elements of Search Bar in Filter Mode

Button	Name	Shortcuts	Description
	Filter Regular Expression	None	A drop down menu that allows you to set the wildcard mode. A text entry box for your filter string.
	Clear Filter	None	Clears the text entry box and removes the filter from the active window.

Wildcard Usage

There are three wildcard modes:

- **glob-style** — Allows you to use the following special wildcard characters:
 - * — matches any sequence of characters in the string
 - ? — matches any single character in the string
 - [<chars>] — matches any character in the set <chars>.
 - \

For more information refer to the Tcl documentation:

Help > Tcl Man Pages
Tcl Commands > string > string match

- **regular-expression** — allows you to use wildcard characters based on Tcl regular expressions. For more information refer to the Tcl documentation:

Help > Tcl Man Pages
Tcl Commands > re_syntax

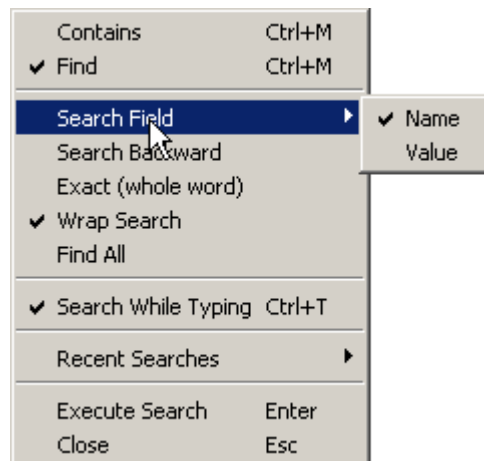
- **exact** — indicates that no characters have special meaning, thus disabling wildcard features.

The text entry box of the Contains toolbar item is case-insensitive, If you need to search for case-sensitive strings use “regular-expression” and prepend the string with (?c)

Using the Find Options Popup Menu

When you click the Find Options icon in the Find entry field it will open a Find Options popup menu (Figure 2-4).

Figure 2-4. Find Options Popup Menu



The Find Options menu displays the search options available to you as well as hot keys for initiating the actions without the menu.

User-Defined Radices

A user definable radix is used to map bit patterns to a set of enumeration labels. After defining a new radix, the radix will be available for use in the List, Watch, and Wave windows or with the [examine](#) command.

There are four commands used to manage user defined radices:

- [radix define](#)

- [radix names](#)
- [radix list](#)
- [radix delete](#)

Using the radix define Command

The [radix define](#) command is used to create or modify a radix. It must include a radix name and a definition body, which consists of a list of number pattern, label pairs. Optionally, it may include the `-color` argument for setting the radix color (see [Example 2-2](#)).

```
{  
    <numeric-value> <enum-label>,  
    <numeric-value> <enum-label>  
    -default <radix>  
}
```

A `<numeric-value>` is any legitimate HDL integer numeric literal. To be more specific:

```
<base>#<base-integer># --- <base> is 2, 8, 10, or 16  
<base>"bit-value" --- <base> is B, O, or X  
<integer>  
<size>'<base><number> --- <size> is an integer, <base> is b, d, o, or h.
```

Check the Verilog and VHDL LRMs for exact definitions of these numeric literals.

The comma (,) in the definition body is optional. The `<enum-label>` is any arbitrary string. It should be quoted (""), especially if it contains spaces.

The `-default` entry is optional. If present, it defines the radix to use if a match is not found for a given value. The `-default` entry can appear anywhere in the list, it does not have to be at the end.

[Example 2-1](#) shows the [radix define](#) command used to create a radix called “States,” which will display state values in the List, Watch, and Wave windows instead of numeric values.

Example 2-1. Using the radix define Command

```
radix define States {  
    11'b000000000001 "IDLE",  
    11'b000000000010 "CTRL",  
    11'b000000000100 "WT_WD_1",  
    11'b000000001000 "WT_WD_2",  
    11'b000000010000 "WT_BLK_1",  
    11'b000000100000 "WT_BLK_2",  
    11'b000001000000 "WT_BLK_3",  
    11'b000010000000 "WT_BLK_4",  
    11'b000100000000 "WT_BLK_5",  
    11'b010000000000 "RD_WD_1",  
    11'b100000000000 "RD_WD_2",  
    -default hex  
}
```


Figure 2-5 shows an FSM signal called `/test-sm/sm_seq0/sm_0/state` in the Wave window with a binary radix and with the user-defined “States” radix (as defined in Example 2-1).

Figure 2-5. User-Defined Radix “States” in the Wave Window

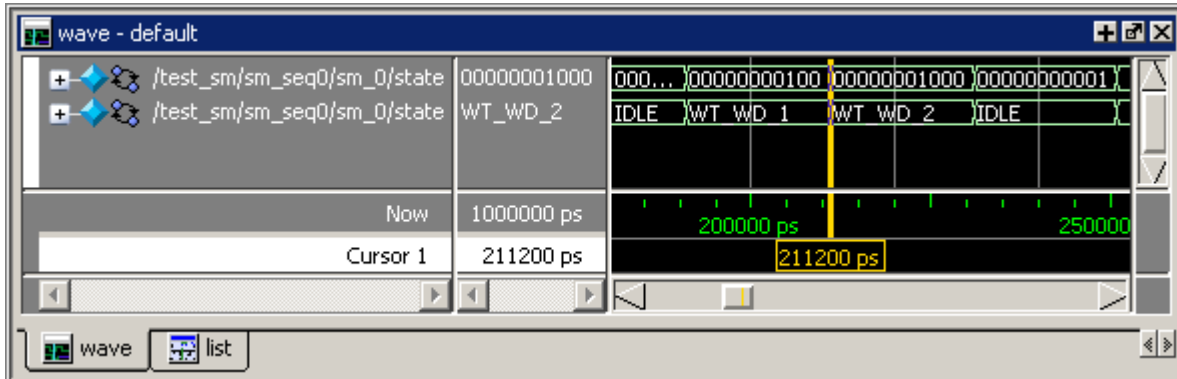
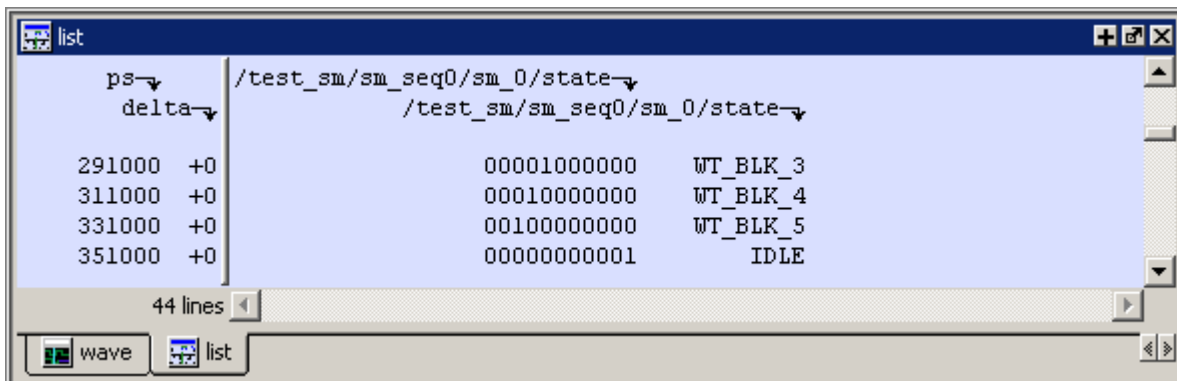


Figure 2-6 shows an FSM signal called `/test-sm/sm_seq0/sm_0/state` in the List window with a binary radix and with the user-defined “States” radix (as defined in Example 2-1)

Figure 2-6. User-Defined Radix “States” in the List Window



Using radix define to Specify Radix Color

The following example illustrates how to use the `radix define` command to specify the radix color:

Example 2-2. Using radix define to Specify Color

```
radix define States {
  11'b000000000001 "IDLE" -color yellow,
  11'b000000000010 "CTRL" -color #ffee00,
  11'b000000000100 "WT_WD_1" -color orange,
  11'b000000001000 "WT_WD_2" -color orange,
  11'b000000010000 "WT_BLK_1",
  11'b000000100000 "WT_BLK_2",
  11'b000001000000 "WT_BLK_3",
  11'b000010000000 "WT_BLK_4",
```

```

11'b001000000000 "WT_BLK_5",
11'b010000000000 "RD_WD_1" -color green,
11'b100000000000 "RD_WD_2" -color green,
-default hex
-defaultcolor white
}

```

If a pattern/label pair does not specify a color, the normal wave window colors will be used. If the value of the waveform does not match any pattern, then the `-default radix` and `-defaultcolor` will be used.

To specify a range of values, wildcards may be specified for bits or characters of the value. The wildcard character is '?', similar to the iteration character in a Verilog UDP, for example:

```

radix define {
  6'b01??00 "Write" -color orange,
  6'b10??00 "Read" -color green
}

```

In this example, the first pattern will match "010000", "010100", "011000", and "011100". In case of overlaps, the first matching pattern is used, going from top to bottom.

Saving and Reloading Formats and Content

You can use the [write format](#) restart command to create a single `.do` file that will recreate all debug windows and breakpoints (see [Saving and Restoring Breakpoints](#)) when invoked with the `do` command in subsequent simulation runs. The syntax is:

```
write format restart <filename>
```

If the [ShutdownFile](#) `modelsim.ini` variable is set to this `.do` filename, it will call the [write format](#) restart command upon exit.

Main Window

The primary access point in the ModelSim GUI is called the Main window. It provides convenient access to design libraries and objects, source files, debugging commands, simulation status messages, and so forth. When you load a design, or bring up debugging tools, ModelSim opens windows appropriate for your debugging environment.

Elements of the Main Window

The following sections outline the GUI terminology used in this manual.

[Menu Bar](#)

[Toolbar Frame](#)

[Toolbar](#)

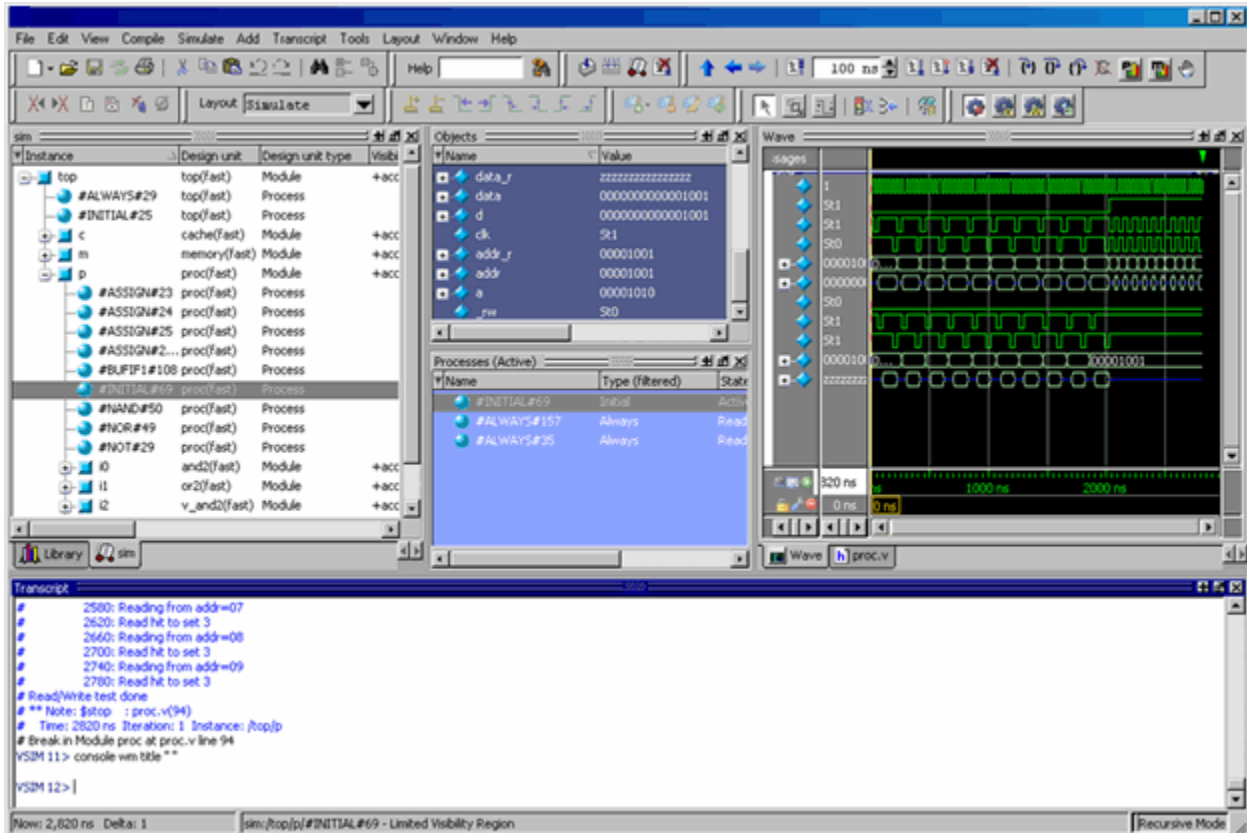
[Window](#)

[Tab Group](#)

[Pane](#)

The Main window is the primary access point in the GUI. [Figure 2-7](#) shows an example of the Main window during a simulation run.

Figure 2-7. Main Window of the GUI



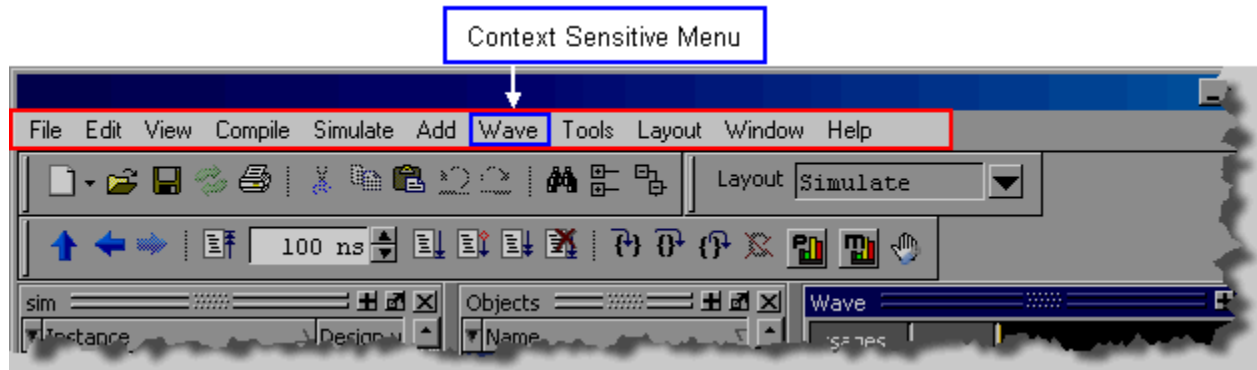
The Main window contains a menu bar, toolbar frame, windows, tab groups, and a status bar, which are described in the following sections.

Menu Bar

The menu bar provides access to many tasks available for your workflow. [Figure 2-8](#) shows the selection in the menu bar that changes based on whichever window is currently active.

The menu items that are available and how certain menu items behave depend on which window is active. For example, if the Structure window is active and you choose Edit from the menu bar, the Clear command is disabled. However, if you click in the Transcript window and choose Edit, the Clear command is enabled. The active window is denoted by a blue title bar.

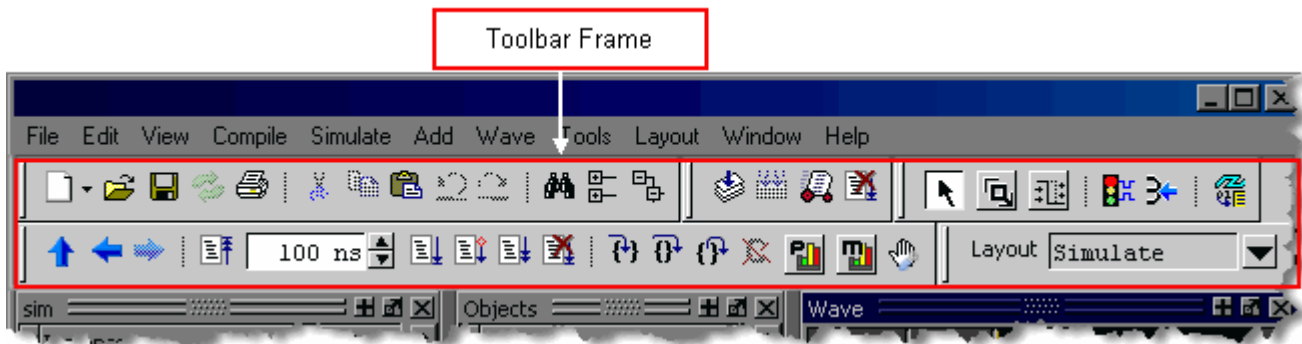
Figure 2-8. Main Window — Menu Bar



Toolbar Frame

The toolbar frame contains several toolbars that provide quick access to various commands and functions.

Figure 2-9. Main Window — Toolbar Frame



Toolbar

A toolbar is a collection of GUI elements in the toolbar frame and grouped by similarity of task. There are many toolbars available within the GUI, refer to the section “[Main Window Toolbar](#)” for more information about each toolbar. [Figure 2-10](#) highlights the Wave toolbar in the toolbar frame.

Figure 2-10. Main Window — Toolbar

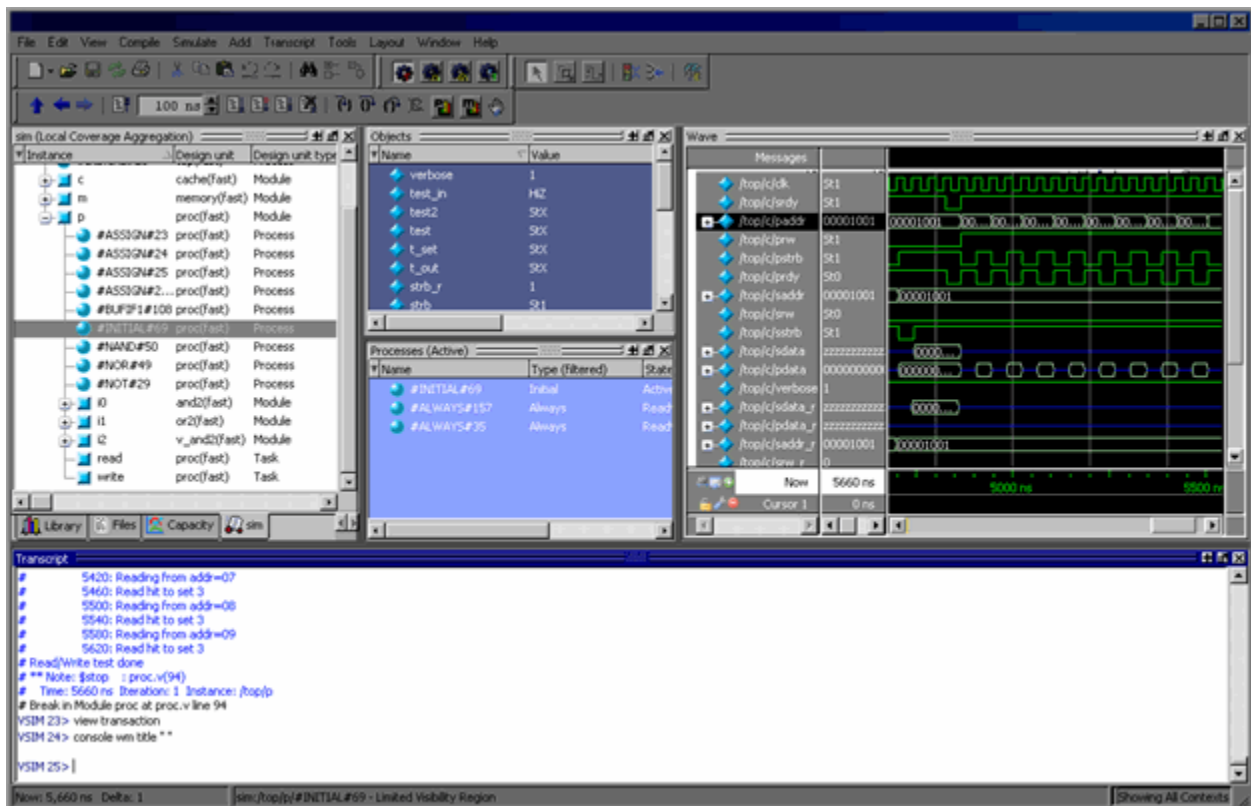


Window

The product contains over 40 different windows you can use with your workflow. This manual refers to all of these objects as windows, even though you can rearrange them such that they appear as a single window with tabs identifying each window.

Figure 2-11 shows an example of a layout with five windows visible; the Structure, Objects, Processes, Wave and Transcript windows.

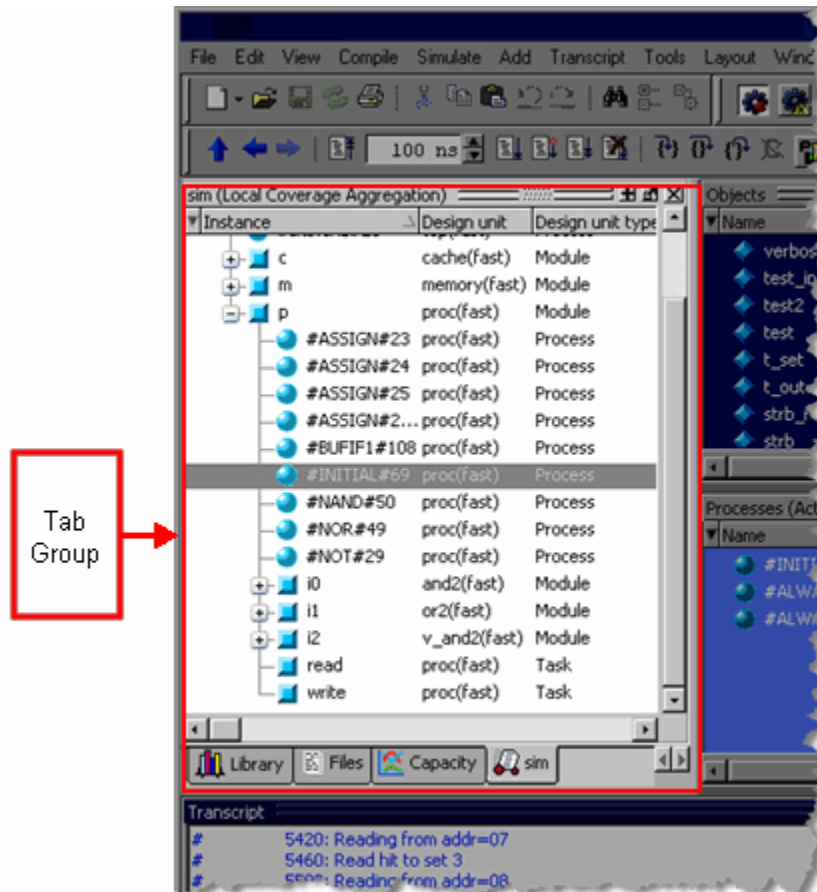
Figure 2-11. GUI Windows



Tab Group

You can group any number of windows into a single space called a tab group, allowing you to show and hide windows by selecting their tabs. [Figure 2-12](#) shows a tab group of the Library, Files, Capacity and Structure windows, with the Structure (sim) window visible.

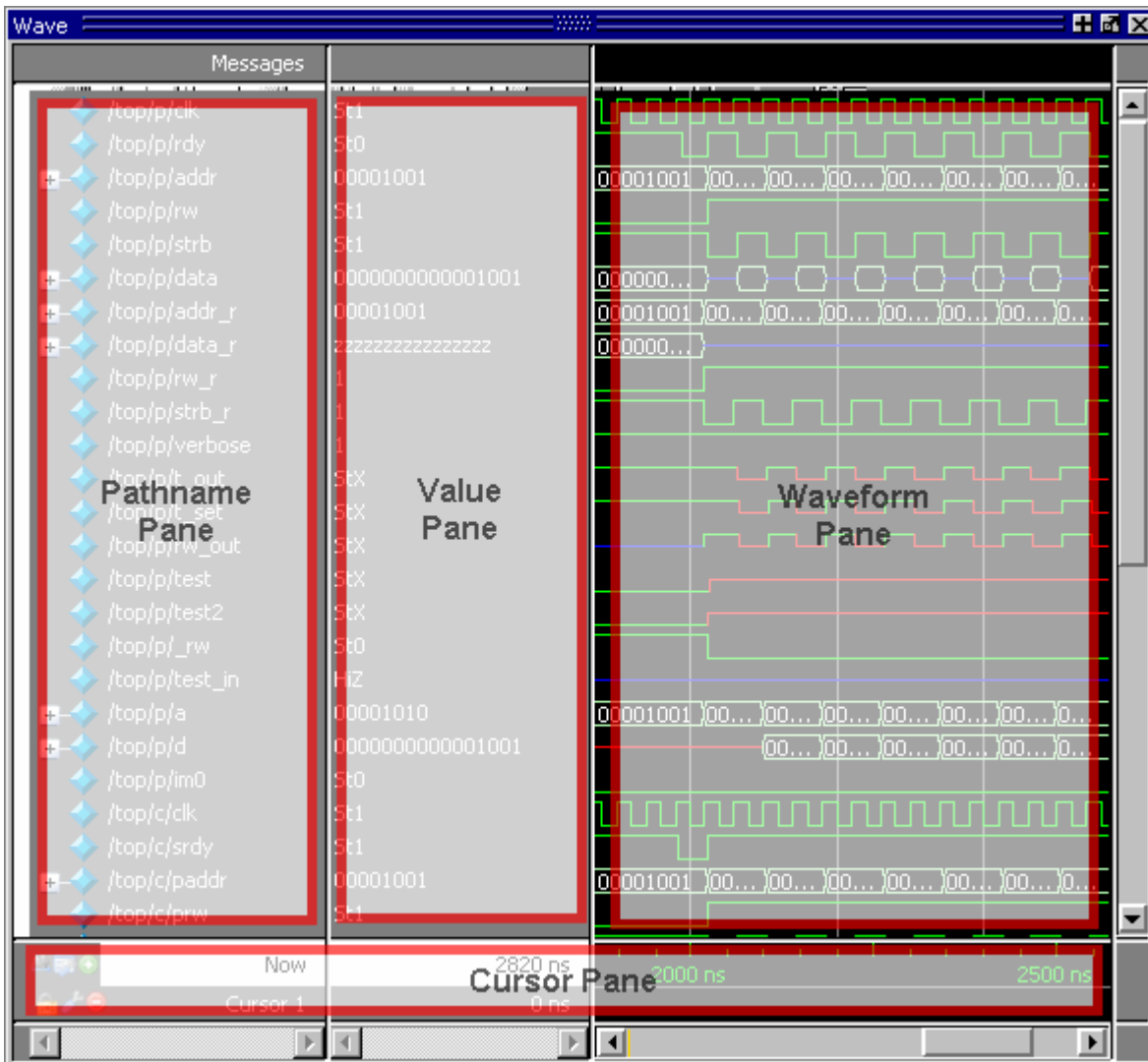
Figure 2-12. GUI Tab Group



Pane

Some windows contain panes, which are separate areas of a window display containing distinct information. One way to tell if a window has panes is whether you receive different popup menus (right-click menu) in different areas. Windows that have panes include the Wave, Source, and List windows. [Figure 2-13](#) shows the Wave window with its three panes.

Figure 2-13. Wave Window Panes



Main Window Status Bar

Fields at the bottom of the Main window provide the following information about the current simulation:

Figure 2-14. Main Window Status Bar

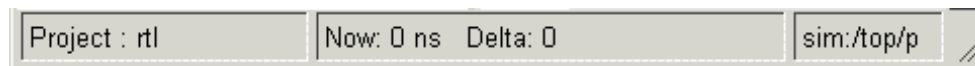


Table 2-7. Information Displayed in Status Bar

Field	Description
Project	name of the current project
Now	the current simulation time
Delta	the current simulation iteration number
Profile Samples	the number of profile samples collected during the current simulation
Memory	the total memory used during the current simulation
environment	name of the current context (object selected in the active Structure window)
line/column	line and column numbers of the cursor in the active Source window

Rearranging the Main Window

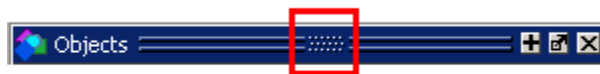
You can alter the layout of the Main window using any of the following methods.

When you exit ModelSim, the current layout is saved for a given design so that it appears the same the next time you invoke the tool.

Moving a Window or Tab Group

1. Click on the header handle in the title bar of the window or tab group.

Figure 2-15. Window Header Handle



2. Drag, without releasing the mouse button, the window or tab group to a different area of the Main window

Wherever you move your mouse you will see a dark blue outline that previews where the window will be placed.

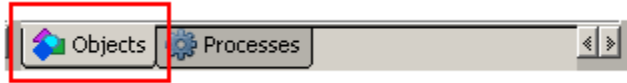
If the preview outline is a rectangle centered within a window, that indicates that you will convert the window or tab group into new tabs within the highlighted window.

3. Release the mouse button to complete the move.

Moving a Tab out of a Tab Group

1. Click on the tab handle that you want to move.

Figure 2-16. Tab Handle



2. Drag, without releasing the mouse button, the tab to a different area of the Main window
Wherever you move your mouse you will see a dark blue outline that previews where the tab will be placed.
If the preview outline is a rectangle centered within a window, that indicates that you will move the tab into the highlighted window.
3. Release the mouse button to complete the move.

Undocking a Window from the Main Window

- Follow the steps in [Moving a Window or Tab Group](#), but drag the window outside of the Main window, or
- Click on the undock button for the window.

Figure 2-17. Window Undock Button



Common Windows

The Main window provides convenient access to projects, libraries, design files, compiled design units, simulation/dataset structures, and Waveform Comparison objects.

Some common windows are listed below.

- **Project window** — Shows all files that are included in the open project. Refer to [Projects](#) for details.
- **Library window** — Shows design libraries and compiled design units. To update the current view of the library, right-click on one of the libraries and select Update. See [Managing Library Contents](#) for details on library management.
- **Structure window** — Shows a hierarchical view of the active simulation and any open datasets. There is one window for the current simulation (named "sim") and one for each open dataset. See [Viewing Dataset Structure](#) for details.

An entry is created by each object within the design. When you select a region in a Structure window, it becomes the *current region* and is highlighted. The [Source Window](#) and [Objects Window](#) change dynamically to reflect the information for the current region. This feature provides a useful method for finding the source code for a selected region because the system keeps track of the pathname where the source is located and displays it automatically, without the need for you to provide the pathname.

Also, when you select a region in the Structure window, the [Processes Window](#) is updated. The Processes window will in turn update the [Locals Window](#).

Objects can be dragged from the Structure window to the Dataflow, List and Wave windows.

The Structure window will display code coverage information (see [Code Coverage in Structure Window](#)).

You can toggle the display of processes by clicking in a Structure window and selecting **View > Filter > Processes**.

You can also control implicit wire processes using a preference variable. By default Structure windows suppress the display of implicit wire processes. To enable the display of implicit wire processes, set PrefMain(HideImplicitWires) to 0 (select **Tools > Edit Preferences**, By Name tab, and expand the Main object).

- **Files window** — Shows the source files for the loaded design.
The file window will display code coverage information.
- **Memory window** — Shows a hierarchical list of all memories in the design. This tab is displayed whenever you load a design containing memories. When you double-click a memory on the window, a Memory Data window opens. See [Memory and Memory Data Windows](#).
- **Compare window**— Shows comparison objects that were created by doing a waveform comparison. See [Waveform Analysis](#) for details.

Navigating in the Main Window

The Main window can contain a number of windows that display various types of information about your design, simulation, or debugging session.

Main Window Toolbar

The Main window contains a toolbar frame that displays context-specific toolbars. The following sections describe the toolbars and their associated buttons.

[Column Layout Toolbar](#)

[Layout Toolbar](#)

[Wave Toolbar](#)

[Compile Toolbar](#)

[Memory Toolbar](#)

[Wave Bookmark Toolbar](#)

- | | | |
|------------------|------------------|--------------------------|
| Coverage Toolbar | Process Toolbar | Wave Compare Toolbar |
| Dataflow Toolbar | Profile Toolbar | Wave Cursor Toolbar |
| FSM Toolbar | Simulate Toolbar | Wave Edit Toolbar |
| Help Toolbar | Source Toolbar | Wave Expand Time Toolbar |
| | Standard Toolbar | Zoom Toolbar |




Column Layout Toolbar

The Column Layout toolbar allows you to control aspects of the Verification Browser window.

Figure 2-18. Column Layout Toolbar



Table 2-8. Change Column Toolbar Buttons

Button	Name	Shortcuts	Description
	Column Layout	Menu: Verification Browser > Configure Column Layout	A dropdown box that allows you to specify the column layout for the Verification Browser window.
	Set Precision for VMgmt	Menu: Verification Browser > Set Precision	A text entry box that allows you to control the precision of the data in the Verification Browser window.
	Restore Default Precision		Restores the precision to the default value (2).

Column Layout Toolbar Usage Information

The Column Layout dropdown menu allows you to select pre-defined column layouts for the Browser tab of the [Verification Browser Window](#).

- AllColumns — displays all available columns.
- AllCoverage — displays all columns related to coverage statistics.
- CodeCoverage — displays all columns related to code coverage statistics.

- FunctionalCoverage — displays all columns related to functional coverage statistics.
- AllCoverageRanked — displays all columns related to ranking results.
- CodeCoverageRanked — displays all columns related to ranked code coverage results.
- FunctionalCoverageRanked - displays all columns related to ranked functional coverage results.
- TestData — displays all columns containing data about the test, including information about how and when the coverage data was generated.





Compile Toolbar

The Compile toolbar provides access to compile and simulation actions.

Figure 2-19. Compile Toolbar



Table 2-9. Compile Toolbar Buttons

Button	Name	Shortcuts	Description
	Compile	Command: <code>vcom</code> or <code>vlog</code> Menu: Compile > Compile	Opens the Compile Source Files dialog box.
	Compile All	Command: <code>vcom</code> or <code>vlog</code> Menu: Compile > Compile all	Compiles all files in the open project.
	Simulate	Command: <code>vsim</code> Menu: Simulate > Start Simulation	Opens the Start Simulation dialog box.
	Break	Menu: Simulate > Break Hotkey: Break	Stop a compilation, elaboration, or the current simulation run.

Coverage Toolbar

The Coverage toolbar provides tools for filtering code coverage data in the Structure and Instance Coverage windows.

Figure 2-20. Coverage Toolbar

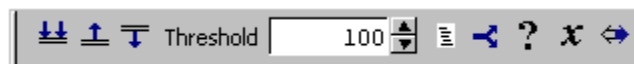











Table 2-10. Coverage Toolbar Buttons

Button	Name	Shortcuts	Description
	Enable Filtering	None	Enables display filtering of coverage statistics in the Structure and Instance Coverage windows.
	Threshold Above	None	Displays all coverage statistics above the Filter Threshold for selected columns.
	Threshold Below	None	Displays all coverage statistics below the Filter Threshold for selected columns
	Filter Threshold	None	Specifies the display coverage percentage for the selected coverage columns
	Statement	None	Applies the display filter to all Statement coverage columns in the Structure and Instance Coverage windows.
	Branch	None	Applies the display filter to all Branch coverage columns in the Structure and Instance Coverage windows.
	Condition	None	Applies the display filter to all Condition coverage columns in the Structure and Instance Coverage windows.
	Expression	None	Applies the display filter to all Expression coverage columns in the Structure and Instance Coverage windows.
	Toggle	None	Applies the display filter to all Toggle coverage columns in the Structure and Instance Coverage windows.

Dataflow Toolbar

The Dataflow toolbar provides access to various tools to use in the Dataflow window.

Figure 2-21. Dataflow Toolbar



Table 2-11. Dataflow Toolbar Buttons

Button	Name	Shortcuts	Description
	Trace Input Net to Event	Menu: Tools > Trace > Trace next event	Move the next event cursor to the next input event driving the selected output.
	Trace Set	Menu: Tools > Trace > Trace event set	Jump to the source of the selected input event.
	Trace Reset	Menu: Tools > Trace > Trace event reset	Return the next event cursor to the selected output.
	Trace Net to Driver of X	Menu: Tools > Trace > TraceX	Step back to the last driver of an unknown value.
	Expand Net to all Drivers	None	Display driver(s) of the selected signal, net, or register.
	Expand Net to all Drivers and Readers	None	Display driver(s) and reader(s) of the selected signal, net, or register.
	Expand Net to all Readers	None	Display reader(s) of the selected signal, net, or register.
	Show Wave	Menu: Dataflow > Show Wave	Display the embedded wave viewer pane.

FSM Toolbar

The FSM toolbar provides access to tools that control the information displayed in the FSM Viewer window.

Figure 2-22. FSM Toolbar

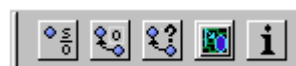







Table 2-12. FSM Toolbar Buttons

Button	Name	Shortcuts	Description
	Show State Counts	Menu: FSM View > Show State Counts	(only available when simulating with -coverage) Displays the coverage count over each state.
	Show Transition Counts	Menu: FSM View > Show Transition Counts	(only available when simulating with -coverage) Displays the coverage count for each transition.
	Show Transition Conditions	Menu: FSM View > Show Transition Conditions	Displays the conditions of each transition.
	Track Wave Cursor	Menu: FSM View > Track Wave Cursor	The FSM Viewer tracks your current cursor location.
	Enable Info Mode Popups	Menu: FSM View > Enable Info Mode Popups	Displays information when you mouse over each state or transition



Help Toolbar

The Help toolbar provides a way for you to search the HTML documentation for a specified string. The HTML documentation will be displayed in a web browser.

Figure 2-23. Help Toolbar



Table 2-13. Help Toolbar Buttons

Button	Name	Shortcuts	Description
	Search Documentation	None	A text entry box for your search string.
	Search Documentation	Hotkey: Enter	Activates the search for the term you entered into the text entry box.

Layout Toolbar

The Layout toolbar allows you to select a predefined or user-defined layout of the graphical user interface. Refer to the section “[Customizing the Simulator GUI Layout](#)” for more information.

Figure 2-24. Layout Toolbar

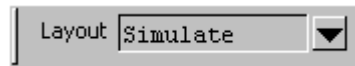



Table 2-14. Layout Toolbar Buttons

Button	Name	Shortcuts	Description
	Change Layout	Menu: Layout > <i>layoutName</i>	A dropdown box that allows you to select a GUI layout.



Memory Toolbar

The Memory toolbar provides access to common functions.

Figure 2-25. Memory Toolbar



Table 2-15. Memory Toolbar Buttons

Button	Name	Shortcuts	Description
	Split Screen	Memory > Split Screen	Splits the memory window.
	Goto Address		Highlights the first element of the specified address.






Mode Toolbar

The Mode toolbar provides access to tools for controlling the mode of mouse navigation.

Figure 2-26. Mode Toolbar



Table 2-16. Mode Toolbar Buttons

Button	Name	Shortcuts	Description
	Select Mode	Menu: Dataflow > Mouse Mode > Select Mode	Set the left mouse button to select mode and middle mouse button to zoom mode.
	Zoom Mode	Menu: Dataflow > Mouse Mode > Zoom Mode	Set left mouse button to zoom mode and middle mouse button to pan mode.
	Pan Mode	Menu: Dataflow > Mouse Mode > Pan Mode	Set left mouse button to pan mode and middle mouse button to zoom mode.
	Edit Mode	Menu: Wave or Dataflow > Mouse Mode > Edit Mode	Set mouse to Edit Mode, where you drag the left mouse button to select a range and drag the middle mouse button to zoom.
	Stop Drawing	None	Halt any drawing currently happening in the window.

Process Toolbar

The Process toolbar contains three toggle buttons (only one can be active at any time) that controls the view of the Process window.

Figure 2-27. Process Toolbar



Table 2-17. Process Toolbar Buttons





Button	Name	Shortcuts	Description
	View Active Processes	Menu: Process > Active	Changes the view of the Processes Window to only show active processes.
	View Processes in Region	Menu: Process > In Region	Changes the view of the Processes window to only show processes in the active region.

Table 2-17. Process Toolbar Buttons

Button	Name	Shortcuts	Description
	View Processes for the Design	Menu: Process > Design	Changes the view of the Processes window to show processes in the design.
	View Process hierarchy	Menu: Process > Hierarchy	Changes the view of the Processes window to show process hierarchy.

Profile Toolbar

The Profile toolbar provides access to tools related to the profiling windows (Ranked, Calltree, Design Unit, and Structural).

Figure 2-28. Profile Toolbar

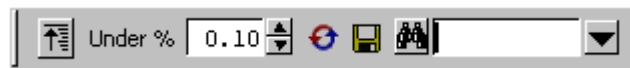




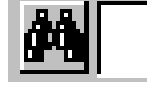


Table 2-18. Profile Toolbar Buttons

Button	Name	Shortcuts	Description
	Collapse Sections	Tools > Profile > Collapse Sections	Toggle the reporting for collapsed processes and functions.
	Profile Cutoff	None	Display performance and memory profile data equal to or greater than set percentage.
	Refresh Profile Data	None	Refresh profile performance and memory data after changing profile cutoff.
	Save Profile Results	Tools > Profile > Profile Report	Save profile data to output file (prompts for file name).
	Profile Find	None	Search for the named string.




Schematic Toolbar

The Schematic toolbar provides access to tools for manipulating highlights.

Figure 2-29. NAME Toolbar



Table 2-19. Schematic Toolbar Buttons

Button	Name	Shortcuts	Description
	Erase Highlight	Menu: Dataflow > Erase highlight	Clear the green highlighting which identifies the path you've traversed through the design.
	Erase All	Menu: Dataflow > Erase all	Clear the window.
	Regenerate	Menu: Dataflow > Regenerate	Clear and redraw the display using an optimal layout.

Simulate Toolbar

The Simulate toolbar provides various tools for controlling your active simulation.

Figure 2-30. Simulate Toolbar

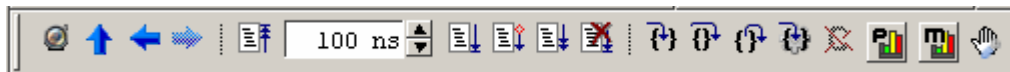


Table 2-20. Simulate Toolbar Buttons





Button	Name	Shortcuts	Description
	Source Navigation	None	Toggles display of hyperlinks in design source files.
	Environment Up	Command: env .. Menu: File > Environment	Changes your environment up one level of hierarchy.
	Environment Back	Command: env -back Menu: File > Environment	Change your environment to its previous location.
	Environment Forward	Command: env -forward Menu: File > Environment	Change your environment forward to a previously selected environment.

Table 2-20. Simulate Toolbar Buttons















Button	Name	Shortcuts	Description
	Restart	Command: <code>restart</code> Menu: Simulate > Run > Restart	Reload the design elements and reset the simulation time to zero, with the option of maintaining various settings and objects.
	Run Length	Command: <code>run</code> Menu: Simulate > Runtime Options	Specify the run length for the current simulation.
	Run	Command: <code>run</code> Menu: Simulate > Run > Run <i>default_run_length</i>	Run the current simulation for the specified run length.
	Continue Run	Command: <code>run -continue</code> Menu: Simulate > Run > Continue	Continue the current simulation run until the end of the specified run length or until it hits a breakpoint or specified break event.
	Run All	Command: <code>run -all</code> Menu: Simulate > Run > Run -All	Run the current simulation forever, or until it hits a breakpoint or specified break event.
	Break	Menu: Simulate > Break Hotkey: Break	Stop a compilation, elaboration, or the current simulation run.
	Step	Command: <code>step</code> Menu: Simulate > Run > Step	Step the current simulation to the next statement.
	Step Over	Command: <code>step -over</code> Menu: Simulate > Run > Step -Over	Execute HDL statements, treating them as simple statements instead of entered and traced line by line.
	Step Out	Command: <code>step -out</code>	Step the current simulation out of the current function or procedure.
	Step Current	Command: <code>step -inst</code>	Step the current simulation into an instance, process or thread.
	C Interrupt	Command: <code>cdbg interrupt</code> Menu: Tools > C Debug > C Interrupt	Reactivate the C debugger when stopped in HDL code.

Table 2-20. Simulate Toolbar Buttons

Button	Name	Shortcuts	Description
	Performance Profiling	Menu: Tools > Profile > Performance	Enable collection of statistical performance data.
	Memory Profiling	Menu: Tools > Profile > Memory	Enable collection of memory usage data.
	Edit Breakpoints	Menu: Tools > Breakpoint	Enable breakpoint editing, loading, and saving.

Source Toolbar

The Source toolbar allows you to perform several activities on Source windows.

Figure 2-31. Source Toolbar

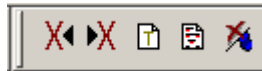







Table 2-21. Source Toolbar Buttons

Button	Name	Shortcuts	Description
	Previous Zero Hits	None	Jump to previous line with zero coverage.
	Next Zero Hits	None	Jump to next line with zero coverage.
	Show Language Templates	Menu: Source > Show Language Templates	Display language templates in the left hand side of every open source file.
	Source Annotation	Menu: Source > Show Annotation	Allows Debugging with Source Annotation in every open source file.
	Clear Bookmarks	Menu: Source > Clear Bookmarks	Removes any bookmarks in the active source file.

Standard Toolbar

The Standard toolbar contains common buttons that apply to most windows.

Figure 2-32. Standard Toolbar

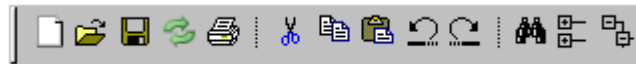


Table 2-22. Standard Toolbar Buttons














Button	Name	Shortcuts	Description
	New File	Menu: File > New > Source	Opens a new Source text file.
	Open	Menu: File > Open	Opens the Open File dialog
	Save	Menu: File > Save	Saves the contents of the active window or Saves the current wave window display and signal preferences to a macro file (DO fie).
	Reload	Command: Dataset Restart Menu: File > Datasets	Reload the current dataset.
	Print	Menu: File > Print	Opens the Print dialog box.
	Cut	Menu: Edit > Cut Hotkey: Ctrl-x	-
	Copy	Menu: Edit > Copy Hotkey: Ctrl-c	-
	Paste	Menu: Edit > Paste Hotkey: ctrl-v	-
	Undo	Menu: Edit > Undo Hotkey: Ctrl-z	-
	Redo	Menu: Edit > Redo Hotkey: Ctrl-y	-
	Find	Menu: Edit > Find Hotkey: Ctrl-f (Windows) or Ctrl-s (UNIX)	Opens the Find dialog box
	Collapse All	Menu: Edit > Expand > Collapse All	-

Table 2-22. Standard Toolbar Buttons

Button	Name	Shortcuts	Description
	Expand All	Menu: Edit > Expand > Expand All	-

Wave Toolbar

The Wave toolbar allows you to perform specific actions in the Wave window.

Figure 2-33. Wave Toolbar

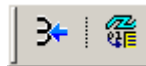




Table 2-23. Wave Toolbar Buttons

Button	Name	Shortcuts	Description
	Show Drivers	None	Display driver(s) of the selected signal, net, or register in the Dataflow or Wave window.
	Export Waveform	Menu: File > Export > Waveform	Export a created waveform.





Wave Bookmark Toolbar

The Wave Bookmark toolbar allows you to manage your bookmarks of the Wave window

Figure 2-34. Wave Bookmark Toolbar



Table 2-24. Wave Bookmark Toolbar Buttons

Button	Name	Shortcuts	Description
	Add Bookmark	Command: Bookmark Add Wave Menu: Add > To Wave > Bookmark	Clicking this button bookmarks the current view of the Wave window. Click and hold the button to access an additional option to create a custom bookmark.
	Delete All Bookmarks	Command: Bookmark Delete Wave -all	Removes all bookmarks, after prompting for your confirmation.
	Manage Bookmarks		Displays the Bookmark Selection dialog box for managing your bookmarks.
	Jump to Bookmark	Command: Bookmark Goto Wave <name>	Displays a selection group for you to pick which bookmark you want to display.

Wave Compare Toolbar

The Wave Compare toolbar allows you to quickly find differences in a waveform comparison.

Figure 2-35. Wave Compare Toolbar



Table 2-25. Wave Compare Toolbar Buttons







Button	Name	Shortcuts	Description
	Find First Difference	None	Find the first difference in a waveform comparison
	Find Previous Annotated Difference	None	Find the previous annotated difference in a waveform comparison
	Find Previous Difference	None	Find the previous difference in a waveform comparison

Table 2-25. Wave Compare Toolbar Buttons

Button	Name	Shortcuts	Description
	Find Next Difference	None	Find the next difference in a waveform comparison
	Find Next Annotated Difference	None	Find the next annotated difference in a waveform comparison
	Find Last Difference	None	Find the last difference in a waveform comparison

Wave Cursor Toolbar

The Wave Cursor toolbar provides various tools for manipulating cursors in the Wave window.

Figure 2-36. Wave Cursor Toolbar

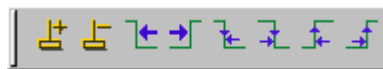


Table 2-26. Wave Cursor Toolbar Buttons









Button	Name	Shortcuts	Description
	Insert Cursor	None	Adds a new cursor to the active Wave window.
	Delete Cursor	Menu: Wave > Delete Cursor	Deletes the active cursor.
	Find Previous Transition	Menu: Edit > Signal Search Hotkey: Shift + Tab	Moves the active cursor to the previous signal value change for the selected signal.
	Find Next Transition	Menu: Edit > Signal Search Hotkey: Tab	Moves the active cursor to the next signal value change for the selected signal.
	Find Previous Falling Edge	Menu: Edit > Signal Search	Moves the active cursor to the previous falling edge for the selected signal.
	Find Next Falling Edge	Menu: Edit > Signal Search	Moves the active cursor to the next falling edge for the selected signal.

Table 2-26. Wave Cursor Toolbar Buttons

Button	Name	Shortcuts	Description
	Find Previous Rising Edge	Menu: Edit > Signal Search	Moves the active cursor to the previous rising edge for the selected signal.
	Find Next Rising Edge	Menu: Edit > Signal Search	Moves the active cursor to the next rising edge for the selected signal.

Wave Edit Toolbar

The Wave Edit toolbar provides easy access to tools for modifying an editable wave.

Figure 2-37. Wave Edit Toolbar



Table 2-27. Wave Edit Toolbar Buttons









Button	Name	Shortcuts	Description
	Insert Pulse	Menu: Wave > Wave Editor > Insert Pulse Command: wave edit insert_pulse	Insert a transition at the selected time.
	Delete Edge	Menu: Wave > Wave Editor > Delete Edge Command: wave edit delete	Delete the selected transition.
	Invert	Menu: Wave > Wave Editor > Invert Command: wave edit invert	Invert the selected section of the waveform.
	Mirror	Menu: Wave > Wave Editor > Mirror Command: wave edit mirror	Mirror the selected section of the waveform.
	Change Value	Menu: Wave > Wave Editor > Value Command: wave edit change_value	Change the value of the selected section of the waveform.
	Stretch Edge	Menu: Wave > Wave Editor > Stretch Edge Command: wave edit stretch	Move the selected edge by increasing/decreasing waveform duration.

Table 2-27. Wave Edit Toolbar Buttons

Button	Name	Shortcuts	Description
	Move Edge	Menu: Wave > Wave Editor > Move Edge Command: wave edit move	Move the selected edge without increasing/decreasing waveform duration.
	Extend All Waves	Menu: Wave > Wave Editor > Extend All Waves Command: wave edit extend	Increase the duration of all editable waves.

Wave Expand Time Toolbar

The Wave Expand Time toolbar provides access to enabling and controlling wave expansion features.

Figure 2-38. Wave Expand Time Toolbar



Table 2-28. Wave Expand Time Toolbar Buttons








Button	Name	Shortcuts	Description
	Expanded Time Off	Menu: Wave > Expanded Time > Off	turns off the expanded time display (default mode)
	Expanded Time Deltas Mode	Menu: Wave > Expanded Time > Deltas Mode	displays delta time steps
	Expanded Time Events Mode	Menu: Wave > Expanded Time > Events Mode	displays event time steps
	Expand All Time	Menu: Wave > Expanded Time > Expand All	expands simulation time over the entire simulation time range, from 0 to current time
	Expand Time at Active Cursor	Menu: Wave > Expanded Time > Expand Cursor	expands simulation time at the simulation time of the active cursor
	Collapse All Time	Menu: Wave > Expanded Time > Collapse All	collapses simulation time over entire simulation time range

Table 2-28. Wave Expand Time Toolbar Buttons

Button	Name	Shortcuts	Description
	Collapse Time at Active Cursor	Menu: Wave > Expanded Time > Collapse Cursor	collapses simulation time at the simulation time of the active cursor





Zoom Toolbar

The Zoom toolbar allows you to change the view of the Wave window.

Figure 2-39. Zoom Toolbar



Table 2-29. Zoom Toolbar Buttons

Button	Name	Shortcuts	Description
	Zoom In	Menu: Wave > Zoom > Zoom In Hotkey: i, I, or +	Zooms in by a factor of 2x
	Zoom Out	Menu: Wave > Zoom > Zoom Out Hotkey: o, O, or -	Zooms out by a factor of 2x
	Zoom Full	Menu: Wave > Zoom > Zoom Full Hotkey: f or F	Zooms to show the full length of the simulation.
	Zoom in on Active Cursor	Menu: Wave > Zoom > Zoom Cursor Hotkey: c or C	Zooms in by a factor of 2x, centered on the active cursor

Processes Window

The Processes window displays a list of HDL and SystemC processes in one of four viewing modes: Active, In Region, Design, and Hierarchical. The Design view mode is intended for primary navigation of ESL (Electronic System Level) designs where processes are a foremost consideration.

Hierarchical mode displays a tree view of any SystemVerilog nested fork-joins.

By default, this window displays the active processes in your simulation (Active view mode). The title bar of the window displays “Processes (Active)” (Figure 2-40).

Figure 2-40. Processes (Active) Window

Name	Type (filtered)	State	Order	Parent Path
#INITIAL#17	Initial	Ready	4	/test_counter
#INITIAL#23	Initial	Ready	5	/test_counter
#INITIAL#30	Initial	Ready	6	/test_counter

You can change the display to show all the processes in a region (Figure 2-42) or in the entire design by doing any one of the following:

- When the Processes window is docked, select **Process > In Region** or **Process > Design** from the Main window menu. This window must be selected (active) for the Process menu selection to appear in the Main window menu bar.
- When the Processes window is undocked, select **View > In Region** or **View > Design** from the menu bar.
- Click (LMB) the **View Processes In Region** or the **View Processes in the Design** button in the **Process Toolbar** (Figure 2-41).

Figure 2-41. Process Toolbar



- Right-click (RMB) in the Process window and select **In Region** or **Design** from the popup context menu.

Figure 2-42. Processes (In Region) Window

Name	Type (filtered)	State	Order	Parent Path
#INITIAL#17	Initial	Ready	4	/test_counter
#INITIAL#23	Initial	Ready	5	/test_counter
#INITIAL#30	Initial	Ready	6	/test_counter

The In Region view mode allows you to display all processes recursively or non-recursively inside the currently selected context. The non-recursive mode is the default.

The view mode you select is persistent and is “remembered” when you exit the simulation. The next time you bring up the tool, this window will initialize in the last view mode used.

Displaying the Processes Window

To display the Process window, do either of the following:

- Select **View > Process** in the Main menu.
- Use the command:

view process

When undocked, the Processes Window contains the following toolbars:

- [Standard Toolbar](#)
- [Process Toolbar](#)

These toolbars are included in the Main window when the Process window is docked.

Viewing Data in the Processes Window

This window is populated when you select a view mode (Active, In Region, Design, or Hierarchical). When you select the In Region view mode, the processes shown in this window will change according to the region you select in the Structure window. In addition, the data in this window will change as you run your simulation and processes change states or become inactive.

Column Descriptions

- **Name** — The name of the process.
- **Type** — The process type, according to the language used.
- **State** — The process state.
- **Order** — The execution order of all processes in the Active and Ready states.
- **Parent Path** — The hierarchical parent pathname of the process.

Each process in the window is identified according to its process state, as shown in the **State** column. The different process states are defined as follows:

- **Idle** — Indicates an inactive SystemC Method, or a process that has never been active.
- **Wait** — Indicates the process is waiting for a wake up trigger (change in VHDL signal, Verilog net, SystemC signal, or a time period).
- **Ready** — Indicates the process is scheduled to be executed in current simulation phase (or in active simulation queue) of current delta cycle.
- **Active** — Indicates the process is currently active and being executed.

- **Queued** — Indicates the process is scheduled to be executed in current delta cycle, but not in current simulation phase (or in active simulation queue).
- **Done** — Indicates the process has been terminated, and will never restart during current simulation run.

Processes in the Idle and Wait states are distinguished as follows. Idle processes (except for ScMethods) have never been executed before in the simulation, and therefore have never been suspended. Idle processes will become Active, Ready, or Queued when a trigger occurs. A process in the Wait state has been executed before but has been suspended, and is now waiting for a trigger.

SystemC methods can have one of the four states: Active, Ready, Idle or Queued. When ScMethods are not being executed (Active), or scheduled (Ready or Queued), they are inactive (Idle). ScMethods execute in 0 time, whenever they get triggered. They are never suspended or terminated.

The Idle state will occur only for SC processes or methods. It will never occur for HDL processes.

The **Type** column displays the process type according to the language used. It includes the following types:

- Always
- Assign
- Final
- Fork-Join (dynamic process like fork-join, sc_spawn, and so forth.)
- Initial
- Implicit (internal processes created by simulator like Implicit wires, and so forth.)
- Primitive (UDP, Gates, and so forth.)
- ScMethod
- ScThread (SC Thread and SC CThread processes)
- VHDL Process

The **Order** column displays the execution order of all processes in the Active and Ready states in the active kernel queue. Processes that are not in the Active or Ready states do not yet have any order. The Order column displays a ‘-’ for such processes. The Process window updates the execution order automatically as simulation proceeds.

By default, this window’s data is sorted according to the Order column. You can sort by another column by simply clicking a column heading. You can also change the sort mode using the

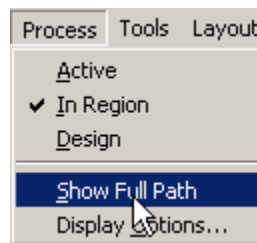
Process Display Options dialog (next section). Four sort modes are available: by process name, type, state, or order.

Processes Window Display Options

By default, all processes are displayed without the full hierarchical context (path). You can display processes with the full path by doing any of the following:

- Select **Process > Show Full Path** from the Main window menus when the Processes window is docked (Figure 2-43).

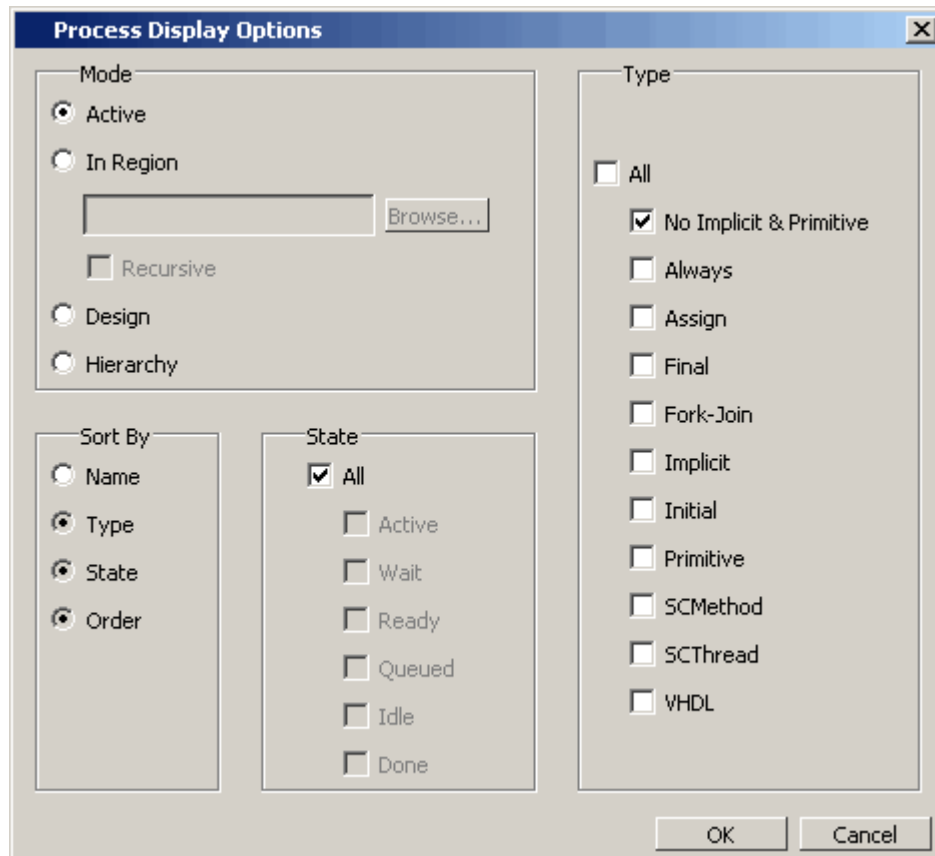
Figure 2-43. Selecting Show Full Path from Process Menu



- Select **View > Show Full Path** when the window is undocked.
- Right-click (RMB) anywhere in this window and select **Show Full Path** from the popup context menu.

This window also displays data based on the display options you select from the Process Display Options dialog (Figure 2-44).

Figure 2-44. Process Display Options Dialog




You can open this dialog by doing one of the following:

- Select **Process > Display Options** from the Main window menu when this window is docked.
- Select **View > Display Options** when this window is undocked.
- Right-click (RMB) anywhere in this window and select **Display Options** from the popup context menu.

With the Process Display Options dialog you can:

- Select which process mode to display (Active is the default). When the In Region display mode is selected you can elect to view the region recursively.
- Sort the displayed process by Name, Type, State, or Order (Order is the default).
- Display All process states (the default) or selected process states. When you filter the display according to specific process states, the heading of the State column changes to “State (filtered)” as shown in [Figure 2-45](#).

Figure 2-45. Column Heading Changes When States are Filtered



Name	Type (filtered)	State (filtered)	Order	Parent Path
#ALWAYS#35	Always	Ready	3	/top/m
#ALWAYS#155	Always	Ready	2(Next Active)	/top/c

- Select the process type to be displayed (“No Implicit & Primitive” is the default). The default “No Implicit & Primitive” selection causes the Process window to display all process types except implicit and primitive types. When you filter the display according to specific process types, the heading of the Type column becomes “Type (filtered)”, as shown in [Figure 2-45](#).

Once you select the options, data will update as the simulation runs and processes change their states. When the In Region view mode is selected, data will update according to the region selected in the Structure window.

Post-Processing Mode

This window also shows data in the post-processing (WLF view or Coverage view) mode. You will need to log processes in the simulation mode to be able to view them in post-processing mode.

In the post-processing mode, the default selection values will be same as the default values in the live simulation mode.

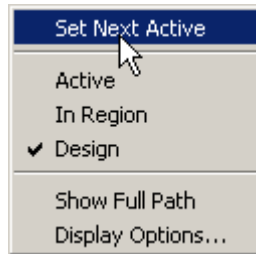
Things to remember about the post-processing mode:

- There are no active processes, so the Active view mode selection will not show anything.
- All processes will have same ‘Done’ state in the post-processing mode.
- There is no order information, so the Order column will show ‘-’ for all processes.

Set Ready Process as Next Active Process

You can select any “Ready” process and set it to be the next Active process executed by the simulator, ahead of any other queued processes. To do this, simply right-click (RMB) any “Ready” process and select **Set Next Active** from the popup context menu ([Figure 2-46](#)).

Figure 2-46. Set Next Active RMB Menu Selection



When you set a process as the next active process, you will see “(Next Active)” in the Order column of that process (Figure 2-47).

Figure 2-47. Next Active Process Displayed in Order Column

Name	Type (filtered)	State	Order	Parent Path
#ALWAYS#35	Always	Ready	3	/top/m
#ALWAYS#155	Always	Ready	2(Next Active)	/top/c
#INITIAL#69	Initial	Active	1	/top/p
#ASSIGN#25	Assign	Wait	-	/top/p
#ASSIGN#24	Assign	Wait	-	/top/p
#ASSIGN#23	Assign	Wait	-	/top/p
#ASSIGN#21	Assign	Wait	-	/top/c/s3

Create Textual Process Report

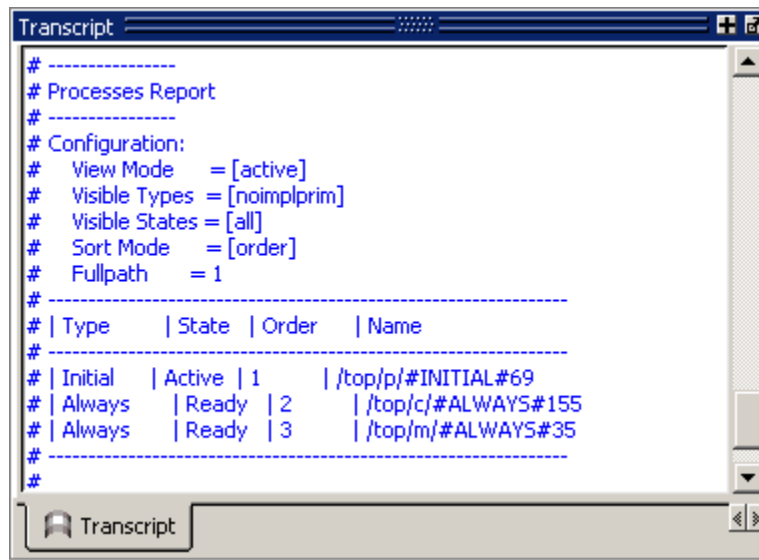
You can create a textual report of all processes by entering the `process report` command at the command line.

Syntax

`process report [-file <filename>] [-append]`

If <filename> is not given, then the output is redirected to stdout (Figure 2-48). If the `-append` option is used, the process report will be appended into the file instead of overwriting it.

Figure 2-48. Sample Process Report in the Transcript Window



Call Stack Window

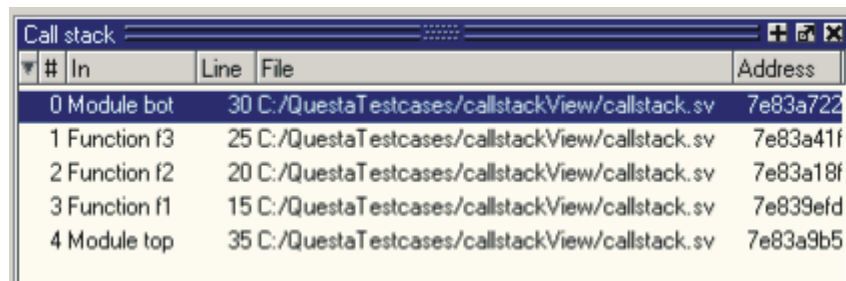
The Call Stack window displays the current call stack when you single step your simulation, when the simulation has encountered a breakpoint, or when you select any process in either the Structure or Processes windows. When debugging your design you can use the call stack data to analyze the depth of function calls, which include Verilog functions and tasks, VHDL functions and procedures, SystemC methods and threads, and C/C++ functions that led up to the current point of the simulation.

The Call Stack window also supports [C Debug](#) mode.

Accessing the Call Stack Window

View > Call Stack

Figure 2-49. Call Stack Window



Using the Call Stack Window

This window contains five columns of information to assist you in debugging your design:

- # — indicates the depth of the function call, with the most recent at the top.

- In — indicates the function.
- Line — indicates the line number containing the function call.
- File — indicates the location of the file containing the function call.
- Address — indicates the address of the execution in a foreign subprogram, such as C.

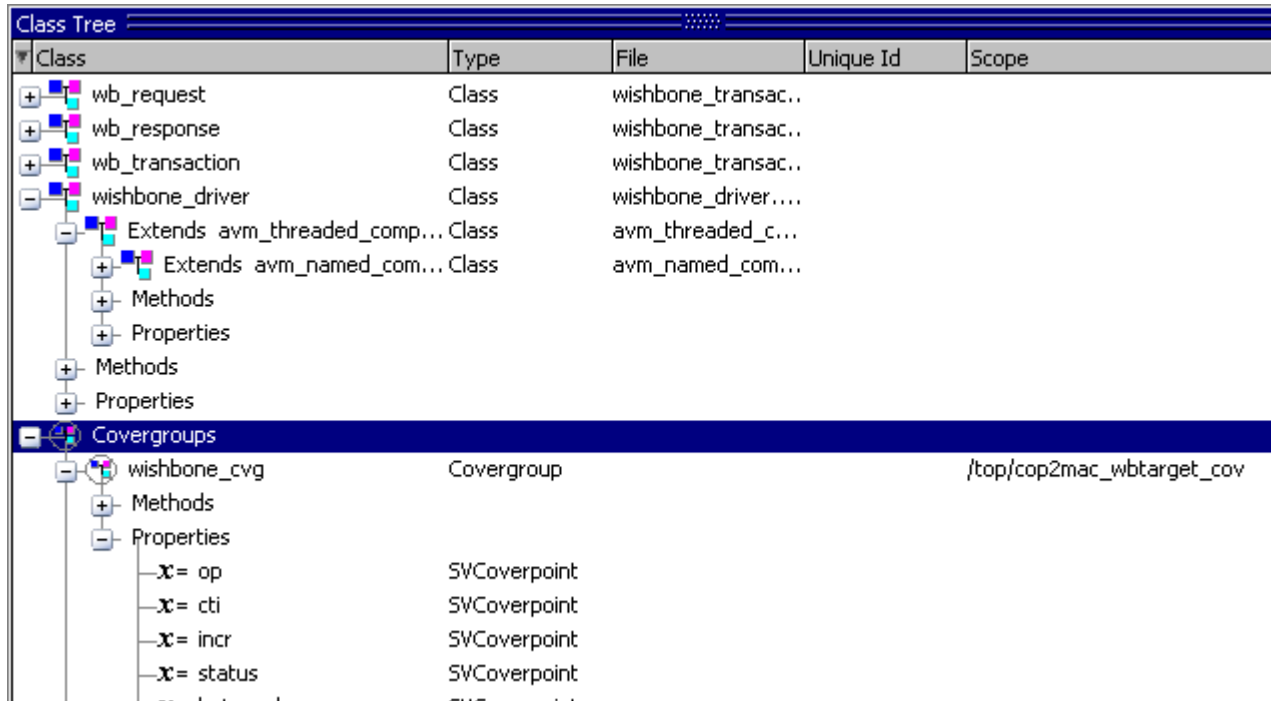
This window allows you to perform the following actions:

- Double-click on the line of any function call:
 - Displays the local variables at that level in the [Locals Window](#).
 - Displays the corresponding source code in the [Source Window](#).
- Right-click in the column headings
 - Displays a pop-up window that allows you to show or hide columns.

Class Tree Window

The Class Tree window provides a hierarchical view of your SystemVerilog classes, including any extensions of other classes, related methods and properties, as well as any covergroups.

Figure 2-50. Class Tree Window



Displaying the Class Tree Window

- Select **View > Class Browser > Class Tree**
- Use the command:









view classtree

GUI Elements of the Class Tree Window

This section describes the GUI elements specific to the Class Tree window.

Icons

Table 2-30. Class Tree Window Icons

Icon	Description
	Class
	Parameterized Class
	Function
	Task
	Variable
	Virtual Interface
	Covergroup
	Structure

Column Descriptions

- Class — The name of the item.
- Type — The type of item.
- File — The source location of item.
- Unique Id — (only parameterized classes) The internal name of the parameterized class.
- Scope — (only covergroups) The scope of the covergroup.

Menu Items

- View Declaration — Highlights the line of code where the item is declared, opening the source file if necessary.

- **View as Graph** — (only available for classes) Displays the class and any dependent classes in the Class Graph window.
- **Filter** — allows you to filter out methods and or properties
- **Organize by Base Class** — reorganizes the window so that the base classes are at the top of the hierarchy.
- **Organize by Extended Class** — (default view) reorganizes the window so that the extended classes are at the top of the hierarchy.

Toolbar Items

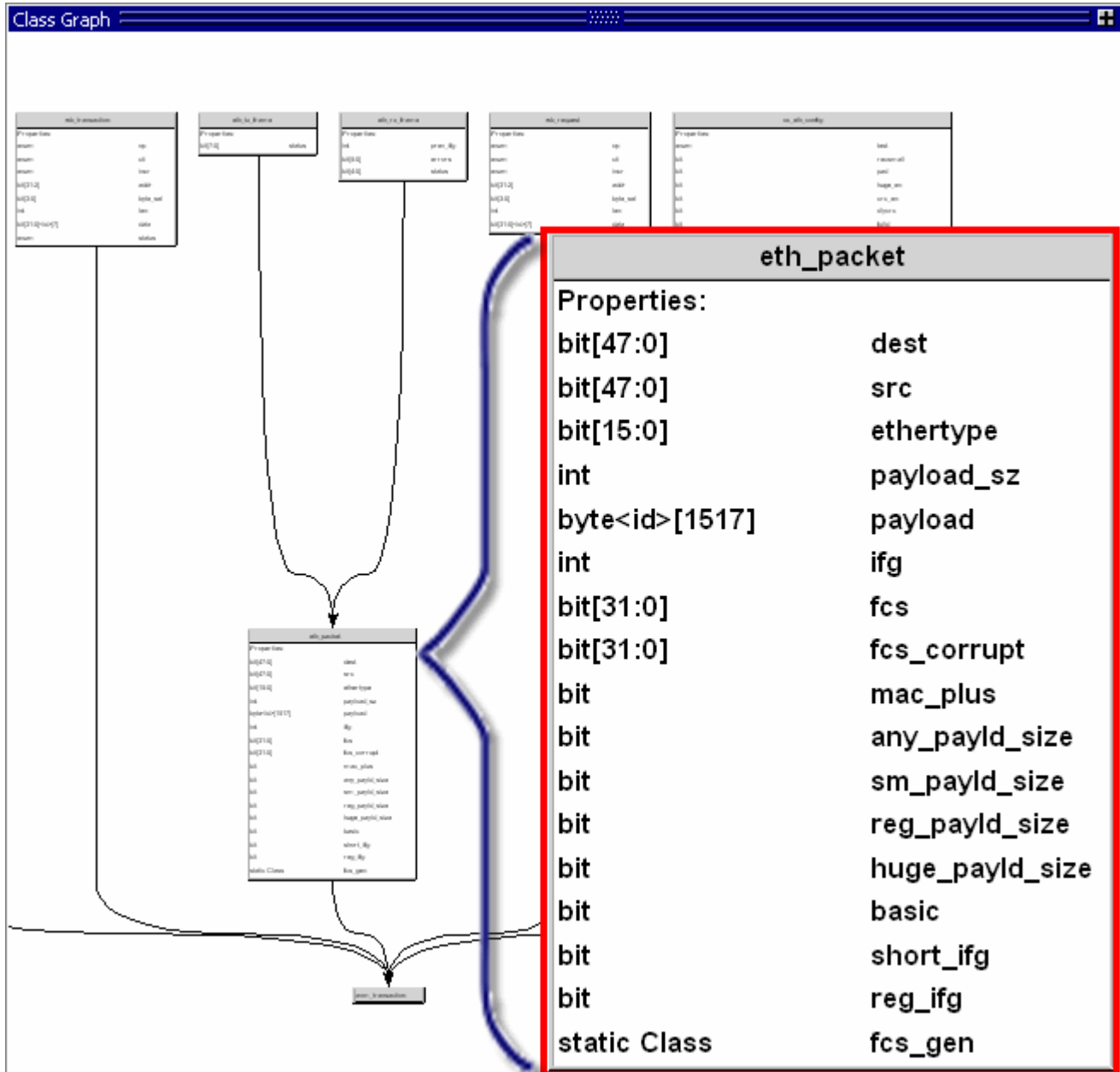
When undocked, this window contains the following toolbars:

- [Help Toolbar](#)
- [Standard Toolbar](#)

Class Graph Window

The Class Graph window provides a graphical view of your SystemVerilog classes, including any extensions of other classes and related methods and properties.

Figure 2-51. Class Graph Window



Displaying the Class Graph Window

- Select **View > Class Browser > Class Graph**
- Use the command:
view classgraph

GUI Elements of the Class Graph Window

This section describes the GUI elements specific to the Class Graph window.

Navigation

- Left click-drag — allows you to move the contents around in the window.
- Middle Mouse scroll — zooms in and out.
- Middle mouse button strokes:
 - Upper left — zoom full
 - Upper right — zoom out. The length of the stroke changes the zoom factor.
 - Lower right — zoom area.
- Arrow Keys — scrolls the window in the specified direction.
 - Unmodified — scrolls by a small amount.
 - Ctrl+<arrow key> — scrolls by a larger amount
 - Shift+<arrow key> — shifts the view to the edge of the display

Menu Items

- Filter — allows you to filter out methods and or properties
- Organize by Base Class — reorganizes the window so that the base classes are at the top of the hierarchy.
- Organize by Extended Class — (default view) reorganizes the window so that the extended classes are at the top of the hierarchy.

Toolbars

When undocked, the window contains the following toolbar:

- [Zoom Toolbar](#)

Windows Containing Code Coverage Data

When you run simulations with code coverage enabled, a tabbed set of windows displays the code coverage data.

Figure 2-52. Windows that Show Code Coverage Data

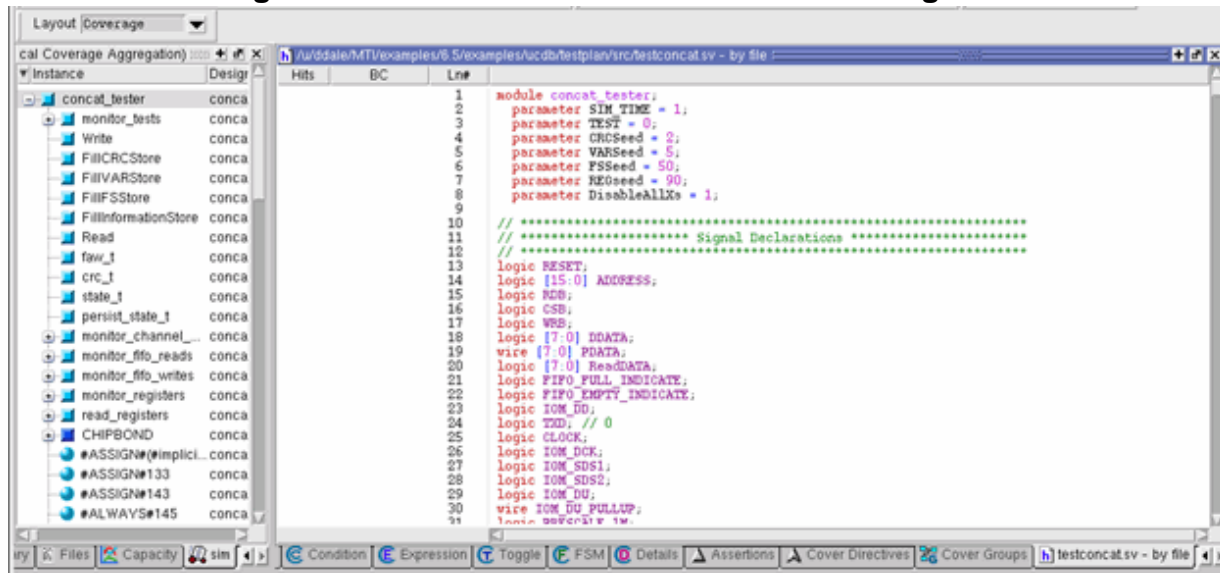


Table 2-31. Windows that Show Code Coverage Data

Windows with Coverage Data	Reference
Structure	Code Coverage in Structure Window
Objects	Toggle Coverage in the Objects Window
Source	Coverage Data in the Source Window
Instance Coverage	Instance Coverage Window
Details	Coverage Details Window
Current Exclusions	Current Exclusions Window
Objects	Coverage Details Window

The information contained in these windows dissect and organize the data collected during coverage analysis. Each window contains context menus (right-click in the window to access the menus) with commands appropriate to that window.

For details about simulating with code coverage and analyzing results refer to the “[Code Coverage](#)” chapter.

Coverage Details Window

After code coverage is invoked and the simulation is loaded and run, you can turn on the Coverage Details window by selecting **View > Coverage > Details**. This window shows the details of missed coverage. When you select (left-click) an object in a Missed Coverage

window, the details of that coverage are displayed in this window. Truth tables will be displayed for condition and expression coverage, as shown here.

Figure 2-53. Coverage Details Window Showing Condition Truth Table

```

Details
File: C:/CodeCoverage5.8/verilog/beh_sram.v
Line: 31
Truth table for:
  if (rd_ || wr_)

      rd_
      | wr_
      | | (rd_ || wr_)
count | | |
-----|---|
      6  1 - 1
     19 - 1 1
       0  0 0 0
       1  unknown

Condition: 2 out of 3 (66.7%) covered.

```

For a description of these truth tables, see [UDP Coverage Details and Examples](#).

Toggle details are displayed as follows:

Figure 2-54. Coverage Details Window Showing Toggle Details

```

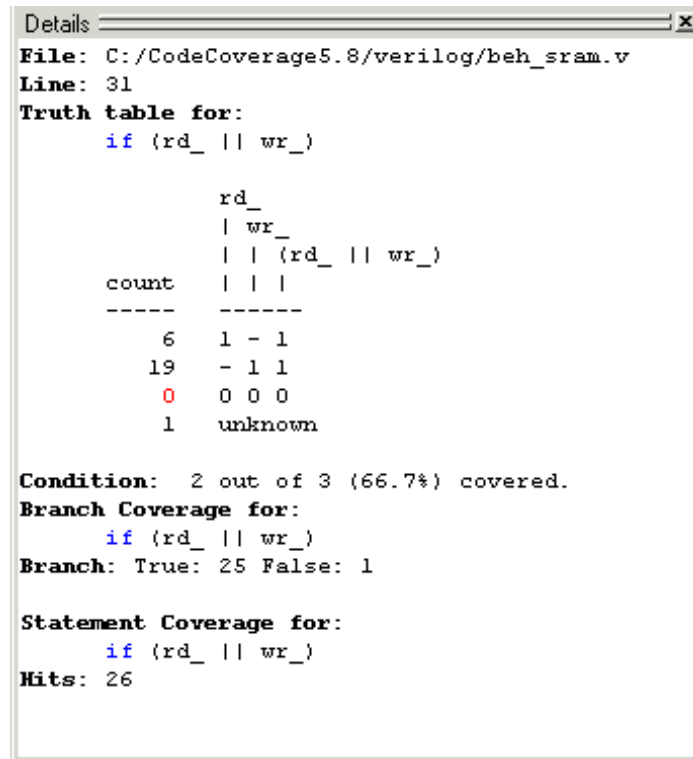
Details
Instance: /test_sm
Signal: dat
Node count: 32

1H->0L: 16817
0L->1H: 20560
0L->Z: 452245
Z->0L: 456015
1H->Z: 85963
Z->1H: 82225
Toggle Coverage: 18.75%
0/1 Coverage: 21.88%
Full Coverage: 47.92%
Z Coverage: 60.94%

```

By clicking the left mouse button on the statement Hits column in the Source window, all coverage information for that line will be displayed as shown here:

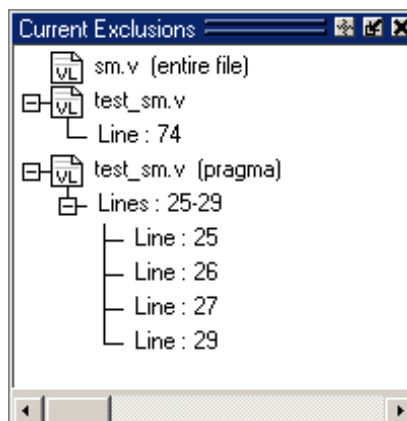
Figure 2-55. Coverage Details Window Showing Information from Source Window



Current Exclusions Window

The Current Exclusions window lists all files and lines that are excluded from coverage statistics. See [Excluding Objects from Coverage](#) for more details.

Figure 2-56. Current Exclusions Window



The window does not display by default. Select **View > Coverage > Current Exclusions** to display.

Dataflow Window

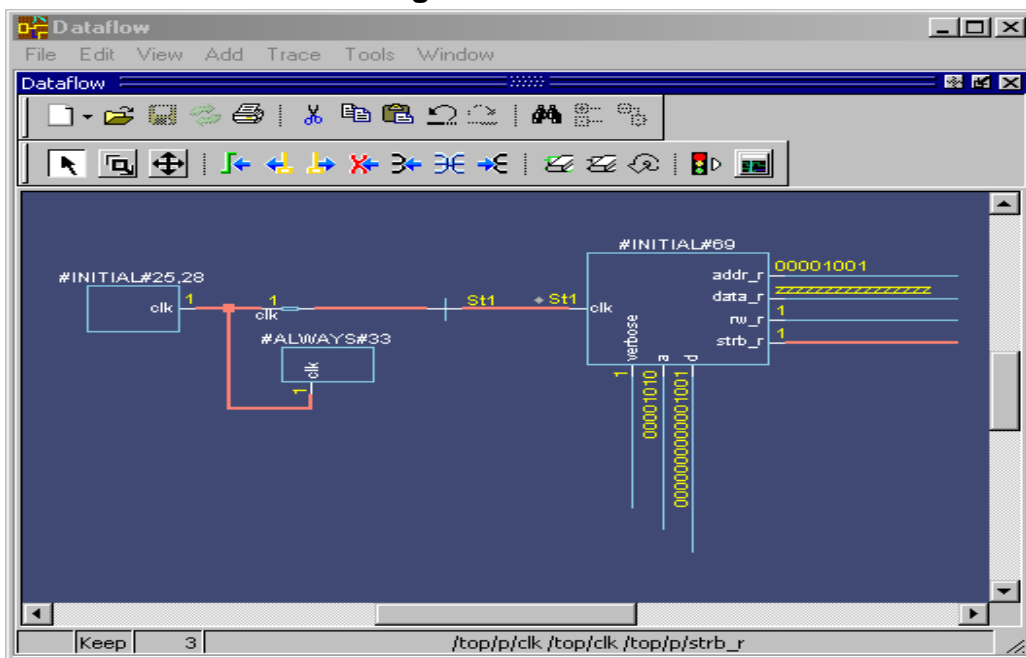
The Dataflow window allows you to explore the "physical" connectivity of your design. It also allows you to trace events that propagate through the design; and to identify the cause of unexpected outputs.

Note



ModelSim versions operating without a dataflow license feature have limited Dataflow functionality. Without the license feature, the window will show only one process and its attached signals or one signal and its attached processes.

Figure 2-57. Dataflow Window



The Dataflow window displays:

- processes
- signals, nets, and registers
- interconnects

The window has built-in mappings for all Verilog primitive gates (that is, AND, OR, PMOS, NMOS, and so forth.). For components other than Verilog primitives, you can define a mapping between processes and built-in symbols. See [Symbol Mapping](#) for details.

Note



You cannot view SystemC objects in the Dataflow window.

When undocked, the Dataflow window contains the following toolbars:

- [Standard Toolbar](#)
- [Compile Toolbar](#)
- [Simulate Toolbar](#)
- [Wave Cursor Toolbar](#)
- [Dataflow Toolbar](#)
- [Wave Toolbar](#)
- [Zoom Toolbar](#)

FSM List Window

Use this window to view a list of finite state machines in your design.

This window is populated when you specify any of the following switches during compilation (vcom/vlog) or optimization (vopt).

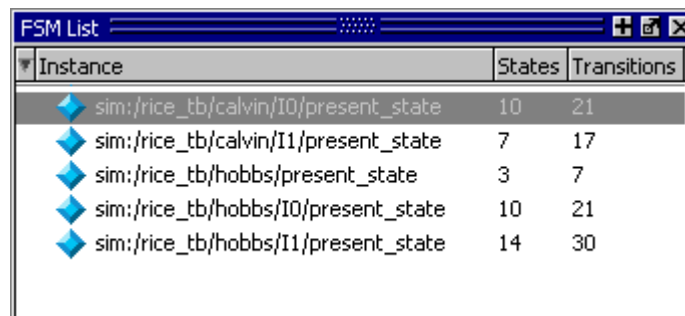
- +cover or +cover=f
- +acc or +acc=f

Accessing

Access the window using either of the following:

- Menu item: View > FSM List
- Command: view fsmlist

Figure 2-58. FSM List Window



The screenshot shows a window titled "FSM List" with a table containing the following data:

Instance	States	Transitions
sim:/rice_tb/calvin/I0/present_state	10	21
sim:/rice_tb/calvin/I1/present_state	7	17
sim:/rice_tb/hobbs/present_state	3	7
sim:/rice_tb/hobbs/I0/present_state	10	21
sim:/rice_tb/hobbs/I1/present_state	14	30

GUI Elements of the FSM List Window

This section describes GUI elements specific to this Window.

Column Descriptions

Table 2-32. FSM List Window Columns

Column Title	Description
Instance	Lists the FSM instances. You can reduce the number of path elements in this column by selecting the FSM List > Options menu item and altering the Number of Path Elements selection box.
States	The number of states in the FSM.
Transitions	The number of transitions in the FSM.

Popup Menu

Right-click on one of the FSMs in the window to display the popup menu and select one of the following options:

Table 2-33. FSM List Window Popup Menu

Popup Menu Item	Description
View FSM	Opens the FSM in the FSM Viewer window.
View Declaration	Opens the source file for the FSM instance.
Set Context	Changes the context to the FSM instance.
Add to <window>	Adds FSM information to the specified window.

FSM Viewer Window

Use the FSM Viewer window to graphically analyze finite state machines in your design. You can view FSMs as follows:

- Analyze FSMs and their coverage data — you must specify `+cover=f` during compilation and `-coverage` on the `vsim` command line to fully analyze FSMs with coverage data.
- Analyze FSMs without coverage data — you must specify the `+acc=f` switch during compilation (`vcom/vlog`) or optimization (`vopt`) to analyze FSMs with the FSM Viewer window.

Accessing

Access the window:


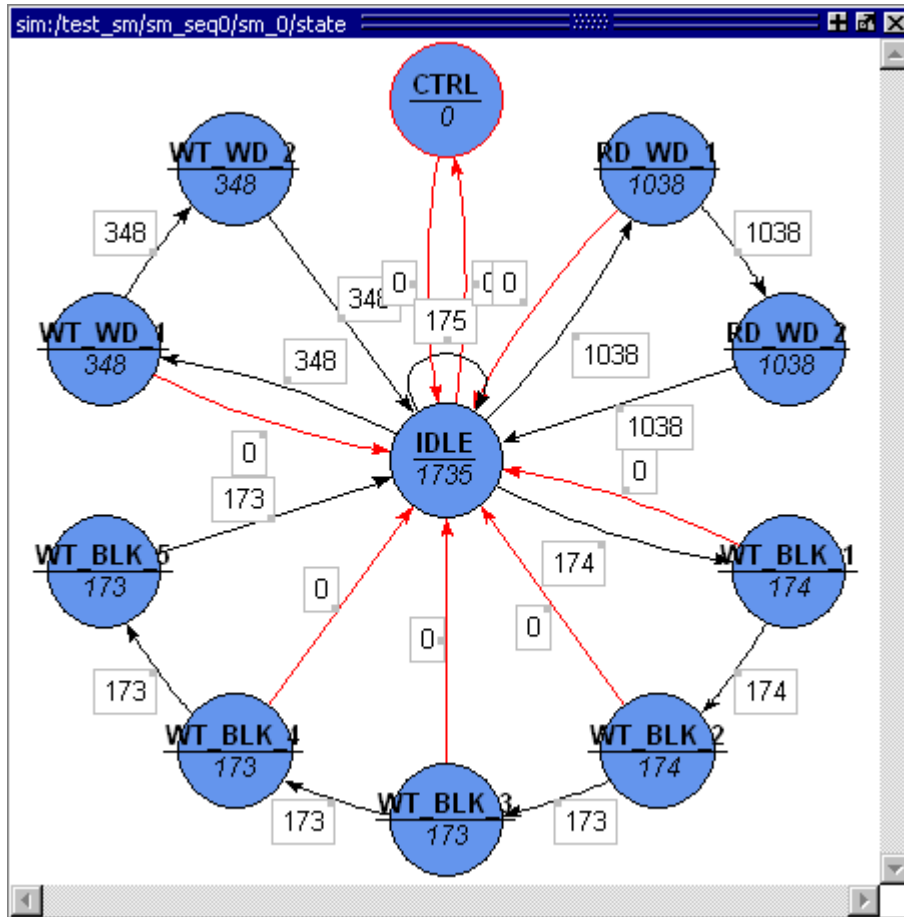
- From the FSM List window, double-click on the FSM you want to analyze.
- From the Objects, Locals, or Missed FSMs windows, click on the FSM button  for the FSM you want to analyze.

Figure 2-59. FSM Viewer Window



FSM Viewer Window Tasks

This section describes tasks for using the FSM Viewer window.

Using the Mouse in the FSM Viewer

These mouse operations are defined for the FSM Viewer:

- The mouse wheel performs zoom & center operations on the diagram.
 - Mouse wheel up — zoom out.
 - Mouse wheel down — zoom in.

Whether zooming in or out, the view will re-center towards the mouse location.

- Left mouse button — click and drag to move the view of the FSM.
- Middle mouse button — click and drag to perform the following stroke actions:
 - Up and left — Zoom Full.
 - Up and right — Zoom Out. The amount is determined by the distance dragged.
 - Down and right — Zoom In on the area of the bounding box.

Using the Keyboard in the FSM Viewer

These keyboard operations are defined for the FSM Viewer:

- Arrow Keys — scrolls the window in the specified direction.
 - Unmodified — scrolls by a small amount.
 - Ctrl+<arrow key> — scrolls by a larger amount.
 - Shift+<arrow key> — shifts the view to the edge of the display.

GUI Elements of the FSM Viewer Window

This section describes GUI elements specific to this Window.

Table 2-34. FSM Viewer Window — Graphical Elements








Graphical Element	Description	Definition
	Blue state bubble	Default appearance for non-reset states.
	Green state bubble	Indicates the FSM's current state, or the state of the wave cursor location (when tracking the wave cursor).
	Yellow state bubble	Indicates the FSM's previous state, or the state of the wave cursor location (when tracking the wave cursor).

Table 2-34. FSM Viewer Window — Graphical Elements

Graphical Element	Description	Definition
	Tan state bubble with double outline.	Indicates a reset state.
	Transition box	Contains information about the transition, <ul style="list-style-type: none"> • Cond: specifies the transition condition¹ • Count: specifies the coverage count
	Black transition line.	Indicates a transition.
	Red transition line.	Indicates a transition that has zero (0) coverage.

1. The condition format is based on the GUI_expression_format [Operators](#).

Popup Menu

Right-click in the window to display the popup menu and select one of the following options:

Table 2-35. FSM View Window Popup Menu

Popup Menu Item	Description
Transition	Only available when right-clicking on a transition. <ul style="list-style-type: none"> • View Source — Opens the source file containing the state machine and highlights the transition code. • View Full Text — Opens the View Transition dialog box, which contains the full text of the condition.
View Declaration	Opens the source file and bookmarks the file line containing the declaration of the state machine
Zoom Full	
Set Context	Executes the env command to change the context to that of the state machine.
Add to Wave Add to List Add to Log Add to Dataflow	Adds information about the state machine to the specific window.

FSM View Menu

This menu becomes available in the Main menu when the FSM View window is active.

Table 2-36. FSM View Menu

FSM View Menu Item	Description
Show State Counts	Displays the coverage counts for each state in the state bubble.
Show Transition Counts	Displays the coverage counts for each transition.
Show Transition Conditions	Displays the condition for each transition. The condition format is based on the GUI_expression_format Operators .
Enable Info Mode Popups	Displays popup information when you hover over a state or transition.
Track Wave Cursor	Displays current and previous state information based on the cursor location in the Wave window.
Show Transitions to “Reset”	Displays any transitions to the reset state.
Options	Displays the FSM Display Options dialog box, which allows you to control the grouping of signals when selecting Add to Wave from the popup menu.

Instance Coverage Window

The Instance Coverage window displays coverage statistics for each instance in a flat, non-hierarchical view. It allows sorting of data columns to be more meaningful, and not confused by hierarchy. This window contains the same code coverage statistics columns as in the Files and Structure windows.

A partial view of the Instance Coverage window is shown below.

Figure 2-60. Instance Coverage Window

Instance	Design unit	Design unit type	Stmt count	Stmt hits	Stmt misses	Stmt %	Stmt g
/test_sm/sram_0	beh_sram	Module	9	8	1	88.9%	Red
/test_sm/sm_seq0/sm_0	sm	Module	28	25	3	89.3%	Red
/test_sm/sm_seq0	sm_seq	Module	21	20	1	95.2%	Green
/test_sm	test_sm	Module	81	73	8	90.1%	Green

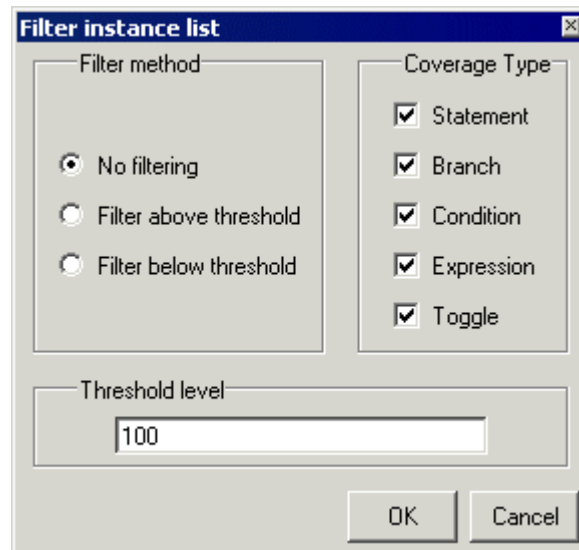
Setting a Coverage Threshold

You can specify a percentage above or below which you don't want to see coverage statistics. For example, you might set a threshold of 85% such that only objects with coverage below that percentage are displayed. Anything above that percentage is filtered.

Procedure

1. Right-click any object in the Instance Coverage window.
2. Select **Set filter**. The “Filter instance list” dialog appears as in [Figure 2-61](#).

Figure 2-61. Filter Instance List Dialog



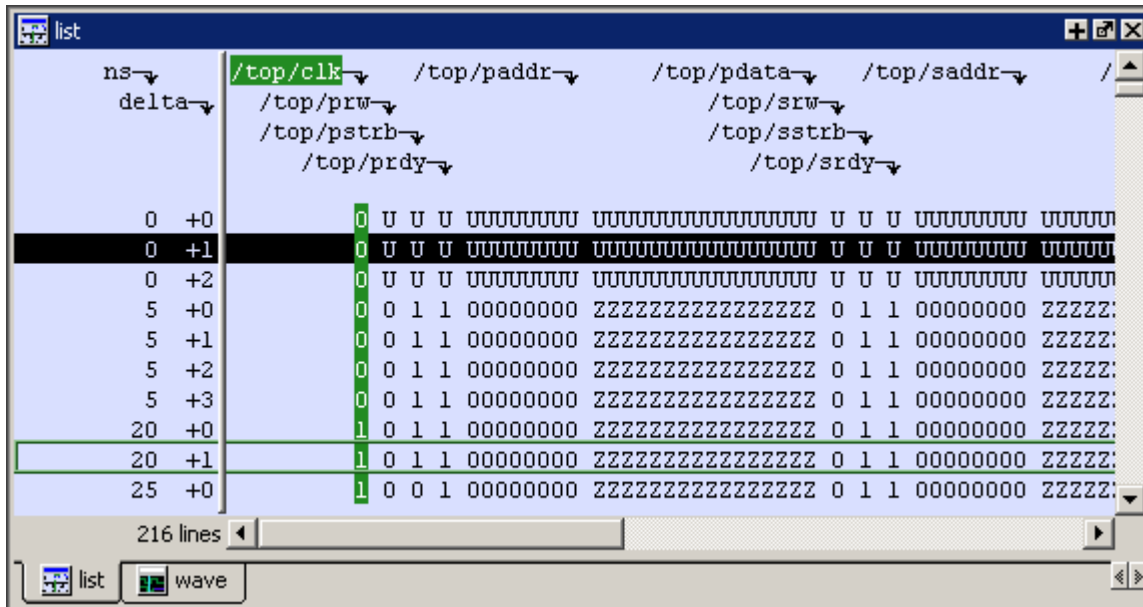
List Window

The List window displays a textual representation of waveforms, which you can configure to show events and delta events for the signals or objects you have added to the window.

You can view the following object types in the List window:

- VHDL — signals, aliases, process variables, and shared variables
- Verilog — nets, registers, and variables
- SystemC — primitive channels, ports, and transactions
- Comparisons — comparison objects; see [Waveform Compare](#) for more information
- Virtuals — Virtual signals and functions
- SystemVerilog — transactions

Figure 2-62. List Window



Displaying the List Window

- Select **View > List**
- Use the command:

view list

Viewing Data in the List Window

You can add information to the List window by right-clicking on signals and objects in the Objects window or the Structure window and selecting Add to List. You can also use the [add list](#) command.

Selecting Multiple Signals

To create a larger group of signals and assign a new name to this group, do the following:

1. Select a group of signals
 - Shift-click on signal columns to select a range of signals.
 - Control-click on signal columns to select a group of specific signals.
2. Select **List > Combine Signals**
3. Complete the Combine Selected Signals dialog box
 - Name — Specify the name you want to appear as the name of the new signal.

- Order of Indexes — Specify the order of the new signal as ascending or descending.
- Remove selected signals after combining — Specify whether the grouped signals should remain in the List window.

This process creates virtual signals. For more information, refer to the section [Virtual Signals](#).

GUI Elements of the List Window

This section describes the GUI elements specific to the List window.

Column Descriptions

The window is divided into two adjustable columns, which allow you to scroll horizontally through the listing on the right, while keeping time and delta visible on the left.

- The left column shows the time and any deltas that exist for a given time.
- The right column contains the data for the signals and objects you have added for each time shown in the left column. The top portion of the window contains the names of the signals. The bottom portion shows the signal values for the related time.

Note



The display of time values in the left column is limited to 10 characters. Any time value of more than 10 characters is replaced with the following:

```
too narrow
```

Markers

The markers in the List window are analogous to cursors in the Wave window. You can add, delete and move markers in the List window similarly to the Wave window. You will notice two different types of markers:

- Active Marker — The most recently selected marker shows as a black highlight.
- Non-active Marker — Any markers you have added that are not active are shown with a green border.

You can manipulate the markers in the following ways:

- Setting a marker — When you click in the right-hand portion of the List window, you will highlight a given time (black horizontal highlight) and a given signal or object (green vertical highlight).
- Moving the active marker — List window markers behave the same as Wave window cursors. There is one active marker which is where you click along with inactive markers generated by the Add Marker command. Markers move based on where you

click. The closest marker (either active or inactive) will become the active marker, and the others remain inactive.

- Adding a marker — You can add an additional marker to the List window by right-clicking at a location in the right-hand side and selecting Add Marker.
- Deleting a marker — You can delete a marker by right-clicking in the List window and selecting Delete Marker. The marker closest to where you clicked is the marker that will be deleted.

Menu Items

The following menu items are available from the right-click menu within the List window:

- Examine — Displays the value of the signal over which you used the right mouse button, at the time selected with the Active Marker
- Annotate Diff — Allows you to annotate a waveform comparison difference with additional information. For more information refer to the [compare annotate](#) command. Available only during a Waveform Comparison.
- Ignore Diff — Flags the waveform compare difference as “ignored”. For more information refer to the [compare annotate](#) command. Available only during a Waveform Comparison.
- Add Marker — Adds a marker at the location of the Active Marker.
- Delete Marker — Deletes the closest marker to your mouse location.

The following menu items are available when the List window is active:

- List > Add Marker — Adds a marker at the location of the Active Marker.
- List > Delete Marker — Deletes the closest marker to your mouse location.
- List > Combine Signals — Combines the signals you’ve selected in the List window.
- List > List Preferences — Allows you to specify the preferences of the List window.
- File > Export > Tabular List — Exports the information in the List window to a file in tabular format. Equivalent to the command:

```
write list <filename>
```

- File > Export > Event List — Exports the information in the List window to a file in print-on-change format. Equivalent to the command:

```
write list -event <filename>
```

- File > Export > TSSI List — Exports the information in the List window to a file in TSSI. Equivalent to the command:

```
write tssi -event <filename>
```

- **Edit > Signal Search** — Allows you to search the List window for activity on the selected signal.

Menu Items

When undocked, the List window contains the following toolbar:

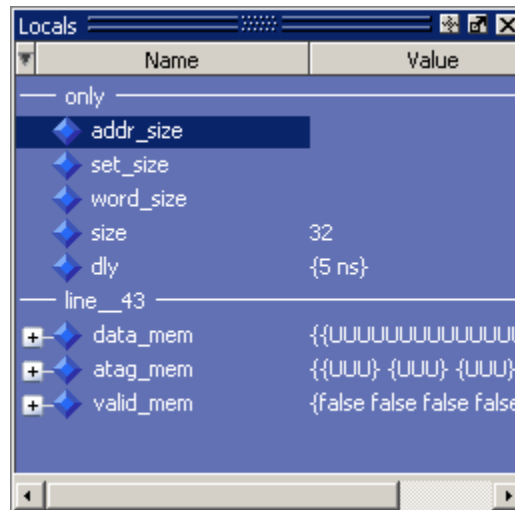
- [Standard Toolbar](#)

Locals Window

The Locals window displays data objects declared in the current, or local, scope of the active process. These data objects are immediately visible from the statement that will be executed next, which is denoted by a blue arrow in a Source window. The contents of the window change from one statement to the next.

When encountering a C breakpoint, the Locals window displays automatic local variables and their value in current C/C++ function scope.

Figure 2-63. Locals Window



Displaying the Locals Window

- Select **View > Locals**
- Use the command:

view locals

Viewing Data in the Locals Window

You cannot actively place information in the Locals window, it is updated as you go through your simulation. However, there are several ways you can trigger the Locals window to be updated.

- Run your simulation while debugging.
- Select a Process from the [Processes Window](#).
- Select a Verilog function or task or VHDL function or procedure from the [Call Stack Window](#).

GUI Elements of the Locals Window

This section describes the GUI elements specific to the Locals Window.

Column Descriptions

- **Name** — lists the names of the immediately visible data objects. This column also includes design object icons for the objects, refer to the section “[Design Object Icons and Their Meaning](#)” for more information.
- **Value** — lists the current value(s) associated with each name.
- **State Count** — Not shown by default. This column, State Hits, and State % are all specific to coverage analysis
- **State Hits** — Not shown by default.
- **State %** — Not shown by default.

Menu Items

- **View Declaration** — Displays, in the Source window, the declaration of the object.

You can access this feature from the Locals menu of the Main window or the right-click menu in the Locals window.

- **Add** — Adds the selected object(s) to the specified window (Wave, List, Log, Dataflow).

You can access this feature from the Add menu of the Main window, the right-click menu of the Locals window, or the Add menu of the undocked Locals window.

- **Change** — Displays the [Change Selected Variable Dialog Box](#), which allows you to alter the value of the object.

You can access this feature from the Locals menu of the Main window or the right-click menu in the Locals window.

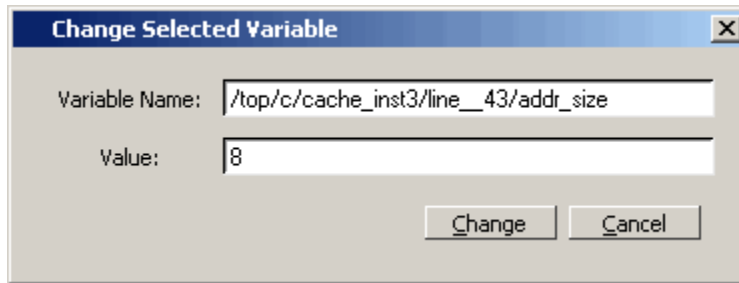
Menu Items

When undocked, the Locals window contains a subset of the [Standard Toolbar](#).

Change Selected Variable Dialog Box

This dialog box allows you to change the value of the object you selected. When you click Change, the tool executes the [change](#) command on the object.

Figure 2-64. Change Selected Variable Dialog Box



The Change Selected Variable dialog is prepopulated with the following information about the object you had selected in the Locals window:

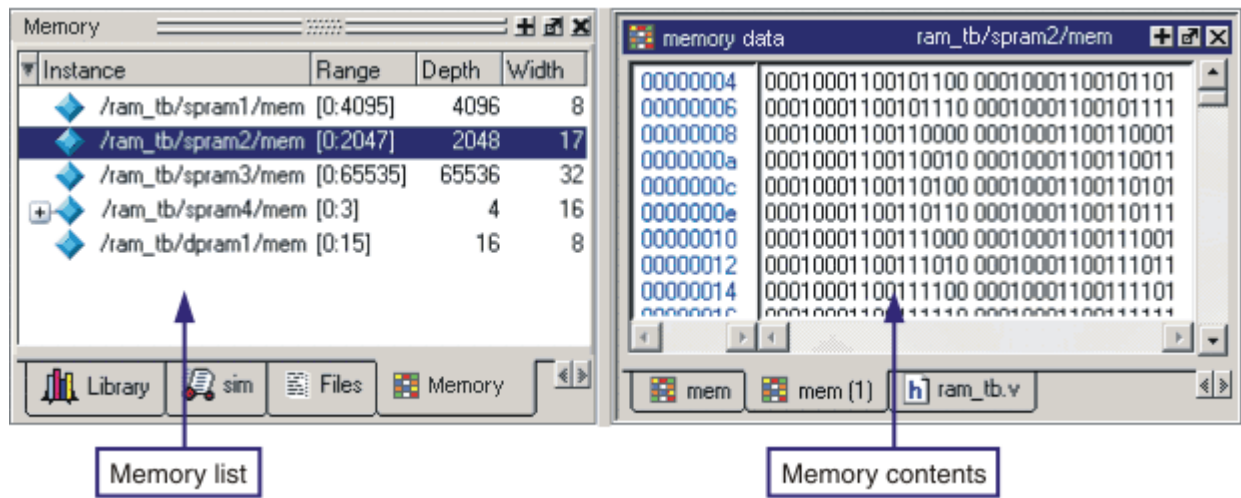
- Variable Name — contains the complete name of the object.
- Value — contains the current value of the object.

When you change the value of the object, you can enter any value that is valid for the variable. An array value must be specified as a string (without surrounding quotation marks). To modify the values in a record, you need to change each field separately.

Memory and Memory Data Windows

The Main window lists all memories in your design in the Memory window and displays the contents of a selected memory in the Memory Data window.

Figure 2-65. Memory and Memory Data Windows



The Memory window is from the top-level of the design. In other words, it is not sensitive to the context selected in the Structure window.

When undocked, the Memory window allows access to the [Memory Toolbar](#).

ModelSim identifies certain kinds of arrays in various scopes as memories. Memory identification depends on the array element kind as well as the overall array kind (that is, associative array, unpacked array, and so forth.).

Table 2-37. Memories

	VHDL	Verilog/SystemVerilog	SystemC
Element Kind¹	enum ² , bit_vector, floating point type, std_logic_vector, std_ulogic_vector, or integer type	any integral type (that is, integer_type): shortint, int, longint, byte, bit (2 state), logic, reg, integer, time (4 state), packed_struct/packed_union (2 state), packed_struct / packed_union (4 state), packed_array (single-Dim, multi-D, 2 state and 4 state), enum or string.	unsigned char, unsigned short, unsigned int, unsigned long, unsigned long long, char, short, int, float double, enum sc_bigint sc_biguint sc_int sc_uint sc_signed sc_unsigned
Scope: Recognizable in	architecture, process, or record	module, interface, package, compilation unit, struct, or static variables within a task / function / named block / class	sc_module

Table 2-37. Memories

	VHDL	Verilog/SystemVerilog	SystemC
Array Kind	single-dimensional or multi-dimensional	any combination of unpacked, dynamic and associative arrays ³ ; real/shortreal and float	single-dimensional or multi-dimensional

1. The element can be "bit" or "std_ulogic" if the array has dimensionality ≥ 2 .
2. These enumerated types must have at least one enumeration literal that is not a character literal. The listed width is the number of entries in the enumerated type definition and the depth is the size of the array itself.
3. Any combination of unpacked, dynamic, and associative arrays is considered a memory, provided the leaf level of the data structure is a string or an integral type.

Associative Arrays in Verilog/SystemVerilog

For an associative array to be recognized as a memory, the index must be of an integral type (see above) or wildcard type.

For associative arrays, the element kind can be any type allowed for fixed-size arrays.

Viewing Single and Multidimensional Memories

For single and multi-dimensional VHDL arrays to be considered memories, the following rules apply:

- Any one-dimensional array whose element type is:
 - an integer type (including type INTEGER),
 - a floating point type (including REAL), or
 - an enumeration subtype whose enumeration literals include at least one non-character literal (this requirement disqualifies any one-dimensional array of BIT or STD_ULOGIC in particular).
- Any one-dimensional array of:
 - BIT_VECTOR,
 - STD_LOGIC_VECTOR, or
 - STD_ULOGIC_VECTOR.
- Any multidimensional ($N \geq 2$) array of:
 - an integer type,
 - a floating point type, or

- an enumeration type whose enumeration literal includes at least one non-character literal.

Single dimensional arrays of integers are interpreted as 2D memory arrays. In these cases, the word width listed in the Memory window is equal to the integer size, and the depth is the size of the array itself.

Memories with three or more dimensions display with a plus sign '+' next to their names in the Memory window. Click the '+' to show the array indices under that level. When you finally expand down to the 2D level, you can double-click on the index, and the data for the selected 2D slice of the memory will appear in a memory contents window.

Viewing Packed Arrays

By default packed dimensions are treated as single vectors in the memory contents window. To expand packed dimensions of packed arrays, select **View > Memory Contents > Expand Packed Memories**.

To change the permanent default, edit the PrefMemory(ExpandPackedMem) variable. This variable affects only packed arrays. If the variable is set to 1, the packed arrays are treated as unpacked arrays and are expanded along the packed dimensions such that they appear as a linearized bit vector. See [Simulator GUI Preferences](#) for details on setting preference variables.

Viewing Memory Contents

When you double-click an instance on the Memory window, ModelSim automatically displays a Memory Data window, where the name used on the tab is taken from the name of the instance, as seen in the Memory window. You can also enter the command **add mem <instance>** at the **vsim** command prompt.

Direct Address Navigation

You can navigate to any address location directly by editing the address in the address column. Double-click on any address, type in the desired address, and hit **Enter**. The address display scrolls to the specified location.

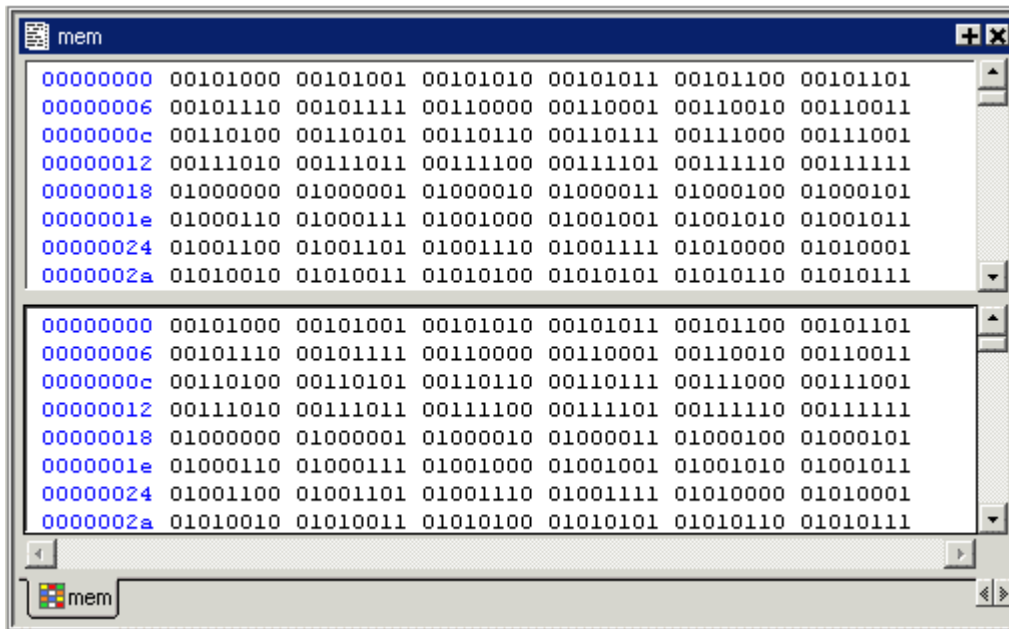
Splitting the Memory Contents Window

To split a memory contents window into two screens displaying the contents of a single memory instance, so any one of the following:

- select **Memory Data > Split Screen** if docked.
- select **View > Split Screen** if undocked.
- right-click in the window and select **Split Screen** from the pop-up menu.

This allows you to view different address locations within the same memory instance simultaneously.

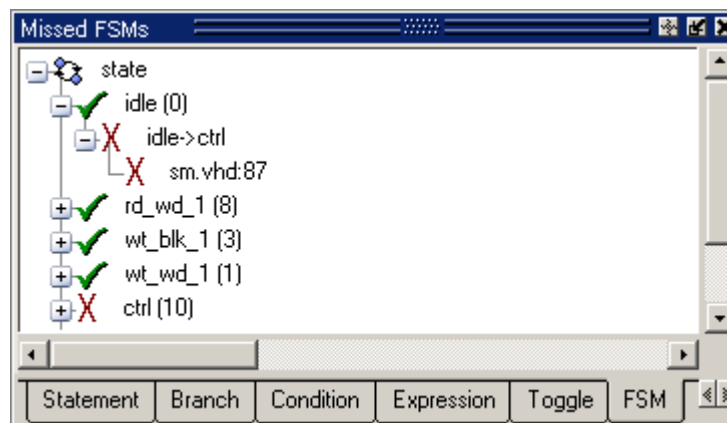
Figure 2-66. Split Screen View of Memory Contents



Missed Coverage Windows

When you select a file in the Files window, the Missed Coverage windows display uncovered (missed) statements, branches, conditions, and expressions, as well as signals that haven't toggled, and finite state machines (FSM) with uncovered states and transitions. There is a window for each coverage type.

Figure 2-67. Missed Coverage Window



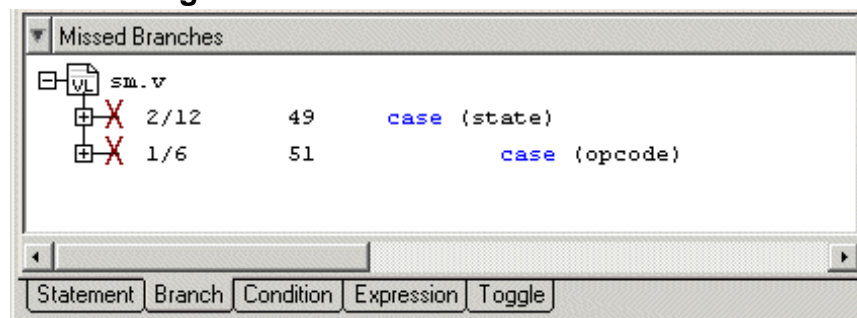
Each window includes a column for the line number and a column for statement, branch, condition, expression, or toggle on that line. An "X" indicates the object was not executed. If

only the UDP coverage has a 0 row, an “Xudp” appears, and if only the FEC coverage has a 0 row, an “Xfec” appears.

When you select (left-click) any object in the Branch, Condition, Expression or Toggle windows, the [Coverage Details Window](#) populates with related details (coverage statistic details, truth tables, and so on) about that object.

The Missed Branches window also includes a column for branch code (conditional "if/then/else" and "case" statements). "X_T" indicates that only the true condition of the branch was not executed. "X_F" indicates that only the false condition of the branch was not executed. Fractional numbers indicate how many case statement labels were not executed. For example, if only one of six case labels executed, the Missed Branches window would indicate "X 1/6."

Figure 2-68. Missed Branches Window



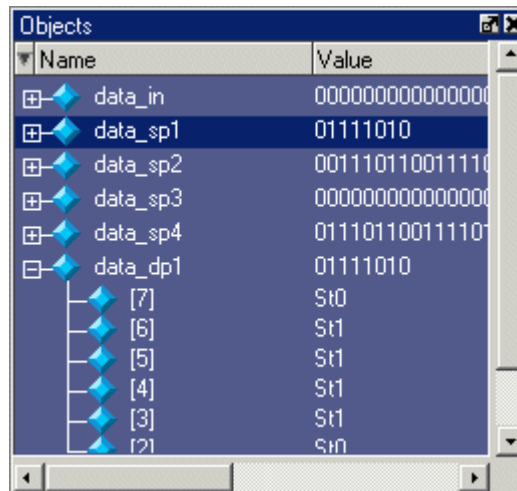
When you right-click any object in the Missed Statement, Branch, Condition, or Expression windows you can select **Exclude Selection** or **Exclude Selection for Instance <name>** to exclude the object from coverage statistics and make it appear in the Current Exclusions window.

Objects Window

The Objects window shows the names and current values of declared data objects in the current region (selected in the Structure window). Data objects include signals, nets, registers, constants and variables not declared in a process, generics, parameters, transactions, SystemC member data variables.

Clicking an entry in the window highlights that object in the Dataflow and Wave windows. Double-clicking an entry highlights that object in a Source window (opening a Source window if one is not open already). You can also right click an object name and add it to the List or Wave window, or the current log file.

Figure 2-69. Objects Window



Filtering the Objects List

You can filter the objects list by name or by object type.

Filtering by Name

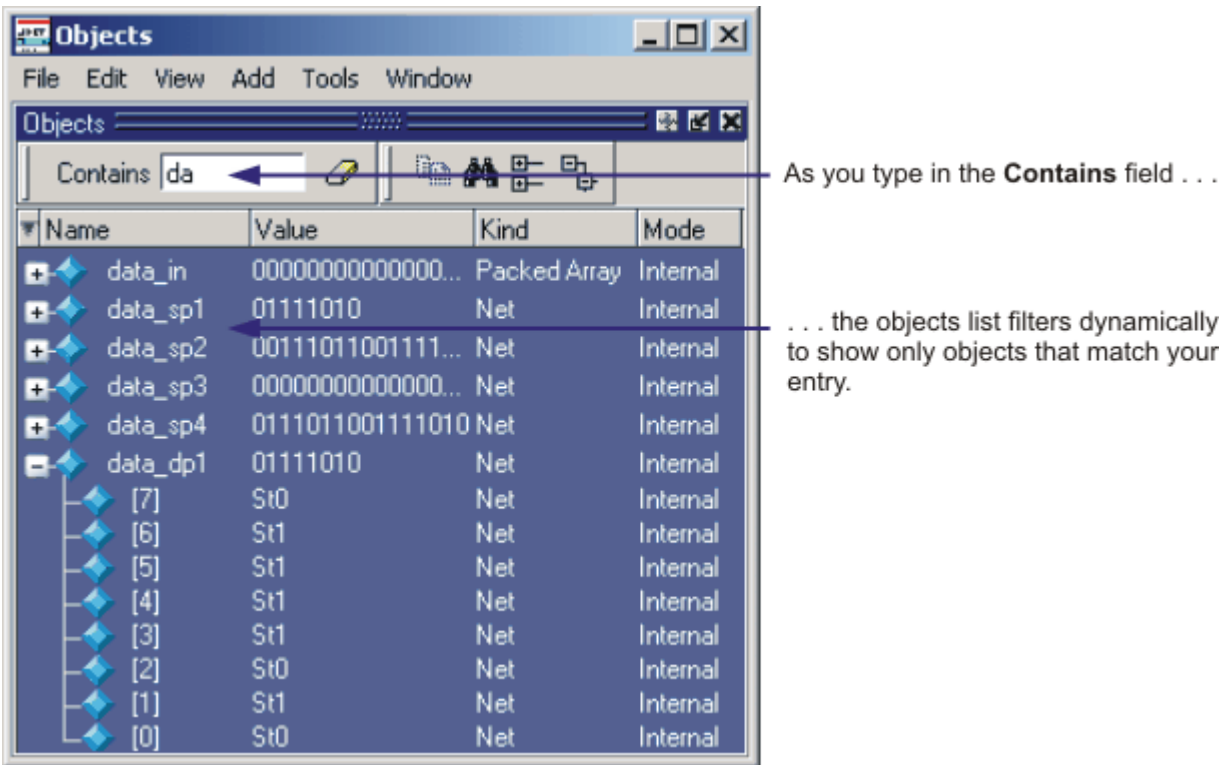
To filter by name, undock the Objects window from the Main window and start typing letters in the **Contains** field in the toolbar.

Figure 2-70. Objects Filter



As you type, the objects list filters to show only those signals that contain those letters.

Figure 2-71. Filtering the Objects List by Name



To display all objects again, click the Eraser icon to clear the entry.

Filters are stored relative to the region selected in the Structure window. If you re-select a region that had a filter applied, that filter is restored. This allows you to apply different filters to different regions.

Filtering by Signal Type

The **View > Filter** menu selection allows you to specify which signal types to display in the Objects window. Multiple options can be selected.

Toggle Coverage in the Objects Window

Toggle coverage data is displayed in the Objects window in multiple columns, as shown below. There is a column for each of the six transition types.

Figure 2-72. Objects Window - Toggle Coverage

Name	Value	Kind	Mode	1H->0L	0L->1H	0L->Z	Z->0L	1H->Z	Z->1H	#Nodes	#Toggled	% Toggled	% 01	% Full	% Z
into	0100000000...	Reg	Internal	119628	119629	0	0	0	0	32	11	34.38%	34.38%	11.46%	0%
outof	0000000000...	Reg	Internal	20800	20804	0	0	0	0	32	6	18.75%	21.88%	7.292%	0%
rst	0	Reg	Internal	2	1	0	0	0	0	1	1	100%	100%	33.33%	0%
clk	1	Reg	Internal	83222	83223	0	0	0	0	1	1	100%	100%	33.33%	0%
out_wire	0000000000...	Net	Internal	20800	20804	0	0	0	0	32	6	18.75%	21.88%	7.292%	0%
dat	0000000000...	Net	Internal	23401	28607629308634542	119620	114418			32	6	18.75%	21.88%	47.92%	60.94%
addr	0000100000	Net	Internal	26006	26007	0	0	0	0	10	4	40%	40%	13.33%	0%
loop	xxxxxxxxxxxx...	Reg	Internal	0	0	0	0	0	0	32	0	0%	0%	0%	0%
i	x	Variable	Internal												
rd_	S10	Net	Internal	15602	15601	0	0	0	0	1	1	100%	100%	33.33%	0%
wr_	S11	Net	Internal	7803	7803	0	0	0	0	1	1	100%	100%	33.33%	0%

Right click any column name to toggle a column on or off.

The following table provides a description of the available columns:

Table 2-38. Toggle Coverage Columns in the Objects Window

Column name	Description
Name	the name of each object in the current region
Value	the current value of each object
Kind	the object type
Mode	the object mode (internal, in, out, and so forth.)
1H -> 0L	the number of times each object has transitioned from a 1 or a High state to a 0 or a Low state
0L -> 1H	the number of times each object has transitioned from a 0 or a Low state to 1 or a High state
0L -> Z	the number of times each object has transitioned from a 0 or a Low state to a high impedance (Z) state
Z -> 0L	the number of times each object has transitioned from a high impedance state to a 0 or a Low state
1H -> Z	the number of times each object has transitioned from a 1 or a High state to a high impedance state
Z -> 1H	the number of times each object has transitioned from a high impedance state to 1 or a High state
State Count	the number of values a state machine variable can have
State Hits	the number of state machine variable values that have been hit
State %	the current ration of State Hits to State Count
# Nodes	the number of scalar bits in each object

Table 2-38. Toggle Coverage Columns in the Objects Window

Column name	Description
# Toggled	the number of nodes that have transitioned at least once. A signal is considered toggled if and only if: <ul style="list-style-type: none"> • it has 0- >1 and 1->0 transitions and NO Z transitions, or • if there are ANY Z transitions, it must have ALL four of the Z transitions. Otherwise, the counts are place in % 01 or % Z columns. For more specifics on what is considered “toggled”, see “Understanding Toggle Counts”
% Toggled	the current ratio of the # Toggled to the # Nodes for each object
% 01	the percentage of 1H -> 0L and 0L -> 1H transitions that have occurred (transitions in the first two columns)
% Full	the percentage of all transitions that have occurred (all six columns)
% Z	the percentage of 0L -> Z , Z -> 0L , 1H -> Z , and Z -> 1H transitions that have occurred (last four columns)

Profiling Windows

The Profiling windows (Ranked, Design Units, Call Tree, and Structural) and the Profile Details window display the results of statistical performance and memory allocation profiling.

For details about using the profiler refer to [Profiling Performance and Memory Use](#).

When undocked, the Profile windows contain the following toolbars:

- [Standard Toolbar](#)
- [Profile Toolbar](#)

Profiling Window Columns

The Profiling windows include the columns described below.

- **Name** — lists the filename of an HDL function or instance, and the line number at which it appears. Most useful names consist of a line of VHDL or Verilog source code. If you use a PLI/VPI or FLI routine, then the name of the C function that implements that routine can also appear in the Name column.
- **Under (raw)** — lists the raw number of Profiler samples collected during the execution of a function, including all support routines under that function; or, the number of

samples collected for an instance, including all instances beneath it in the structural hierarchy.

- **In (raw)** — lists the raw number of Profiler samples collected during a function or instance.
- **Under%** — lists the ratio (as a percentage) of the samples collected during the execution of a function and all support routines under that function to the total number of samples collected; or, the ratio of the samples collected during an instance, including all instances beneath it in the structural hierarchy, to the total number of samples collected.
- **In%** — lists the ratio (as a percentage) of the total samples collected during a function or instance.
- **%Parent** — (not in Ranked view) lists the ratio, as a percentage, of the samples collected during the execution of a function or instance to the samples collected in the parent function or instance.
- **Mem under** — lists the amount of memory allocated to a function, including all support routines under that function; or, the amount of memory allocated to an instance, including all instances beneath it in the structural hierarchy.
- **Mem in** — lists the amount of memory allocated to a function or instance.
- **Mem under (%)** — lists the ratio (as a percentage) of the amount of memory allocated to a function and all of its support routines to the total memory available; or, the ratio of the amount of memory allocated to an instance, including all instances beneath it in the structural hierarchy, to the total memory available.
- **Mem in (%)** — lists the ratio (as a percentage) of the amount of memory allocated to a function or instance to the total memory available.
- **%Parent** — lists (not in Ranked view) the ratio, as a percentage, of the memory allocated to a function or instance to the memory allocated to the parent function or instance.
- **sum(Mem in)** — lists the cumulative memory allocated.
- **sum(Mem in(%))** — lists the ratio of the cumulative memory allocated.

Source Window

The Source window allows you to view and edit source files as well as set breakpoints, step through design files, and view code coverage statistics.

By default, the Source window displays your source code with line numbers. You may also see the following graphic elements:

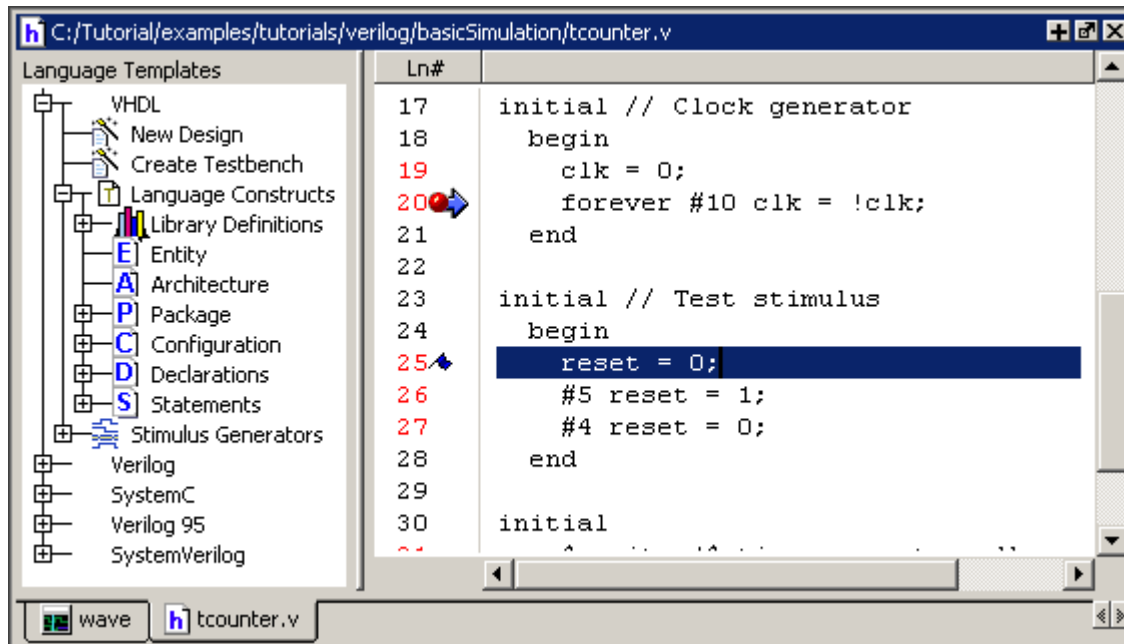
- Red line numbers — denote executable lines, where you can set a breakpoint

- Blue arrow — denotes the currently active line or a process that you have selected in the [Processes Window](#)
- Red ball in line number column — denotes file-line breakpoints; gray ball denotes breakpoints that are currently disabled
- Blue flag in line number column — denotes line bookmarks
- Language Templates pane — displays templates for writing code in VHDL, Verilog, SystemC, Verilog 95, and SystemVerilog ([Figure 2-73](#)). See [Using Language Templates](#).
- Green check mark — denotes statements, branches or expressions in a particular line that have been covered.
- Red X with no subscripts denotes that multiple kinds of coverage on the line are not covered.
- Red X with subscripts — denotes a statement, branch (false or true), condition or expression was not covered. (see “[Coverage Data in the Source Window](#)” for details)
- Green E with no subscripts— denotes a line of code to which active coverage exclusions have been applied. Every item on line is excluded; none are hit.
- Green E with subscripts — denotes a line of codes with various degrees of exclusion (see “[Coverage Data in the Source Window](#)” for details)
- Underlined text — denotes a hypertext link that jumps to a linked location, either in the same file or to another Source window file. Display is toggled on and off by the Source Navigation button.

When undocked, the Source window provides access to the following toolbars:

- [Standard Toolbar](#)
- [Compile Toolbar](#)
- [Simulate Toolbar](#)
- [Coverage Toolbar](#)
- [Source Toolbar](#)

Figure 2-73. Source Window Showing Language Templates



Opening Source Files

You can open source files using the **File > Open** command or by clicking the **Open** icon. Alternatively, you can open source files by double-clicking objects in other windows. For example, if you double-click an item in the Objects window or in the structure tab (**sim** tab), the underlying source file for the object will open in the Source window and scroll to the line where the object is defined.

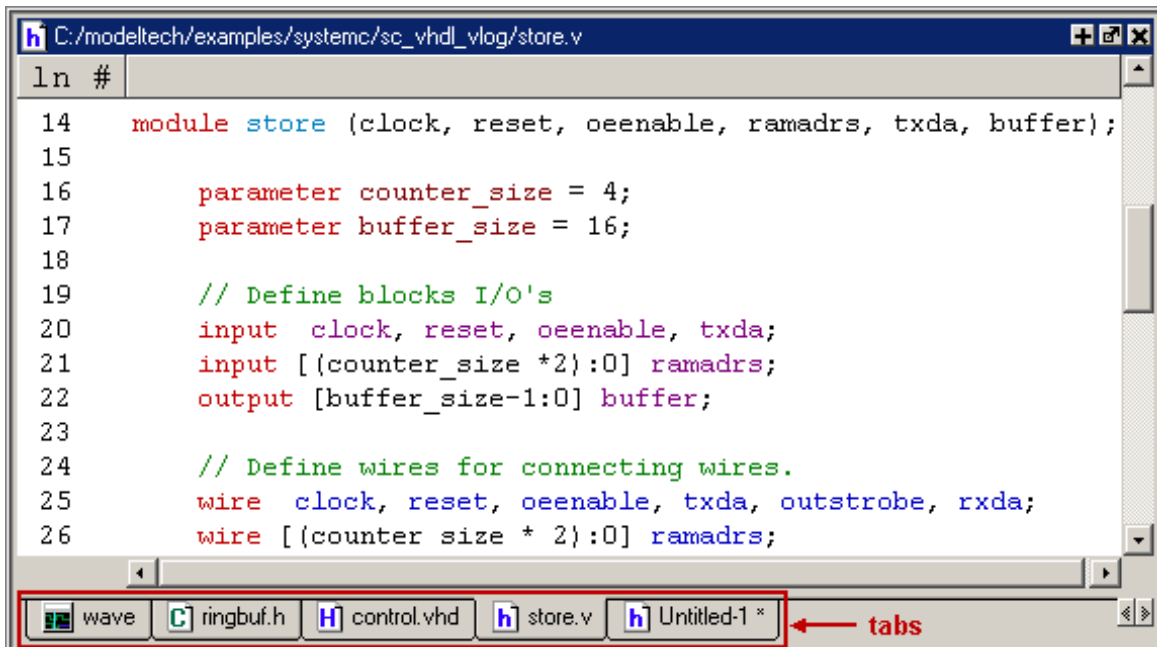
From the command line you can use the [edit](#) command.

By default, files you open from within the design (such as when you double-click an object in the Objects window) open in Read Only mode. To make the file editable, right-click in the Source window and select (uncheck) Read Only. To change this default behavior, set the PrefSource(ReadOnly) variable to 0. See [Simulator GUI Preferences](#) for details on setting preference variables.

Displaying Multiple Source Files

By default each file you open or create is marked by a window tab, as shown in the graphic below.

Figure 2-74. Displaying Multiple Source Files



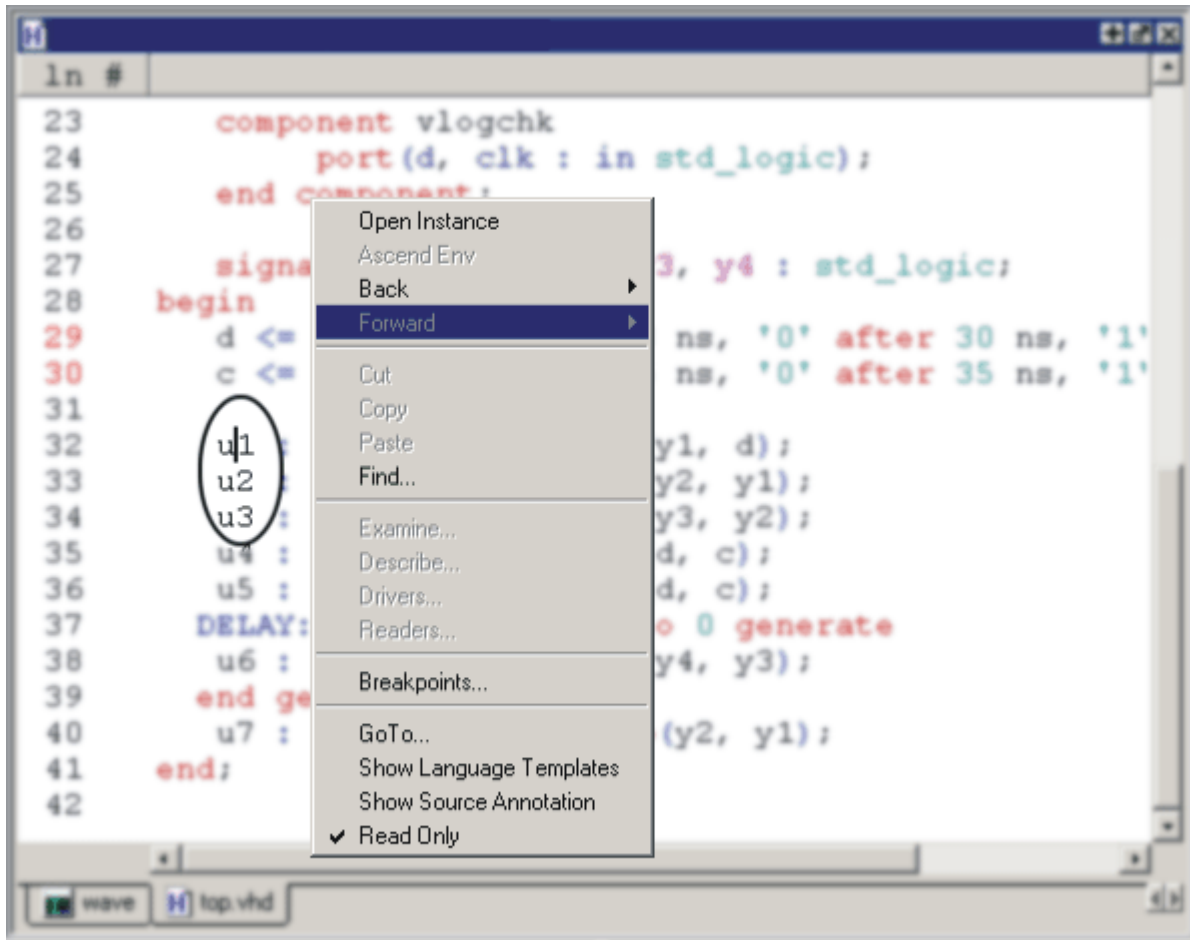
Dragging and Dropping Objects into the Wave and List Windows

ModelSim allows you to drag and drop objects from the Source window to the Wave and List windows. Double-click an object to highlight it, then drag the object to the Wave or List window. To place a group of objects into the Wave and List windows, drag and drop any section of highlighted code.

Setting your Context by Navigating Source Files

When debugging your design from within the GUI, you can change your context while analyzing your source files. Figure 2-75 shows the pop-up menu the tool displays after you select then right-click an instance name in a source file.

Figure 2-75. Setting Context from Source Files



This functionality allows you to easily navigate your design for debugging purposes by remembering where you have been, similar to the functionality in most web browsers. The navigation options in the pop-up menu function as follows:

- **Open Instance** — changes your context to the instance you have selected within the source file. This is not available if you have not placed your cursor in, or highlighted the name of, an instance within your source file.

If any ambiguities exists, most likely due to generate statements, this option opens a dialog box allowing you to choose from all available instances.

- **Ascend Env** — changes your context to the next level up within the design. This is not available if you are at the top-level of your design.
- **Forward/Back** — allows you to change to previously selected contexts. This is not available if you have not changed your context.

The Open Instance option is essentially executing an [environment](#) command to change your context, therefore any time you use this command manually at the command prompt, that information is also saved for use with the Forward/Back options.

Highlighted Text in a Source Window

The Source window can display text that is highlighted as a result of various conditions or operations, such as the following:

- Double-clicking an error message in the transcript shown during compilation
- Using "Goto Driver"
- Coverage-related operations

In these cases, the relevant text in the source code is shown with a persistent highlighting. To remove this highlighted display, choose Clear Highlights from the popup menu of the Source window. You can display this popup menu from the main menu, the docked Source window, or the undocked Source window, as follows:

Main menu: Source > More > Clear Highlights

Docked: (right-click) More > Clear Highlights

Undocked: (right-click) Edit > Advanced > Clear Highlights

Note



Clear Highlights does not affect text that you have selected with the mouse cursor.

Example

To produce a compile error that displays highlighted text in the Source window, do the following:

1. Choose Compile > Compile Options...
2. In the Compiler Options dialog box, click either the VHDL tab or the Verilog & System Verilog tab.
3. Enable Show source lines with errors and click OK.
4. Open a design file and create a known compile error (such as changing the word "entity" to "entry" or "module" to "nodule").
5. Choose Compile > Compile... and then complete the Compile Source Files dialog box to finish compiling the file.
6. When the compile error appears in the Transcript window, double-click on it.
7. The source window is opened (if needed), and the text containing the error is highlighted.
8. To remove the highlighting, choose Source > More > Clear Highlights.

Hyperlinked (Underlined) Text in a Source Window

The Source window supports hyperlinked navigation, providing links displayed as underlined text. To turn hyperlinked text on or off in the Source window, do the following:

1. Click anywhere in the Source window. This enables the display of the Source toolbar (see [Table 2-21](#)).
2. Click the Source Navigation button.

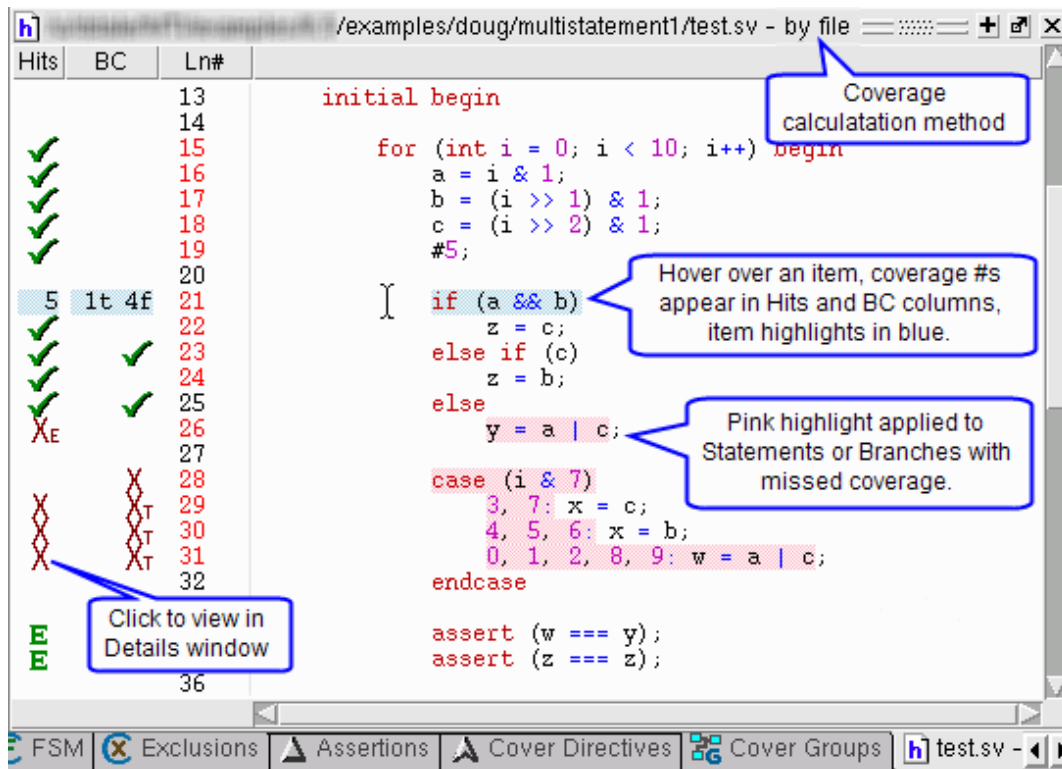
When you double-click on hyperlinked text, the selection jumps from the usage of an object to its declaration. This provides the following operations:

- Jump from the usage of a signal, parameter, macro, or a variable to its declaration.
- Jump from a module declaration to its instantiation, and vice versa.
- Navigate back and forth between visited source files.

Coverage Data in the Source Window

The [Source Window](#) includes two columns for code coverage statistics – the Hits column and the BC (Branch Coverage) column. These columns provide an immediate visual indication about how your source code is executing. The code coverage indicators are check marks, Xs and Es, the complete variety of which are described in [Table 2-39](#).

Figure 2-76. Coverage in Source Window
















To see more information about any coverage item, click on the indicator icon, or in the Hits or BC column for the line of interest. This brings up detailed coverage information for that line in the Coverage Details window.

For example, when you select an expression in the Missed Expressions window, and you click in the column of a line containing an expression, the associated truth tables appear in the Coverage Details window. Each line in the truth table is one of the possible combinations for the expression. The expression is considered to be covered (gets a green check mark) only if the entire truth table is covered.

When you hover over statements, conditions or branches in the Source window, the Hits and BC columns display the coverage numbers for that line of code. For example, in Figure 2-76, the blue line shows that the expression (a && b) was hit 5 times and that the branch (if) was evaluated as true once (1t) and false four times (4f). The value in the Hits column shows the total coverage for all items in the UDP table (as shown in the Coverage Details window when you click the specific line in the hits column).

Source Window Code Coverage Indicator Icons

Table 2-39. Source Window Code Coverage Indicators

Icon	Description/Indication
	All statements, branches or expressions on a particular line have been covered
	Multiple kinds of coverage on the line are not covered
	True branch not covered (BC column)
	False branch not covered (BC column)
	Condition not covered (Hits column)
	Expression not covered (Hits column)
	Branch not covered (Hits column)
	Statement not covered (Hits column)
	Indicates a line of code to which active coverage exclusions have been applied. Every item on the line is excluded; none are hit.
	Some excluded items are hit
	Some items are excluded, and all items not excluded are hit
	Some items are excluded, and some items not excluded have missing coverage
	Auto exclusions have been applied to this line. Hover the cursor over the E _A and a tool tip balloon appears with the reason for exclusion,

Coverage data presented in the Source window is either calculated “by file” or “by instance”, as indicated just after the source file name. If coverage numbers are mismatched between Missed <coverage_type> window and the Source window, check to make sure that both are being calculated the same — either “by file” or “by instance”.

To display only numbers in Hits and BC columns, select **Tools > Code Coverage > Show Coverage Numbers**.

When the source window is active, you can skip to "missed lines" three ways:

- select **Edit > Previous Coverage Miss** and **Edit > Next Coverage Miss** from the menu bar
- click the Previous zero hits and Next zero hits icons on the toolbar
- press Shift-Tab (previous miss) or Tab (next miss)

Controlling Data Displayed in a Source Window

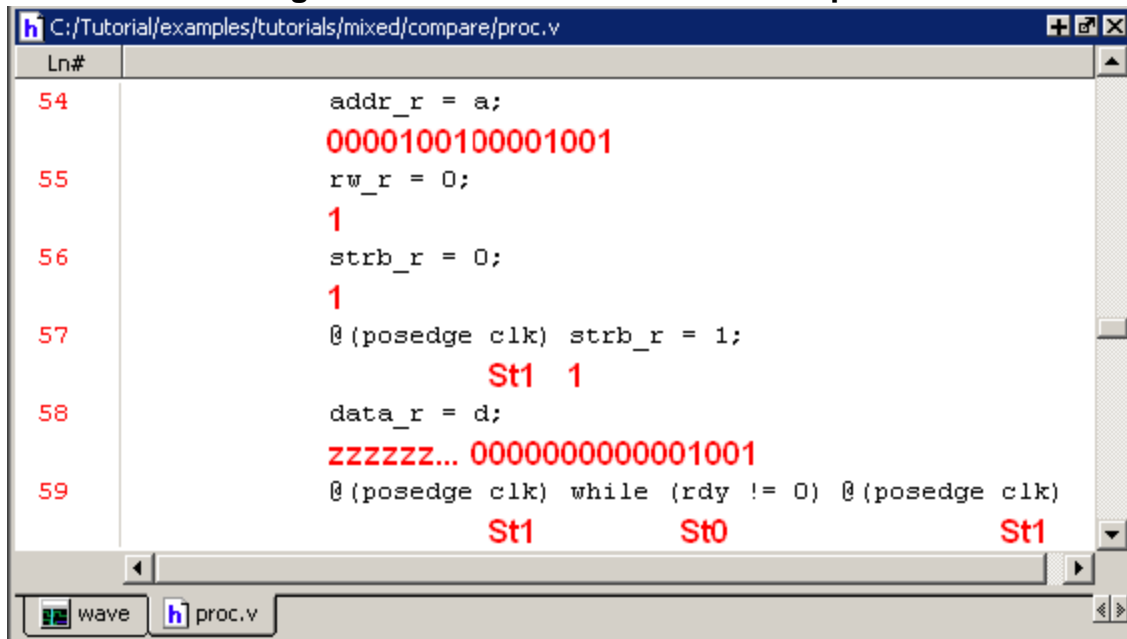
The **Tools > Code Coverage** menu contains several commands for controlling coverage data display in a Source window.

- **Hide/Show coverage data** toggles the *Hits* column off and on.
- **Hide/Show branch coverage** toggles the *BC* column off and on.
- **Hide/Show coverage numbers** displays the number of executions in the *Hits* and *BC* columns rather than check marks and Xs. When multiple statements occur on a single line an ellipsis ("...") replaces the Hits number. In such cases, hover the cursor over each statement to highlight it and display the number of executions for that statement.
- **Show coverage By Instance** displays only the number of executions for the currently selected instance in the Main window workspace.

Debugging with Source Annotation

With source annotation you can interactively debug your design by analyzing your source files in addition to using the Wave and Signal windows. Source annotation displays simulation values, including transitions, for each signal in your source file. [Figure 2-77](#) shows an example of source annotation, where the red values are added below the signals.

Figure 2-77. Source Annotation Example



Turn on source annotation by selecting **Source > Show Source Annotation** or by right-clicking a source file and selecting **Show Source Annotation**. Note that transitions are displayed only for those signals that you have logged.

To analyze the values at a given time of the simulation you can either:

- Show the signal values at the current simulation time. This is the default behavior. The window automatically updates the values as you perform a run or a single-step action.
- Show the signal values at current cursor position in the Wave window.

You can switch between these two settings by performing the following actions:

- When Docked:
 - **Source > Examine Now**
 - **Source > Examine Current Cursor**
- When Undocked:
 - **Tools > Options > Examine Now**
 - **Tools > Options > Examine Current Cursor**

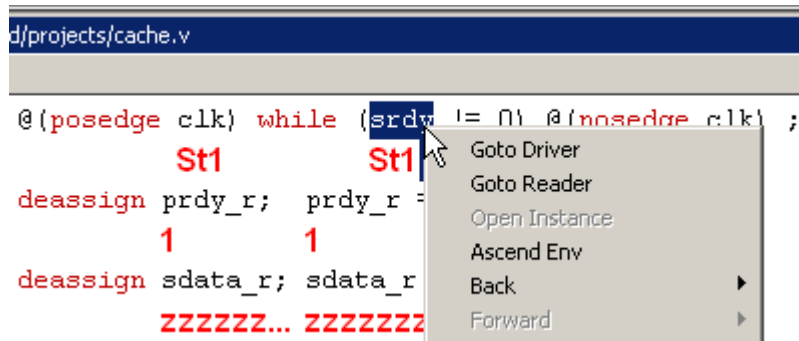
You can highlight a specific signal in the Wave window by double-clicking on an annotation value in the source file.

Accessing Textual Dataflow Information

The Source window contains textual dataflow information that allows you to explore the connectivity of your design through the source code. This feature is especially useful when used with source annotation turned on.

When you double-click an instance name in the Structure (sim) window, a Source window will open at the appropriate instance. You can then access textual dataflow information in the Source window by right-clicking any signal. This opens a popup menu that gives you the choices shown in Figure 2-78.

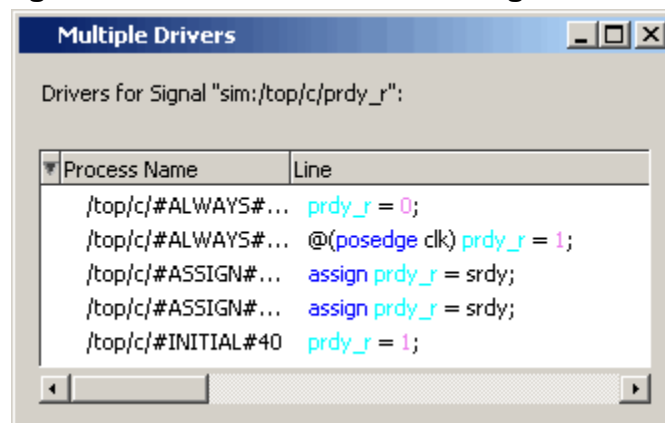
Figure 2-78. Popup Menu Choices for Textual Dataflow Information



- The **Goto Driver** selection causes the Source window to jump to the source code defining the driver of the selected signal. If the Driver is in a different Source file, that file will open in a new Source window tab and the driver code will be highlighted. You can also jump to the driver of a signal by simply double-clicking the signal.

If there is more than one driver for the signal, a Multiple Drivers dialog will open showing all drivers (Figure 2-79).

Figure 2-79. Window Shows all Signal Drivers

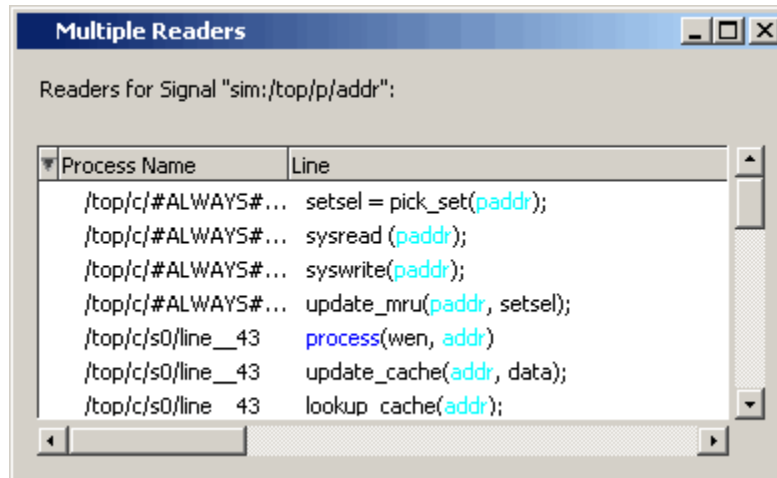


Select any driver to open the code for that driver.

- The **Goto Reader** selection causes the Source window to jump to the source code defining the reader of the selected signal. If the Reader is in a different Source file, that file will open in a new Source window tab and the reader code will be highlighted.

If there is more than one reader for the signal, a Multiple Readers dialog will open showing all readers (Figure 2-80).

Figure 2-80. Window Shows all Signal Readers



Select any reader to open the code for that reader.

Limitations

The Source window's textual dataflow functions only work for pure HDL. It will not work for SystemC or for complex data types like SystemVerilog classes.

Using Language Templates

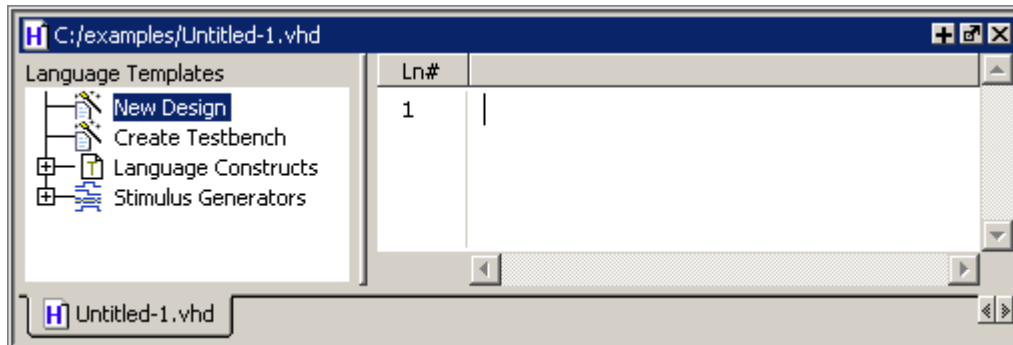
ModelSim language templates help you write code. They are a collection of wizards, menus, and dialogs that produce code for new designs, test benches, language constructs, logic blocks, and so forth.

Note



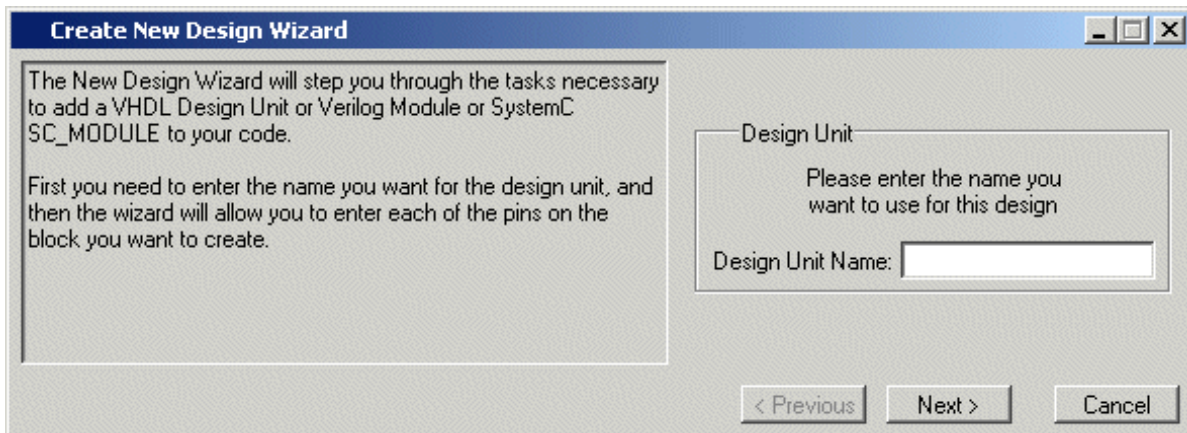
The language templates are not intended to replace thorough knowledge of coding. They are intended as an interactive reference for creating small sections of code. If you are unfamiliar with a particular language, you should attend a training class or consult one of the many available books.

To use the templates, either open an existing file, or select **File > New > Source** to create a new file. Once the file is open, select **Source > Show Language Templates** if the Source window is docked in the Main window; select **View > Show Language Templates** if the Source window is undocked. This displays a pane that shows the available templates.

Figure 2-81. Language Templates

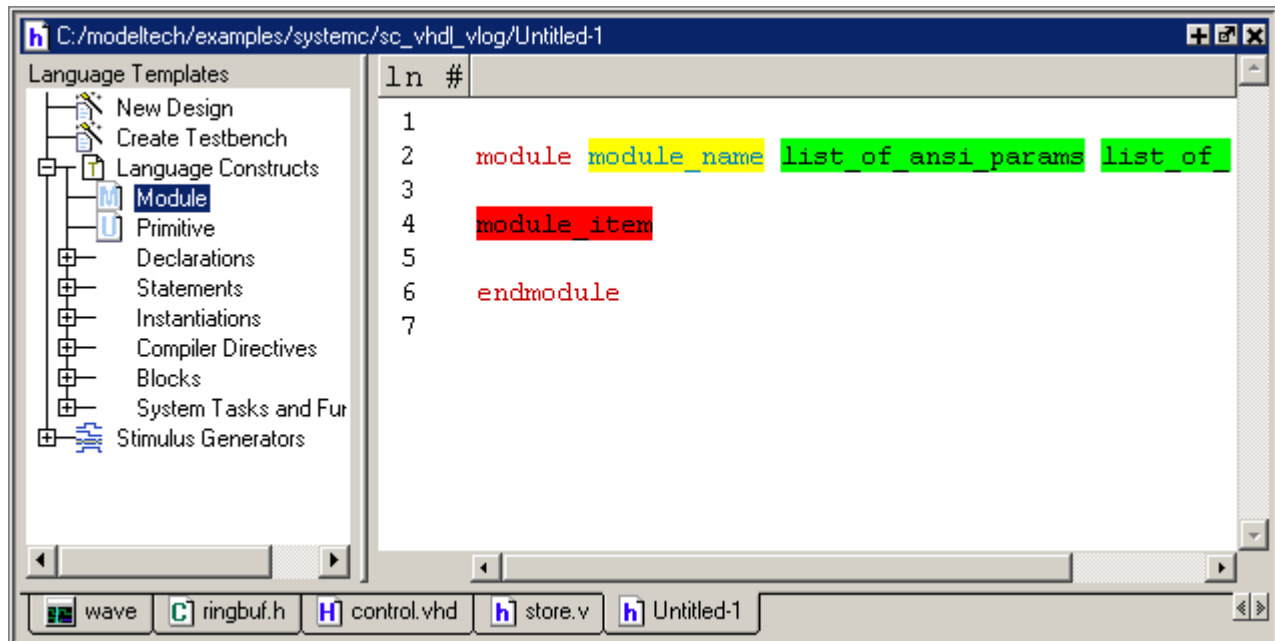
The templates that appear depend on the type of file you create. For example Module and Primitive templates are available for Verilog files, and Entity and Architecture templates are available for VHDL files.

Double-click an object in the list to open a wizard or to begin creating code. Some of the objects bring up wizards while others insert code into your source file. The dialog below is part of the wizard for creating a new design. Simply follow the directions in the wizards.

Figure 2-82. Create New Design Wizard

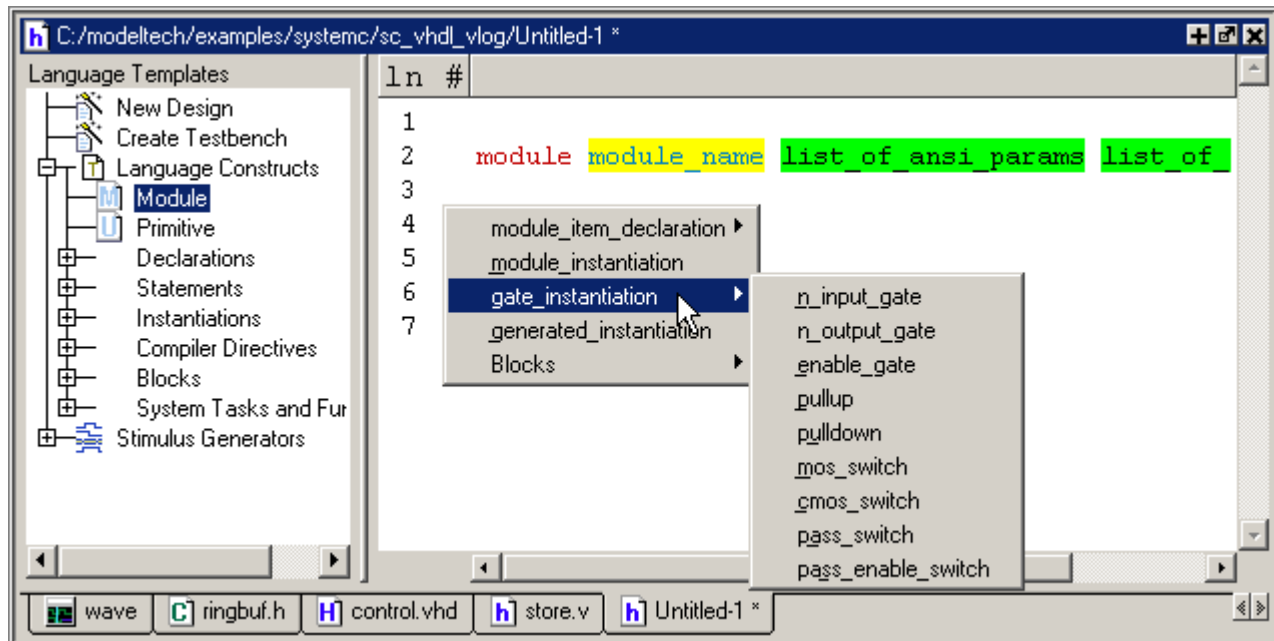
Code inserted into your source contains a variety of highlighted fields. The example below shows a module statement inserted from the Verilog template.

Figure 2-83. Inserting Module Statement from Verilog Language Template



Some of the fields, such as *module_name* in the example above, are to be replaced with names you type. Other fields can be expanded by double-clicking and still others offer a context menu of options when double-clicked. The example below shows the menu that appears when you double-click *module_item* then select *gate_instantiation*.

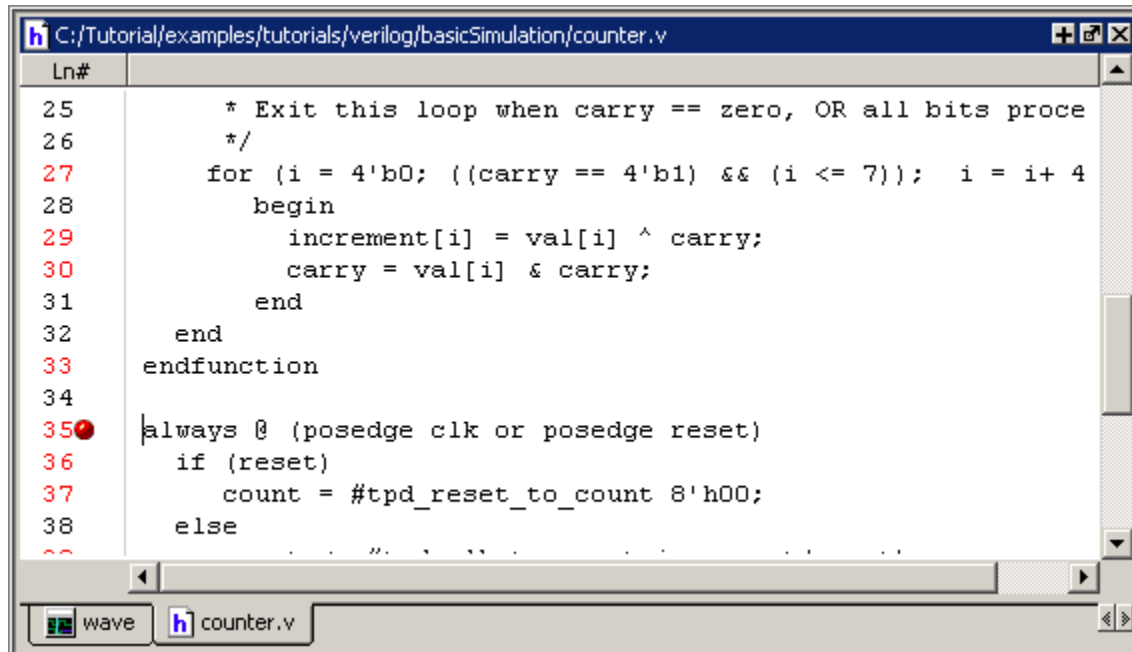
Figure 2-84. Language Template Context Menus



Setting File-Line Breakpoints with the GUI

You can easily set file-line breakpoints in your source code by clicking your mouse cursor in the line number column of a Source window. Click the left mouse button in the line number column next to a red line number and a red ball denoting a breakpoint will appear (Figure 2-85).

Figure 2-85. Breakpoint in the Source Window



The breakpoint markers are toggles. Click once to create the breakpoint; click again to disable or enable the breakpoint.

Note



When running in full optimization mode, breakpoints may not be set. Run the design in non-optimized mode (or set +acc arguments) to enable you to set breakpoints in the design. See [Preserving Object Visibility for Debugging Purposes](#) and [Design Object Visibility for Designs with PLI](#).

To delete the breakpoint completely, right click the red breakpoint marker, and select **Remove Breakpoint**. Other options on the context menu include:

- **Disable Breakpoint** — Deactivate the selected breakpoint.
- **Edit Breakpoint** — Open the File Breakpoint dialog to change breakpoint arguments.
- **Edit All Breakpoints** — Open the Modify Breakpoints dialog
- **Add/Remove Bookmark** — Add or remove a file-line bookmark.

Adding File-Line Breakpoints with the bp Command

Use the **bp** command to add a file-line breakpoint from the VSIM> prompt.

For example:

```
bp top.vhd 147
```

sets a breakpoint in the source file *top.vhd* at line 147.

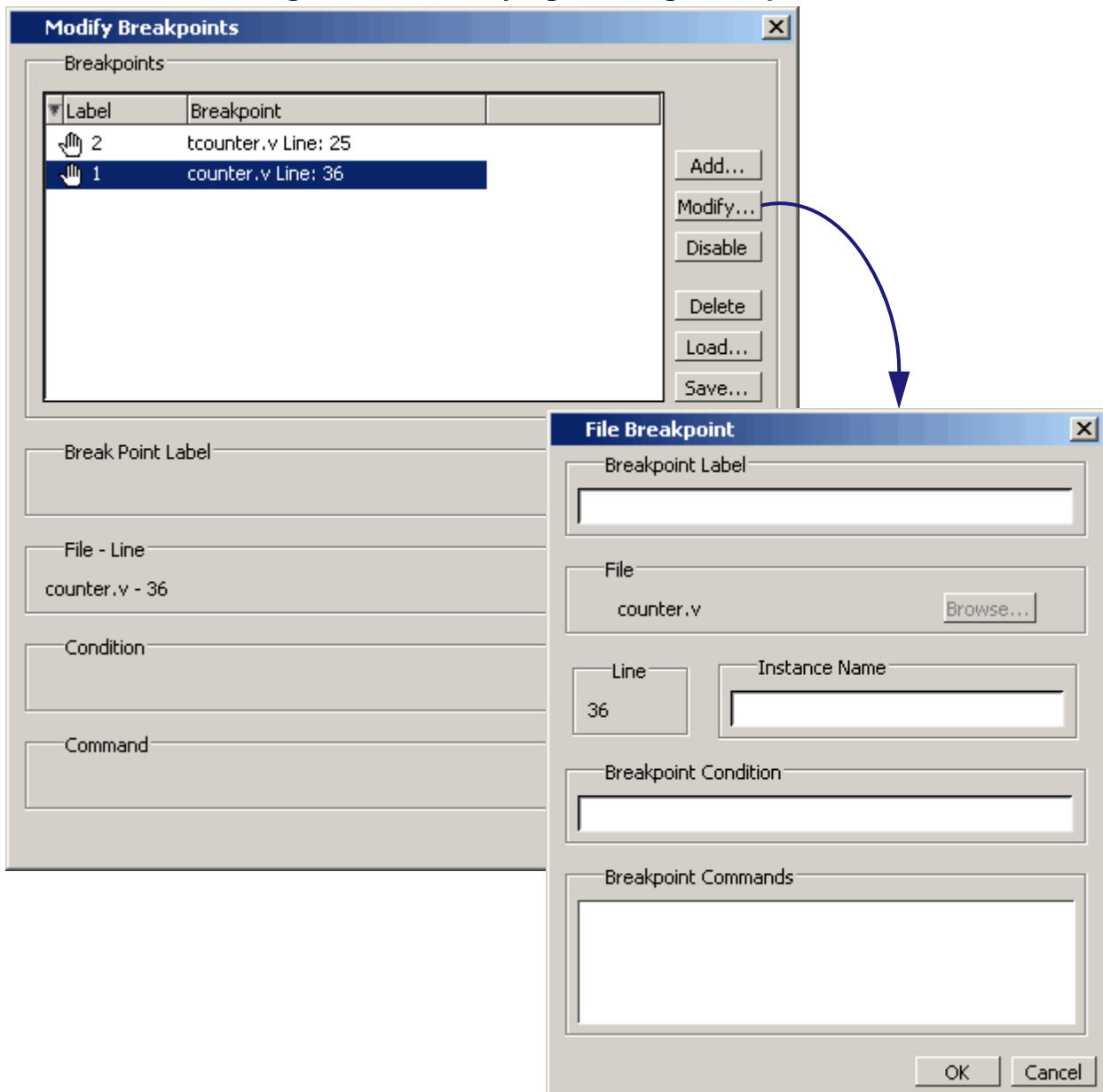
Modifying File-Line Breakpoints

To modify (or add) a breakpoint according to the line number in a source file, do any one of the following:

- Select **Tools > Breakpoints** from the Main menu.
- Right-click a breakpoint and select **Edit All Breakpoints** from the popup menu.
- Click the **Edit Breakpoints** toolbar button. See [Simulate Toolbar](#).

This displays the Modify Breakpoints dialog box shown in [Figure 2-86](#).

Figure 2-86. Modifying Existing Breakpoints



The Modify Breakpoints dialog box provides a list of all breakpoints in the design. To modify a breakpoint, do the following:

1. Select a file-line breakpoint from the list.
2. Click Modify, which opens the File Breakpoint dialog box shown in [Figure 2-86](#).
3. Fill out any of the following fields to modify the selected breakpoint:
 - Breakpoint Label — Designates a label for the breakpoint.

- **Instance Name** — The full pathname to an instance that sets a SystemC breakpoint so it applies only to that specified instance.
- **Breakpoint Condition** — One or more conditions that determine whether the breakpoint is observed. You must enclose the condition expression within quotation marks ("). If the condition is true, the simulation stops at the breakpoint. If false, the simulation bypasses the breakpoint. A condition cannot refer to a VHDL variable (only a signal).
- **Breakpoint Command** — A string, enclosed in braces ({}), that specifies one or more commands to be executed at the breakpoint. Use a semicolon (;) to separate multiple commands.



These fields in the File Breakpoint dialog box use the same syntax and format as the `-inst` switch, the `-cond` switch, and the command string of the `bp` command. For more information on these command options, refer to the `bp` command in the [Reference Manual](#).

4. Click OK to close the File Breakpoints dialog box.
5. Click OK to close the Modify Breakpoints dialog box.

Loading and Saving Breakpoints

The Modify Breakpoints dialog ([Figure 2-86](#)) includes Load and Save buttons that allow you to load or save breakpoints.

Checking Object Values and Descriptions

There are two quick methods to determine the value and description of an object displayed in the Source window:

- select an object, then right-click and select **Examine** or **Describe** from the context menu
- pause over an object with your mouse pointer to see an examine pop-up

Select **Tools > Options > Examine Now** or **Tools > Options > Examine Current Cursor** to choose at what simulation time the object is examined or described.

You can also invoke the `examine` and/or `describe` commands on the command line or in a macro.

Marking Lines with Bookmarks

Source window bookmarks are blue flags that mark lines in a source file. These graphical icons may ease navigation through a large source file by highlighting certain lines.

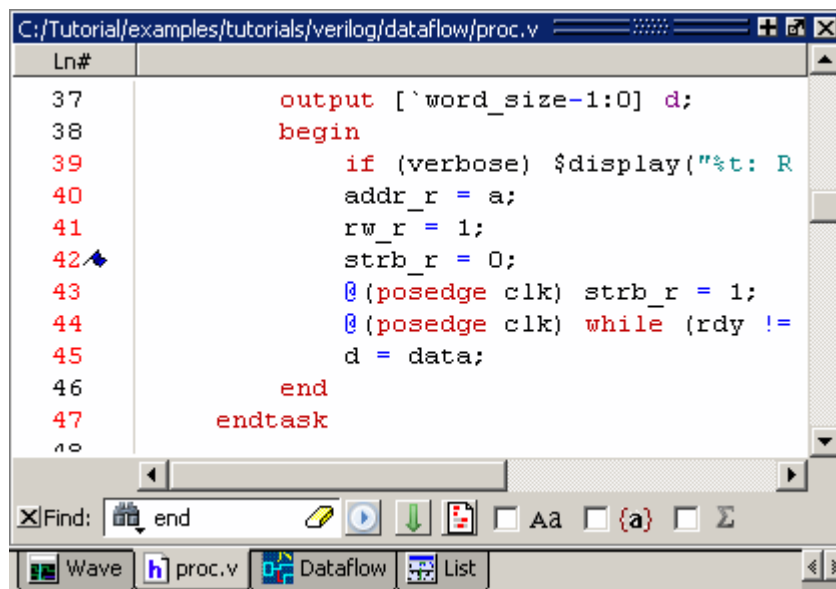
As noted above in the discussion about finding text in the Source window, you can insert bookmarks on any line containing the text for which you are searching. The other method for inserting bookmarks is to right-click a line number and select **Add/Remove Bookmark**. To remove a bookmark, right-click the line number and select Add/Remove Bookmark again.

Performing Incremental Search for Specific Code



The Source window includes an Find feature that allows you to do an incremental search for specific code. To activate the Find bar (Figure 2-87) in the Source window select **Edit > Find** from the Main menus or click the **Find** icon in the Main toolbar. For more information see [Using the Find and Filter Functions](#).

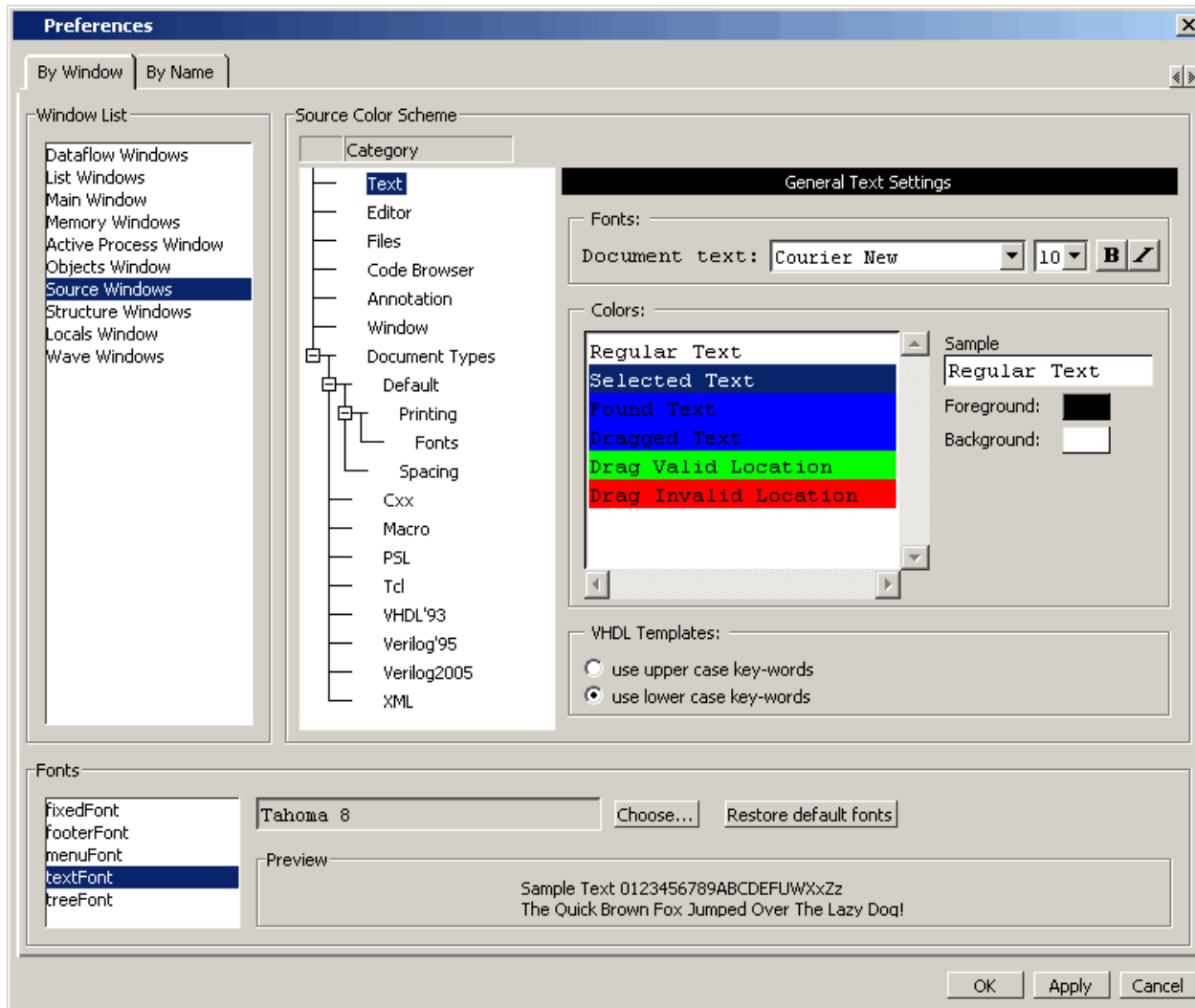
Figure 2-87. Source Window with Find Toolbar



Customizing the Source Window

You can customize a variety of settings for Source windows. For example, you can change fonts, spacing, colors, syntax highlighting, and so forth. To customize Source window settings, select **Tools > Edit Preferences**. This opens the Preferences dialog. Select **Source Windows** from the Window List.

Figure 2-88. Preferences Dialog for Customizing Source Window



Select an item from the Category list and then edit the available properties on the right. Click OK or Apply to accept the changes.

The changes will be active for the next Source window you open. The changes are saved automatically when you quit ModelSim. See [Setting Preference Variables from the GUI](#) for details.

Structure Window

The Structure window shows a hierarchical view of the active simulation. The name of the structure window, as shown in the title bar or in the tab if grouped with other windows, can vary:

- sim — This is the name shown for the Structure window for the active simulation.

- *dataset_name* — The Structure window takes the name of any dataset you load through the **File > Datasets** menu item or the dataset open command.

By default, the Structure window opens in a tab group with the Library and Files Window after starting a simulation.

The hierarchical view includes an entry for each object within the design. When you select an object in a Structure window, it becomes the current region.

By default, the coverage statistics displayed in the columns within the Structure window are valid for the local instance only, non-recursively. You can select to view coverage recursively by selecting **Code Coverage > Enable Recursive Coverage Sums**.

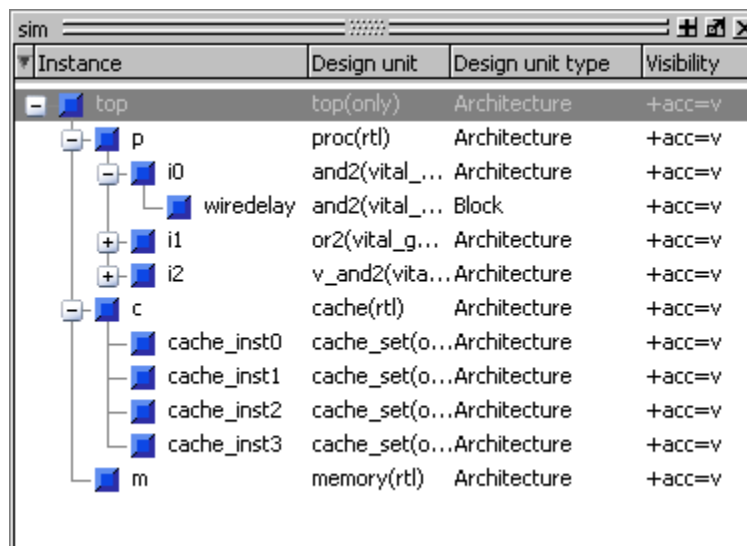
The contents of several windows automatically update based on which object you select, including the Source Window, Objects Window, Processes Window, and Locals Window.

Accessing

Access the window using either of the following:

- Menu item: **View > Structure**
- Command: view structure

Figure 2-89. Structure Window



Structure Window Tasks

Display Source Code of a Structure Window Object

You can highlight the line of code that declares a given object in the following ways:

1. Double-click on an object — Opens the file in a new Source window, or activates the file if it is already open.
2. Single-click on an object — Highlights the code if the file is already showing in an active Source window.

Add Structure Window Objects to Other Windows

You can add objects from the Structure window to the Dataflow Window, List Window, or Wave Window in the following ways:

- Mouse — Drag and drop
- Menu Selection — **Add > To *window***
- Command — add list, add wave, add dataflow

Filtering Structure Window Objects

1. View > Filter > object type

Processes — Implicit wire processes

Functions — Verilog and VHDL Functions

Packages — VHDL Packages

Tasks — Verilog Tasks

Statement — Verilog Statements

VIPackage — Verilog Packages

VITypedef — Verilog Type Definitions

Capacity —

GUI Elements of the Structure Window

This section describes GUI elements specific to this Window. For a complete list of all columns in the Structure window and a description of their contents, see [Table 2-40](#).

Column Descriptions

The table below summarizes the columns in the Structure window. For a complete list of all columns in the Structure window with a description of their contents, see [Table 2-40](#).

Table 2-40. Columns in the Structure Window

Column name	Description
Design Unit	The name of the design unit
Design Unit Type	The type of design unit
Visibility	The +acc settings used for compilation/optimization
Total Coverage	The weighted average of all the coverage types (functional coverage and code coverage) for local instance only. Use Code Coverage > Enable Recursive Coverage Sums to view recursive results.
Covergroup %	the number of hits from the total number of covergroups, as a percentage
Cover hits	the number of cover directives whose count values are greater than or equal to the at_least value.
Cover misses	the number of cover directives whose count values are less than the at_least value
Cover %	the number of hits from the total number of cover directives, as a percentage
Cover graph	a bar chart displaying the Cover directive %; if the percentage is below 90%, the bar is red; 90% or more, the bar is green; you can change this threshold percentage by editing the PrefCoverage(cutoff) preference variable
Assertion hits	Assertion hits shows different counts based on whether the -assertdebug is used: <ul style="list-style-type: none"> • with -assertdebug argument to vsim command: number of assertions whose pass count is greater than 0, and fail count is equal to 0. • without -assertdebug: number of assertions whose fail count is equal to 0.
Assertion misses	the number of assertions whose fail counts are greater than 0
Assertion %	the number of hits from the total number of assertions, as a percentage
Assertion graph	a bar chart displaying the Assertion %; if the percentage is below 90%, the bar is red; 90% or more, the bar is green; you can change this threshold percentage by editing the PrefCoverage(cutoff) preference variable
Stmt count	the number of executable statements in each level and all levels under that level
Stmts hit	the number of executable statements that were executed in each level and all levels under that level
Stmts missed	the number of executable statements that were not executed in each level and all levels under that level

Table 2-40. Columns in the Structure Window

Column name	Description
Stmt %	the current ratio of Stmt hits to Stmt count
Stmt graph	a bar chart displaying the Stmt %; if the percentage is below 90%, the bar is red; 90% or more, the bar is green; you can change this threshold percentage by editing the PrefCoverage(cutoff) preference variable
Branch count	Files window — the number of executable branches in each file Structure window — the number of executable branches in each level and all levels under that level
Branches hit	the number of executable branches that have been executed in the current simulation
Branches missed	the number of executable branches that were not executed in the current simulation
Branch %	the current ratio of Branch hits to Branch count
Branch graph	a bar chart displaying the Branch %; if the percentage is below 90%, the bar is red; 90% or more, the bar is green; you can change this threshold percentage by editing the PrefCoverage(cutoff) preference variable
Condition rows	Files window — the number of conditions in each file Structure window — the number of conditions in each level and all levels under that level
Conditions hit	Files window — the number of times the conditions in a file have been executed Structure window — the number of times the conditions in a level, and all levels under that level, have been executed
Conditions missed	Files window — the number of conditions in a file that were not executed Structure window — the number of conditions in a level, and all levels under that level, that were not executed
Condition %	the current ratio of Condition hits to Condition rows
Condition graph	a bar chart displaying the Condition %; if the percentage is below 90%, the bar is red; 90% or more, the bar is green; you can change this threshold percentage by editing the PrefCoverage(cutoff) preference variable
Expression rows	the number of executable expressions in each level and all levels subsumed under that level
Expressions hit	the number of times expressions in a level, and each level under that level, have been executed
Expressions missed	the number of executable expressions in a level, and all levels under that level, that were not executed
Expression %	the current ratio of Expression hits to Expression rows

Table 2-40. Columns in the Structure Window

Column name	Description
Expression graph	a bar chart displaying the Expression %; if the percentage is below 90%, the bar is red; 90% or more, the bar is green; you can change this threshold percentage by editing the PrefCoverage(cutoff) preference variable
Toggle nodes	the number of points in each instance where the logic will transition from one state to another
Toggles hit	the number of nodes in each instance that have transitioned at least once
Toggles missed	the number of nodes in each instance that have not transitioned at least once
Toggle %	the current ratio of Toggle hits to Toggle nodes
Toggle graph	a bar chart displaying the Toggle %; if the percentage is below 90%, the bar is red; 90% or more, the bar is green; you can change this threshold percentage by editing the PrefCoverage(cutoff) preference variable
States	Files window — the number of states encountered in each file Structure window — the number of states encountered in each level and all levels subsumed under that level
States hit	Files window — the number of times the states were hit Structure window — the number of times states in a level, and each level under that level, have been hit
States missed	Files window — the number of states in a file that were not hit Structure window — the number of states in a level, and all levels under that level, that were not hit
State %	the current ratio of State hits to State rows
State graph	a bar chart displaying the State %; if the percentage is below 90%, the bar is red; 90% or more, the bar is green; you can change this threshold percentage by editing the PrefCoverage(cutoff) preference variable
Transitions	Files window — the number of transitions encountered in each file Structure window — the number of states encountered in each level and all levels subsumed under that level
Transitions hit	Files window — the number of times the transitions were hit Structure window — the number of times transitions in a level, and each level under that level, have been hit
Transitions missed	Files window — the number of transitions in a file that were not hit Structure window — the number of transitions in a level, and all levels under that level, that were not hit
Transition %	the current ratio of Transition hits to Transition rows

Table 2-40. Columns in the Structure Window

Column name	Description
Transition graph	a bar chart displaying the State %; if the percentage is below 90%, the bar is red; 90% or more, the bar is green; you can change this threshold percentage by editing the PrefCoverage(cutoff) preference variable
FEC Condition rows	Files window — the number of FEC conditions in each file Structure window — the number of conditions in each level and all levels under that level
FEC Conditions hit	Files window — the number of times the FEC conditions in a file have been executed Structure window — the number of times the conditions in a level, and all levels under that level, have been executed
FEC Conditions missed	Files window — the number of FEC conditions in a file that were not executed Structure window — the number of conditions in a level, and all levels under that level, that were not executed
FEC Condition %	the current ratio of FEC Condition hits to FEC Condition rows
FEC Condition graph	a bar chart displaying the FEC Condition %; if the percentage is below 90%, the bar is red; 90% or more, the bar is green; you can change this threshold percentage by editing the PrefCoverage(cutoff) preference variable
FEC Expression rows	Files window — the number of executable expressions in each file Structure window — the number of executable expressions in each level and all levels subsumed under that level
FEC Expressions hit	Files window — the number of times expressions in a file have been executed Structure window — the number of times expressions in a level, and each level under that level, have been executed
FEC Expressions missed	Files window — the number of executable expressions in a file that were not executed Structure window — the number of executable expressions in a level, and all levels under that level, that were not executed
FEC Expression %	the current ratio of FEC Expression hits to FEC Expression rows
FEC Expression graph	a bar chart displaying the FEC Expression %; if the percentage is below 90%, the bar is red; 90% or more, the bar is green; you can change this threshold percentage by editing the PrefCoverage(cutoff) preference variable

Toolbars (undocked)

When this window is undocked, you have access to the following toolbars:

- Standard Toolbar

Code Coverage in Structure Window

The Structure window displays code coverage information in the Structure (sim) tab for any datasets being simulated. When coverage is invoked, several columns for displaying coverage data are added to these windows. You can toggle columns on/off by right-clicking on a column name and selecting from the context menu that appears. Figure 2-90 shows a portion of the Structure window with code coverage data displayed.

Figure 2-90. Code Coverage Data in the Structure Window

Stmt misses	Stmt %	Stmt graph	Branch count	Branch hits	Branch misses	Branch %	Branch gr
4	89.5%		34	30	4	88.2%	
1	83.3%		10	9	1	90%	

The screenshot also shows a toolbar at the bottom with icons for Library, sim, Files, and Memories.

You can sort code coverage information for any column by clicking the column heading. Clicking the column heading again will reverse the order.

Coverage information in the Structure window is dynamically linked to the Missed Coverage windows and the Current Exclusions window. Click the left mouse button on any file in the Files window to display that file's un-executed statements, branches, conditions, expressions, and toggles in the Missed Coverage windows. Lines from the selected file that are excluded from coverage statistics are displayed in the Current Exclusions window.

Verification Browser Window

The Verification Browser window displays summary information for original test results in UCDBs, ranking files, and merged test results in a UCDB. It has a feature for customizing and saving the organization of the tabs. It also supports features for re-running tests, generating HTML reports from test results, and executing merges and test ranking.

Accessing

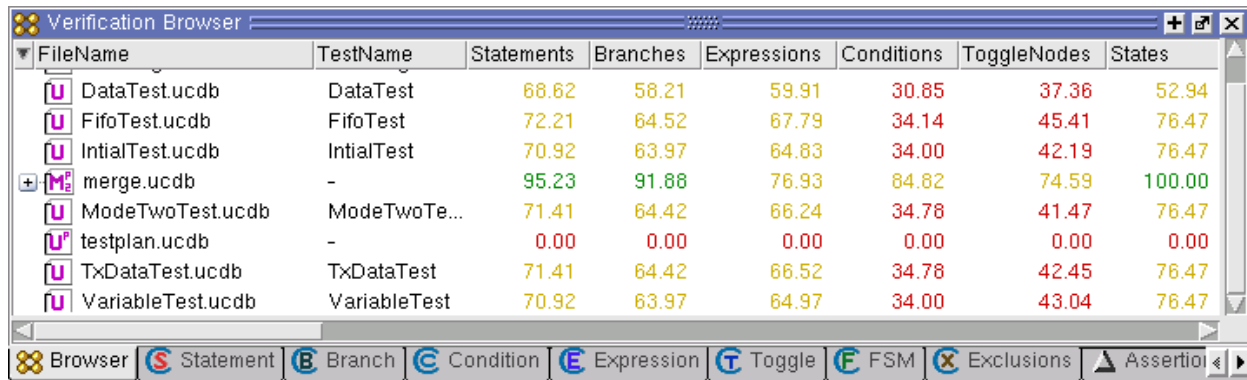
Access the window using either of the following:

- Select **View > Verification Management > Browser**
- Execute the view command, as shown:

view testbrowser

Figure 2-91 shows the Verification Browser window using the Code Coverage column view setting, refer to [Controlling the Verification Browser Columns](#) for more information.

Figure 2-91. Browser Tab



Verification Browser Icons

The Browser uses the following icons to identify the type of file loaded into the browser:

Table 2-41. Verification Browser Icons

Browser Icon	Description
	Indicates the file is an unmerged UCDB file. A “P” notation in the upper right hand corner of the icon indicates that a Verification Plan is included in UCDB.
	Indicates the file is a rank file.
	Indicates the file is a merged UCDB file. Notations on right hand side mean the following: <ul style="list-style-type: none"> • P - verification (test) plan is included in merged UCDB • 1 - Totals merge • 2 - Test-associated merge See “ Test-Associated Merge versus Totals Merge Algorithm ” for more information.

Controlling the Verification Browser Columns

You can customize the appearance of the Browser using either of the following methods:

- Use the “[Column Layout Toolbar](#)” to select from several pre-defined column arrangements.

- Right-click in the column headings to display a list of all column headings which allows you to toggle the columns on or off.

Saving Verification Browser Column and Filter Settings

Save your column layout and any filter settings to an external file (*browser_column_layout.do*) by selecting **File > Export > Column Layout** while the window is active. You can reload these settings with the do command. This export does not retain changes to column width.

GUI Elements of the Verification Browser Window

This section provides an overview of the GUI elements specific to this window.

Toolbar

The Browser allows access to the [Column Layout Toolbar](#) and the [Help Toolbar](#).

Menu Items

The following menu items are related to the Verification Browser window:

- **Add File** — adds UCDB (.ucdb) and ranking results (.rank) files to the browser. Refer to the section [Viewing Test Data in the GUI](#) for more information.
- **Remove File** — removes an entry from this window (**From Browser Only**), as well as from the file system (**Browser and File System**).
- **Remove Non-Contributing Test(s)** — operates on ranked (.rank) files; menu selection is grayed out unless a ranked file is selected. Removes any tests that do not contribute toward the coverage.
- **Merge** — displays the Merge Files Dialog Box, which allows you to merge any selected UCDB files. Refer to the section [Merging Coverage Test Data](#) for more information.
- **Rank** — displays the Rank Files Dialog Box, which allows you to create a ranking results file based on the selected UCDB files. Refer to the section [Ranking Coverage Test Data](#) for more information.
- **HTML Report** — displays the HTML Coverage Report Dialog Box, which allows you to view your coverage statistics in an HTML viewer.
- **Command Execution** — allows you to re-run simulations based on the resultant UCDB file based on the simulation settings to create the file. You can rerun any test whose test record appears in an individual .ucdb file, a merged .ucdb file, or ranking results (.rank) file. See [Test Attribute Records in UCDB](#) for more information on test records.
 - Setup — Displays the Command Setup Dialog box, which allows you to create and edit your own setups which can be used to control the execution of commands.

- “Restore All Defaults” removes any changes you make to the list of setups and the associated commands.
- Execute on all — Executes the specified command(s) on all *.ucdb* files in the browser, even those used in merged *.ucdb* files and *.rank* files.
 - Execute on selected — Executes the specified command(s) on the selected *.ucdb* file(s).
 - **Show Full Path** — toggles whether the FileName column shows only the filename or its full path.
 - **Set Precision** — allows you to control the decimal point precision of the data in the Verification Browser window.
 - **Configure Colorization** — opens the Colorization Threshold dialog box which allows you to off the colorization of coverage results displayed in the “Coverage” column, as well as set the low and high threshold coverage values for highlighting coverage values:
 - < low threshold — RED
 - > high threshold — GREEN
 - > low and < high — YELLOW
 - **Save Current Column Layout**— opens the Save Current Column Layout Dialog Box, which saves the current layout of the columns displayed in the browser to the pulldown list of layouts.
 - **Configure Column Layout** — opens the Create/Edit/Remove Column Layout Dialog Box, which allows you to edit, create, or save the current layout of the columns.
 - **Expand / Collapse Selected** — Expand or collapse selected UCDBs.
 - **Expand / Collapse All** — Expand or collapse all UCDBs.
 - **Save Format** — saves the current contents of the browser to a *.do* file.
 - **Load** — loads a *.do* file that contains a previously saved browser layout.
 - **Invoke CoverageView Mode** — opens the selected UCDB in viewcov mode, creating a new dataset. Refer to the section [Invoking Coverage View Mode](#) for more information.

Transcript Window

The Transcript window maintains a running history of commands that are invoked and messages that occur as you work with ModelSim. When a simulation is running, the Transcript displays a VSIM prompt, allowing you to enter command-line commands from within the graphic interface.

You can scroll backward and forward through the current work history by using the vertical scrollbar. You can also use arrow keys to recall previous commands, or copy and paste using the mouse within the window (see [Main and Source Window Mouse and Keyboard Shortcuts](#) for details).

Displaying the Transcript Window

The Transcript window is always open in the Main window and cannot be closed.

Viewing Data in the Transcript Window

The Transcript tab contains the command line interface, identified by the ModelSim prompt, and the simulation interface, identified by the VSIM prompt.

Transcript Window Tasks

This section introduces you to several tasks you can perform, related to the Transcript tab.

Saving the Transcript File

Variable settings determine the filename used for saving the transcript. If either **PrefMain(file)** in the *.modelsim* file or **TranscriptFile** in the *modelsim.ini* file is set, then the transcript output is logged to the specified file. By default the **TranscriptFile** variable in *modelsim.ini* is set to *transcript*. If either variable is set, the transcript contents are always saved and no explicit saving is necessary.

If you would like to save an additional copy of the transcript with a different filename, click in the Transcript window and then select **File > Save As**, or **File > Save**. The initial save must be made with the **Save As** selection, which stores the filename in the Tcl variable **PrefMain(saveFile)**. Subsequent saves can be made with the **Save** selection. Since no automatic saves are performed for this file, it is written only when you invoke a **Save** command. The file is written to the specified directory and records the contents of the transcript at the time of the save.

Using the Saved Transcript as a Macro (DO file)

Saved transcript files can be used as macros (DO files). Refer to the [do](#) command for more information.

Changing the Number of Lines Saved in the Transcript Window

By default, the Transcript window retains the last 5000 lines of output from the transcript. You can change this default by selecting **Transcript > Saved Lines**. Setting this variable to 0 instructs the tool to retain all lines of the transcript.

Disabling Creation of the Transcript File

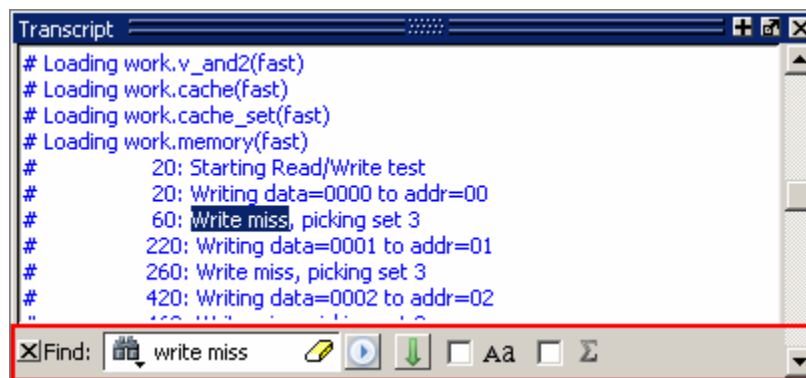
You can disable the creation of the transcript file by using the following ModelSim command immediately after ModelSim starts:

```
transcript file ""
```

Performing an Incremental Search

The Transcript tab includes an Find function (Figure 2-92) that allows you to do an incremental search for specific text. To activate the Find bar select **Edit > Find** from the menus or click the **Find** icon in the toolbar. For more information see [Using the Find and Filter Functions](#).

Figure 2-92. Transcript Window with Find Toolbar



GUI Elements of the Transcript Window

This section describes the GUI elements specific to the Transcript window.

Automatic Command Help

When you start typing a command at the prompt, a dropdown box appears which lists the available commands matching what has been typed so far. You may use the Up and Down arrow keys or the mouse to select the desired command. When a unique command has been entered, the command usage is presented in the drop down box.

You can toggle this feature on and off by selecting **Help > Command Completion**.

Transcript Menu Items

- **Adjust Font Scaling** — Displays the Adjust Scaling dialog box, which allows you to adjust how fonts appear for your display environment. Directions are available in the dialog box.
- **Transcript File** — Allows you to change the default name used when saving the transcript file. The saved transcript file will contain all the text in the current transcript file.

- **Command History** — Allows you to change the default name used when saving command history information. This file is saved at the same time as the transcript file.
- **Save File** — Allows you to change the default name used when selecting File > Save As.
- **Saved Lines** — Allows you to change how many lines of text are saved in the transcript window. Setting this value to zero (0) saves all lines.
- **Line Prefix** — Allows you to change the character(s) that precedes the lines in the transcript.
- **Update Rate** — Allows you to change the length of time (in ms) between transcript refreshes.
- **ModelSim Prompt** — Allows you to change the string used for the command line prompt.
- **VSIM Prompt** — Allows you to change the string used for the simulation prompt.
- **Paused Prompt** — Allows you to change the string used for when the simulation is paused.

Transcript Toolbar Items

When undocked, the Transcript window allows access to the following toolbars:

- [Standard Toolbar](#)
- [Help Toolbar](#)
- [Help Toolbar](#)

Message Viewer Window

The Message Viewer window allows you to easily access, organize, and analyze any Note, Warning, Error or other elaboration and runtime messages written to the transcript during the simulation run.

Displaying the Message Viewer Window

- Select **View > Message Viewer**
- Use the command:
view msgviewer
- Open a dataset:
dataset open <WLF_file>

Viewing Data in the Message Viewer Window

By default, the tool writes transcribed messages during elaboration and runtime to both the transcript and the WLF file. By writing messages to the WLF file, the Message Viewer window is able to organize the messages for your analysis during the current simulation as well as during post simulation.

You can control what messages are available in the transcript, WLF file, or both with the following switches:

- `displaymsgmode` messages — User generated messages resulting from calls to Verilog Display System Tasks and PLI/FLI print function calls. By default, these messages are written only to the transcript, which means you cannot access them through the Message Viewer window. In many cases, these user generated messages are intended to be output as a group of transcribed messages, thus the default of transcript only. The Message Viewer treats each message individually, therefore you could lose the context of these grouped messages by modifying the view or sort order of the Message Viewer.

To change this default behavior you can use the `-displaymsgmode` argument to [vsim](#). The syntax is:

```
vsim -displaymsgmode {both | tran | wlf}
```

You can also use the [displaymsgmode](#) variable in the `modelsim.ini` file.

The message transcribing methods that are controlled by `-displaymsgmode` include:

- Verilog Display System Tasks — `$write`, `$display`, `$monitor`, and `$strobe`. The following also apply if they are sent to `STDOUT`: `$fwrite`, `$fdisplay`, `$fmonitor`, and `$fstrobe`.
- FLI Print Function Calls — `mti_PrintFormatted` and `mti_PrintMessage`.
- PLI Print Function Calls — `io_printf` and `vpi_printf`.
- `msgmode` messages — All elaboration and runtime messages not part of the `displaymsgmode` messages. By default, these messages are written to the transcript and the WLF file, which provides access to the messages through the Message Viewer window. To change this default behavior you can use the `-msgmode` argument to [vsim](#). The syntax is:

```
vsim -msgmode {both | tran | wlf}
```

You can also use the [msgmode](#) variable in the `modelsim.ini` file.

Message Viewer Window Tasks

[Figure 2-93](#) and [Table 2-42](#) provide an overview of the Message Viewer and several tasks you can perform.

Figure 2-93. Message Viewer Window

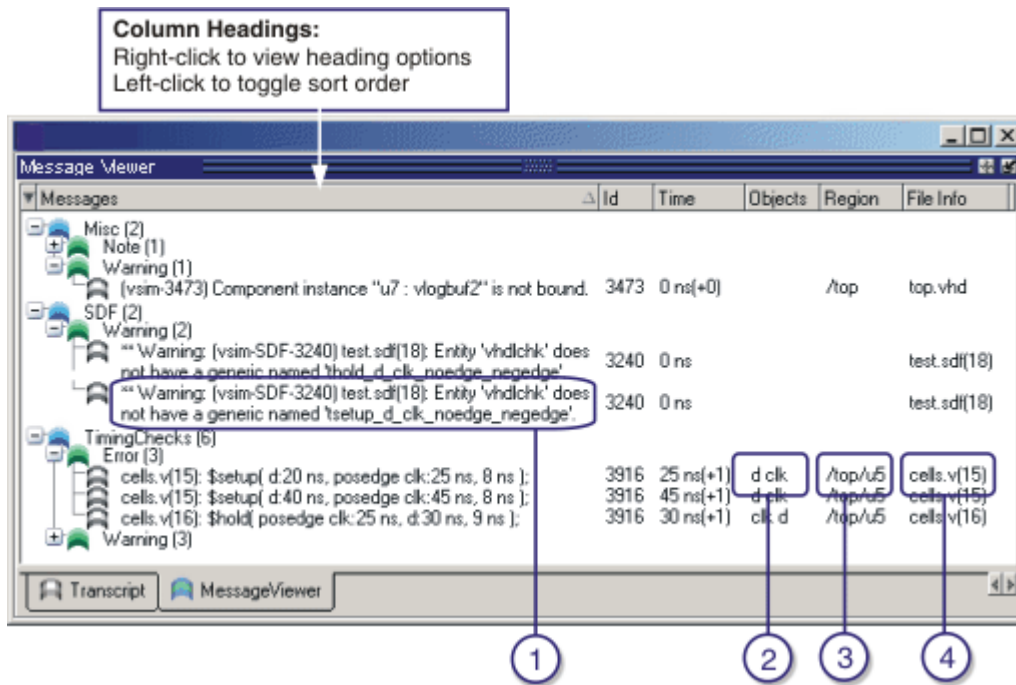


Table 2-42. Message Viewer Tasks

Icon	Task	Action
1	Display a detailed description of the message.	right click the message text then select View Verbose Message .
2	Open the source file and add a bookmark to the location of the object(s).	double click the object name(s).
3	Change the focus of the Structure and Objects windows.	double click the hierarchical reference.
4	Open the source file and set a marker at the line number.	double click the file name.

GUI Elements of the Message Viewer Window

This section describes the GUI elements specific to this window.

Column Descriptions

- Messages — contains the organized tree-structure of the sorted messages, as well as, when expanded, the text of the messages.
- Time — displays the time of simulation when the message was issued.
- Objects — displays the object(s) related to the message, if any.

- Region — displays the hierarchical region related to the message, if any.
- File Info — displays the filename related to the cause of the message, and in some cases the line number in parentheses.
- Category — displays a keyword for the various categories of messages:

DISPLAY	Related to Verilog display system tasks
FLI	
PA	Related to Power Aware designs
PLI	
SDF	
TCHK	Related to timing checks
VCD	
VITAL	
WLF	
MISC	
<user-defined>	Related to \$messagelog system tasks used in your design code.

- Severity — displays the message severity, such as Warning, Note or Error.
- Timing Check Kind — displays additional information about timing checks
- Assertion Start Time
- Assertion Name
- Verbosity — displays verbosity information from [\\$messagelog](#) system tasks.
- Id — displays the message number

Message Viewer Menu Items

Right-click anywhere in the Message Viewer to open a popup menu that contains the following selections:

- **Source** — opens the Source window for the file, and in some cases takes you to the associated line number.
- **Verbose Message** — displays the Verbose Message dialog box containing further details about the selected message.
- **Object Declaration** — opens and highlights the object declaration related to the selected message.

- **Filter** — displays the [Message Viewer Filter Dialog Box](#), which allows you to create specialized rules for filtering the Message Viewer.
- **Clear Filter** — restores the Message Viewer to an unfiltered view by issuing the `messages clearfilter` command.
- **Display Reset** — resets the display of the window.
- **Display Options** — displays the Message Viewer Display Options dialog box, which allows you to further control which messages appear in the window.

Related GUI Features

- The [Messages Bar](#) in the Wave window provides indicators as to when a message occurred.

Message Viewer Display Options Dialog Box

This dialog box allows you to control display options for the message viewer tab of the transcript window.

- **Hierarchy Selection** — This field allows you to control the appearance of message hierarchy, if any.
 - **Display with Hierarchy** — enables or disables a hierarchical view of messages.
 - **First by, Then by** — specifies the organization order of the hierarchy, if enabled.
- **Time Range** — Allows you to filter which messages appear according to simulation time. The default is to display messages for the complete simulation time.
- **Displayed Objects** — Allows you to filter which messages appear according to the values in the Objects column. The default is to display all messages, regardless of the values in the Objects column. The Objects in the list text entry box allows you to specify filter strings, where each string must be on a new line.

Message Viewer Filter Dialog Box

This dialog box allows you to create filter rules that specify which messages should be shown in the message viewer. It contains a series of dropdown and text entry boxes for creating the filter rules and supports the addition of additional rule (rows) to create logical groupings .

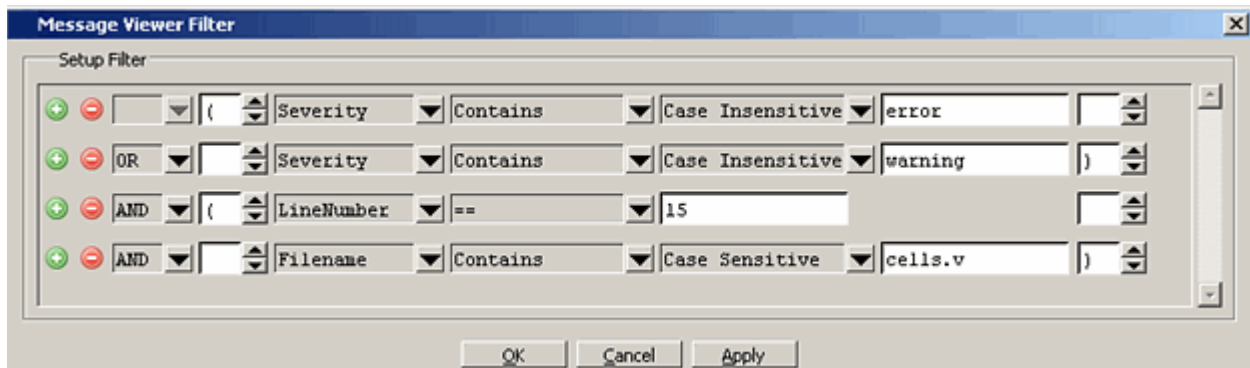
From left to right, each filter rule is made up of the following:

- **Add and Remove buttons** — either add a rule filter row below the current row or remove that rule filter row.
- **Logic field** — specifies a logical argument for combining adjacent rules. Your choices are: AND, OR, NAND, and NOR. This field is greyed out for the first rule filter row.

- Open Parenthesis field — controls rule groupings by specifying, if necessary, any open parentheses. The up and down arrows increase or decrease the number of parentheses in the field.
- Column field — specifies that your filter value applies to a specific column of the Message Viewer.
- Inclusion field — specifies whether the Column field should or should not contain a given value.
 - For text-based filter values your choices are: Contains, Doesn't Contain, or Exact.
 - For numeric- and time-based filter values your choices are: ==, !=, <, <=, >, and >=.
- Case Sensitivity field — specifies whether your filter rule should treat your filter value as Case Sensitive or Case Insensitive. This field only applies to text-based filter values.
- Filter Value field — specifies the filter value associated with your filter rule.
- Time Unit field — specifies the time unit. Your choices are: fs, ps, ns, us, ms. This field only applies to the Time selection from the Column field.
- Closed Parenthesis field — controls rule groupings by specifying, if necessary, any closed parentheses. The up and down arrows increase or decrease the number of parentheses in the field.

Figure 2-94 shows an example where you want to show all messages, either errors or warnings, that reference the 15th line of the file *cells.v*.

Figure 2-94. Message Viewer Filter Dialog Box



When you select OK or Apply, the Message Viewer is updated to contain only those messages that meet the criteria defined in the Message Viewer Filter dialog box.

Also, when selecting OK or Apply, the Transcript window will contain an echo of the messages setfilter command, where the argument is a Tcl definition of the filter. You can then cut/paste this command for reuse at another time.

Watch Window

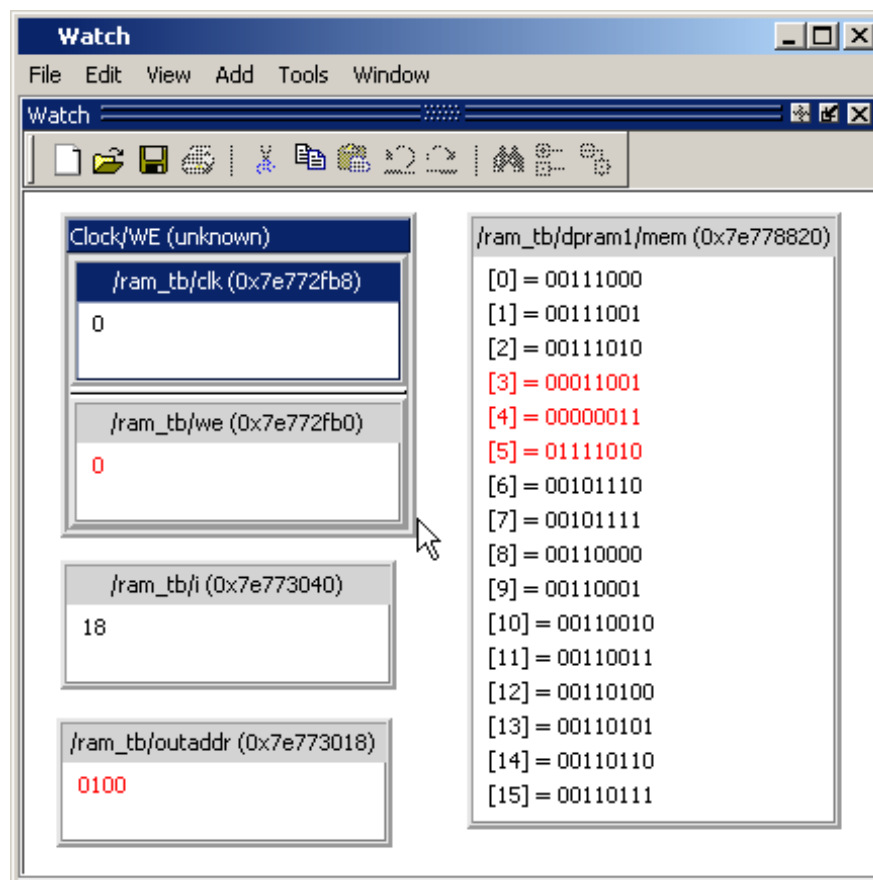
The Watch window shows values for signals and variables at the current simulation time, allows you to explore the hierarchy of object oriented designs. Unlike the Objects or Locals windows, the Watch window allows you to view any signal or variable in the design regardless of the current context. You can view the following objects:

- VHDL objects — signals, aliases, generics, constants, and variables
- Verilog objects — nets, registers, variables, named events, and module parameters
- SystemC objects — primitive channels and ports
- Virtual objects — virtual signals and virtual functions

The address of an object, if one can be obtained, is displayed in the title in parentheses as shown in [Figure 2-95](#).

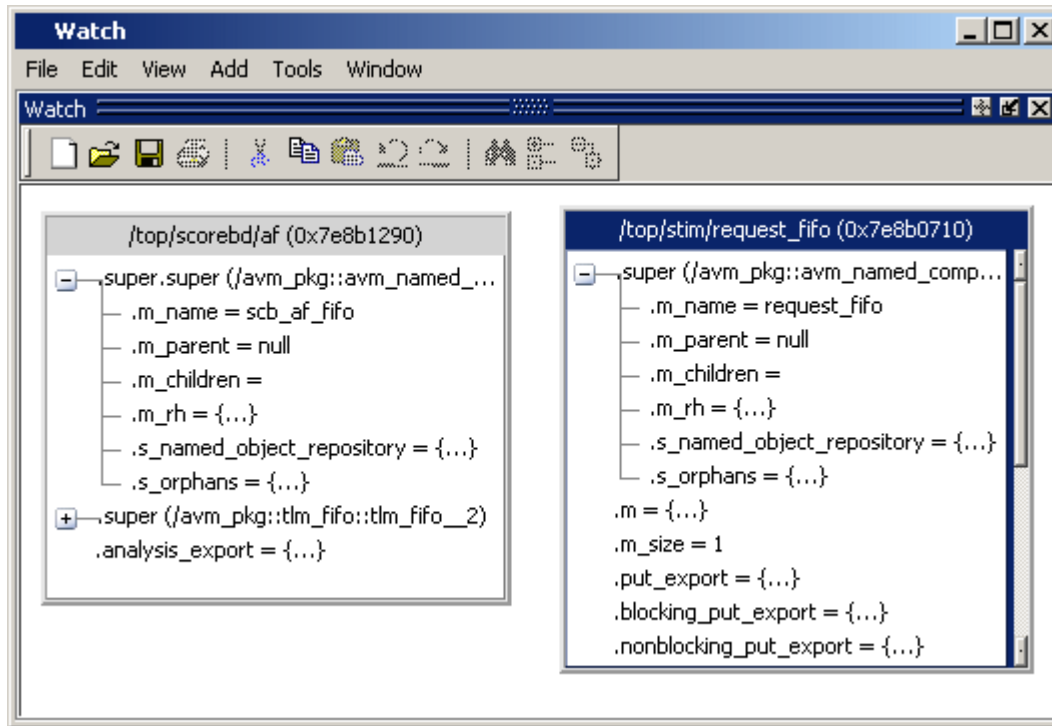
Items displayed in red are values that have changed during the previous Run command. You can change the radix of displayed values by selecting an item, right-clicking to open a popup context menu, then selecting **Properties**.

Figure 2-95. Watch Window



Items are displayed in a scrollable, hierarchical list, such as in [Figure 2-96](#) where extended SystemVerilog classes hierarchically display their super members.

Figure 2-96. Scrollable Hierarchical Display



Two Ref handles that refer to the same object will point to the same Watch window box, even if the name used to reach the object is different. This means circular references will be drawn as circular.

Selecting a line item in the window adds the item's full name to the global selection. This allows you to paste the full name in the Transcript (by simply clicking the middle mouse button) or other external application that accepts text from the global selection.

Adding Objects to the Watch Window

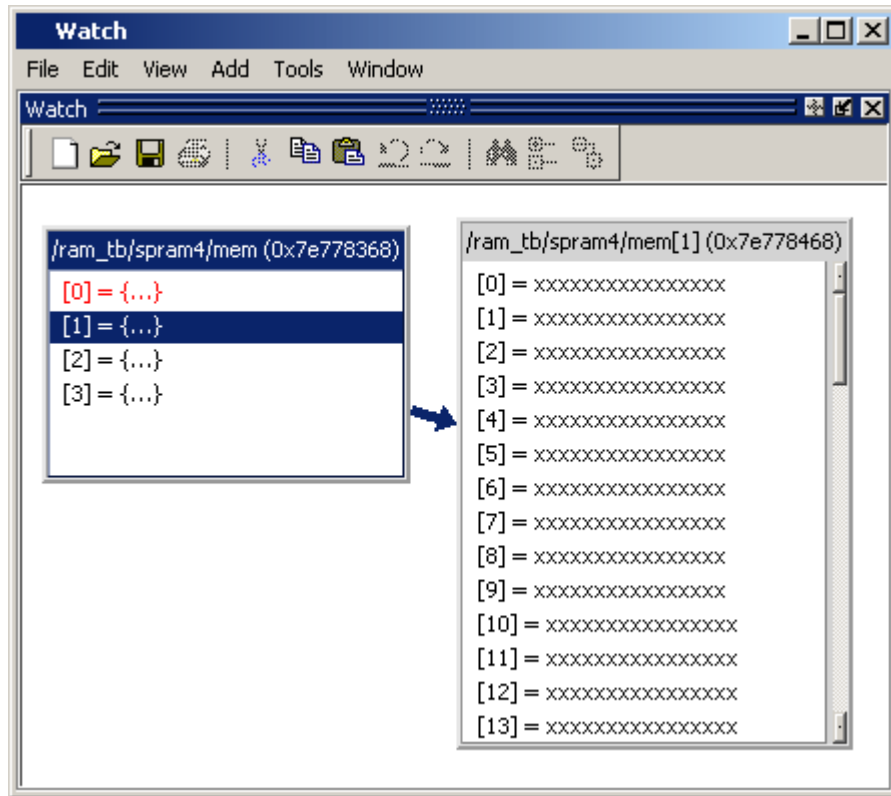
To add objects to the Watch window, drag-and-drop objects from the Structure window or from any of the following windows: List, Locals, Objects, Source, and Wave.

Alternatively, you can use the [add watch](#) command.

Expanding Objects to Show Individual Bits

If you add an array or record to the window, you can view individual bit values by double-clicking the array or record. As shown in [Figure 2-97](#), `/ram_tb/spram4/mem` has been expanded to show all the individual bit values. Notice the arrow that "ties" the array to the individual bit display.

Figure 2-97. Expanded Array

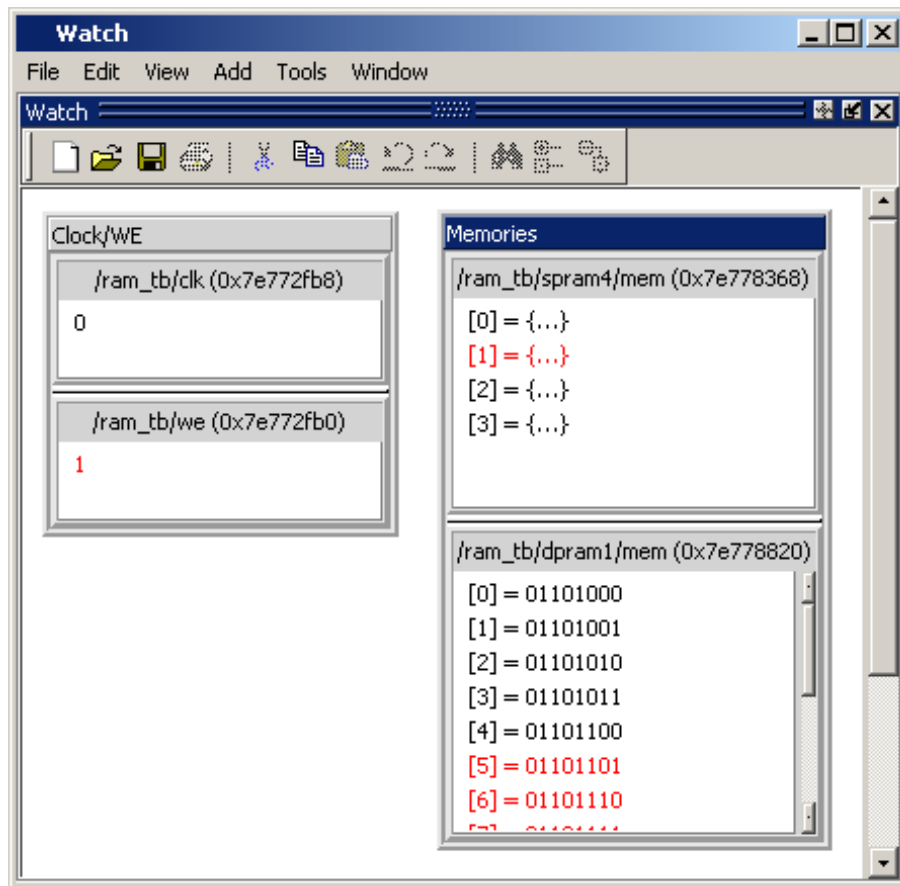


Grouping and Ungrouping Objects

You can group objects in the window so they display and move together. Select the objects, then right click one of the objects and choose **Group**.

In [Figure 2-98](#), two different sets of objects have been grouped together.

Figure 2-98. Grouping Objects in the Watch Window



To ungroup them, right-click the group and select **Ungroup**.

Saving and Reloading Format Files

You can save a format file (a DO file, actually) that will redraw the contents of the window. Right-click anywhere in the window and select **Save Format**. The default name of the format file is *watch.do*.

Once you have saved the file, you can reload it by right-clicking and selecting **Load Format**.

Wave Window

The Wave window, like the List window, allows you to view the results of your simulation. In the Wave window, however, you can see the results as waveforms and their values.

Wave Window Panes

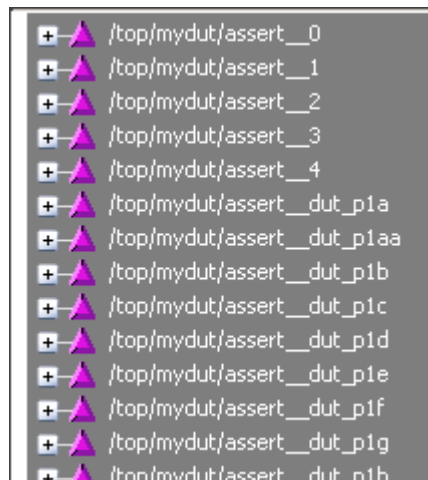
The Wave window is divided into a number of window panes. All window panes in the Wave window can be resized by clicking and dragging the bar between any two panes.

Pathname Pane

The pathname pane displays signal pathnames. Signals can be displayed with full pathnames, as shown here, or with only the leaf element displayed. You can increase the size of the pane by clicking and dragging on the right border. The selected signal is highlighted.

The white bar along the left margin indicates the selected dataset (see [Splitting Wave Window Panes](#)).

Figure 2-99. Pathnames Pane



Values Pane

The values pane displays the values of the displayed signals.

The radix for each signal can be symbolic, binary, octal, decimal, unsigned, hexadecimal, ASCII, or default. The default radix can be set by selecting **Simulate > Runtime Options**.

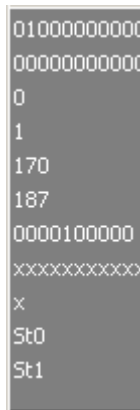
Note



When the symbolic radix is chosen for SystemVerilog reg and integer types, the values are treated as binary. When the symbolic radix is chosen for SystemVerilog bit and int types, the values are considered to be decimal.

The data in this pane is similar to that shown in the [Objects Window](#), except that the values change dynamically whenever a cursor in the waveform pane is moved.

Figure 2-100. Values Pane



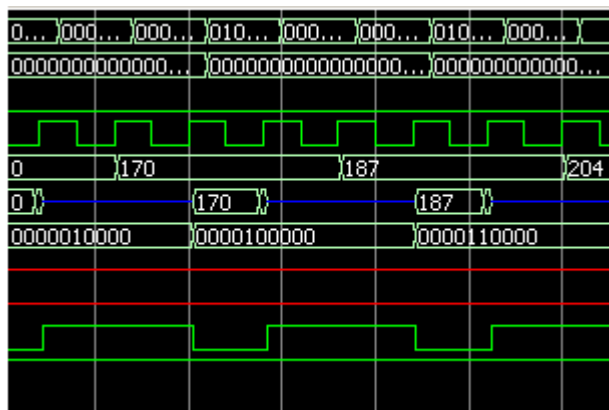
Waveform Pane

Figure 2-101 shows waveform pane, which displays waveforms that correspond to the displayed signal pathnames. It can also display as many as 20 user-defined cursors. Signal values can be displayed in analog step, analog interpolated, analog backstep, literal, logic, and event formats. You can set the radix of each signal individually by right-clicking the signal and choosing Radix > *format* (the default radix is Logic).

If you place your mouse pointer on a signal in the waveform pane, a popup menu displays with information about the signal. You can toggle this popup on and off in the **Wave Window Properties** dialog box.

Dashed signal lines in the waveform pane indicate weak or ambiguous strengths of Verilog states. See [Verilog States](#) in the [Mixed-Language Simulation](#) chapter.

Figure 2-101. Waveform Pane



Analog Sidebar Toolbox






When the waveform pane contains an analog waveform, you can hover your mouse pointer over the left edge of the waveform to display the Analog Sidebar toolbox (see [Figure 2-102](#)). This

toolbox shows a group of icons that gives you quick access to actions you can perform on the waveform display, as described in [Table 2-43](#).

Figure 2-102. Analog Sidebar Toolbox



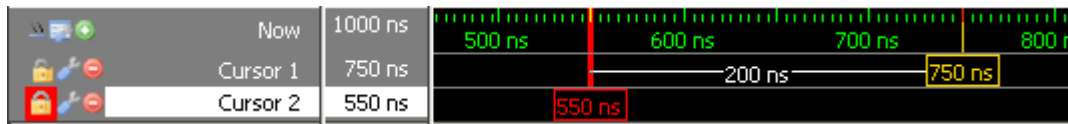
Table 2-43. Analog Sidebar Icons

Icon	Action	Description
	Open Wave Properties	Opens the Format tab of the Wave Properties dialog box, with the Analog format already selected. This dialog box duplicates the Wave Analog dialog box displayed by choosing Format > Format... > Analog (custom) from the main menu.
	Toggle Row Height	Changes the height of the row that contains the analog waveform. Toggles the height between the Min and Max values (in pixels) you specified in the Open Wave Properties dialog box under Analog Display.
	Rescale to fit Y data	Changes the waveform height so that it fits top-to-bottom within the current height of the row.
	Show menu of other actions	Displays <ul style="list-style-type: none"> • View Min Y • View Max Y • Overlay Above • Overlay Below • Colorize All • Colorize Selected
	Drag to resize waveform height	Creates an up/down dragging arrow that you can use to temporarily change the height of the row containing the analog waveform.

Cursor Pane

Figure 2-103 shows the Cursor Pane, which displays cursor names, cursor values and the cursor locations on the timeline. You can link cursors so that they move across the timeline together. See [Linking Cursors](#) in the [Waveform Analysis](#) chapter.

Figure 2-103. Cursor Pane

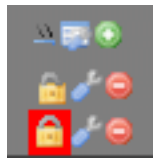


On the left side of this pane is a group of icons called the Cursor and Timeline Toolbox (see [Figure 2-104](#)). This toolbox gives you quick access to cursor and timeline features and configurations. See [Measuring Time with Cursors in the Wave Window](#) for more information.

Cursors and Timeline Toolbox

The Cursor and Timeline Toolbox displays several icons that give you quick access to cursor and timeline features.

Figure 2-104. Toolbox for Cursors and Timeline



The action for each toolbox icon is shown in [Table 2-44](#).

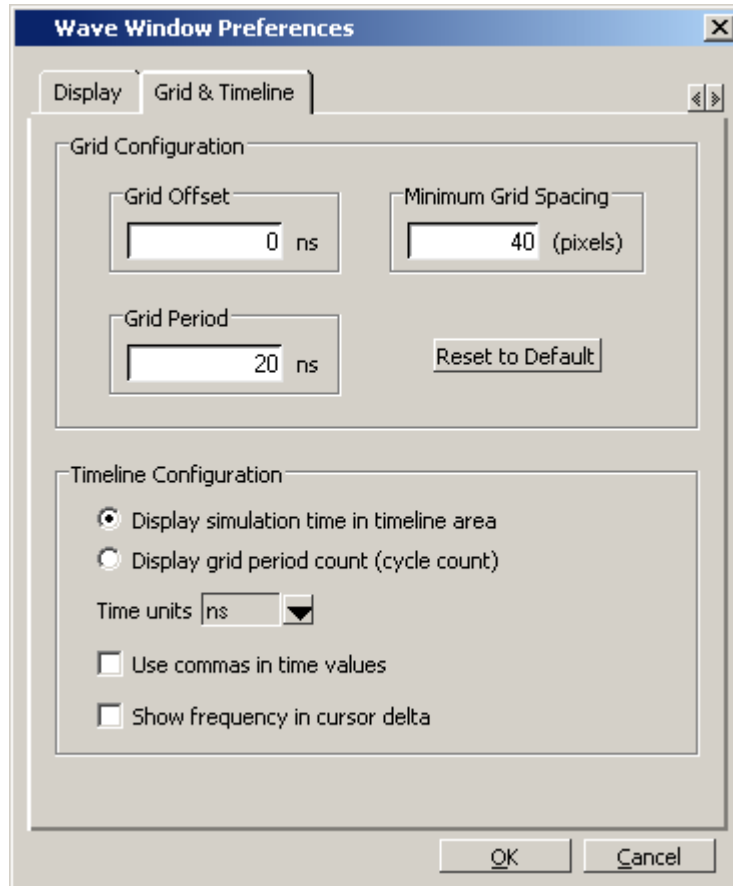
Table 2-44. Icons and Actions

Icon	Action
	Toggle short names <-> full names
	Edit grid and timeline properties
	Insert cursor
	Toggle lock on cursor to prevent it from moving
	Edit this cursor
	Remove this cursor

The **Toggle short names <-> full names** icon allows you to switch from displaying full pathnames (the default) in the Pathnames Pane to displaying short pathnames.

The **Edit grid and timeline properties** icon opens the Wave Window Properties dialog to the Grid & Timeline tab (Figure 2-105).

Figure 2-105. Editing Grid and Timeline Properties



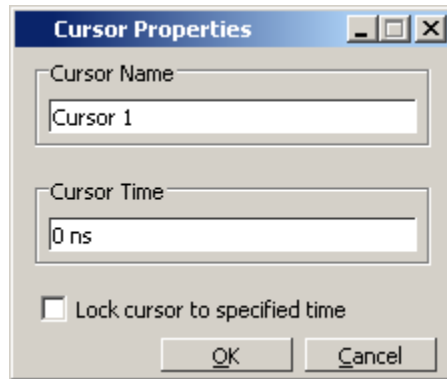
The Grid Configuration selections allow you to set grid offset, minimum grid spacing, and grid period; or you can reset the grid configuration to default values.

The Timeline Configuration selections give you a user-definable time scale. You can display simulation time on the timeline or a clock cycle count. The time value is scaled appropriately for the selected unit.

By default, the timeline will display time delta between any two adjacent cursors. By clicking the **Show frequency in cursor delta** box, you can display the cursor delta as a frequency instead.

You can add cursors when the Wave window is active by clicking the Insert Cursor icon, or by choosing **Add > Wave > Cursor** from the menu bar. Each added cursor is given a default cursor name (Cursor 2, Cursor 3, and so forth.) which you can be change by right-clicking the cursor name, then typing in a new name, or by clicking the **Edit this cursor** icon. The Edit this cursor icon opens the Cursor Properties dialog box (Figure 2-106), where you assign a cursor name and time. You can also lock the cursor to the specified time.

Figure 2-106. Cursor Properties Dialog



Messages Bar

The messages bar, located at the top of the Wave window, contains indicators pointing to the times at which a message was output from the simulator.

Figure 2-107. Wave Window - Message Bar



The message indicators (the down-pointing arrows) are color-coded as follows:

- Red — indicates an error or an assertion failure
- Yellow — indicates a warning
- Green — indicates a note
- Grey — indicates any other type of message

You can use the Message bar in the following ways.

- Move the cursor to the next message — You can do this in two ways:
 - Click on the word “Messages” in the message bar to cycle the cursor to the next message after the current cursor location.
 - Click anywhere in the message bar, then use Tab or Shift+Tab to cycle the cursor between error messages either forward or backward, respectively.
- Display the [Message Viewer Window](#) — Double-click anywhere amongst the message indicators.
- Display, in the Message Viewer window, the message entry related to a specific indicator — Double-click on any message indicator.

This function only works if you are using the Message Viewer in flat mode. To display your messages in flat mode:

- a. Right-click in the Message Viewer and select Display Options
- b. In the Message Viewer Display Options dialog box, deselect Display with Hierarchy.

Objects You Can View in the Wave Window

The following types of objects can be viewed in the Wave window

- VHDL objects (indicated by a dark blue diamond) — signals, aliases, process variables, and shared variables
- Verilog objects (indicated by a light blue diamond) — nets, registers, variables, and named events

The GUI displays inout variables of a clocking block separately, where the output of the inout variable is appended with “__o”, for example you would see following two objects:

```
clock1.cl           /input portion of the inout cl
clock1.cl__o       /output portion of the inout cl
```

This display technique also applies to the Objects window

- Verilog and SystemVerilog transactions (indicated by a blue four point star)
- SystemC objects
(indicated by a green diamond) — primitive channels and ports
(indicated by a green four point star) — transaction streams and their element
- Virtual objects (indicated by an orange diamond) — virtual signals, buses, and functions, see; [Virtual Objects](#) for more information
- Comparison objects (indicated by a yellow triangle) — comparison region and comparison signals; see [Waveform Compare](#) for more information
- Created waveforms (indicated by a red dot on a diamond) — see [Generating Stimulus with Waveform Editor](#)

The data in the object values pane is very similar to the Objects window, except that the values change dynamically whenever a cursor in the waveform pane is moved.

At the bottom of the waveform pane you can see a time line, tick marks, and the time value of each cursor's position. As you click and drag to move a cursor, the time value at the cursor location is updated at the bottom of the cursor.

You can resize the window panes by clicking on the bar between them and dragging the bar to a new location.

Waveform and signal-name formatting are easily changed via the Format menu. You can reuse any formatting changes you make by saving a Wave window format file (see [Saving the Window Format](#)).

Wave Window Toolbar

The Wave window (in the undocked Wave window) gives you quick access to the following toolbars:

- [Standard Toolbar](#)
- [Compile Toolbar](#)
- [Simulate Toolbar](#)
- [Wave Cursor Toolbar](#)
- [Wave Edit Toolbar](#)
- [Wave Toolbar](#)
- [Wave Compare Toolbar](#)
- [Zoom Toolbar](#)
- [Wave Expand Time Toolbar](#)

Chapter 3

Protecting Your Source Code

As today's IC designs increase in complexity, silicon manufacturers are leveraging third-party intellectual property (IP) to maintain or shorten design cycle times. This third-party IP is often sourced from several IP vendors, each of whom may require different levels of protection in EDA tool flows. The number of protection/encryption schemes developed by IP vendors has complicated the use of protected IP in design flows made up of tools from several EDA providers.

ModelSim's encryption solution allows IP vendors to deliver encrypted IP code that can be used in a wide range of EDA tools and design flows. This enables usage scenarios such as making module ports, parameters, and specify blocks publicly visible while keeping the implementation private.

ModelSim supports encryption of VHDL, Verilog, and SystemVerilog IP code in protected encryption envelopes. VHDL encryption is defined by the IEEE Standard 1076-2008 section 24.1 (titled "Protect tool directives") and Annex H, section H.3 (titled "Digital envelopes"). Verilog/SystemVerilog encryption is defined by the IEEE Standard 1364-2005 section 28 (titled "Protected envelopes") and Annex H, section H.3 (titled "Digital envelopes"). The protected envelopes usage model, as presented in Annex H section H.3 of both standards, is the recommended methodology for users of VHDL's ``protect` and Verilog's ``pragma protect` compiler directives. We recommend that you obtain these specifications for reference.

ModelSim also supports encryption of VHDL files using the `vcom -nodebug` command.

Usage Models for Protecting Verilog Source Code

ModelSim's encryption capabilities support the following Verilog and SystemVerilog usage models for IP vendors and their customers.

- IP vendors may use the [vencrypt](#) utility to deliver Verilog and SystemVerilog code containing undefined macros and ``directives`. (The [vencrypt](#) utility is not supported for VHDL.) The IP user can then define the macros and ``directives` and use the code in a wide range of EDA tools and design flows. See [Delivering IP Code with Undefined Macros](#).
- IP vendors may use ``pragma protect` directives to protect Verilog and SystemVerilog code containing vendor-defined macros and ``directives`. The IP code can be delivered to IP customers for use in a wide range of EDA tools and design flows. See [Delivering IP Code with Vendor-Defined Macros](#).

- IP vendors and IP users may use the ModelSim-specific ``protect`/``endprotect` compiler directives to define regions of Verilog and SystemVerilog code to be protected. The code is then compiled with the `vlog +protect` command and simulated with ModelSim. (See [Compiling a Design with +protect](#).) The `vencrypt` utility may be used if the code contains undefined macros or ``directives`, but the code must then be compiled and simulated with ModelSim. See [Delivering Protected Verilog IP with `protect](#).

Note

While ModelSim supports both ``protect` and ``pragma protect` encryption directives, these two approaches to encryption are incompatible. Code encrypted by one type of directive cannot be decoded by another.

Delivering IP Code with Undefined Macros

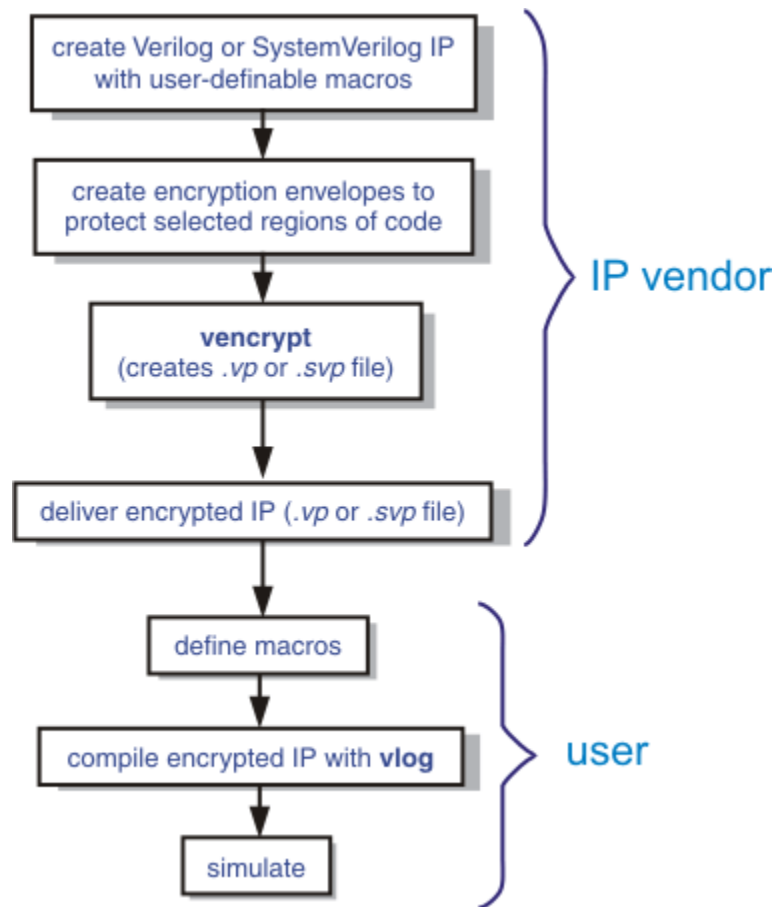
The `vencrypt` utility enables IP vendors to deliver Verilog and SystemVerilog IP code that contains undefined macros and ``directives`. The resulting encrypted IP code can then be used in a wide range of EDA tools and design flows.

Note

The `vencrypt` utility is not currently supported for VHDL.

The recommended `vencrypt` usage flow is shown in [Figure 3-1](#).

Figure 3-1. vencrypt Usage Flow



1. The IP vendor creates Verilog or SystemVerilog IP that contains undefined macros and ``directives`.
2. The IP vendor creates encryption envelopes (see [Creating an Encryption Envelope](#)) with ``pragma protect` expressions to protect selected regions of code or entire files (see [Protection Expressions](#)).
3. The IP vendor uses ModelSim's `vencrypt` utility to encrypt Verilog and SystemVerilog IP code contained within encryption envelopes. The resulting code is not pre-processed before encryption so macros and other ``directives` are unchanged.

The `vencrypt` utility produces a file with a `.vp` or a `.svp` extension to distinguish it from other non-encrypted Verilog and SystemVerilog files, respectively. The file extension may be changed for use with simulators other than ModelSim. The original file extension is preserved if the `-directive=<path>` argument is used with `vencrypt`, or if a ``directive` is used in the file to be encrypted.

With the `-h <filename>` argument for `vencrypt`, the IP vendor may specify a header file that can be used to encrypt a large number of files that do not contain the ``pragma protect` or ``protect` information about how to encrypt the file. Instead, encryption

information is provided in the <filename> specified by `-h <filename>`. This argument essentially concatenates the header file onto the beginning of each file and saves the user from having to edit hundreds of files in order to add in the same ``pragma protect` to every file. For example,

```
vencrypt -h encrypt_head top.v cache.v gates.v memory.v
```

concatenates the information in the `encrypt_head` file into each verilog file listed. The `encrypt_head` file may look like the following:

```
`pragma protect data_method = "aes128-cbc"  
`pragma protect author = "IP Provider"  
`pragma protect key_keyowner = "Mentor Graphics Corporation"  
`pragma protect key_method = "rsa"  
`pragma protect key_keyname = "MGC-VERIF-SIM-RSA-1"  
`pragma protect encoding = (enctype = "base64")  
`pragma protect begin
```

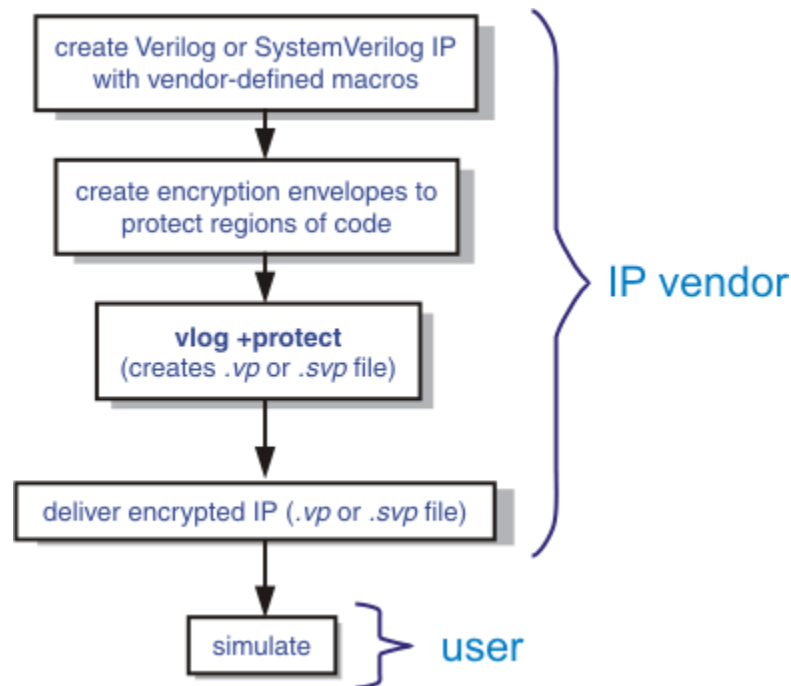
Notice, there is no ``pragma protect end` expression in the header file, just the header block that starts the encryption. The ``pragma protect end` expression is implied by the end of the file.

4. The IP vendor delivers encrypted IP with undefined macros and ``directives`.
5. The IP user defines macros and ``directives`.
6. The IP user compiles the design with `vlog`.
7. Simulation can be performed with ModelSim or other simulation tools.

Delivering IP Code with Vendor-Defined Macros

IP vendors may use ``pragma protect` expressions to protect Verilog and SystemVerilog code containing vendor-defined macros and ``directives`. The resulting encrypted IP code can be delivered to IP customers for use in a wide range of EDA tools and design flows. The recommended usage flow is shown in [Figure 3-2](#).

Figure 3-2. Delivering IP Code with Vendor-Defined Macros



1. The IP vendor creates Verilog or SystemVerilog IP that contains vendor-defined macros and ``directives`.
2. The IP vendor creates encryption envelopes with ``pragma protect` expressions to protect regions of code or entire files. See [Creating an Encryption Envelope and Protection Expressions](#).
3. The IP vendor uses the `vlog +protect` command to encrypt IP code contained within encryption envelopes. The ``pragma protect` expressions are ignored unless the `+protect` argument is used with `vlog`. (See [Compiling a Design with +protect](#).)

The `vlog +protect` command produces a `.vp` or a `.svp` extension to distinguish it from other non-encrypted Verilog and SystemVerilog files, respectively. The file extension may be changed for use with simulators other than ModelSim. The original file extension is preserved if a ``directive` is used in the file to be encrypted. For more information, see [Compiling a Design with +protect](#).

4. The IP vendor delivers the encrypted IP.
5. The IP user simulates the code like any other Verilog file.

When encrypting Verilog source text, any macros without parameters defined on the command line are substituted (not expanded) into the encrypted Verilog file. This makes certain Verilog macros unavailable in the encrypted source text.

ModelSim takes every simple macro that is defined with the `vlog` command and substitutes it into the encrypted text. This prevents third party users of the encrypted blocks from having access to or modifying these macros.

Note



Macros not specified with `vlog` via the `+define+` option are unmodified in the encrypted block.

For example, the code below is an example of a file that might be delivered by an IP provider. The filename for this module is *example00.sv*.

```
`pragma protect data_method = "aes128-cbc"
`pragma protect key_keyowner = "Mentor Graphics Corporation"
`pragma protect key_method = "rsa"
`pragma protect key_keyname = "MGC-VERIF-SIM-RSA-1"
`pragma protect author = "Mentor", author_info = "Mentor_author"
`pragma protect begin
`timescale 1 ps / 1 ps

module example00 ();
  `ifdef IPPROTECT
    reg `IPPROTECT ;
    reg otherReg ;
    initial begin
      `IPPROTECT = 1;
      otherReg    = 0;

      $display("ifdef defined as true");

      `define FOO 0
      $display("FOO is defined as: ", `FOO);
      $display("reg IPPROTECT has the value: ", `IPPROTECT );
    end
  `else
    initial begin
      $display("ifdef defined as false");
    end
  `endif

endmodule

`pragma protect end
```

We encrypt the *example00.sv* module with the `vlog` command as follows:

```
vlog +define+IPPROTECT=ip_value +protect=encrypted00.sv example00.sv
```

This creates an encrypted file called *encrypted00.sv*. We can then compile this file with a macro override for the macro “FOO” as follows:

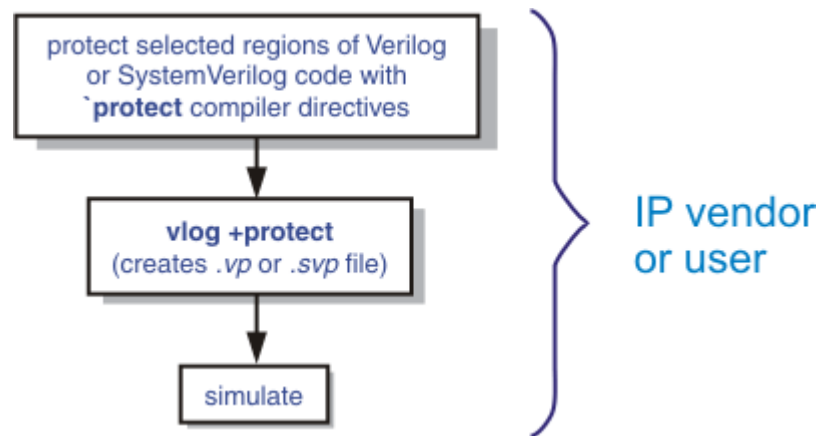
```
vlog +define+FOO=99 encrypted00.sv
```

The macro FOO can be overridden by a customer while the macro IPPROTECT retains the value specified at the time of encryption, and the macro IPPROTECT no longer exists in the encrypted file.

Delivering Protected Verilog IP with ``protect`

The ModelSim-specific ``protect` and ``endprotect` Verilog/SystemVerilog compiler directives are not compatible with other simulators. Though other simulators have a ``protect` directive, the algorithm ModelSim uses to encrypt Verilog and SystemVerilog source files is different. Hence, even though an uncompiled source file with ``protect` is compatible with another simulator, once the source is compiled in ModelSim, the resulting `.vp` or `.svp` source file is not compatible.

Figure 3-3. Delivering IP with ``protect` Compiler Directives



1. The IP vendor protects selected regions of Verilog or SystemVerilog IP with the ``protect / `endprotect` directive pair. The code in ``protect / `endprotect` encryption envelopes has all debug information stripped out. This behaves exactly as if using

```
vlog -nodebug=ports+pli
```

except that it applies to selected regions of code rather than the whole file.

2. The IP vendor uses the `vlog +protect` command to encrypt IP code contained within encryption envelopes. The ``protect / `endprotect` directives are ignored by default unless the `+protect` argument is used with `vlog`.

Once compiled, the original source file is copied to a new file in the current work directory. The `vlog +protect` command produces a `.vp` or a `.svp` extension to distinguish it from other non-encrypted Verilog and SystemVerilog files, respectively. For example, `"top.v"` becomes `"top.vp"` and `"cache.sv"` becomes `"cache.svp."` This new file can be delivered and used as a replacement for the original source file. (See [Compiling a Design with +protect.](#))

Note



The `vencrypt` utility may be used if the code also contains undefined macros or ``directives`, but the code must then be compiled and simulated with ModelSim.

You can use `vlog +protect=<filename>` to create an encrypted output file, with the designated filename, in the current directory (not in the *work* directory, as in the default case where [`=<filename>`] is not specified). For example:

```
vlog test.v +protect=test.vp
```

If the filename is specified in this manner, all source files on the command line will be concatenated together into a single output file. Any ``include` files will also be inserted into the output file.

Caution



``protect` and ``endprotect` directives cannot be nested.

If errors are detected in a protected region, the error message always reports the first line of the protected block.

Using the ``include` Compiler Directive

If any ``include` directives occur within a protected region and you use `vlog +protect` to compile, the compiler generates a copy of the include file with a `.vp` or a `.svp` extension and encrypts the entire contents of the include file. For example, if we have a header file, *header.v*, with the following source code:

```
initial begin
  a <= b;
  b <= c;
end
```

and the file we want to encrypt, *top.v*, contains the following source code:

```
module top;
  `protect
  `include "header.v"
  `endprotect
endmodule
```

then, when we use the `vlog +protect` command to compile, the source code of the header file will be encrypted. If we could decrypt the resulting *work/top.vp* file it would look like:

```
module top;
  `protect
  initial begin
    a <= b;
    b <= c;
  end
  `endprotect
```

```
endmodule
```

In addition, `vlog +protect` creates an encrypted version of `header.v` in `work/header.vp`.

In the `vencrypt` flow (see [Delivering IP Code with Undefined Macros](#)), any ``include` statements will be treated as text just like any other source code and will be encrypted with the other Verilog/SystemVerilog source code. So, if we used the `vencrypt` utility on the `top.v` file above, the resulting `work/top.vp` file would look like the following (if we could decrypt it):

```
module top;
  `protect
  `include "header.v"
  `endprotect
endmodule
```

The `vencrypt` utility will not create an encrypted version of `header.h`.

When you use `vlog +protect` to generate encrypted files, the original source files must all be complete Verilog or SystemVerilog modules or packages. Compiler errors will result if you attempt to perform compilation of a set of parameter declarations within a module. (See also [Compiling a Design with +protect](#).)

You can avoid such errors by creating a dummy module that includes the parameter declarations. For example, if you have a file that contains your parameter declarations and a file that uses those parameters, you can do the following:

```
module dummy;
  `protect
  `include "params.v" // contains various parameters
  `include "tasks.v" // uses parameters defined in params.v
  `endprotect
endmodule
```

Then, compile the dummy module with the `+protect` switch to generate an encrypted output file with no compile errors.

`vlog +protect dummy.v`

After compilation, the work library will contain encrypted versions of `params.v` and `tasks.v`, called `params.vp` and `tasks.vp`. You may then copy these encrypted files out of the work directory to more convenient locations. These encrypted files can be included within your design files; for example:

```
module main
  'include "params.vp"
  'include "tasks.vp"
  ...
endmodule
```

Usage Models for Protecting VHDL Source Code

ModelSim's encryption capabilities support the following VHDL usage models.

- IP vendors may use ``protect` directives to create an encryption envelope (see [Creating an Encryption Envelope](#)) for the VHDL code to be protected and use ModelSim's default encryption and decryption actions. The IP code can be delivered to IP customers for use in a wide range of EDA tools and design flows. See [Using ModelSim Default Encryption for VHDL](#).
- IP vendors may use ``protect` directives to create an encryption envelope for VHDL code and select encryption methods and encoding other than ModelSim's default methods. See [User-Selected Encryption for VHDL](#).
- IP vendors may use "raw" encryption and encoding to aid debugging. See [Using raw Encryption for VHDL](#).
- IP vendors may encrypt several parts of the source file, choose the encryption method for encrypting the source (the `data_method`), and use a key automatically provided by ModelSim. See [Encrypting Several Parts of a VHDL Source File](#).
- IP vendors can use the concept of multiple key blocks to produce code that is secure and portable across different simulators. See [Using Portable Encryption for Multiple Simulators](#).

The usage models are illustrated by examples in the sections below.

Using ModelSim Default Encryption for VHDL

Suppose an IP vendor needs to make a design entity, called IP1, visible to the user, so the user can instantiate the design; but the vendor wants to hide the architecture implementation from the user. In addition, suppose that IP1 instantiates entity IP2, which the vendor wants to hide completely from the user. The easiest way to accomplish this is to surround the regions to be protected with ``protect begin` and ``protect end` directives and let ModelSim choose default actions. For this example, all the source code exists in a single file, *example1.vhd*:

```
===== file example1.vhd =====  
  
-- The entity "ip1" is not protected  
...  
entity ip1 is  
...  
end ip1;  
  
-- The architecture "a" is protected  
-- The internals of "a" are hidden from the user  
`protect begin  
architecture a of ip1 is  
...  
end a;
```



```

`protect end

-- Both the entity "ip2" and its architecture "a" are completely protected
`protect begin
entity ip2 is
...
end ip2;
architecture a of ip2 is
...
end a;
`protect end

===== end of file example1.vhd =====

```

The IP vendor compiles this file with the `vcom +protect` command as follows:

`vcom +protect=example1.vhdp example1.vhd`

The compiler produces an encrypted file, *example1.vhdp* which looks like the following:

```

===== file example1.vhdp =====

-- The entity "ip1" is not protected
...
entity ip1 is
...
end ip1;

-- The architecture "a" is protected
-- The internals of "a" are hidden from the user
`protect BEGIN_PROTECTED
`protect encrypt_agent = "Model Technology", encrypt_agent_info = "DEV"
`protect key_keyowner = "Mentor Graphics Corporation" , key_keyname =
"MGC-VERIF-SIM-RSA-1" , key_method = "rsa"
`protect encoding = ( enctype = "base64" )
`protect KEY_BLOCK
    <encoded encrypted session key>
`protect data_method="aes128-cbc"
`protect encoding = ( enctype = "base64" , bytes = 224 )
`protect DATA_BLOCK
    <encoded encrypted IP>
`protect END_PROTECTED

-- Both the entity "ip2" and its architecture "a" are completely protected
`protect BEGIN_PROTECTED
`protect encrypt_agent = "Model Technology", encrypt_agent_info = "DEV"
`protect key_keyowner = "Mentor Graphics Corporation" , key_keyname =
"MGC-VERIF-SIM-RSA-1" , key_method = "rsa"
`protect encoding = ( enctype = "base64" )
`protect KEY_BLOCK
    <encoded encrypted session key>
`protect data_method = "aes128-cbc"
`protect encoding = ( enctype = "base64" , bytes = 224 )
`protect DATA_BLOCK
    <encoded encrypted IP>
`protect END_PROTECTED

```

```
===== end of file example1.vhdp =====
```

When the IP vendor surrounds a text region using only ``protect begin` and ``protect end`, ModelSim uses default values for both encryption and encoding. The first few lines following the ``protect BEGIN_PROTECTED` region in file *example1.vhdp* contain the `key_keyowner`, `key_keyname`, `key_method` and `KEY_BLOCK` directives. The session key is generated into the key block and that key block is encrypted using the "rsa" method. The `data_method` indicates that the default data encryption method is aes128-cbc and the "enctype" value shows that the default encoding is base64.

Alternatively, the IP vendor can compile file *example1.vhd* with the command:

```
vcom +protect example1.vhd
```

Here, the vendor does not supply the name of the file to contain the protected source. Instead, ModelSim creates a protected file, gives it the name of the original source file with a 'p' placed at the end of the file extension, and puts the new file in the current work library directory. With the command described above, ModelSim creates file *work/example1.vhdp*. (See [Compiling a Design with +protect.](#))

The IP user compiles the encrypted file *work/example1.vhdp* the ordinary way. The `+protect` switch is not needed and the IP user does not have to treat the *.vhdp* file in any special manner. ModelSim automatically decrypts the file internally and keeps track of protected regions.

If the IP vendor compiles the file *example1.vhd* and does not use the `+protect` argument, then the file is compiled, various ``protect` directives are checked for correct syntax, but no protected file is created and no protection is supplied.

Encryptions done using ModelSim's default encryption methods are portable to other decryption tools if they support the "rsa" method and if they have access to the Mentor Graphics public encryption key. See [Using the Mentor Graphics Public Encryption Key.](#)

User-Selected Encryption for VHDL

Suppose that the IP vendor wants to produce the same code as in the *example1.vhd* file used above, but wants to provide specific values and not use any default values. To do this the vendor adds ``protect` directives for keys, encryption methods, and encoding, and places them before each ``protect begin` directive. The input file would look like the following:

```
===== file example2.vhd =====

-- The entity "ipl" is not protected
...
entity ipl is
...
end ipl;

-- The architecture "a" is protected
-- The internals of "a" are hidden from the user
```

```

\protect data_method = "aes128-cbc"
\protect encoding = ( enctype = "base64" )
\protect key_keyowner = "Mentor Graphics Corporation" , key_keyname =
"MGC-VERIF-SIM-RSA-1" , key_method = "rsa"
\protect KEY_BLOCK
\protect begin
architecture a of ip1 is
...
end a;
\protect end

-- Both the entity "ip2" and its architecture "a" are completely protected
\protect data_method = "aes128-cbc"
\protect encoding = ( enctype = "base64" )
\protect key_keyowner = "Mentor Graphics Corporation" , key_keyname =
"MGC-VERIF-SIM-RSA-1" , key_method = "rsa"
\protect KEY_BLOCK
\protect begin
library ieee;
use ieee.std_logic_1164.all;
entity ip2 is
...
end ip2;
architecture a of ip2 is
...
end a;
\protect end

===== end of file example2.vhd =====

```

The `data_method` directive indicates that the encryption algorithm "aes128-cbc" should be used to encrypt the source code (data). The `encoding` directive selects the "base64" encoding method, and the various key directives specify that the Mentor Graphic key named "MGC-VERIF-SIM-RSA-1" and the "RSA" encryption method are to be used to produce a key block containing a randomly generated session key to be used with the "aes128-cbc" method to encrypt the source code. See [Using the Mentor Graphics Public Encryption Key](#).

Using raw Encryption for VHDL

Suppose that the IP vendor wants to use "raw" encryption and encoding to help with debugging the following entity:

```

entity example3_ent is

    port (
        in1 : in bit;
        out1 : out bit);

end example3_ent;

```

Then the architecture the vendor wants to encrypt might be this:

```

===== File example3_arch.vhd

```

```
`protect data_method = "raw"
`protect encoding = ( enctype = "raw" )
`protect begin
architecture arch of example3_ent is

begin

out1 <= in1 after 1 ns;

end arch;
`protect end

===== End of file example3_arch.vhd =====
```

If (after compiling the entity) the example3_arch.vhd file were compiled using the command:

vcom +protect example3_arch.vhd

Then the following file would be produced in the work directory

```
===== File work/example3_arch.vhdp =====

`protect data_method = "raw"
`protect encoding = ( enctype = "raw" )
`protect BEGIN_PROTECTED
`protect encrypt_agent = "Model Technology", encrypt_agent_info = "DEV"
`protect data_method = "raw"
`protect encoding = ( enctype = "raw", bytes = 81 )
`protect DATA_BLOCK
architecture arch of example3_ent is

begin

out1 <= in1 after 1 ns;

end arch;
`protect END_PROTECTED

===== End of file work/example3_arch.vhdp
```

Notice that the protected file is very similar to the original file. The differences are that **`protect begin** is replaced by **`protect BEGIN_PROTECTED**, **`protect end** is replaced by **`protect END_PROTECTED**, and some additional encryption information is supplied after the **BEGIN PROTECTED** directive.

See [Encryption and Encoding Methods](#) for more information about raw encryption and encoding.

Encrypting Several Parts of a VHDL Source File

This example shows the use of symmetric encryption. (See [Encryption and Encoding Methods](#) for more information on symmetric and asymmetric encryption and encoding.) It also demonstrates another common use model, in which the IP vendor encrypts several parts of a

source file, chooses the encryption method for encrypting the source code (the `data_method`), and uses a key automatically provided by ModelSim. This is very similar to the ``protect` method in Verilog.

```

===== file example4.vhd =====

entity ex4_ent is

end ex4_ent;

architecture ex4_arch of ex4_ent is
    signal s1: bit;
    `protect data_method = "aes128-cbc"
    `protect begin
        signal s2: bit;
    `protect end
        signal s3: bit;

begin -- ex4_arch

    `protect data_method = "aes128-cbc"
    `protect begin
s2 <= s1 after 1 ns;
    `protect end

s3 <= s2 after 1 ns;

end ex4_arch;

===== end of file example4.vhd

```

If this file were compiled using the command:

vcom +protect example4.vhd

Then the following file would be produced in the work directory:

```

===== File work/example4.vhdp =====

entity ex4_ent is

end ex4_ent;

architecture ex4_arch of ex4_ent is
    signal s1: bit;
    `protect data_method = "aes128-cbc"
    `protect BEGIN_PROTECTED
    `protect encrypt_agent = "Model Technology", encrypt_agent_info = "DEV"
    `protect data_method = "aes128-cbc"
    `protect encoding = ( enctype = "base64" , bytes = 18 )
    `protect DATA_BLOCK
    <encoded encrypted declaration of s2>
    `protect END_PROTECTED
        signal s3: bit;

begin -- ex4_arch

```

```
`protect data_method = "aes128-cbc"
`protect BEGIN_PROTECTED
`protect encrypt_agent = "Model Technology", encrypt_agent_info = "DEV"
`protect data_method = "aes128-cbc"
`protect encoding = ( enctype = "base64" , bytes = 21 )
`protect DATA_BLOCK
<encoded encrypted signal assignment to s2>
`protect END_PROTECTED

s3 <= s2 after 1 ns;

end ex4_arch;

==== End of file work/example4.vhdp
```

The encrypted *example4.vhdp* file shows that an IP vendor can encrypt both declarations and statements. Also, note that the signal assignment

```
s3 <= s2 after 1 ns;
```

is not protected. This assignment compiles and simulates even though signal *s2* is protected. In general, executable VHDL statements and declarations simulate the same whether or not they refer to protected objects.

Using Portable Encryption for Multiple Simulators

An IP vendor can use the concept of multiple key blocks to produce code that is secure and portable across different simulators.

Suppose the vendor wants to modify the *example2.vhd* file in the [User-Selected Encryption for VHDL](#) section (above) so the encrypted model can be decrypted and simulated by both ModelSim and by a hypothetical company named "XYZ inc". The vendor does this by writing a key block for each decrypting tool. If XYZ publishes a public key, the two key blocks in the IP source code might look like the following:

```
`protect key_keyowner = "Mentor Graphics Corporation", key_method = "rsa",
key_keyname = "MGC-VERIF-SIM-RSA-1"
`protect KEY_BLOCK
`protect key_keyowner = "XYZ inc", key_method = "rsa", key_keyname = "XYZ-
keyPublicKey"
`protect KEY_BLOCK
```

The encrypted code would look very much like *example2.vhd* , with the addition of another key block:

```
`protect key_keyowner = "XYZ inc", key_method = "rsa", key_keyname = "XYZ-
keyPublicKey"
`protect KEY_BLOCK
  <encoded encrypted key information for "XYZ inc">
```

ModelSim uses its key block to determine the encrypted session key and XYZ inc uses the second key block to determine the same key. Consequently, both implementations could successfully decrypt the VHDL code.

Protecting Source Code Using -nodebug

Verilog/SystemVerilog and VHDL IP vendors and users may use the `vlog -nodebug` or `vcom -nodebug` command, respectively, to protect entire files. The `-nodebug` argument for both `vcom` and `vlog` hides internal model data. This allows a model supplier to provide pre-compiled libraries without providing source code and without revealing internal model variables and structure.

Note



The `-nodebug` argument encrypts entire files. The ``protect` compiler directive allows you to encrypt regions within a file. Refer to [Compiler Directives](#) for details.

When you compile with `-nodebug`, all source text, identifiers, and line number information are stripped from the resulting compiled object, so ModelSim cannot locate or display any information of the model except for the external pins. Specifically, this means that:

- a Source window will not display the design units' source code
- a Structure window will not display the internal structure
- the Objects window will not display internal signals
- the Processes window will not display internal processes
- the Locals window will not display internal variables
- none of the hidden objects may be accessed through the Dataflow window or with ModelSim commands

You can access the design units comprising your model via the library, and you may invoke `vsim` directly on any of these design units and see the ports. To restrict even this access in the lower levels of your design, you can use the following `-nodebug` options when you compile:

Table 3-1. Compile Options for the -nodebug Compiling

Command and Switch	Result
<code>vcom -nodebug=ports</code>	makes the ports of a VHDL design unit invisible
<code>vlog -nodebug=ports</code>	makes the ports of a Verilog design unit invisible
<code>vlog -nodebug=pli</code>	prevents the use of PLI functions to interrogate the module for information

Table 3-1. Compile Options for the -nodebug Compiling (cont.)

Command and Switch	Result
vlog -nodebug=ports+pli	combines the functions of -nodebug=ports and -nodebug=pli

Note



Do not use the =ports option on a design without hierarchy, or on the top level of a hierarchical design. If you do, no ports will be visible for simulation. Rather, compile all lower portions of the design with -nodebug=ports first, then compile the top level with -nodebug alone.

Design units or modules compiled with -nodebug can only instantiate design units or modules that are also compiled -nodebug.

Do not use -nodebug=ports when the parent is part of a vopt -bbox flow or for mixed language designs, especially for Verilog modules to be instantiated inside VHDL.

Encryption and Encoding Methods

There are two basic encryption techniques: symmetric and asymmetric. Symmetric encryption uses the same key for both encrypting and decrypting the code region. For symmetric encryption, security of the key is critical and information about the key must be supplied to ModelSim. Under certain circumstances (described below) ModelSim will generate a random key for use with a symmetric encryption method or will use an internal key.

The symmetric encryption algorithms ModelSim supports are:

- des-cbc
- 3des-cbc
- aes128-cbc
- aes192-cbc
- aes256-cbc
- blowfish-cbc
- cast128-cbc

The default symmetric encryption method ModelSim uses for encrypting IP source code (data_method) is aes128-cbc.

Asymmetric encryption methods use two keys: a public key for encryption, and a private key for decryption. The public key is openly available and is published using some form of key distribution system. The private key is secret and is used by the decrypting tool, such as

ModelSim. Asymmetric methods are more secure than symmetric methods, but take much longer to encrypt and decrypt data.

The only asymmetric method ModelSim supports is:

rsa

This method is only supported for specifying key information, not for encrypting IP source code (i.e., only for key methods, no for data methods).

For testing purposes, ModelSim also supports raw encryption, which doesn't change the protected source code (the simulator still hides information about the protected region).

All encryption algorithms (except raw) produce byte streams that contain non-graphic characters, so there needs to be an encoding mechanism to transform arbitrary byte streams into portable sequences of graphic characters which can be used to put encrypted text into source files. The encoding methods supported by ModelSim are:

- uuencode
- base64
- raw

Base 64 encoding, which is technically superior to uuencode, is the default encoding used by ModelSim, and is the recommended encoding for all applications.

Raw encoding must only be used in conjunction with raw encryption for testing purposes.

Creating an Encryption Envelope

Symmetric and asymmetric keys can be combined in encryption envelopes to provide the safety of asymmetric keys with the efficiency of symmetric keys. Encryption envelopes can also be used by the IP vendor to produce encrypted source files that can be safely decrypted by multiple vendors. For these reasons, encryption envelopes are the preferred method of protection.

Encryption envelopes work as follows: The encrypting tool generates a random key for use with a symmetric method, called a "session key". The IP protected source code is encrypted using this session key. The encrypting tool needs to communicate the session key to the decrypting tool, which could be ModelSim or some other tool. It does this by means of a `KEY_BLOCK`. For each potential decrypting tool, information about that tool must be provided in the encryption envelope. This information includes the owner of the key (the `key_keyowner`), the name of the key (the `key_keyname`), and the asymmetric method for encrypting/decrypting the key (the `key_method`). The encrypting tool uses this information to encrypt and encode the session key into a `KEY_BLOCK`. The occurrence of a `KEY_BLOCK` in the source code tells the encrypting tool to generate an encryption envelope.

The decrypting tool reads each KEY_BLOCK until it finds one that specifies a key it knows about. It then decrypts the associated KEY_BLOCK data to determine the original session key and uses that session key to decrypt the IP source code.

Encryption envelopes specify a region of source code to be encrypted. These regions are delimited by protection directives (``protect` for VHDL and ``pragma protect` for Verilog and SystemVerilog) that specify the encryption algorithm, key, and envelope attributes. The encryption envelope may be configured two ways:

- The encryption envelope contains the textual design data to be encrypted (Example 3-1).
- The encryption envelope contains ``include` compiler directives that point to files containing the textual design data to be encrypted (Example 3-2).

Note



Source code that incorporates ``include` compiler directives cannot be used in `vencrypt` usage flow.

Example 3-1. Encryption Envelope Contains Verilog IP Code to be Protected

```
module test_dff4(output [3:0] q, output err);
    parameter WIDTH = 4;
    parameter DEBUG = 0;
    reg [3:0] d;
    reg    clk;

    dff4 d4(q, clk, d);

    assign    err = 0;

    initial
    begin
        $dump_all_vpi;
        $dump_tree_vpi(test_dff4);
        $dump_tree_vpi(test_dff4.d4);
        $dump_tree_vpi("test_dff4");
        $dump_tree_vpi("test_dff4.d4");
        $dump_tree_vpi("test_dff4.d", "test_dff4.clk", "test_dff4.q");
        $dump_tree_vpi("test_dff4.d4.d0", "test_dff4.d4.d3");
        $dump_tree_vpi("test_dff4.d4.q", "test_dff4.d4.clk");
    end
endmodule

module dff4(output [3:0] q, input clk, input [3:0] d);
    `pragma protect data_method = "aes128-cbc"
    `pragma protect author = "IP Provider"
    `pragma protect author_info = "Widget 5 version 3.2"
    `pragma protect key_keyowner = "Mentor Graphics Corporation"
    `pragma protect key_method = "rsa"
    `pragma protect key_keyname = "MGC-VERIF-SIM-RSA-1"
    `pragma protect begin
        dff_gate d0(q[0], clk, d[0]);
        dff_gate d1(q[1], clk, d[1]);
    end
endmodule
```

```

    dff_gate d2(q[2], clk, d[2]);
    dff_gate d3(q[3], clk, d[3]);
endmodule // dff4

module dff_gate(output q, input clk, input d);
    wire preset = 1;
    wire clear = 1;

    nand #5
        g1(l1,preset,l4,l2),
        g2(l2,l1,clear,clk),
        g3(l3,l2,clk,l4),
        g4(l4,l3,clear,d),
        g5(q,preset,l2,qbar),
        g6(qbar,q,clear,l3);
endmodule
`pragma protect end

```

If the example file had been VHDL, the encryption envelope would have used ``protect` directives instead of ``pragma protect`.

Example 3-2. Encryption Envelope Contains ``include` Compiler Directives

```

`timescale 1ns / 1ps
`cell define

module dff (q, d, clear, preset, clock);
    output q;
    input d, clear, preset, clock;
    reg q;

    `pragma protect data_method = "aes128-cbc"
    `pragma protect author = "IP Provider", author_info = "Widget 5 v3.2"
    `pragma protect key_keyowner = "Mentor Graphics Corporation"
    `pragma protect key_method = "rsa"
    `pragma protect key_keyname = "MGC-VERIF-SIM-RSA-1"
    `pragma protect begin

    `include diff.v
    `include prim.v
    `include top.v

    `pragma protect end

    always @(posedge clock)
        q = d;

endmodule

`endcelldefine

```

In both examples, the code to be encrypted follows the ``pragma protect begin` expression and ends with the ``pragma protect end` expression. In [Example 3-2](#), the entire contents of `diff.v`, `prim.v`, and `top.v` will be encrypted.

Protection Expressions

The protection envelope contains a number of **`pragma protect** (Verilog/SystemVerilog) or **`protect** (VHDL) expressions. The following expressions are expected when creating an encryption envelope:

- **data_method** — defines the encryption algorithm that will be used to encrypt the designated source text. ModelSim supports the following encryption algorithms: des-cbc, 3des-cbc, aes128-cbc, aes256-cbc, blowfish-cbc, cast128-cbc, and rsa.
- **key_keyowner** — designates the owner of the encryption key.
- **key_keyname** — specifies the keyowner's key name.
- **key_method** — specifies an encryption algorithm that will be used to encrypt the key.

Note



The combination of **key_keyowner**, **key_keyname**, and **key_method** expressions uniquely identify a key.

- **begin** — designates the beginning of the source code to be encrypted.
- **end** — designates the end of the source code to be encrypted

Note



Encryption envelopes cannot be nested. A **`pragma protect begin/end** pair cannot bracket another **`pragma protect begin/end** pair.

Optional **`protect** (VHDL) or **`pragma protect** (Verilog/SystemVerilog) expressions that may be included are as follows:

- **author** — designates the IP provider.
- **author_info** — designates optional author information.
- **encoding** — specifies an encoding method. The default encoding method, if none is specified, is “base 64.”

If a number of protection expressions occur in a single protection directive, the expressions are evaluated in sequence from left to right. In addition, the interpretation of protected envelopes is not dependent on this sequence occurring in a single protection expression or a sequence of protection expression. However, the most recent value assigned to a protection expression keyword will be the one used.

Unsupported Protection Expressions

Optional protection expressions that are not currently supported include:

- any digest_* expression
- decrypt_license
- runtime_license
- viewpoint

Using Public Encryption Keys

If IP vendors want to encrypt for third party EDA tools, other public keys need to be specified with the `key_public_key` directive as follows.

For Verilog and SystemVerilog:

```
`pragma protect key_keyowner="Acme"  
`pragma protect key_keyname="AcmeKeyName"  
`pragma protect key_public_key  
MIGfMA0GCSqGSIb3DQEBAQUAA4GNADCBiQKBgQC38SzR8u6xw1MKRDQPrZOyQMAX  
ID+/1BTN7Dl2bl25++tbKUcQkVMo6ZkCnt1WZ/wT22X7I5aTkagn6vpAXR8XQBu3  
san+chVulnr2p1Qxe1GVm5tt4jCgCfr0BWNfHXWLwE0yBXR9+zvaatCWb0WpS1UN  
5eqofIisn8Hj2ToOdQIDAQAB
```

For VHDL:

```
`protect key_keyowner="Acme"  
`protect key_keyname="AcmeKeyName"  
`protect key_public_key  
MIGfMA0GCSqGSIb3DQEBAQUAA4GNADCBiQKBgQC38SzR8u6xw1MKRDQPrZOyQMAX  
ID+/1BTN7Dl2bl25++tbKUcQkVMo6ZkCnt1WZ/wT22X7I5aTkagn6vpAXR8XQBu3  
san+chVulnr2p1Qxe1GVm5tt4jCgCfr0BWNfHXWLwE0yBXR9+zvaatCWb0WpS1UN  
5eqofIisn8Hj2ToOdQIDAQAB
```

This defines a new key named "AcmeKeyName" with a key owner of "Acme". The data block following `key_public_key` directive is an example of a base64 encoded version of a public key that should be provided by a tool vendor.

Using the Mentor Graphics Public Encryption Key

The Mentor Graphics base64 encoded RSA public key is:

```
MIGfMA0GCSqGSIb3DQEBAQUAA4GNADCBiQKBgQC38SzR8u6xw1MKRDQPrZOyQ  
MAXID+/1BTN7Dl2bl25++tbKUcQkVMo6ZkCnt1WZ/wT22X7I5aTkagn6vpAXR8XQBu3sa  
n+chVulnr2p1Qxe1GVm5tt4jCgCfr0BWNfHXWLwE0yBXR9+zvaatCWb0WpS1UN5eqofIis  
n8Hj2ToOdQIDAQAB
```

In Verilog and SystemVerilog applications, the `vincrypt` utility will recognize the Mentor Graphics public key in the following `pragma protect` directives:

```
`pragma protect key_keyowner = "Mentor Graphics Corporation"
```

```
`pragma protect key_method = "rsa"  
`pragma protect key_keyname = "MGC-VERIF-SIM-RSA-1"
```

The **vincrypt** utility is not supported for VHDL but ModelSim will recognize the Mentor Graphics public key in the following **`protect** directives:

```
`protect key_keyowner = "Mentor Graphics Corporation"  
`protect key_method = "rsa"  
`protect key_keyname = "MGC-VERIF-SIM-RSA-1"
```

Example 3-3 illustrates the encryption envelope methodology for using this key in Verilog/SystemVerilog. With this methodology you can collect the public keys from the various companies whose tools process your IP, then create a template that can be included into the files you want encrypted. During the encryption phase a new key is created for the encryption algorithm each time the source is compiled and also for each separate segment of encrypted code. These keys are never seen by a human. They are encrypted using the supplied RSA public keys.

Example 3-3. Using the Mentor Graphics Public Encryption Key in Verilog/SystemVerilog

```
//  
// Copyright 1991-2009 Mentor Graphics Corporation  
//  
// All Rights Reserved.  
//  
// THIS WORK CONTAINS TRADE SECRET AND PROPRIETARY INFORMATION WHICH IS THE  
PROPERTY OF  
// MENTOR GRAPHICS CORPORATION OR ITS LICENSORS AND IS SUBJECT TO LICENSE TERMS.  
//  
  
`timescale 1ns / 1ps  
`celldefine  
  
module dff (q, d, clear, preset, clock); output q; input d, clear, preset, clock;  
reg q;  
  
`pragma protect data_method = "aes128-cbc"  
`pragma protect key_keyowner = "Mentor Graphics Corporation"  
`pragma protect key_method = "rsa"  
`pragma protect key_keyname = "MGC-VERIF-SIM-RSA-1"  
`pragma protect key_public_key  
MIGfMA0GCSqGSIB3DQEBAQUAA4GNADCBiQKBgQCnJfQb+LLzTMX3NRARsv7A8+LV5SgMEJCvIf9Tif2em  
i4z0qtp8E+nX7QFzocTlClC6Dcq2qIvEJcpqUgTTD+mJ6grJSJ+R4AxxCgvHYUwoT80Xs0QgRqkrGYxWl  
RUnNbcJm4ZULexYz89720j6rQ99n5e  
1kDa/eBcszMJyOkcGQIDAQAB  
  
`pragma protect key_keyowner = "XYZ inc"  
`pragma protect key_method = "rsa"  
`pragma protect key_keyname = "XYZ-keyPublicKey"  
`pragma protect key_public_key  
MIGfMA0GCSqGSIB3DQEBAQUAA4GNADCBiQKBgQC38SzR8u6xw1MKRDQPrZOyQMAXID+/1BTN7D12bl25+  
+tbKUcQkVMo6ZkCntlWZ/wT22X7I5aTkagn6vpAXR8XQBu3san+chVulnr2p1QxelGVm5tt4jCgCfr0BW  
NfHXWLwE0yBXR9+zvaatCwb0WpS1UN5eqofIiisn8Hj2ToOdQIDAQAB  
  
`pragma protect begin  
always @(clear or preset)  
    if (!clear)  
        assign q = 0;  
    else if (!preset)  
        assign q = 1;  
    else
```

```
    deassign q;
`pragma protect end
always @(posedge clock)
    q = d;

endmodule

`endcelldefine
```

Compiling a Design with +protect

To encrypt IP code with ModelSim, the **+protect** argument must be used with either the **vcom** command (for VHDL) or the **vlog** command (for Verilog and SystemVerilog). For example, if a Verilog source code file containing encryption envelopes is named *encrypt.v*, it would be compiled as follows:

```
vlog +protect encrypt.v
```

When **+protect** is used with **vcom** or **vlog**, encryption envelope expressions are transformed into decryption envelope expressions and decryption content expressions. Source text within encryption envelopes is encrypted using the specified key and is recorded in the decryption envelope within a `data_block`. The new encrypted file is created with the same name as the original unencrypted file but with a *'p'* added to the filename extension. For Verilog, then filename extension for the encrypted file is *.vp*; for SystemVerilog it is *.svp*, and for VHDL it is *.vhdp*. This encrypted file is placed in the current work library directory.

You can designate the name of the encrypted file using the **+protect=<filename>** argument with **vcom** or **vlog** as follows:

```
vlog +protect=encrypt.vp encrypt.v
```

[Example 3-4](#) shows the resulting source code when the Verilog IP code used in [Example 3-1](#) is compiled with **vlog +protect**.

Example 3-4. Results After Compiling with vlog +protect

```
module test_dff4(output [3:0] q, output err);
    parameter WIDTH = 4;
    parameter DEBUG = 0;
    reg [3:0] d;
    reg clk;

    dff4 d4(q, clk, d);

    assign err = 0;

    initial
    begin
        $dump_all_vpi;
        $dump_tree_vpi(test_dff4);
        $dump_tree_vpi(test_dff4.d4);
        $dump_tree_vpi("test_dff4");
        $dump_tree_vpi("test_dff4.d4");
    end
endmodule
```

```
    $dump_tree_vpi("test_dff4.d", "test_dff4.clk", "test_dff4.q");
    $dump_tree_vpi("test_dff4.d4.d0", "test_dff4.d4.d3");
    $dump_tree_vpi("test_dff4.d4.q", "test_dff4.d4.clk");
end
endmodule

module dff4(output [3:0] q, input clk, input [3:0] d);
`pragma protect data_method = "aes128-cbc"
`pragma protect author = "IP Provider"
`pragma protect author_info = "Widget 5 version 3.2"
`pragma protect key_keyowner = "Mentor Graphics Corporation"
`pragma protect key_method = "rsa"
`pragma protect key_keyname = "MGC-VERIF-SIM-RSA-1"
`pragma protect begin_protected
`pragma protect encrypt_agent = "Mentor Graphics Corporation"
`pragma protect encrypt_agent_info = "DEV"
`pragma protect data_method = "aes128-cbc"
`pragma protect key_keyowner = "Mentor Graphics Corporation"
`pragma protect key_method = "rsa"
`pragma protect key_keyname = "MGC-VERIF-SIM-RSA-1"
`pragma protect key_block encoding = (enctype = "base64")
RkFpQLpt/2PEyyIkeR8c5fhZi/QTachzLFh2iCMuWJtVVdl7ggjjfiCanXaBtpT3
xzgIx4frhkcZD2L6DphLZ0s6m9fIfi808Ccs2V5uO25U7Q2hpfCbLVsD80Xlj0/g
yxRAi2FdMyfJE31BcojE+RGY2yv9kJePt6w7Qjdxm3o=
`pragma protect data_block encoding = ( enctype = "base64", bytes = 389
)
xH0w19CUbo98hGy+6TWfMFwXc7T9T82m07WNv+CqsJtjm6PiI4Iif6N7oDBLJdqP
3QuI1Zhwbr1M8kZFAyDHSS66qKJe5yLjGvezfrj/GJp57vIKkAhaVAFI6LwPJJNu
Ogr0hhj2WrfDwx4yCezZ4c00MUj2knUvs60ymXeAEzpNWGhpOMf2BhcjUC55/M/C
nspNi0t2xSYtSMlIPpnOe8hIxT+EYB9G66Nvr33A3kfQEf4+0+B4ksRRkGVFlMDN
s9CQIpcezvQo369q7at6nKhqA+LuHhdCGsXGr1nsX0hMQ2Rg9LRl+HJSP5q/I3g7
JEn103Bk8C9FAw0Sjk573trT+MSwQZkx/+SCSIq180kYaWg/TDVPC7KLMkrRnaLx
C5R1KwTkkZbeqGW31FDyWbluK9MiAx13fOtWgGpOMBnpdJM33URFMk6dDKWSePTn
ZvE4RbYJhdA7arT0l6XCFpOgU4BiaD3ihg78uysv3/FB0sN8lMugtMVY+AYAmDzQ
E9xj1whTpHEMMycw6Tln8A==
`pragma protect end_protected
```

In this example, the **`pragma protect data_method** expression designates the encryption algorithm used to encrypt the Verilog IP code. The key for this encryption algorithm is also encrypted. In this cases, the key is encrypted with the RSA public key. The key is recorded in the **key_block** of the protected envelope. The encrypted IP code is recorded in the **data_block** of the envelope. ModelSim allows more than one key_block to be included so that a single protected envelope can be decrypted by tools from different users.

Chapter 4

Optimizing Designs with vopt

ModelSim, by default, performs built-in tool optimizations on your design to maximize simulator performance. These optimizations yield performance improvements over non-optimized runs. The optimizations will limit the visibility of design objects, but you can increase visibility of any objects for debugging purposes, as described in the section "[Preserving Object Visibility for Debugging Purposes](#)".

The command that performs global optimizations in ModelSim is called **vopt**. This chapter discusses the **vopt** functionality, the effects of optimization on your design, and how to customize the application of **vopt** to your design. For details on command syntax and usage, please refer to **vopt** in the Reference Manual.

Optimization Flows

There are two basic flows that you can use to control optimizations for your simulation run.

- **Three-Step Flow** — where you perform compilation, optimization, and simulation in three separate steps.
- **Two-Step Flow** — where you perform compilation and simulation in two separate steps and optimization is implicitly run prior to simulation.

Three-Step Flow

The three-step flow allows you to have the most control over the optimization process, where the steps refer to the following:

- Compilation — vcom or vlog
- Optimization — vopt
 - The optimization step, using vopt, requires you to specify the name of the generated output by using the -o switch. Refer to the section "[Naming the Optimized Design](#)" for additional information. You can use this optimized output for many simulation runs.
- Simulation — vsim

This flow allows you to use ModelSim for several purposes including:

- Using the -bbox option — the Three-step flow is required when using the -bbox option, as described in the section "[Optimizing Portions of your Design](#)".

- Performing a simulation for debug — preserve the highest level of visibility by specifying the `+acc` argument to `vopt`, for example you could use the following:

```
vlog -work <required_files>
vopt +acc top -o dbugver
vsim dbugver
```

- Performing a simulation for regression — reduce the amount of visibility because you are not as concerned about debugging, for example you could use the following:

```
vlog -work <required_files>
vopt top -o optver
vsim optver
```

Naming the Optimized Design

You must provide a name for the optimized design using the `-o` argument to `vopt`:

```
vopt testbench -o opt1
```

Note



The filename must not contain capital letters or any character that is illegal for your platform (for example, on Windows you cannot use “\”).

Incremental Compilation of Named Designs

The default operation of `vopt -o <name>` is incremental compilation: The tool reuses elements of the design that have not changed, resulting in a reduction of runtime for `vopt` when a design has been minimally modified.

Preserving Object Visibility for Debugging Purposes

For a debugging flow you can preserve object visibility by using the `+acc` switch to the `vopt` command. The `+acc` switch specifies which objects are to remain "accessible" for the simulation. The following examples show some common uses of the `vopt +acc` combination, refer to the [vopt](#) reference page for a description of all `+acc` options:

- Preserve visibility of all objects in the design by specifying no arguments to `+acc`:

```
vopt +acc mydesign -o mydesign_opt
```

- Preserve visibility of all objects in a specific module by specifying the name of the module as an argument to `+acc`:

```
vopt top +acc+mod1 mydesign -o mydesign_opt
```

- Preserve visibility of only registers (=r) within a specific module:

```
vopt top +acc=r+mod1 mydesign -o mydesign_opt
```

- Preserve visibility of line numbers (=l) in addition to registers within a specific module:

vopt top +acc=lr+mod1 mydesign -o mydesign_opt

- Preserve visibility of line numbers and registers within a specific module and all children in that module by adding a period (.) after the module name:

vopt top +acc=lr+mod1. mydesign -o mydesign_opt

- Preserve visibility of a unique instance:

vopt +acc=mrp+/top/u1 mydesign -o mydesign_opt

- Preserve visibility of a unique object:

vopt +acc=r+/top/myreg mydesign -o mydesign_opt

Using an External File to Control Visibility Rules

You can use the `-f` switch to specify a file that contains your `+acc` arguments. This is most useful when you have numerous `+acc` arguments that you use regularly or because you provide a very fine control of visibility. For example:

vopt -f acc_file.txt mydesign -o mydesign_opt

where *acc_file.txt* contains:

```
// Add the following flags to the vopt command line.
+acc=rn+tb
+acc=n+tb.dut.u_core
+acc=pn+tb.dut.u_core.u_sub
+acc=pn+tb.dut.u_core.u_sub.u_bp
+acc=rpn+tb.dut.u_core.u_sub.u_bb.U_bb_compare
+acc=pn+tb.dut.u_core.u_sub.u_bb.U_bb_control
+acc=r+tb.dut.u_core.u_sub.u_bb.U_bb_control.U_bb_regs
+acc=rpn+tb.dut.u_core.u_sub.u_bb.U_bb_delay0
```

Creating Specialized Designs for Parameters and Generics

You can use `vopt` to create specialized designs where generics or parameters are predefined by using the `-g` or `-G` switches, as shown in the following example:

vopt top -GTEST=1 -o test1_opt

vopt top -GTEST=2 -o test2_opt

vsim test1_opt

vsim test2_opt

Increase Visibility to Retain Breakpoints

When running in full optimization mode, breakpoints can not be set. To retain visibility of breakpoints you should set the `+acc` option such that the object related to the breakpoint is visible.

Two-Step Flow

The two-step flow allows you to perform design optimizations using existing scripts, in that vsim automatically performs optimization. The two steps refer to the following:

1. Compile — **vcom** or **vlog** compiles all your modules.
2. Simulate — vsim performs the following actions:
 - a. Load — Runs **vopt** in the background when it loads the design.

You can pass arguments to **vopt** using the **-voptargs** argument to **vsim**. For example,

```
vsim mydesign -voptargs="+acc=rn"
```

The optimization step of vsim loads compiled design units from their libraries and regenerates optimized code.

- b. Simulate — Runs **vsim** on the optimized design unit.

Because vopt is called implicitly when using the two-step flow, it creates, internally, an optimized design for the simulator to use. By default, the maximum number of these designs is set to 3, after which, vsim removes the oldest optimized design and creates a new one. You can increase this limit by using the **-unnamed_designs** argument to **vlib**.

Preserving Object Visibility in the Two-Step Flow

When using the three-step flow you can preserve object visibility by using the **+acc** argument to the vopt command as described in the section [Preserving Object Visibility for Debugging Purposes](#). To access this same functionality in the two-step flow you can use the **-voptargs** switch to the vsim command, which passes the arguments to the automatic invocation of vopt.

The following are some examples of how you could pass optimization arguments from the vsim command line:

```
vsim -voptargs="+acc" mydesign
```

```
vsim -voptargs="+acc+mod1" mydesign
```

```
vsim -voptargs="+acc=rnl" mydesign
```

Optimizing Parameters and Generics

During the optimization step you have several options on how parameters and generics affect the optimization of the design:

- **Override** — you can override any design parameters and generics with either the **-G** or **-g** switches to the vopt command. The tool optimizes your design based on how you have overridden any parameters and generics.

Once you override a parameter or generic in the optimization step you will not be able to change its value during the simulation. Therefore, if you attempt to override these same generics or parameters during the simulation, the tool will ignore those specifications of -g/-G.

```
vopt -o opt_top top -GtimingCheck=1 -Gtop/a/noAssertions=0
```

Note



The IEEE Standard for System Verilog (1800-2005) states that local parameters (localparam) cannot be overridden. Due to this definition, the -g, -G, or +floatparameters switches will not override any localparam statements. The document also states that you cannot specify a parameter in a generate scope, and that if one exists, it should be treated as a localparam statement. Therefore, any parameters in a generate scope will not be overridden with -g, -G, or +floatparameters switches.

- **Float** — you can specify that parameters and generics should remain floating by using the +floatparameters or +floatgenerics switches, respectively, to the vopt command. The tool will optimize your design, retaining any information related to these floating parameters and generics so that you can override them during the simulation step.

```
vopt -o opt_top top +floatparameters+timingCheck+noAssertions
```

The +floatgenerics or +floatparameters switches do affect simulation performance. If this is a concern, it is suggested that you create an optimized design for each generic or parameter value you may need to simulate. Refer to the section "[Creating Specialized Designs for Parameters and Generics](#)" for more information.

- **Combination** — you can combine the use of the -g/-G and +floatparameters/+floatgenerics with the vopt command to have more control over the use of parameters and generics for the optimization and simulation steps.

Due to the fact that -g/-G and +floatparameters/+floatgenerics allow some use of wildcards, ambiguities could occur. If, based on your options, a parameter or generic is considered floating and also is overridden the override value take precedence.

```
vopt -o opt_top top +floatparameters+timingCheck  

-Gtop/a/noAssertions=0
```

- **No Switches** — if you do not use any of the above scenarios, where you do not use -g/-G or +floatparameters/+floatgenerics, the tool optimizes the design based on how the design defines parameter and generic values. Due to the optimizations that the tool performs, you may lose the opportunity to override any parameters or generics of the optimized design at simulation time.

If your design contains blackboxed portions (refer to the section [Optimizing Portions of your Design](#)) the -g/-G switches will override any floating parameters or generics in the blackboxed portion. For example:

```
vopt -bbox -o dut_design dut +floatparameters+design.noAssertions
```

```
### creates a blackbox of dut with design.noAssertions floating

vopt -o test_design test -GnoAssertions=0
### the design test uses the blackboxed portion dut
### the vopt command overrides any occurrence of noAssertions,
### including the one in dut.

vsim test_design
### performs the simulation where noAssertions is set to 0.
```

Optimizing Portions of your Design

The **vopt** command allows you to specify the **-bbox** argument, which instructs vopt to optimize, or black box, only a portion of a design. This feature is useful for providing better throughput by allowing you to optimize large portions of your design that may be static or not changing. One example includes: [Simulating Designs with Several Different Test Benches](#).

For any future use of this blackboxed portion, the tool automatically recognizes and uses that portion of the design, which reduces the runtime of vopt.

When you are using vopt **-bbox**, you should associate the optimized name, using the **-o** argument, with the original name, similar to:

```
vopt moda -bbox -o moda_bb_opt
```

For the above example, any design that contains an instantiation of the module *moda*, the tool automatically recognizes during design analysis that it should use the optimized module *moda_bb_opt*.

When using this method, you should be aware of the following:

- When you instantiate a blackboxed portion, you do not need to run vopt on the top level module.
- During optimization, the tool does not descend into the black boxed portion, allowing the tool to run faster. However, parameters passing and hierarchical references across the black box are restricted. You can specify **+acc** as an argument to vopt to remove this restriction, but it will reduce simulation performance.
- You will need to manage both the original portion (*moda*) and its optimized version (*moda_bb_opt*), specifically you must not remove the optimized version without also removing or recompiling the original version.

Simulating Designs with Several Different Test Benches

For this scenario, you would use vopt and **-bbox** to optimize the design. Then you could use the [Three-Step Flow](#) on the different test benches, which prevents having to optimize the design for each test bench. For example:

```

1  vlib work
2  vlib asic_lib
3  vlog -work asic_lib cell_lib.v
4  vlog netlist.v
5  vopt -L asic_lib -debugCellOpt +nocheckALL -bbox netlist -o opt_netlist

6  vlog tb.v test1.v
7  vopt tb -o opt_tb
8  vsim -c opt_tb -do sim.do

9  vlog test2.v
10 vopt tb -o opt_tb
11 vsim -c tb -do sim.do

```

- Lines 3 and 4 — compile the library and netlist
- Line 5 — enable the black box feature and optimize the netlist
- Line 6 — compile the remainder of the design
- Line 7 — optimize the test bench
- Line 8 — simulate the first test bench
- Lines 9 through 11 — compile and optimize a second test bench and resimulate without recompiling or optimizing the black boxed netlist.

Alternate Optimization Flows

The sections below outline usage flows for optimization, using variants of the Three- and Two-Step Flows. We suggest that you primarily use the Three-Step Flow, but offer these alternates that may be useful in your environment.

Simulating Designs with Read-Only Libraries

When you must perform simulations on designs where the library files have restricted file permissions, it is suggested that you create a local library for vopt and vsim to work from. This scenario is illustrated in the following commands:

1. Generation of the restricted libraries:

```

vlib lib1
vlog -work lib1 *.v
vcom -work lib1 util.vhd set.vhd top.vhd

```

2. Lock down of **lib1**.
3. Create a local library for you to work from so you do not run into permission issues.

```

vlib write_design

```

4. Optimize your design using the -work and -L switches:

```
vopt -work write_design -o opt_top -L lib1 lib1.top
```

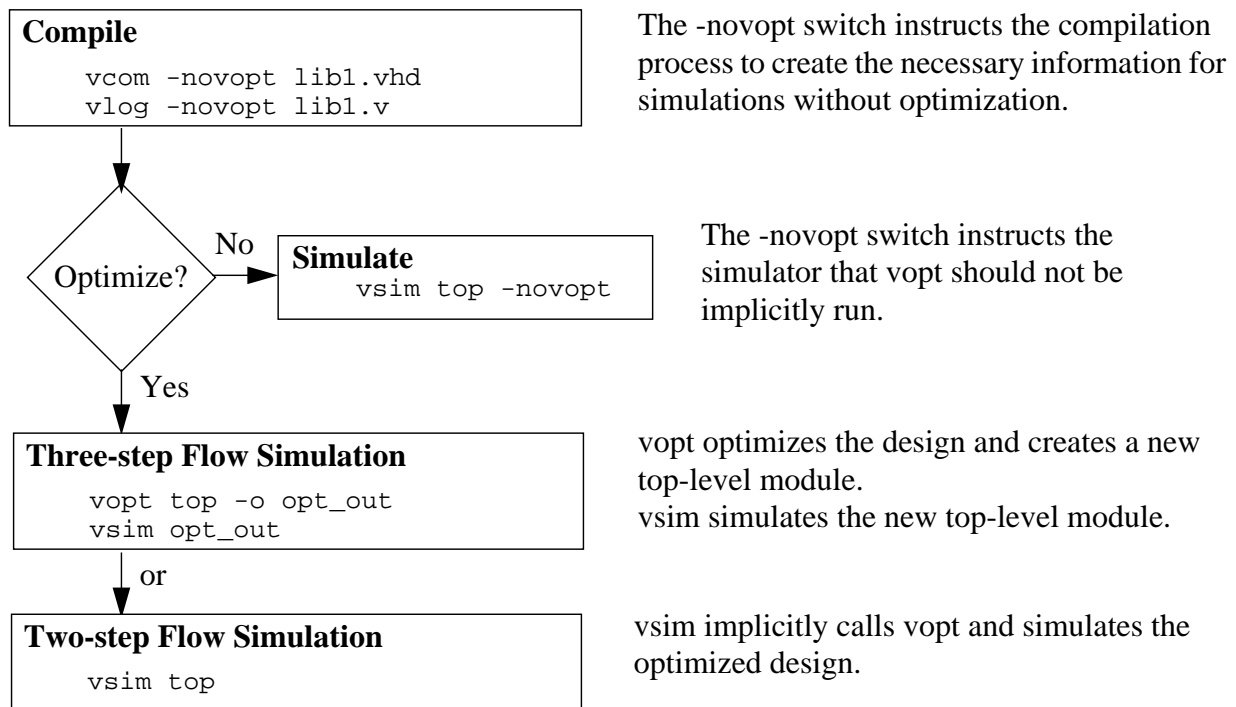
5. Simulate your design using the -lib switch:

```
vsim opt_top -lib write_design
```

Creating an Environment for Optimized and Unoptimized Flows

Some work environments require that a user decide whether they need to simulate using optimizations or no optimizations at all. The following flow outlines one process for accomplishing this goal.

A more efficient process is to use the [Three-Step Flow](#) and use +acc for [Preserving Object Visibility for Debugging Purposes](#).



Preserving Design Visibility with the Learn Flow

To ensure that you retain the proper level of design visibility when performing an optimized simulation (using vopt in the [Three-Step Flow](#)) you can use the -learn switch to vsim, which creates control files that include instructions for preserving visibility.

The control files created in this flow allow you to retain information during optimization for the following:

- ACC/TF PLI routines
- VPI PLI routines
- SignalSpy accesses
- force Run-time command
- FLI instances (regions), signals, ports, and variables.
- Objects specified as arguments to commands executed after -learn is started, such as add wave /top/p/*.

The following steps describe the use of the Learn Flow for preserving visibility using PLI routines:

1. Invoke the simulator

```
vsim -novopt -learn top_pli_learn -pli mypli.sl top
```

When you specify the -learn switch, where an argument defines the root name (top_pli_learn) of the generated control files, vsim analyzes your design as well as your PLI to determine what information needs to be retained during the optimization. Based on this analysis it then creates the following control files and places them in the current directory:

```
top_pli_learn.acc  
top_pli_learn.ocf  
top_pli_learn.ocm
```

Refer to the section “[Description of Learn Flow Control Files](#)” for a description of these files.

The learn flow is sensitive to the PathSeparator variable in the *modelsim.ini* file at the time of creation of the control files. Be sure to use a consistent PathSeparator throughout this flow.

2. Run the simulation to generate the control files (*.acc*, *.ocf*, and *.ocm*).

```
run <time_step><time_unit>
```

When running the simulation, the Learn Flow tracks and records the objects required for your PLI routines or used for commands executed before or after the run, for which you need to retain visibility. It is difficult to suggest how long you should run the simulation; your knowledge of the design and test bench should allow a guideline for you to follow.

To ensure that the simulator records every possible access, you should run a complete simulation (run -all).

Because the files are saved at the end of simulation, you should not restart or restore the simulation when working with the Learn Flow.

3. Create an optimized design, retaining the visibility as defined in the control files. You can determine which type of control file you wish to use. A command line example for each type include:

```
vopt -f top_pli_learn.acc -o top_opt
```

```
vopt -ocf top_pli_learn.ocf -o top_opt
```

```
vopt -ocf top_pli_learn.ocm -o top_opt
```

vopt creates the optimized design, *top_opt*, and retains visibility to the objects required by your PLI routines.

4. Simulate the optimized design.

```
vsim -pli mypli.sl top_opt
```

This performs the simulation on the optimized design, where you retained visibility to the objects required by your PLI routines.

Description of Learn Flow Control Files

The control files for the learn flow are text files that instruct vopt to retain visibility to objects required by the specified PLI routines. All three file formats are considered to be non-lossy, in that information about every object touched by the PLI during the -learn run is retained.

- .acc Learn Flow control file — This format (.acc) creates the information in the traditional +acc format used by the vopt command. However, this format does not allow for precise targeting of objects that you can get with the .ocf format.
- .ocf Learn Flow control file — This format (.ocf) is the most verbose and precisely targeted of the three control files. It is suggested that you use this file for situations where there is sparse access to objects. If you access every object in a module, this file can get considerably large.
- .ocm Learn Flow control file — This format (.ocm) is similar to the .ocf format, except that the file is factorized by design unit, which results in a smaller and more easily read file, but provides less precise targeting.

These files are text-based and can be edited by anyone.

Controlling Optimization from the GUI

Optimization (**vopt**) in the GUI is controlled from the **Simulate > Design Optimization** dialog box.

To restore total design visibility from within the GUI:

1. Select **Simulate > Design Optimization > Visibility** tab
2. Select “Apply full visibility to all modules (full debug mode)”

3. Select Design tab and select the top-level design unit to simulate
4. Specify an Output Design Name.
5. Select Start Immediately and then click OK.

Optimization Considerations for Verilog Designs

The optimization considerations for Verilog designs include:

- [Design Object Visibility for Designs with PLI](#)
- [Reporting on Gate-Level Optimizations](#)
- [Using Pre-Compiled Libraries](#)
- [Event Order and Optimized Designs](#)
- [Timing Checks in Optimized Designs](#)

Design Object Visibility for Designs with PLI

Some of the optimizations performed by **vopt** impact design object visibility. For example, many objects do not have PLI Access handles, potentially affecting the operation of PLI applications. However, a handle is guaranteed to exist for any object that is an argument to a system task or function.

In the early stages of design, you may use one or more **+acc** arguments in conjunction with **vopt** to enable access to specific design objects. See the **vopt** command in the Reference Manual for specific syntax of the **+acc** argument.

Automatic **+acc** for Designs with PLI

By default, if your design contains any PLI, and the automatic vopt flow is enabled, **vsim** automatically adds a **+acc** to the sub-invocation of **vopt**, which disables most optimizations.

If you want to override the automatic disabling of the optimizations for modules containing PLI, specify the **-no_autoacc** argument to **vsim**.

Manual **+acc** for Designs with PLI

If you are manually controlling vopt optimizations, and your design uses PLI applications that look for object handles in the design hierarchy, then it is likely that you will need to use the **+acc** option. For example, the built-in **\$dumpvars** system task is an internal PLI application that requires handles to nets and registers so that it can call the PLI routine **acc_vcl_add()** to monitor changes and dump the values to a VCD file. This requires that access is enabled for the nets and registers on which it operates.

Suppose you want to dump all nets and registers in the entire design, and that you have the following \$dumpvars call in your test bench (no arguments to \$dumpvars means to dump everything in the entire design):

```
initial $dumpvars;
```

Then you need to optimize your design as follows to enable net and register access for all modules in the design:

vopt +acc=rn testbench

As another example, suppose you only need to dump nets (n) and registers (r) of a particular instance in the design (the first argument of **1** means to dump just the variables in the instance specified by the second argument):

```
initial $dumpvars(1, testbench.u1);
```

Then you need to optimize your design as follows (assuming *testbench.u1* is an instance of the module *design*):

vopt +acc=rn+design testbench

Finally, suppose you need to dump everything in the children instances of *testbench.u1* (the first argument of **0** means to also include all children of the instance):

```
initial $dumpvars(0, testbench.u1);
```

Then you need to optimize your design as follows:

vopt +acc=rn+design. testbench

To gain maximum performance, it may be necessary to enable the minimum required access within the design.

Performing Optimization on Designs Containing SDF

For both optimization flows ([Two-Step Flow](#) and [Three-Step Flow](#)) they will both automatically perform SDF compilation using [sdfcom](#) if any of the following apply:

- \$sdf_annotate system task exists in the test bench.
- -sdfmin, -sdfmax, or -sdftyp on the [vopt](#) command line in the Three-Step Flow
- -sdfmin, -sdfmax, or -sdftyp on the [vsim](#) command line in the Two-Step Flow

You can disable the automatic SDF compilation during optimization by setting the [VoptAutoSDFCompile](#) variable in the *modelsim.ini* file to 0

```
[vsim]  
...  
VoptAutoSDFCompile = 0
```

...

The following arguments to vopt are useful when you are dealing with SDF:

- vopt +notimingchecks — Allows you to simulate your gate-level design without taking into consideration timing checks, giving you performance benefits. For example:

```
vlog cells.v netlist.v tb.v
vopt tb -o tb_opt -O5 +nocheckALL +delay_mode_path +notimingchecks \
-debugCellOpt
vsim tb_opt
```

By default, **vopt** does not fix the TimingChecksOn generic in Vital models. Instead, it lets the value float to allow for overriding at simulation time. If best performance and no timing checks are desired, +notimingchecks should be specified with vopt.

vopt +notimingchecks topmod

Specifying **vopt +notimingchecks** or -GTimingChecks=<FALSE/TRUE> will fix the generic value for simulation. As a consequence, using **vsim +notimingchecks** at simulation may not have any effect on the simulation depending on the optimization of the model.

- vopt {-sdfmin | -sdftyp | -sdfmax } [<instance>=]<sdf_filename> — Annotates cells in the specified SDF files with minimum, typical, or maximum timing. This invocation will trigger the automatic SDF compilation.
- vopt +nocheck{ALL | CLUP | DELAY | DNET | OPRD | SUDP} — Disables specific optimization checks (observe uppercase). Refer to the [vopt](#) reference page for details.

Reporting on Gate-Level Optimizations

You can use the [write cell_report](#) and the **-debugCellOpt** argument to the **vopt** command to obtain information about which cells have and have not been optimized.

write cell_report produces a text file that lists all modules.

```
vopt tb -o tb_opt -debugCellOpt
vsim tb_opt -do "write cell_report cell.rpt; quit -f"
```

Modules with "(cell)" following their names are optimized cells. For example,

```
Module: top
Architecture: fast

Module: bottom (cell)
Architecture: fast
```

In this case, top was not optimized and bottom was.

Using Pre-Compiled Libraries

If the source code is unavailable for any of the modules referenced in a design, then you must search libraries for the precompiled modules using the **-L** or **-Lf** arguments to **vopt**. The **vopt** command optimizes pre-compiled modules the same as if the source code is available. The optimized code for a pre-compiled module is written to the default 'work' library.

The **vopt** command automatically searches libraries specified in the ``uselib` directive (see [Verilog-XL uselib Compiler Directive](#)). If your design uses ``uselib` directives exclusively to reference modules in other libraries, then you do not need to specify library search arguments.

Event Order and Optimized Designs

The Verilog language does not require that the simulator execute simultaneous events in any particular order. Optimizations performed by **vopt** may expose event order dependencies that cause a design to behave differently than when run unoptimized. Event order dependencies are considered errors and should be corrected (see [Event Ordering in Verilog Designs](#) for details).

Timing Checks in Optimized Designs

Timing checks are performed whether you optimize the design or not. In general, you'll see the same results in either case. However, in a cell where there are both interconnect delays and conditional timing checks, you might see different timing check results.

- Without **vopt** — The conditional checks are evaluated with non-delayed values, complying with the original IEEE Std 1364-1995 specification. You can use the `-v2k_int_delays` switch with **vsim** to ensure compatibility by forcing the IEEE Std 1364-2005 implementation.
- With **vopt** — the conditional checks will be evaluated with delayed values, complying with the new IEEE Std 1364-2005 specification.

Projects simplify the process of compiling and simulating a design and are a great tool for getting started with ModelSim.

What are Projects?

Projects are collection entities for designs under specification or test. At a minimum, projects have a root directory, a work library, and "metadata" which are stored in an *.mpf* file located in a project's root directory. The metadata include compiler switch settings, compile order, and file mappings. Projects may also include:

- Source files or references to source files
- other files such as READMEs or other project documentation
- local libraries
- references to global libraries
- Simulation Configurations (see [Creating a Simulation Configuration](#))
- Folders (see [Organizing Projects with Folders](#))

Note



Project metadata are updated and stored *only* for actions taken within the project itself. For example, if you have a file in a project, and you compile that file from the command line rather than using the project menu commands, the project will not update to reflect any new compile settings.

What are the Benefits of Projects?

Projects offer benefits to both new and advanced users. Projects

- simplify interaction with ModelSim; you don't need to understand the intricacies of compiler switches and library mappings
- eliminate the need to remember a conceptual model of the design; the compile order is maintained for you in the project. Compile order is maintained for HDL-only designs.
- remove the necessity to re-establish compiler switches and settings at each session; these are stored in the project metadata as are mappings to source files

- allow users to share libraries without copying files to a local directory; you can establish references to source files that are stored remotely or locally
- allow you to change individual parameters across multiple files; in previous versions you could only set parameters one file at a time
- enable "what-if" analysis; you can copy a project, manipulate the settings, and rerun it to observe the new results
- reload the initial settings from the project *.mpf* file every time the project is opened

Project Conversion Between Versions

Projects are generally not backwards compatible for either number or letter releases. When you open a project created in an earlier version, you will see a message warning that the project will be converted to the newer version. You have the option of continuing with the conversion or cancelling the operation.

As stated in the warning message, a backup of the original project is created before the conversion occurs. The backup file is named *<project name>.mpf.bak* and is created in the same directory in which the original project is located.

Getting Started with Projects

This section describes the four basic steps to working with a project.

- [Step 1 — Creating a New Project](#)

This creates an *.mpf* file and a working library.

- [Step 2 — Adding Items to the Project](#)

Projects can reference or include source files, folders for organization, simulations, and any other files you want to associate with the project. You can copy files into the project directory or simply create mappings to files in other locations.

- [Step 3 — Compiling the Files](#)

This checks syntax and semantics and creates the pseudo machine code ModelSim uses for simulation.

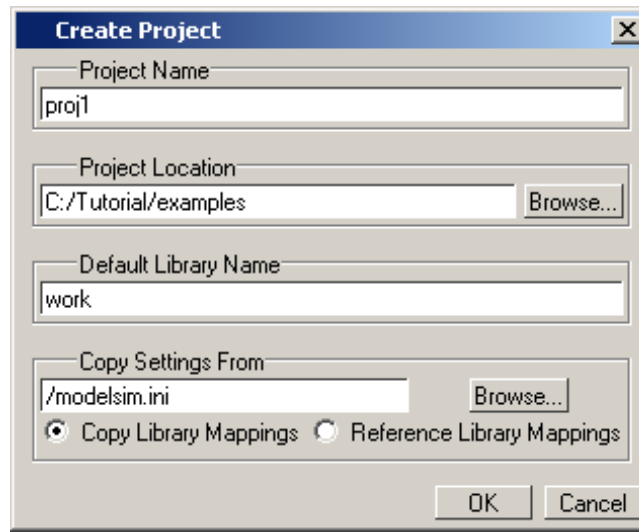
- [Step 4 — Simulating a Design](#)

This specifies the design unit you want to simulate and opens a structure tab in the Workspace pane.

Step 1 — Creating a New Project

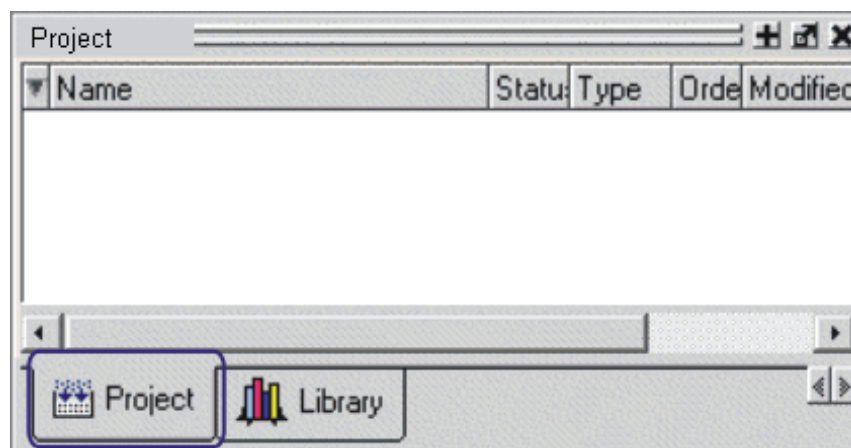
Select **File > New > Project** to create a new project. This opens the **Create Project** dialog where you can specify a project name, location, and default library name. You can generally leave the **Default Library Name** set to "work." The name you specify will be used to create a working library subdirectory within the Project Location. This dialog also allows you to reference library settings from a selected *.ini* file or copy them directly into the project.

Figure 5-1. Create Project Dialog



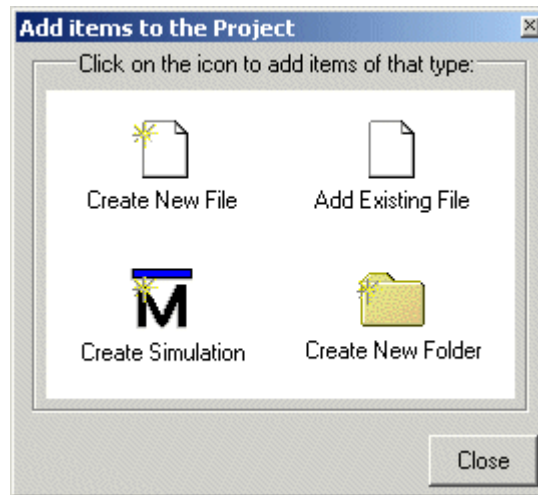
After selecting OK, you will see a blank Project window in the Main window ([Figure 5-2](#))

Figure 5-2. Project Window Detail



and the **Add Items to the Project** dialog ([Figure 5-3](#)).

Figure 5-3. Add items to the Project Dialog



The name of the current project is shown at the bottom left corner of the Main window.

Step 2 — Adding Items to the Project

The **Add Items to the Project** dialog includes these options:

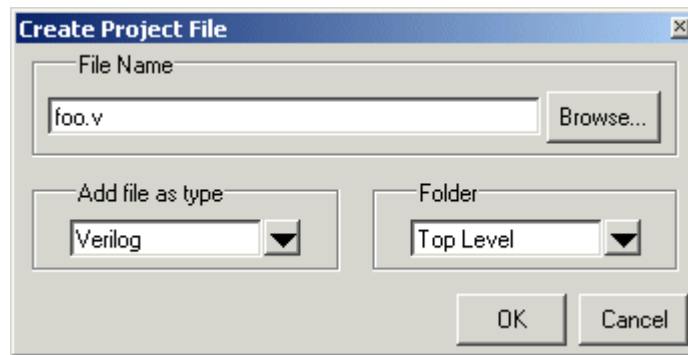
- **Create New File** — Create a new VHDL, Verilog, SystemC, Tcl, or text file using the Source editor. See below for details.
- **Add Existing File** — Add an existing file. See below for details.
- **Create Simulation** — Create a Simulation Configuration that specifies source files and simulator options. See [Creating a Simulation Configuration](#) for details.
- **Create New Folder** — Create an organization folder. See [Organizing Projects with Folders](#) for details.

Create New File

The **File > New > Source** menu selections allow you to create a new VHDL, Verilog, SystemC, Tcl, or text file using the Source editor.

You can also create a new project file by selecting **Project > Add to Project > New File** (the Project tab in the Workspace must be active) or right-clicking in the Project tab and selecting **Add to Project > New File**. This will open the Create Project File dialog ([Figure 5-4](#)).

Figure 5-4. Create Project File Dialog



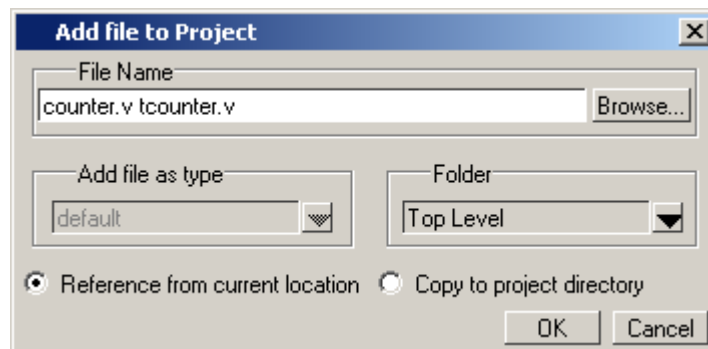
Specify a name, file type, and folder location for the new file.

When you select OK, the file is listed in the Project tab. Double-click the name of the new file and a Source editor window will open, allowing you to create source code.

Add Existing File

You can add an existing file to the project by selecting **Project > Add to Project > Existing File** or by right-clicking in the Project tab and selecting **Add to Project > Existing File**.

Figure 5-5. Add file to Project Dialog

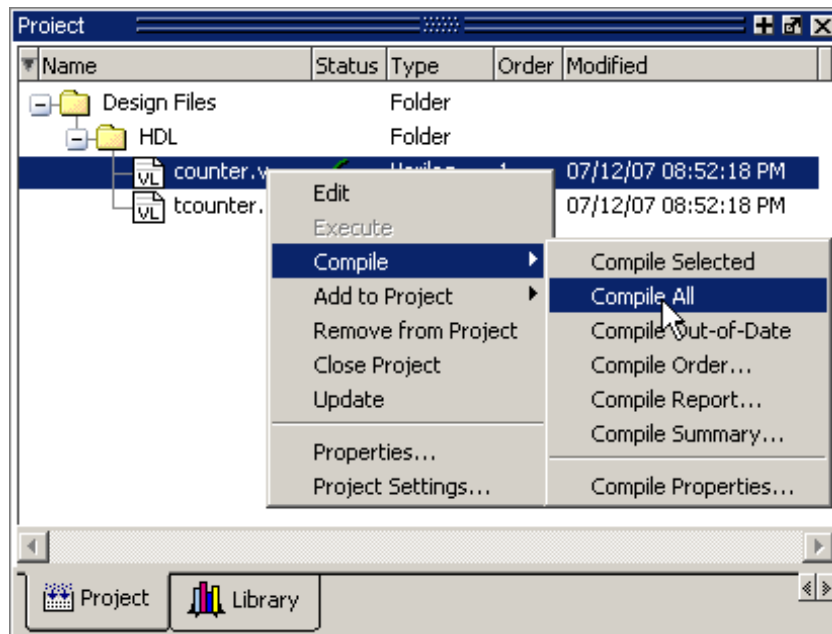


When you select OK, the file(s) is added to the Project tab.

Step 3 — Compiling the Files

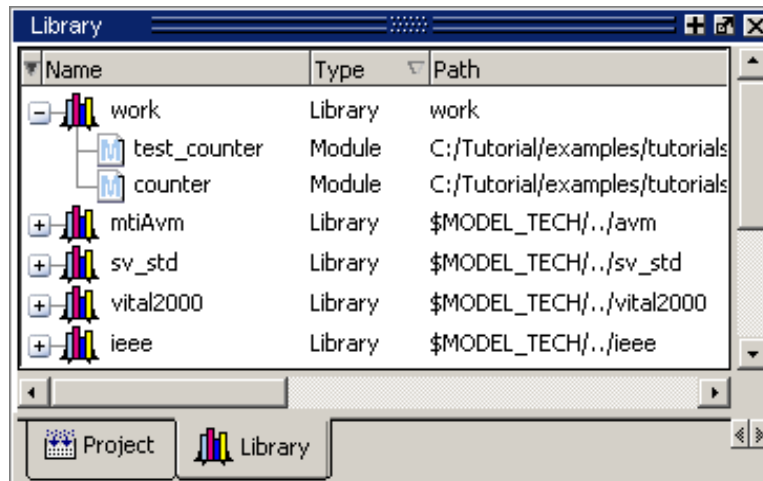
The question marks in the Status column in the Project tab denote either the files haven't been compiled into the project or the source has changed since the last compile. To compile the files, select **Compile > Compile All** or right click in the Project tab and select **Compile > Compile All** (Figure 5-6).

Figure 5-6. Right-click Compile Menu in Project Window



Once compilation is finished, click the Library window, expand library *work* by clicking the "+", and you will see the compiled design units.

Figure 5-7. Click Plus Sign to Show Design Hierarchy



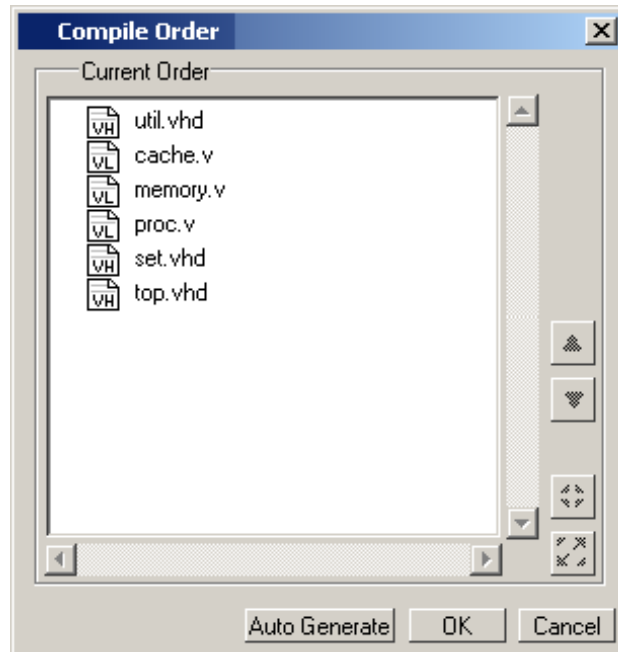
Changing Compile Order

The Compile Order dialog box is functional for HDL-only designs. When you compile all files in a project, ModelSim by default compiles the files in the order in which they were added to the project. You have two alternatives for changing the default compile order: 1) select and compile each file individually; 2) specify a custom compile order.

To specify a custom compile order, follow these steps:

1. Select **Compile > Compile Order** or select it from the context menu in the Project tab.

Figure 5-8. Setting Compile Order



2. Drag the files into the correct order or use the up and down arrow buttons. Note that you can select multiple files and drag them simultaneously.

Auto-Generating Compile Order

Auto Generate is supported for HDL-only designs. The **Auto Generate** button in the Compile Order dialog (see above) "determines" the correct compile order by making multiple passes over the files. It starts compiling from the top; if a file fails to compile due to dependencies, it moves that file to the bottom and then recompiles it after compiling the rest of the files. It continues in this manner until all files compile successfully or until a file(s) can't be compiled for reasons other than dependency.

Files can be displayed in the Project window in alphabetical or compile order (by clicking the column headings). Keep in mind that the order you see in the Project tab is not necessarily the order in which the files will be compiled.

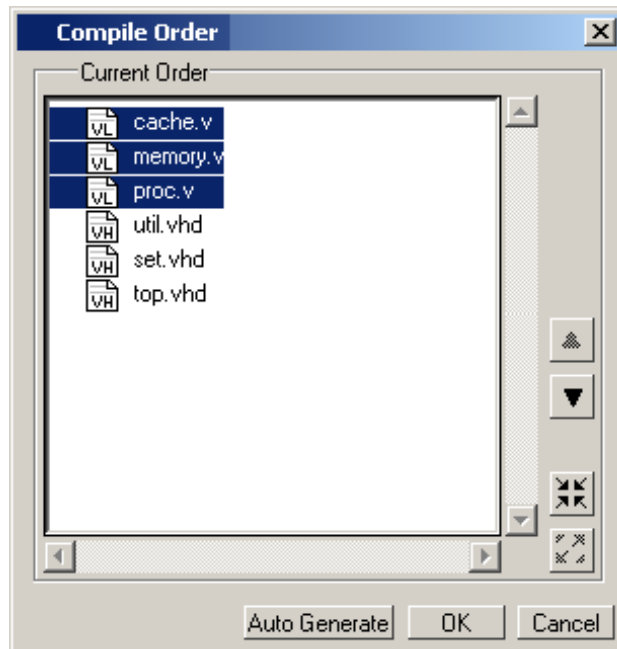
Grouping Files

You can group two or more files in the Compile Order dialog so they are sent to the compiler at the same time. For example, you might have one file with a bunch of Verilog define statements and a second file that is a Verilog module. You would want to compile these two files together.

To group files, follow these steps:

1. Select the files you want to group.

Figure 5-9. Grouping Files



2. Click the Group button.



To ungroup files, select the group and click the Ungroup button.

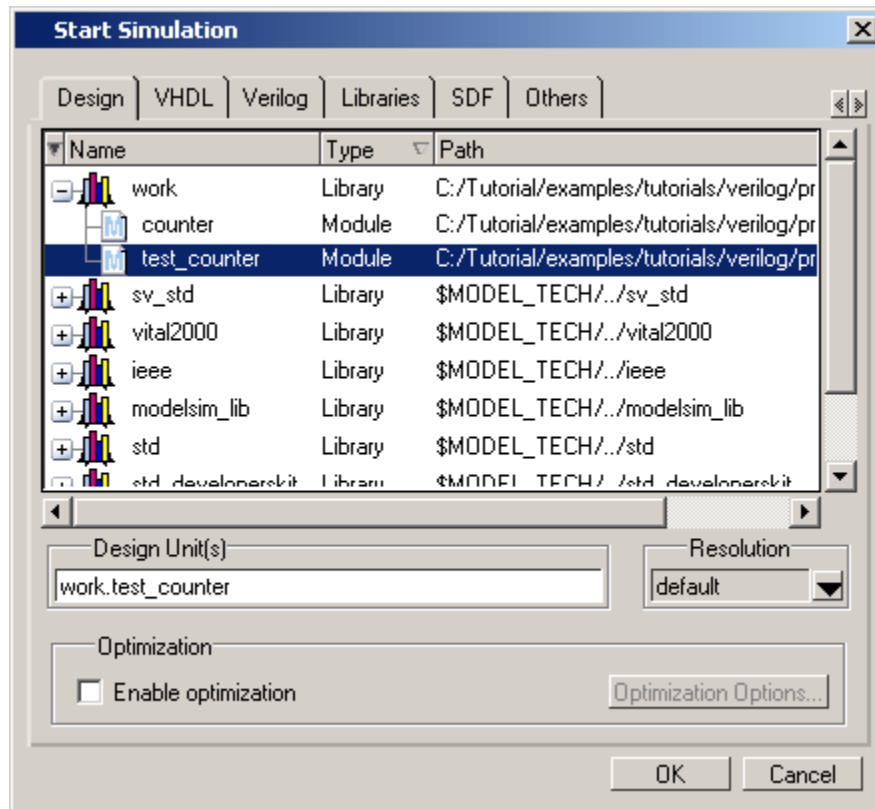


Step 4 — Simulating a Design

To simulate a design, do one of the following:

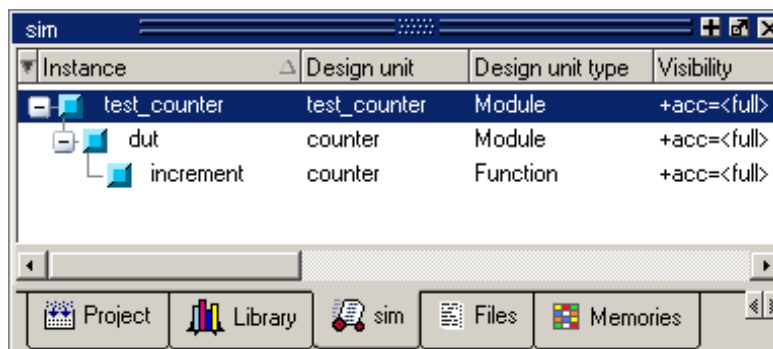
- double-click the Name of an appropriate design object (such as a test bench module or entity) in the Library window
- right-click the Name of an appropriate design object and select **Simulate** from the popup menu
- select **Simulate > Start Simulation** from the menus to open the Start Simulation dialog (Figure 5-10). Select a design unit in the Design tab. Set other options in the VHDL, Verilog, Libraries, SDF, and Others tabs. Then click OK to start the simulation.

Figure 5-10. Start Simulation Dialog



A new Structure window, named *sim*, appears that shows the structure of the active simulation (Figure 5-11).

Figure 5-11. Structure Window with Projects



At this point you are ready to run the simulation and analyze your results. You often do this by adding signals to the Wave window and running the simulation for a given period of time. See the *ModelSim Tutorial* for examples.

Other Basic Project Operations

Open an Existing Project

If you previously exited ModelSim with a project open, ModelSim automatically will open that same project upon startup. You can open a different project by selecting **File > Open** and choosing Project Files from the **Files of type** drop-down.

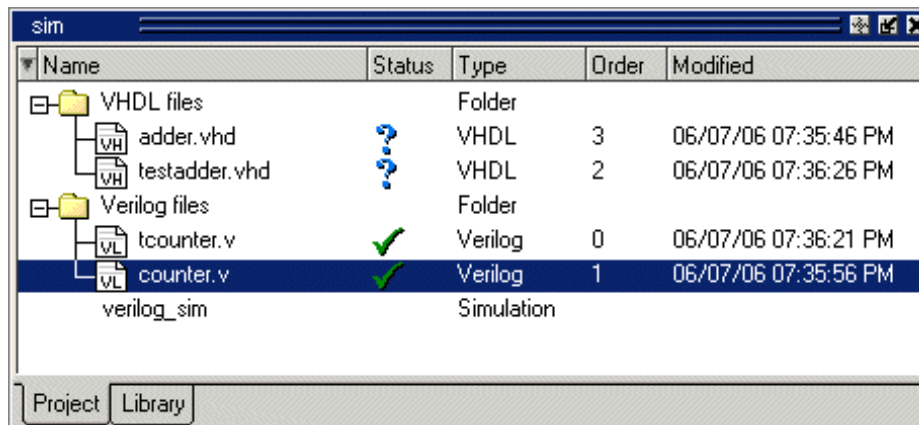
Close a Project

Right-click in the Project window and select **Close Project**. This closes the Project window but leaves the Library window open. Note that you cannot close a project while a simulation is in progress.

The Project Window

The Project window contains information about the objects in your project. By default the window is divided into five columns.

Figure 5-12. Project Window Overview



The screenshot shows a window titled 'sim' with a table of project files. The table has five columns: Name, Status, Type, Order, and Modified. The files are organized into folders: 'VHDL files' and 'Verilog files'. The 'VHDL files' folder contains 'adder.vhd' and 'testadder.vhd'. The 'Verilog files' folder contains 'tcounter.v' and 'counter.v'. The 'verilog_sim' folder is also listed. The 'counter.v' file is highlighted in blue. The 'Status' column shows question marks for the VHDL files, a green checkmark for 'tcounter.v', and a green checkmark with a yellow triangle for 'counter.v'. The 'Type' column shows 'Folder' for the folders and 'VHDL' or 'Verilog' for the files. The 'Order' column shows 3, 2, 0, 1, and 'verilog_sim'. The 'Modified' column shows dates and times for the files.

Name	Status	Type	Order	Modified
VHDL files		Folder		
adder.vhd	?	VHDL	3	06/07/06 07:35:46 PM
testadder.vhd	?	VHDL	2	06/07/06 07:36:26 PM
Verilog files		Folder		
tcounter.v	✓	Verilog	0	06/07/06 07:36:21 PM
counter.v	✓	Verilog	1	06/07/06 07:35:56 PM
verilog_sim		Simulation		

- **Name** – The name of a file or object.
- **Status** – Identifies whether a source file has been successfully compiled. Applies only to VHDL or Verilog files. A question mark means the file hasn't been compiled or the source file has changed since the last successful compile; an X means the compile failed; a check mark means the compile succeeded; a checkmark with a yellow triangle behind it means the file compiled but there were warnings generated.
- **Type** – The file type as determined by registered file types on Windows or the type you specify when you add the file to the project.
- **Order** – The order in which the file will be compiled when you execute a Compile All command.

- **Modified** – The date and time of the last modification to the file.

You can hide or show columns by right-clicking on a column title and selecting or deselecting entries.

Sorting the List

You can sort the list by any of the five columns. Click on a column heading to sort by that column; click the heading again to invert the sort order. An arrow in the column heading indicates which field the list is sorted by and whether the sort order is descending (down arrow) or ascending (up arrow).

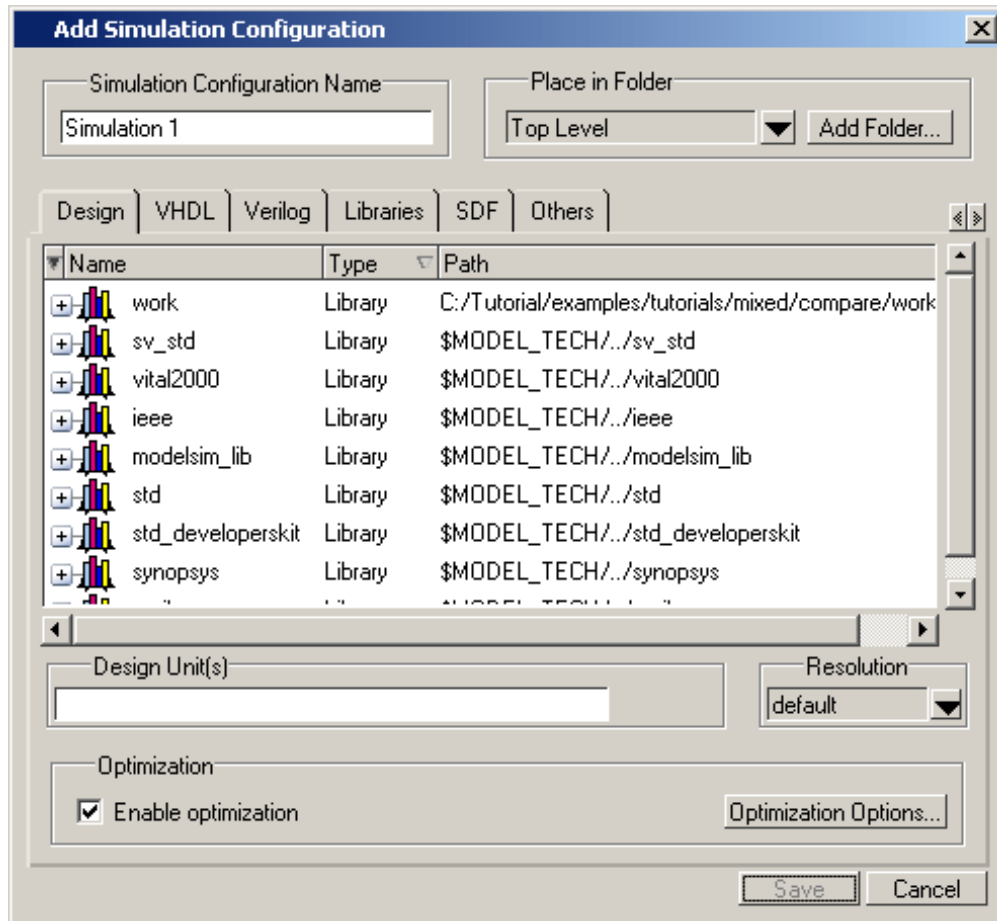
Creating a Simulation Configuration

A Simulation Configuration associates a design unit(s) and its simulation options. For example, assume you routinely load a particular design and you also have to specify the simulator resolution limit, generics, and SDF timing files. Ordinarily you would have to specify those options each time you load the design. With a Simulation Configuration, you would specify the design and those options and then save the configuration with a name (for example, *top_config*). The name is then listed in the Project tab and you can double-click it to load the design along with its options.

To create a Simulation Configuration, follow these steps:

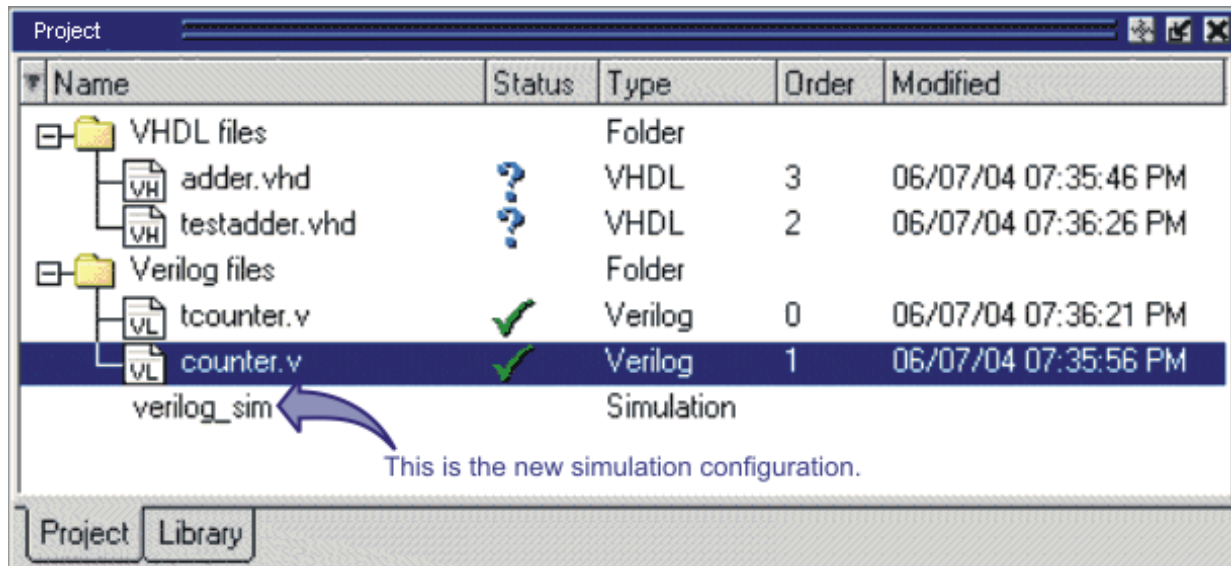
1. Select **Project > Add to Project > Simulation Configuration** from the main menu, or right-click the Project tab and select **Add to Project > Simulation Configuration** from the popup context menu in the Project window.

Figure 5-13. Add Simulation Configuration Dialog



2. Specify a name in the **Simulation Configuration Name** field.
 3. Specify the folder in which you want to place the configuration (see [Organizing Projects with Folders](#)).
 4. Select one or more design unit(s). Use the Control and/or Shift keys to select more than one design unit. The design unit names appear in the **Simulate** field when you select them.
 5. Use the other tabs in the dialog to specify any required simulation options.
- Click **OK** and the simulation configuration is added to the Project window.

Figure 5-14. Simulation Configuration in the Project Window



Double-click the Simulation Configuration *verilog_sim* to load the design.

Optimization Configurations

Similar to Simulation Configurations, Optimization Configurations are named objects that represent an optimized simulation. The process for creating and using them is similar to that for Simulation Configurations (see above). You create them by selecting **Project > Add to Project > Optimization Configuration** and specifying various options in a dialog.

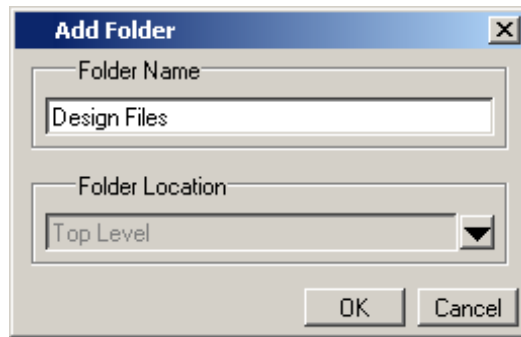
Organizing Projects with Folders

The more files you add to a project, the harder it can be to locate the item you need. You can add "folders" to the project to organize your files. These folders are akin to directories in that you can have multiple levels of folders and sub-folders. However, no actual directories are created via the file system—the folders are present only within the project file.

Adding a Folder

To add a folder to your project, select **Project > Add to Project > Folder** or right-click in the Project window and select **Add to Project > Folder** (Figure 5-15).

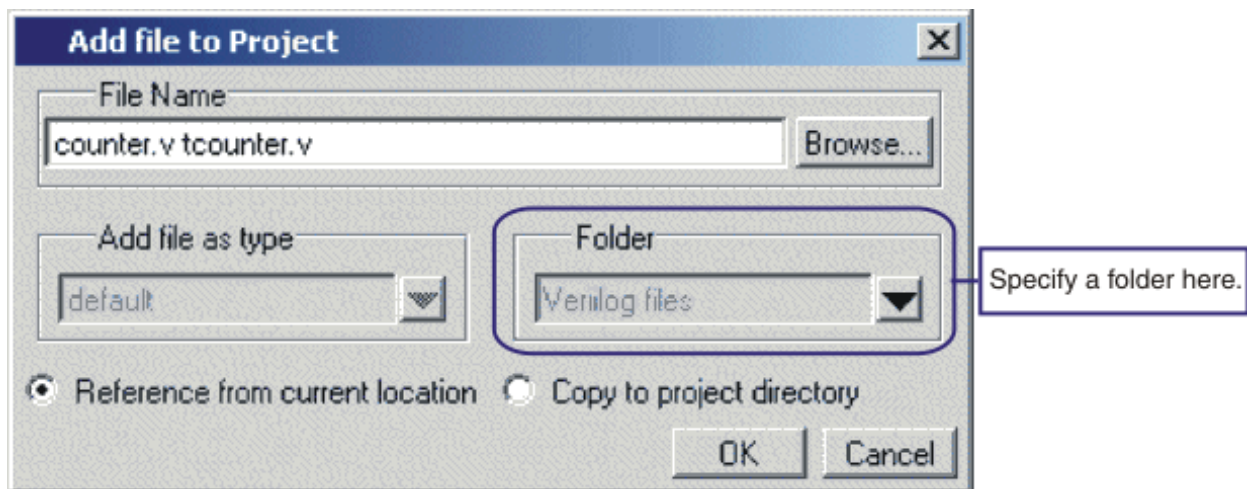
Figure 5-15. Add Folder Dialog



Specify the Folder Name, the location for the folder, and click **OK**. The folder will be displayed in the Project tab.

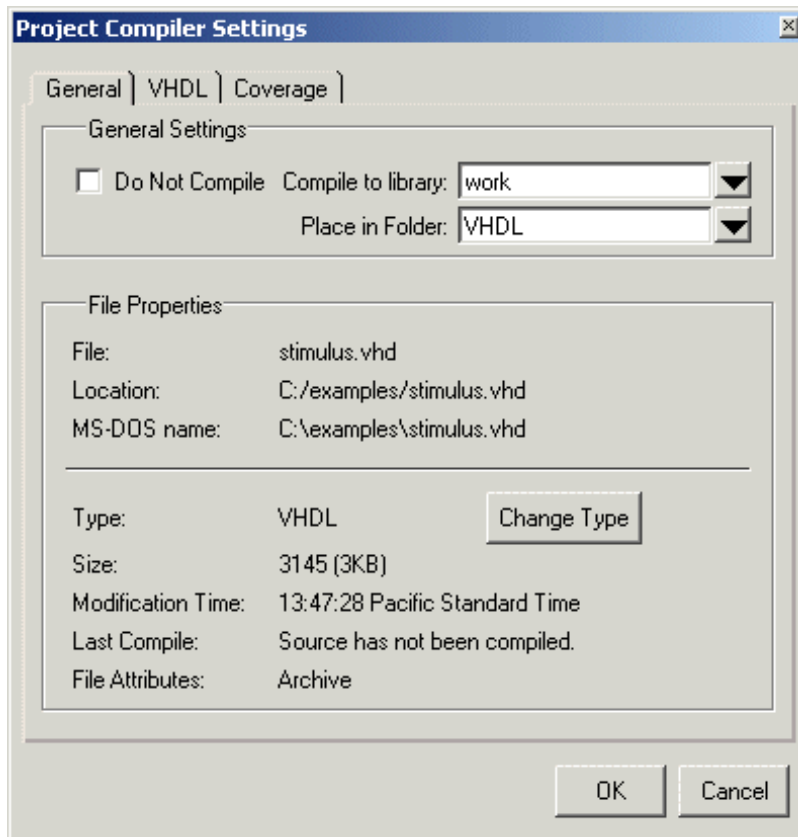
You use the folders when you add new objects to the project. For example, when you add a file, you can select which folder to place it in.

Figure 5-16. Specifying a Project Folder



If you want to move a file into a folder later on, you can do so using the Properties dialog for the file. Simply right-click on the filename in the Project window and select Properties from the context menu that appears. This will open the Project Compiler Settings Dialog (Figure 5-17). Use the Place in Folder field to specify a folder.

Figure 5-17. Project Compiler Settings Dialog



On Windows platforms, you can also just drag-and-drop a file into a folder.

Specifying File Properties and Project Settings

You can set two types of properties in a project: file properties and project settings. File properties affect individual files; project settings affect the entire project.

File Compilation Properties

The VHDL and Verilog compilers (**vcom** and **vlog**, respectively) have numerous options that affect how a design is compiled and subsequently simulated. You can customize the settings on individual files or a group of files.

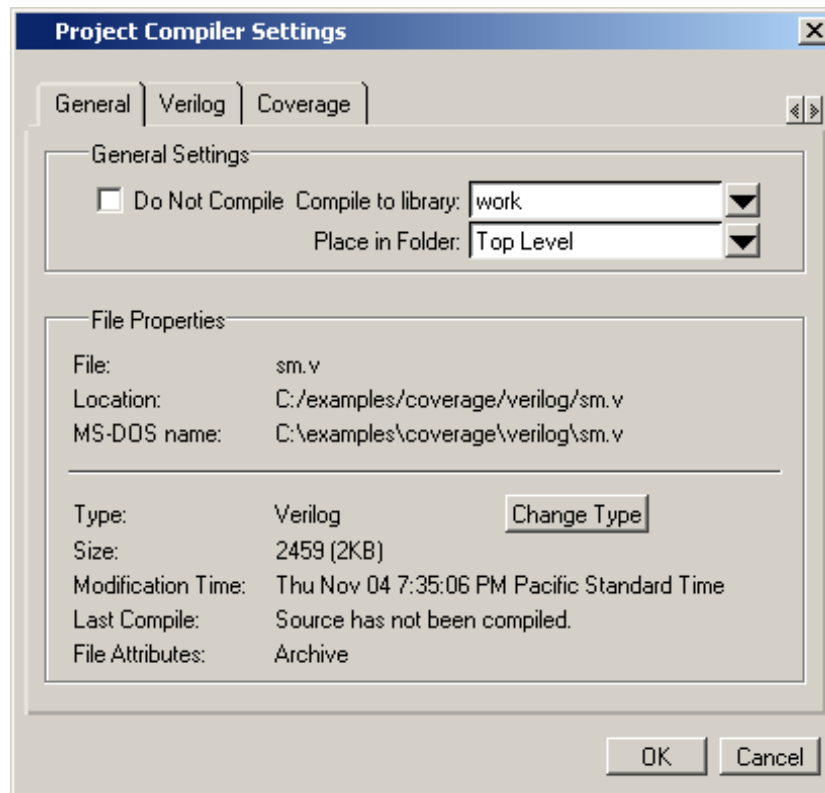
Note



Any changes you make to the compile properties outside of the project, whether from the command line, the GUI, or the *modelsim.ini* file, *will not* affect the properties of files already in the project.

To customize specific files, select the file(s) in the Project window, right click on the file names, and select **Properties**. The resulting Project Compiler Settings dialog (Figure 5-18) varies depending on the number and type of files you have selected. If you select a single VHDL or Verilog file, you will see the General tab, Coverage tab, and the VHDL or Verilog tab, respectively. If you select a SystemC file, you will see only the General tab. On the General tab, you will see file properties such as Type, Location, and Size. If you select multiple files, the file properties on the General tab are not listed. Finally, if you select both a VHDL file and a Verilog file, you will see all tabs but no file information on the General tab.

Figure 5-18. Specifying File Properties



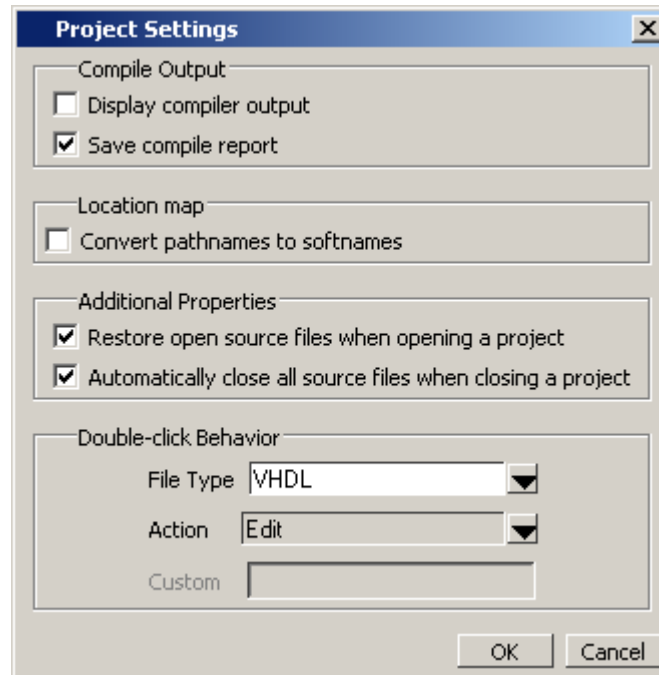
When setting options on a group of files, keep in mind the following:

- If two or more files have different settings for the same option, the checkbox in the dialog will be "grayed out." If you change the option, you cannot change it back to a "multi- state setting" without cancelling out of the dialog. Once you click OK, ModelSim will set the option the same for all selected files.
- If you select a combination of VHDL and Verilog files, the options you set on the VHDL and Verilog tabs apply only to those file types.

Project Settings

To modify project settings, right-click anywhere within the Project tab and select **Project Settings**.

Figure 5-19. Project Settings Dialog



Converting Pathnames to Softnames for Location Mapping

If you are using location mapping, you can convert the following into a soft pathname:

- a relative pathname
- full pathname
- pathname with an environment variable



Tip: A softname is a term for a pathname that uses location mapping with `MGC_LOCATION_MAP`. The soft pathname looks like a pathname containing an environment variable, it locates the source using the location map rather than the environment.

To convert the pathname to a softname for projects using location mapping, follow these steps:

1. Right-click anywhere within the Project tab and select **Project Settings**
2. Enable the **Convert pathnames to softnames** within the Location map area of the **Project Settings** dialog box (Figure 5-19).

Once enabled, all pathnames currently in the project and any that are added later are then converted to softnames.

During conversion, if there is no softname in the mgc location map matching the entry, the pathname is converted in to a full (hardened) pathname. A pathname is hardened by removing the environment variable or the relative portion of the path. If this happens, any existing pathnames that are either relative or use environment variables are also changed: either to softnames if possible, or to hardened pathnames if not.

For more information on location mapping and pathnames, see [Using Location Mapping](#).

Accessing Projects from the Command Line

Generally, projects are used from within the ModelSim GUI. However, standalone tools will use the project file if they are invoked in the project's root directory. If you want to invoke outside the project directory, set the **MODELSIM** environment variable with the path to the project file (*<Project_Root_Dir>/<Project_Name>.mpf*).

You can also use the [project](#) command from the command line to perform common operations on projects.

VHDL designs are associated with libraries, which are objects that contain compiled design units. SystemC, Verilog and SystemVerilog designs simulated within ModelSim are compiled into libraries as well.

Design Library Overview

A *design library* is a directory or archive that serves as a repository for compiled design units. The design units contained in a design library consist of VHDL entities, packages, architectures, and configurations; Verilog modules and UDPs (user-defined primitives); and SystemC modules. The design units are classified as follows:

- **Primary design units** — Consist of entities, package declarations, configuration declarations, modules, UDPs, and SystemC modules. Primary design units within a given library must have unique names.
- **Secondary design units** — Consist of architecture bodies, package bodies, and optimized Verilog modules. Secondary design units are associated with a primary design unit. Architectures by the same name can exist if they are associated with different entities or modules.

Design Unit Information

The information stored for each design unit in a design library is:

- retargetable, executable code
- debugging information
- dependency information

Working Library Versus Resource Libraries

Design libraries can be used in two ways:

1. as a local working library that contains the compiled version of your design;
2. as a resource library.

The contents of your working library will change as you update your design and recompile. A resource library is typically static and serves as a parts source for your design. You can create

your own resource libraries or they may be supplied by another design team or a third party (for example, a silicon vendor).

Only one library can be the working library.

Any number of libraries can be resource libraries during a compilation. You specify which resource libraries will be used when the design is compiled, and there are rules to specify in which order they are searched (refer to [Specifying Resource Libraries](#)).

A common example of using both a working library and a resource library is one in which your gate-level design and test bench are compiled into the working library and the design references gate-level models in a separate resource library.

The Library Named "work"

The library named "work" has special attributes within ModelSim — it is predefined in the compiler and need not be declared explicitly (that is, **library work**). It is also the library name used by the compiler as the default destination of compiled design units (that is, it does not need to be mapped). In other words, the **work** library is the default *working* library.

Archives

By default, design libraries are stored in a directory structure with a sub-directory for each design unit in the library. Alternatively, you can configure a design library to use archives. In this case, each design unit is stored in its own archive file. To create an archive, use the `-archive` argument to the `vlib` command.

Generally you would do this only in the rare case that you hit the reference count limit on I-nodes due to the `..` entries in the lower-level directories (the maximum number of sub-directories on UNIX and Linux is 65533). An example of an error message that is produced when this limit is hit is:

```
mkdir: cannot create directory `65534': Too many links
```

Archives may also have limited value to customers seeking disk space savings.

Working with Design Libraries

The implementation of a design library is not defined within standard VHDL or Verilog. Within ModelSim, design libraries are implemented as directories and can have any legal name allowed by the operating system, with one exception: extended identifiers are not supported for library names.

Creating a Library

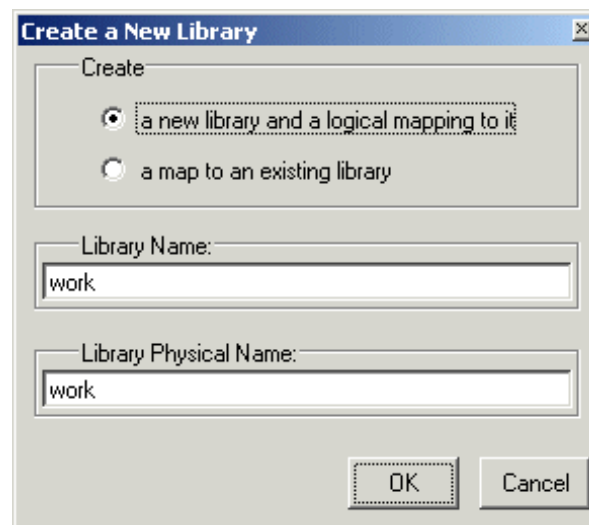
When you create a project (refer to [Getting Started with Projects](#)), ModelSim automatically creates a working design library. If you don't create a project, you need to create a working design library before you run the compiler. This can be done from either the command line or from the ModelSim graphic interface.

From the ModelSim prompt or a UNIX/DOS prompt, use this `vlib` command:

```
vlib <directory_pathname>
```

To create a new library with the graphic interface, select **File > New > Library**.


Figure 6-1. Creating a New Library



When you click **OK**, ModelSim creates the specified library directory and writes a specially-formatted file named `_info` into that directory. The `_info` file must remain in the directory to distinguish it as a ModelSim library.

The new map entry is written to the `modelsim.ini` file in the [Library] section. Refer to [modelsim.ini Variables](#) for more information.

Note

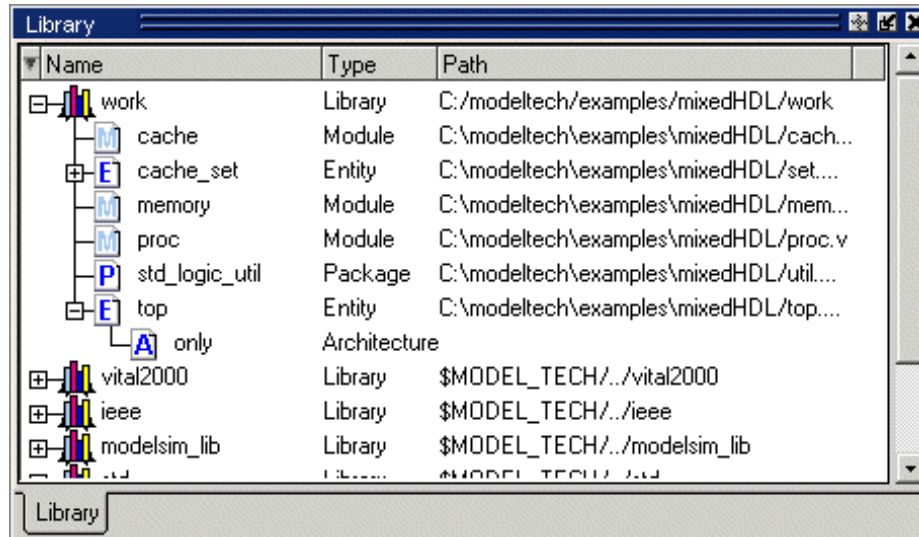
 Remember that a design library is a special kind of directory. The **only** way to create a library is to use the ModelSim GUI or the `vlib` command. Do not try to create libraries using UNIX, DOS, or Windows commands.

Managing Library Contents

Library contents can be viewed, deleted, recompiled, edited and so on using either the graphic interface or command line.

The Library window provides access to design units (configurations, modules, packages, entities, architectures, and SystemC modules) in a library. Various information about the design units is displayed in columns to the right of the design unit name.

Figure 6-2. Design Unit Information in the Workspace



The Library window has a popup menu with various commands that you access by clicking your right mouse button.

The context menu includes the following commands:

- **Simulate** — Loads the selected design unit and opens Structure (sim) and Files windows. Related command line command is [vsim](#).
- **Simulate with Coverage** — Loads the selected design unit and collects code coverage data. Related command line command is [vsim -coverage](#).
- **Edit** — Opens the selected design unit in the Source window; or, if a library is selected, opens the Edit Library Mapping dialog (refer to [Library Mappings with the GUI](#)).
- **Refresh** — Rebuilds the library image of the selected library without using source code. Related command line command is [vcom](#) or [vlog](#) with the -refresh argument.
- **Recompile** — Recompiles the selected design unit. Related command line command is [vcom](#) or [vlog](#).
- **Optimize** — Optimizes a Verilog design unit. Related command line command is [vopt](#).
- **Update** — Updates the display of available libraries and design units.

Assigning a Logical Name to a Design Library

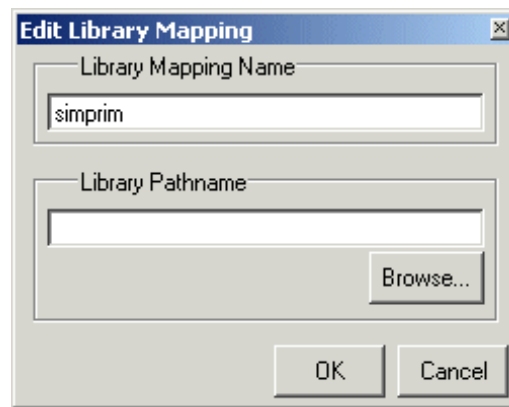
VHDL uses logical library names that can be mapped to ModelSim library directories. By default, ModelSim can find libraries in your current directory (assuming they have the right name), but for it to find libraries located elsewhere, you need to map a logical library name to the pathname of the library.

You can use the GUI, a command, or a project to assign a logical name to a design library.

Library Mappings with the GUI

To associate a logical name with a library, select the library in the Library window, right-click your mouse, and select **Edit** from the context menu that appears. This brings up a dialog box that allows you to edit the mapping.

Figure 6-3. Edit Library Mapping Dialog



The dialog box includes these options:

- **Library Mapping Name** — The logical name of the library.
- **Library Pathname** — The pathname to the library.

Library Mapping from the Command Line

You can set the mapping between a logical library name and a directory with the `vmap` command using the following syntax:

```
vmap <logical_name> <directory_pathname>
```

You may invoke this command from either a UNIX/DOS prompt or from the command line within ModelSim.

The `vmap` command adds the mapping to the library section of the `modelsim.ini` file. You can also modify `modelsim.ini` manually by adding a mapping line. To do this, use a text editor and add a line under the [Library] section heading using the syntax:

```
<logical_name> = <directory_pathname>
```

More than one logical name can be mapped to a single directory. For example, suppose the *modelsim.ini* file in the current working directory contains following lines:

```
[Library]
work = /usr/rick/design
my_asic = /usr/rick/design
```

This would allow you to use either the logical name **work** or **my_asic** in a **library** or **use** clause to refer to the same design library.

Unix Symbolic Links

You can also create a UNIX symbolic link to the library using the host platform command:

```
ln -s <directory_pathname> <logical_name>
```

The **vmap** command can also be used to display the mapping of a logical library name to a directory. To do this, enter the shortened form of the command:

```
vmap <logical_name>
```

Library Search Rules

The system searches for the mapping of a logical name in the following order:

- First the system looks for a *modelsim.ini* file.
- If the system doesn't find a *modelsim.ini* file, or if the specified logical name does not exist in the *modelsim.ini* file, the system searches the current working directory for a subdirectory that matches the logical name.

An error is generated by the compiler if you specify a logical name that does not resolve to an existing directory.

Moving a Library

Individual design units in a design library cannot be moved. An *entire* design library can be moved, however, by using standard operating system commands for moving a directory or an archive.

Setting Up Libraries for Group Use

By adding an “others” clause to your *modelsim.ini* file, you can have a hierarchy of library mappings. If the tool does not find a mapping in the *modelsim.ini* file, then it will search the [library] section of the initialization file specified by the “others” clause. For example:

```
[library]
```

```
asic_lib = /cae/asic_lib
work = my_work
others = /usr/modeltech/modelsim.ini
```

You can specify only one "others" clause in the library section of a given *modelsim.ini* file.

The "others" clause only instructs the tool to look in the specified *modelsim.ini* file for a library. It does not load any other part of the specified file.

If there are two libraries with the same name mapped to two different locations – one in the current *modelsim.ini* file and the other specified by the "others" clause – the mapping specified in the current *.ini* file will take effect.

Specifying Resource Libraries

Verilog Resource Libraries

ModelSim supports separate compilation of distinct portions of a Verilog design. The [vlog](#) compiler is used to compile one or more source files into a specified library. The library thus contains pre-compiled modules and UDPs that are referenced by the simulator as it loads the design.

Resource libraries are specified differently for Verilog and VHDL. For Verilog you use either the `-L` or `-Lf` argument to [vlog](#). Refer to [Library Usage](#) for more information.

The [LibrarySearchPath](#) variable in the *modelsim.ini* file (in the [vlog] section) can be used to define a space-separated list of resource library paths. This is identical behavior with the `-L` argument for the [vlog](#) command.

```
LibrarySearchPath = <path>/lib1 <path>/lib2 <path>/lib3
```

The default for [LibrarySearchPath](#) is `$MODEL_TECH/./avm`.

VHDL Resource Libraries

Within a VHDL source file, you use the VHDL **library** clause to specify logical names of one or more resource libraries to be referenced in the subsequent design unit. The scope of a **library** clause includes the text region that starts immediately after the **library** clause and extends to the end of the declarative region of the associated design unit. *It does not extend to the next design unit in the file.*

Note that the **library** clause is not used to specify the working library into which the design unit is placed after compilation. The [vcom](#) command adds compiled design units to the current working library. By default, this is the library named **work**. To change the current working library, you can use [vcom -work](#) and specify the name of the desired target library.

Predefined Libraries

Certain resource libraries are predefined in standard VHDL. The library named **std** contains the packages **standard**, **env**, and **textio**, which should not be modified. The contents of these packages and other aspects of the predefined language environment are documented in the *IEEE Standard VHDL Language Reference Manual, Std 1076*. Refer also to, [Using the TextIO Package](#).

A VHDL **use** clause can be specified to select particular declarations in a library or package that are to be visible within a design unit during compilation. A **use** clause references the compiled version of the package—not the source.

By default, every VHDL design unit is assumed to contain the following declarations:

```
LIBRARY std, work;  
USE std.standard.all
```

To specify that all declarations in a library or package can be referenced, add the suffix *.all* to the library/package name. For example, the **use** clause above specifies that all declarations in the package *standard*, in the design library named *std*, are to be visible to the VHDL design unit immediately following the **use** clause. Other libraries or packages are not visible unless they are explicitly specified using a **library** or **use** clause.

Another predefined library is **work**, the library where a design unit is stored after it is compiled as described earlier. There is no limit to the number of libraries that can be referenced, but only one library is modified during compilation.

Alternate IEEE Libraries Supplied

The installation directory may contain two or more versions of the IEEE library:

- *ieeepure* — Contains only IEEE approved packages (accelerated for ModelSim).
- *ieee* — Contains precompiled Synopsys and IEEE arithmetic packages which have been accelerated for ModelSim including *math_complex*, *math_real*, *numeric_bit*, *numeric_std*, *std_logic_1164*, *std_logic_misc*, *std_logic_textio*, *std_logic_arith*, *std_logic_signed*, *std_logic_unsigned*, *vital_primitives*, and *vital_timing*.

You can select which library to use by changing the mapping in the *modelsim.ini* file. The *modelsim.ini* file in the installation directory defaults to the *ieee* library.

Rebuilding Supplied Libraries

Resource libraries are supplied precompiled in the installation directory. If you need to rebuild these libraries, the sources are provided in the *vhdl_src* directory; a macro file is also provided for Windows platforms (*rbldlibs.do*). To rebuild the libraries, invoke the DO file from within ModelSim with this command:

do rblldlibs.do

Make sure your current directory is the install directory before you run this file.

Note

Because accelerated subprograms require attributes that are available only under the 1993 standard, many of the libraries are built using [vcom](#) with the **-93** option.

Shell scripts are provided for UNIX (*rebuild_libs.csh* and *rebuild_libs.sh*). To rebuild the libraries, execute one of the *rebuild_libs* scripts while in the *modeltech* directory.

Regenerating Your Design Libraries

Depending on your current ModelSim version, you may need to regenerate your design libraries before running a simulation. Check the installation README file to see if your libraries require an update. You can regenerate your design libraries using the **Refresh** command from the Library tab context menu (refer to [Managing Library Contents](#)), or by using the `-refresh` argument to [vcom](#) and [vlog](#).

From the command line, you would use [vcom](#) with the `-refresh` argument to update VHDL design units in a library, and [vlog](#) with the `-refresh` argument to update Verilog design units. By default, the work library is updated. Use either **vcom** or **vlog** with the `-work <library>` argument to update a different library. For example, if you have a library named *mylib* that contains both VHDL and Verilog design units:

```
vcom -work mylib -refresh
```

```
vlog -work mylib -refresh
```

Note

You may specify a specific design unit name with the `-refresh` argument to [vcom](#) and [vlog](#) in order to regenerate a library image for only that design, but you may not specify a file name.

An important feature of **-refresh** is that it rebuilds the library image without using source code. This means that models delivered as compiled libraries without source code can be rebuilt for a specific release of ModelSim. In general, this works for moving forwards or backwards on a release. Moving backwards on a release may not work if the models used compiler switches, directives, language constructs, or features that do not exist in the older release.

Note

You don't need to regenerate the *std*, *ieee*, *vital22b*, and *verilog* libraries. Also, you cannot use the **-refresh** option to update libraries that were built before the 4.6 release.

Maintaining 32- and 64-bit Versions in the Same Library

ModelSim allows you to maintain 32-bit and 64-bit versions of a design in the same library, as long as you have not optimized them using the `vopt` command.

To do this, you must compile the design with the 32-bit version and then "refresh" the design with the 64-bit version. For example:

Using the 32-bit version of ModelSim:

```
vlog -novopt file1.v file2.v -work asic_lib
```

Next, using the 64-bit version of ModelSim:

```
vlog -novopt -work asic_lib -refresh
```

This allows you to use either version without having to do a refresh.

Do not compile the design with one version, and then recompile it with the other. If you do this, ModelSim will remove the first module, because it could be "stale."

Importing FPGA Libraries

ModelSim includes an import wizard for referencing and using vendor FPGA libraries. The wizard scans for and enforces dependencies in the libraries and determines the correct mappings and target directories.

Note



The FPGA libraries you import must be pre-compiled. Most FPGA vendors supply pre-compiled libraries configured for use with ModelSim.

To import an FPGA library, select **File > Import > Library**.

Figure 6-4. Import Library Wizard

Follow the instructions in the wizard to complete the import.

Protecting Source Code

The [Protecting Your Source Code](#) chapter provides details about protecting your internal model data. This allows a model supplier to provide pre-compiled libraries without providing source code and without revealing internal model variables and structure.

Chapter 7

VHDL Simulation

This chapter covers the following topics related to using VHDL in a ModelSim design:

- [Basic VHDL Usage](#) — A brief outline of the steps for using VHDL in a ModelSim design.
- [Compilation and Simulation of VHDL](#) — How to compile, optimize, and simulate a VHDL design
- [Using the TextIO Package](#) — Using the TextIO package provided with ModelSim
- [VITAL Usage and Compliance](#) — Implementation of the VITAL (VHDL Initiative Towards ASIC Libraries) specification for ASIC modeling
- [VHDL Utilities Package \(util\)](#) — Using the special built-in utilities package (Util Package) provided with ModelSim
- [Modeling Memory](#) — The advantages of using VHDL variables or protected types instead of signals for memory designs.

Basic VHDL Usage

Simulating VHDL designs with ModelSim consists of the following general steps:

1. Compile your VHDL code into one or more libraries using the [vcom](#) command. Refer to [Compiling a VHDL Design—the vcom Command](#) for more information.
2. (Optional) Elaborate and optimize your design using the [vopt](#) command. Refer to Chapter 4, [Optimizing Designs with vopt](#) for more information.
3. Load your design with the [vsim](#) command. Refer to [Simulating a VHDL Design](#).
4. Simulate the loaded design, then debug as needed.

Compilation and Simulation of VHDL

Creating a Design Library for VHDL

Before you can compile your VHDL source files, you must create a library in which to store the compilation results. Use [vlib](#) to create a new library. For example:

```
vlib work
```

This creates a library named work. By default, compilation results are stored in the work library.

The work library is actually a subdirectory named work. This subdirectory contains a special file named `_info`. Do not create a VHDL library as a directory by using a UNIX, Linux, Windows, or DOS command—always use the `vlib` command.

See [Design Libraries](#) for additional information on working with VHDL libraries.

Compiling a VHDL Design—the `vcom` Command

ModelSim compiles one or more VHDL design units with a single invocation of the `vcom` command, the VHDL compiler. The design units are compiled in the order that they appear on the command line. For VHDL, the order of compilation is important—you must compile any entities or configurations before an architecture that references them.

You can simulate a design written with the following versions of VHDL:

- 1076-1987
- 1076-1993
- 1076-2002
- 1076-2008

To do so you need to compile units from each VHDL version separately.

The `vcom` command compiles using 1076-2002 rules by default; use the `-87`, `-93`, or `-2008` arguments to `vcom` to compile units written with version 1076-1987, 1076-1993, or 1076-2008 respectively. You can also change the default by modifying the `VHDL93` variable in the `modelsim.ini` file (see [modelsim.ini Variables](#) for more information).

Note



Only a limited number of VHDL 1076-2008 constructs are currently supported.

Dependency Checking

You must re-analyze dependent design units when you change the design units they depend on in the library. The `vcom` command determines whether or not the compilation results have changed.

For example, if you keep an entity and its architectures in the same source file and you modify only an architecture and recompile the source file, the entity compilation results will remain unchanged. This means you do not have to recompile design units that depend on the entity.

Range and Index Checking

A range check verifies that a scalar value defined with a range subtype is always assigned a value within its range. An index check verifies that whenever an array subscript expression is evaluated, the subscript will be within the array's range.

Range and index checks are performed by default when you compile your design. You can disable range checks (potentially offering a performance advantage) and index checks using arguments to the `vcom` command. Or, you can use the `NoRangeCheck` and `NoIndexCheck` variables in the `modelsim.ini` file to specify whether or not they are performed. See [modelsim.ini Variables](#).

Range checks in ModelSim are slightly more restrictive than those specified by the VHDL Language Reference Manual (LRM). ModelSim requires any assignment to a signal to also be in range whereas the LRM requires only that range checks be done whenever a signal is updated. Most assignments to signals update the signal anyway, and the more restrictive requirement allows ModelSim to generate better error messages.

Subprogram Inlining

ModelSim attempts to inline subprograms at compile time to improve simulation performance. This happens automatically and should be largely transparent. However, you can disable automatic inlining two ways:

- Invoke `vcom` with the `-O0` or `-O1` argument
- Use the `mti_inhibit_inline` attribute as described below

Single-stepping through a simulation varies slightly, depending on whether inlining occurred. When single-stepping to a subprogram call that has not been inlined, the simulator stops first at the line of the call, and then proceeds to the line of the first executable statement in the called subprogram. If the called subprogram has been inlined, the simulator does not first stop at the subprogram call, but stops immediately at the line of the first executable statement.

`mti_inhibit_inline` Attribute

You can disable inlining for individual design units (a package, architecture, or entity) or subprograms with the `mti_inhibit_inline` attribute. Follow these rules to use the attribute:

- Declare the attribute within the design unit's scope as follows:

```
attribute mti_inhibit_inline : boolean;
```

- Assign the value `true` to the attribute for the appropriate scope. For example, to inhibit inlining for a particular function (for example, "foo"), add the following attribute assignment:

```
attribute mti_inhibit_inline of foo : procedure is true;
```

To inhibit inlining for a particular package (for example, "pack"), add the following attribute assignment:

```
attribute mti_inhibit_inline of pack : package is true;
```

Do similarly for entities and architectures.

Simulating a VHDL Design

A VHDL design is ready for simulation after it has been compiled with `vcom` and possibly optimized with `vopt` (see [Optimizing Designs with vopt](#)). You can then use the `vsim` command to invoke the simulator with the name of the configuration or entity/architecture pair or the name you assigned to the optimized version of the design.

Note



This section discusses simulation from the UNIX or Windows/DOS command line. You can also use a project to simulate (see [Getting Started with Projects](#)) or the **Start Simulation** dialog box (open with **Simulate > Start Simulation** menu selection).

This example begins simulation on a design unit with an entity named **my_asic** and an architecture named **structure**:

```
vsim my_asic structure
```

Timing Specification

The `vsim` command can annotate a design using VITAL-compliant models with timing data from an SDF file. You can specify delay by invoking `vsim` with the `-sdfmin`, `-sdftyp`, or `-sdfmax` arguments. The following example uses an SDF file named `f1.sdf` in the current work directory, and an invocation of `vsim` annotating maximum timing values for the design unit `my_asic`:

```
vsim -sdfmax /my_asic=f1.sdf my_asic
```

By default, the timing checks within VITAL models are enabled. You can disable them with the **+notimingchecks** argument. For example:

```
vsim +notimingchecks topmod
```

If you specify `vsim +notimingchecks`, the generic `TimingChecksOn` is set to `FALSE` for all VITAL models with the `Vital_level0` or `Vital_level1` attribute (refer to [VITAL Usage and Compliance](#)). Setting this generic to `FALSE` disables the actual calls to the timing checks along with anything else that is present in the model's timing check block. In addition, if these models use the generic `TimingChecksOn` to control behavior beyond timing checks, this behavior will not occur. This can cause designs to simulate differently and provide different results.

By default, `vopt` does not fix the `TimingChecksOn` generic in VITAL models. Instead, it lets the value float to allow for overriding at simulation time. If best performance and no timing checks are desired, `+notimingchecks` should be specified with `vopt`.

```
vopt +notimingchecks topmod
```

Specifying `vopt +notimingchecks` or `-GTimingChecks=<FALSE/TRUE>` will fix the generic value for simulation. As a consequence, using `vsim +notimingchecks` at simulation may not have any effect on the simulation depending on the optimization of the model.

Differences Between Versions of VHDL

There are three versions of the IEEE VHDL 1076 standard: VHDL-1987, VHDL-1993, and VHDL-2002. The default language version for ModelSim is VHDL-2002. If your code was written according to the 1987 or 1993 version, you may need to update your code or instruct ModelSim to use the earlier versions' rules.

To select a specific language version, do one of the following:

- Select the appropriate version from the compiler options menu in the GUI
- Invoke `vcom` using the argument `-87`, `-93`, or `-2002`
- Set the `VHDL93` variable in the `[vcom]` section of the `modelsim.ini` file. Appropriate values for `VHDL93` are:
 - 0, 87, or 1987 for VHDL-1987
 - 1, 93, or 1993 for VHDL-1993
 - 2, 02, or 2002 for VHDL-2002

The following is a list of language incompatibilities that may cause problems when compiling a design.

- VHDL-93 and VHDL-2002 — The only major problem between VHDL-93 and VHDL-2002 is the addition of the keyword "PROTECTED". VHDL-93 programs which use this as an identifier should choose a different name.

All other incompatibilities are between VHDL-87 and VHDL-93.

- VITAL and SDF — It is important to use the correct language version for VITAL. VITAL2000 must be compiled with VHDL-93 or VHDL-2002. VITAL95 must be compiled with VHDL-87. A typical error message that indicates the need to compile under language version VHDL-87 is:

```
"VITALPathDelay DefaultDelay parameter must be locally static"
```

- Purity of NOW — In VHDL-93 the function "now" is impure. Consequently, any function that invokes "now" must also be declared to be impure. Such calls to "now" occur in VITAL. A typical error message:

```
"Cannot call impure function 'now' from inside pure function
'<name>' "
```

- Files — File syntax and usage changed between VHDL-87 and VHDL-93. In many cases vcom issues a warning and continues:

```
"Using 1076-1987 syntax for file declaration."
```

In addition, when files are passed as parameters, the following warning message is produced:

```
"Subprogram parameter name is declared using VHDL 1987 syntax."
```

This message often involves calls to `endfile(<name>)` where `<name>` is a file parameter.

- Files and packages — Each package header and body should be compiled with the same language version. Common problems in this area involve files as parameters and the size of type CHARACTER. For example, consider a package header and body with a procedure that has a file parameter:

```
procedure procl ( out_file : out std.textio.text) ...
```

If you compile the package header with VHDL-87 and the body with VHDL-93 or VHDL-2002, you will get an error message such as:

```
"** Error: mixed_package_b.vhd(4): Parameter kinds do not conform
between declarations in package header and body: 'out_file'."
```

- Direction of concatenation — To solve some technical problems, the rules for direction and bounds of concatenation were changed from VHDL-87 to VHDL-93. You won't see any difference in simple variable/signal assignments such as:

```
v1 := a & b;
```

But if you (1) have a function that takes an unconstrained array as a parameter, (2) pass a concatenation expression as a formal argument to this parameter, and (3) the body of the function makes assumptions about the direction or bounds of the parameter, then you will get unexpected results. This may be a problem in environments that assume all arrays have "downto" direction.

- xnor — "xnor" is a reserved word in VHDL-93. If you declare an xnor function in VHDL-87 (without quotes) and compile it under VHDL-2002, you will get an error message like the following:

```
** Error: xnor.vhd(3): near "xnor": expecting: STRING IDENTIFIER
```

- **'FOREIGN' attribute** — In VHDL-93 package STANDARD declares an attribute 'FOREIGN'. If you declare your own attribute with that name in another package, then ModelSim issues a warning such as the following:

```
-- Compiling package foopack

** Warning: foreign.vhd(9): (vcom-1140) VHDL-1993 added a definition
of the attribute foreign to package std.standard. The attribute is
also defined in package 'standard'. Using the definition from
package 'standard'.
```

- **Size of CHARACTER type** — In VHDL-87 type CHARACTER has 128 values; in VHDL-93 it has 256 values. Code which depends on this size will behave incorrectly. This situation occurs most commonly in test suites that check VHDL functionality. It's unlikely to occur in practical designs. A typical instance is the replacement of warning message:

```
"range nul downto del is null"

by

"range nul downto 'ÿ' is null" -- range is nul downto y(umlaut)
```

- **bit string literals** — In VHDL-87 bit string literals are of type bit_vector. In VHDL-93 they can also be of type STRING or STD_LOGIC_VECTOR. This implies that some expressions that are unambiguous in VHDL-87 now become ambiguous in VHDL-93. A typical error message is:

```
** Error: bit_string_literal.vhd(5): Subprogram '=' is ambiguous.
Suitable definitions exist in packages 'std_logic_1164' and
'standard'.
```

- **Sub-element association** — In VHDL-87 when using individual sub-element association in an association list, associating individual sub-elements with NULL is discouraged. In VHDL-93 such association is forbidden. A typical message is:

```
"Formal '<name>' must not be associated with OPEN when subelements
are associated individually."
```

Foreign Language Interface

Foreign language interface (FLI) routines are C programming language functions that provide procedural access to information within the HDL simulator, vsim. A user-written application can use these functions to traverse the hierarchy of an HDL design, get information about and set the values of VHDL objects in the design, get information about a simulation, and control (to some extent) a simulation run.

The ModelSim FLI interface is described in detail in the Foreign Language Interface Reference Manual.

Simulator Resolution Limit for VHDL

The simulator internally represents time as a 64-bit integer in units equivalent to the smallest unit of simulation time, also known as the simulator resolution limit. The default resolution limit is set to the value specified by the [Resolution](#) variable in the *modelsim.ini* file. You can view the current resolution by invoking the [report](#) command with the **simulator state** argument.

Note



In Verilog, this representation of time units is referred to as precision or timescale.

Overriding the Resolution

To override the default resolution of ModelSim, specify a value for the `-t` argument of the **vsim** command line or select a different Simulator Resolution in the **Simulate** dialog box. Available values of simulator resolution are:

1 fs, 10 fs, 100 fs
1 ps, 10 ps, 100 ps
1 ns, 10 ns, 100 ns
1 us, 10 us, 100 us
1 ms, 10 ms, 100 ms
1 s, 10 s, 100 s

For example, the following command sets resolution to 10 ps:

```
vsim -t 10ps topmod
```

Note that you need to take care in specifying a resolution value larger than a delay value in your design—delay values in that design unit are rounded to the closest multiple of the resolution. In the example above, a delay of 4 ps would be rounded down to 0 ps.

Choosing the Resolution for VHDL

You should specify the coarsest value for time resolution that does not result in undesired rounding of your delay times. The resolution value should not be unnecessarily small because it decreases the maximum simulation time limit and can cause longer simulations.

Default Binding

By default, ModelSim performs binding when you load the design with **vsim**. The advantage of this default binding at load time is that it provides more flexibility for compile order. Namely, VHDL entities don't necessarily have to be compiled before other entities/architectures that instantiate them.

However, you can force ModelSim to perform default binding at compile time instead. This may allow you to catch design errors (for example, entities with incorrect port lists) earlier in the flow. Use one of these two methods to change when default binding occurs:

- Specify the **-bindAtCompile** argument to `vcom`
- Set the `BindAtCompile` variable in the `modelsim.ini` to 1 (true)

Default Binding Rules

When searching for a VHDL entity to bind with, ModelSim searches the currently visible libraries for an entity with the same name as the component. ModelSim does this because IEEE Std 1076-1987 contained a flaw that made it almost impossible for an entity to be directly visible if it had the same name as the component. This meant if a component was declared in an architecture, any entity with the same name above that declaration would be hidden because component/entity names cannot be overloaded. As a result, ModelSim observes the following rules for determining default binding:

- If performing default binding at load time, search the libraries specified with the **-Lf** argument to `vsim`.
- If a directly visible entity has the same name as the component, use it.
- If an entity would be directly visible in the absence of the component declaration, use it.
- If the component is declared in a package, search the library that contained the package for an entity with the same name.

If none of these methods is successful, ModelSim then does the following:

- Search the work library.
- Search all other libraries that are currently visible by means of the **library** clause.
- If performing default binding at load time, search the libraries specified with the **-L** argument to `vsim`.

Note that these last three searches are an extension to the 1076 standard.

Disabling Default Binding

If you want default binding to occur using only configurations, you can disable normal default binding methods by setting the `RequireConfigForAllDefaultBinding` variable in the `modelsim.ini` file to 1 (true).

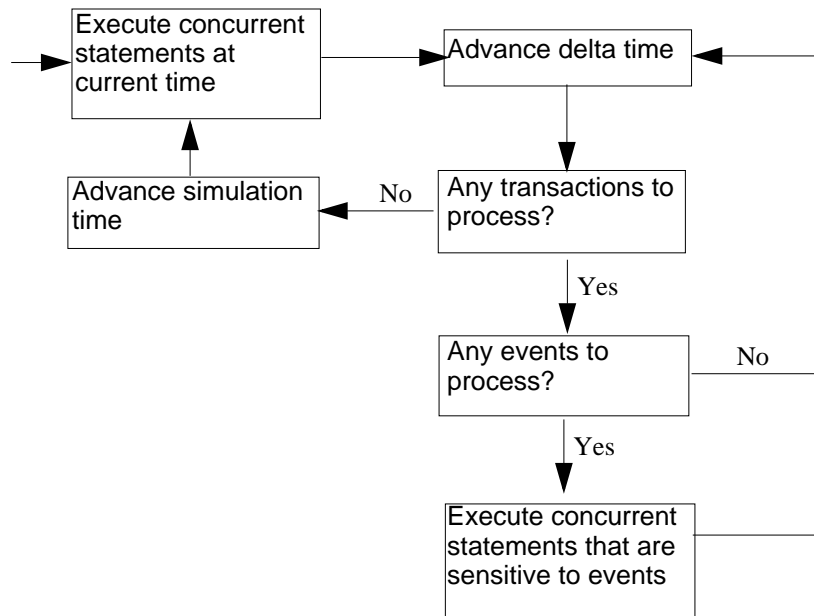
Delta Delays

Event-based simulators such as ModelSim may process many events at a given simulation time. Multiple signals may need updating, statements that are sensitive to these signals must be

executed, and any new events that result from these statements must then be queued and executed as well. The steps taken to evaluate the design without advancing simulation time are referred to as "delta times" or just "deltas."

The diagram below represents the process for VHDL designs. This process continues until the end of simulation time.

Figure 7-1. VHDL Delta Delay Process



This mechanism in event-based simulators may cause unexpected results. Consider the following code fragment:

```
clk2 <= clk;

process (rst, clk)
begin
  if(rst = '0')then
    s0 <= '0';
  elsif(clk'event and clk='1') then
    s0 <= inp;
  end if;
end process;

process (rst, clk2)
begin
  if(rst = '0')then
    s1 <= '0';
  elsif(clk2'event and clk2='1') then
    s1 <= s0;
  end if;
end process;
```

In this example you have two synchronous processes, one triggered with *clk* and the other with *clk2*. To your surprise, the signals change in the *clk2* process on the same edge as they are set in the *clk* process. As a result, the value of *inp* appears at *s1* rather than *s0*.

During simulation an event on *clk* occurs (from the test bench). From this event ModelSim performs the "*clk2* <= *clk*" assignment and the process which is sensitive to *clk*. Before advancing the simulation time, ModelSim finds that the process sensitive to *clk2* can also be run. Since there are no delays present, the effect is that the value of *inp* appears at *s1* in the same simulation cycle.

In order to get the expected results, you must do one of the following:

- Insert a delay at every output
- Make certain to use the same clock
- Insert a delta delay

To insert a delta delay, you would modify the code like this:

```
process (rst, clk)
begin
  if(rst = '0')then
    s0 <= '0';
  elsif(clk'event and clk='1') then
    s0 <= inp;
    s0_delayed <= s0;
  end if;
end process;

process (rst, clk2)
begin
  if(rst = '0')then
    s1 <= '0';
  elsif(clk2'event and clk2='1') then
    s1 <= s0_delayed;
  end if;
end process;
```

The best way to debug delta delay problems is observe your signals in the List window. There you can see how values change at each delta time.

Detecting Infinite Zero-Delay Loops

If a large number of deltas occur without advancing time, it is usually a symptom of an infinite zero-delay loop in the design. In order to detect the presence of these loops, ModelSim defines a limit, the "iteration limit", on the number of successive deltas that can occur. When ModelSim reaches the iteration limit, it issues a warning message.

The iteration limit default value is 5000 . If you receive an iteration limit warning, first increase the iteration limit and try to continue simulation. You can set the iteration limit from the

Simulate > Runtime Options menu or by modifying the [IterationLimit](#) variable in the *modelsim.ini*. See [modelsim.ini Variables](#) for more information on modifying the *modelsim.ini* file.

If the problem persists, look for zero-delay loops. Run the simulation and look at the source code when the error occurs. Use the step button to step through the code and see which signals or variables are continuously oscillating. Two common causes are a loop that has no exit, or a series of gates with zero delay where the outputs are connected back to the inputs.

Using the TextIO Package

The TextIO package is defined within the *VHDL Language Reference Manual, IEEE Std 1076*. This package allows human-readable text input from a declared source within a VHDL file during simulation.

To access the routines in TextIO, include the following statement in your VHDL source code:

```
USE std.textio.all;
```

A simple example using the package TextIO is:

```
USE std.textio.all;
ENTITY simple_textio IS
END;

ARCHITECTURE simple_behavior OF simple_textio IS
BEGIN
  PROCESS
    VARIABLE i: INTEGER:= 42;
    VARIABLE LLL: LINE;
  BEGIN
    WRITE (LLL, i);
    WRITELINE (OUTPUT, LLL);
    WAIT;
  END PROCESS;
END simple_behavior;
```

Syntax for File Declaration

The VHDL 1987 syntax for a file declaration is:

```
file identifier : subtype_indication is [ mode ] file_logical_name ;
```

where "file_logical_name" must be a string expression.

In newer versions of the 1076 spec, syntax for a file declaration is:

```
file identifier_list : subtype_indication [ file_open_information ] ;
```

where "file_open_information" is:


```
[open file_open_kind_expression] is file_logical_name
```

You can specify a full or relative path as the `file_logical_name`; for example (VHDL 1987):

```
file filename : TEXT is in "/usr/rick/myfile";
```

Normally if a file is declared within an architecture, process, or package, the file is opened when you start the simulator and is closed when you exit from it. If a file is declared in a subprogram, the file is opened when the subprogram is called and closed when execution RETURNS from the subprogram. Alternatively, the opening of files can be delayed until the first read or write by setting the [DelayFileOpen](#) variable in the `modelsim.ini` file. Also, the number of concurrently open files can be controlled by the [ConcurrentFileLimit](#) variable. These variables help you manage a large number of files during simulation. See [modelsim.ini Variables](#) for more details.

Using STD_INPUT and STD_OUTPUT Within ModelSim

The standard VHDL1987 TextIO package contains the following file declarations:

```
file input: TEXT is in "STD_INPUT";  
file output: TEXT is out "STD_OUTPUT";
```

Updated versions of the TextIO package contain these file declarations:

```
file input: TEXT open read_mode is "STD_INPUT";  
file output: TEXT open write_mode is "STD_OUTPUT";
```

STD_INPUT is a `file_logical_name` that refers to characters that are entered interactively from the keyboard, and STD_OUTPUT refers to text that is displayed on the screen.

In ModelSim, reading from the STD_INPUT file allows you to enter text into the current buffer from a prompt in the Transcript pane. The lines written to the STD_OUTPUT file appear in the Transcript.

TextIO Implementation Issues

Writing Strings and Aggregates

A common error in VHDL source code occurs when a call to a WRITE procedure does not specify whether the argument is of type STRING or BIT_VECTOR. For example, the VHDL procedure:

```
WRITE (L, "hello");
```

will cause the following error:

```
ERROR: Subprogram "WRITE" is ambiguous.
```

In the TextIO package, the WRITE procedure is overloaded for the types STRING and BIT_VECTOR. These lines are reproduced here:

```
procedure WRITE(L: inout LINE; VALUE: in BIT_VECTOR;
  JUSTIFIED: in SIDE:= RIGHT; FIELD: in WIDTH := 0);

procedure WRITE(L: inout LINE; VALUE: in STRING;
  JUSTIFIED: in SIDE:= RIGHT; FIELD: in WIDTH := 0);
```

The error occurs because the argument "hello" could be interpreted as a string or a bit vector, but the compiler is not allowed to determine the argument type until it knows which function is being called.

The following procedure call also generates an error:

```
WRITE (L, "010101");
```

This call is even more ambiguous, because the compiler could not determine, even if allowed to, whether the argument "010101" should be interpreted as a string or a bit vector.

There are two possible solutions to this problem:

- Use a qualified expression to specify the type, as in:

```
WRITE (L, string("hello"));
```

- Call a procedure that is not overloaded, as in:

```
WRITE_STRING (L, "hello");
```

The WRITE_STRING procedure simply defines the value to be a STRING and calls the WRITE procedure, but it serves as a shell around the WRITE procedure that solves the overloading problem. For further details, refer to the WRITE_STRING procedure in the io_utils package, which is located in the file *<install_dir>/modeltech/examples/misc/io_utils.vhd*.

Reading and Writing Hexadecimal Numbers

The reading and writing of hexadecimal numbers is not specified in standard VHDL. The Issues Screening and Analysis Committee of the VHDL Analysis and Standardization Group (ISAC-VASG) has specified that the TextIO package reads and writes only decimal numbers.

To expand this functionality, ModelSim supplies hexadecimal routines in the package io_utils, which is located in the file *<install_dir>/modeltech/examples/misc/io_utils.vhd*. To use these routines, compile the io_utils package and then include the following use clauses in your VHDL source code:

```
use std.textio.all;
use work.io_utils.all;
```

Dangling Pointers

Dangling pointers are easily created when using the TextIO package, because WRITELINE deallocates the access type (pointer) that is passed to it. Following are examples of good and bad VHDL coding styles:

Bad VHDL (because L1 and L2 both point to the same buffer):

```
READLINE (infile, L1);    -- Read and allocate buffer
L2 := L1;                 -- Copy pointers
WRITELINE (outfile, L1); -- Deallocate buffer
```

Good VHDL (because L1 and L2 point to different buffers):

```
READLINE (infile, L1);    -- Read and allocate buffer
L2 := new string'(L1.all); -- Copy contents
WRITELINE (outfile, L1);  -- Deallocate buffer
```

The ENDLINE Function

The ENDLINE function described in the *IEEE Standard VHDL Language Reference Manual, IEEE Std 1076-1987* contains invalid VHDL syntax and cannot be implemented in VHDL. This is because access values must be passed as variables, but functions do not allow variable parameters.

Based on an ISAC-VASG recommendation the ENDLINE function has been removed from the TextIO package. The following test may be substituted for this function:

```
(L = NULL) OR (L'LENGTH = 0)
```

The ENDFILE Function

In the *VHDL Language Reference Manuals*, the ENDFILE function is listed as:

```
-- function ENDFILE (L: in TEXT) return BOOLEAN;
```

As you can see, this function is commented out of the standard TextIO package. This is because the ENDFILE function is implicitly declared, so it can be used with files of any type, not just files of type TEXT.

Using Alternative Input/Output Files

You can use the TextIO package to read and write to your own files. To do this, just declare an input or output file of type TEXT. For example, for an input file:

The VHDL1987 declaration is:

```
file myinput : TEXT is in "pathname.dat";
```

The VHDL1993 declaration is:

```
file myinput : TEXT open read_mode is "pathname.dat";
```

Then include the identifier for this file ("myinput" in this example) in the READLINE or WRITELINE procedure call.

Flushing the TEXTIO Buffer

Flushing of the TEXTIO buffer is controlled by the [UnbufferedOutput](#) variable in the *modelsim.ini* file.

Providing Stimulus

You can provide an input stimulus to a design by reading data vectors from a file and assigning their values to signals. You can then verify the results of this input. A VHDL test bench has been included with the ModelSim install files as an example. Check for this file:

```
<install_dir>/modeltech/examples/misc/stimulus.vhd
```

VITAL Usage and Compliance

The VITAL (VHDL Initiative Towards ASIC Libraries) modeling specification is sponsored by the IEEE to promote the development of highly accurate, efficient simulation models for ASIC (Application-Specific Integrated Circuit) components in VHDL.

The IEEE 1076.4 VITAL ASIC Modeling Specification is available from the Institute of Electrical and Electronics Engineers, Inc.

IEEE Customer Service
445 Hoes Lane
Piscataway, NJ 08854-1331

Tel: (732) 981-0060
Fax: (732) 981-1721

<http://www.ieee.org>

VITAL Source Code

The source code for VITAL packages is provided in the following ModelSim installation directories:

```
/<install_dir>/vhdl_src/vital2.2b  
/vital95
```

/vital2000

VITAL 1995 and 2000 Packages

VITAL 1995 accelerated packages are pre-compiled into the **ieee** library in the installation directory. VITAL 2000 accelerated packages are pre-compiled into the **vital2000** library. If you need to use the newer library, you either need to change the **ieee** library mapping or add a **use** clause to your VHDL code to access the VITAL 2000 packages.

To change the **ieee** library mapping, issue the following command:

```
vmap ieee <modeltech>/vital2000
```

Or, alternatively, add **use** clauses to your code:

```
LIBRARY vital2000;  
USE vital2000.vital_primitives.all;  
USE vital2000.vital_timing.all;  
USE vital2000.vital_memory.all;
```

Note that if your design uses two libraries—one that depends on **vital95** and one that depends on **vital2000**—then you will have to change the references in the source code to **vital2000**. Changing the library mapping will not work.

VITAL Compliance

A simulator is VITAL-compliant if it implements the SDF mapping and if it correctly simulates designs using the VITAL packages—as outlined in the VITAL Model Development Specification. ModelSim is compliant with the IEEE 1076.4 VITAL ASIC Modeling Specification. In addition, ModelSim accelerates the **VITAL_Timing**, **VITAL_Primitives**, and **VITAL_memory** packages. The optimized procedures are functionally equivalent to the IEEE 1076.4 VITAL ASIC Modeling Specification (VITAL 1995 and 2000).

VITAL Compliance Checking

Compliance checking is important in enabling VITAL acceleration; to qualify for global acceleration, an architecture must be VITAL-level-one compliant. **vcom** automatically checks for VITAL 2000 compliance on all entities with the **VITAL_Level0** attribute set, and all architectures with the **VITAL_Level0** or **VITAL_Level1** attribute set.

If you are using VITAL 2.2b, you must turn off the compliance checking either by not setting the attributes, or by invoking **vcom** with the argument **-novitalcheck**.

You can turn off compliance checking for VITAL 1995 and VITAL 2000 as well, but it strongly recommended that you leave checking on to ensure optimal simulation.

VITAL Compliance Warnings

The following LRM errors are printed as warnings (if they were considered errors they would prevent VITAL level 1 acceleration); they do not affect how the architecture behaves.

- Starting index constraint to DataIn and PreviousDataIn parameters to VITALStateTable do not match (1076.4 section 6.4.3.2.2)
- Size of PreviousDataIn parameter is larger than the size of the DataIn parameter to VITALStateTable (1076.4 section 6.4.3.2.2)
- Signal q_w is read by the VITAL process but is NOT in the sensitivity list (1076.4 section 6.4.3)

The first two warnings are minor cases where the body of the VITAL 1995 LRM is slightly stricter than the package portion of the LRM. Since either interpretation will provide the same simulation results, both of these cases are provided as warnings.

The last warning is a relaxation of the restriction on reading an internal signal that is not in the sensitivity list. This is relaxed only for the CheckEnabled parameters of the timing checks, and only if they are not read elsewhere.

You can control the visibility of VITAL compliance-check warnings in your `vcom` transcript. They can be suppressed by using the `vcom -nowarn` switch, as in `vcom -nowarn 6`. The number 6 represents the warning level printed as part of the warning, such as `** WARNING: [6]`. You can also add the following line to your `modelsim.ini` file in the `vcom` section:

```
[vcom]
Show_VitalChecksWarnings = 0
```

See [modelsim.ini Variables](#) for more information.

Compiling and Simulating with Accelerated VITAL Packages

The `vcom` command automatically recognizes that a VITAL function is being referenced from the `ieee` library and generates code to call the optimized built-in routines.

Optimization occurs on two levels:

- **VITAL Level-0 optimization** — This is a function-by-function optimization. It applies to all level-0 architectures, and any level-1 architectures that failed level-1 optimization.
- **VITAL Level-1 optimization** — Performs global optimization on a VITAL 3.0 level-1 architecture that passes the VITAL compliance checker. This is the default behavior. Note that your models will run faster but at the cost of not being able to see the internal workings of the models.

Compiler Options for VITAL Optimization

The `vcom` command has several arguments that control and provide feedback on VITAL optimization:

- `-novital`

Causes `vcom` to use VHDL code for VITAL procedures rather than the accelerated and optimized timing and primitive packages. Allows breakpoints to be set in the VITAL behavior process and permits single stepping through the VITAL procedures to debug your model. Also, all of the VITAL data can be viewed in the Locals or Objects pane.

- `-O0` | `-O4`

Lowers the optimization to a minimum with `-O0` (capital oh zero). Optional. Use this to work around bugs, increase your debugging visibility on a specific cell, or when you want to place breakpoints on source lines that have been optimized out.

Enable optimizations with `-O4` (default).

- `-debugVA`

Prints a confirmation if a VITAL cell was optimized, or an explanation of why it was not, during VITAL level-1 acceleration.

ModelSim VITAL built-ins will be updated in step with new releases of the VITAL packages.

VHDL Utilities Package (util)

The `util` package contains various VHDL utilities that you can run as commands. The package is part of the `modelsim_lib` library, which is located in the `/modeltech` tree and is mapped in the default `modelsim.ini` file.

To include the utilities in this package, add the following lines similar to your VHDL code:

```
library modelsim_lib;  
use modelsim_lib.util.all;
```

get_resolution

The `get_resolution` utility returns the current simulator resolution as a real number. For example, a resolution of 1 femtosecond (1 fs) corresponds to $1e-15$.

Syntax

```
resval := get_resolution;
```

Returns

Name	Type	Description
resval	real	The simulator resolution represented as a real

Arguments

None

Related functions

- [to_real\(\)](#)
- [to_time\(\)](#)

Example

If the simulator resolution is set to 10ps, and you invoke the command:

```
resval := get_resolution;
```

the value returned to resval would be 1e-11.

init_signal_driver()

The `init_signal_driver()` utility drives the value of a VHDL signal or Verilog net onto an existing VHDL signal or Verilog net. This allows you to drive signals or nets at any level of the design hierarchy from within a VHDL architecture (such as a test bench).

See [init_signal_driver](#) for complete details.

init_signal_spy()

The `init_signal_spy()` utility mirrors the value of a VHDL signal or Verilog register/net onto an existing VHDL signal or Verilog register. This allows you to reference signals, registers, or nets at any level of hierarchy from within a VHDL architecture (such as a test bench).

See [init_signal_spy](#) for complete details.

signal_force()

The `signal_force()` utility forces the value specified onto an existing VHDL signal or Verilog register or net. This allows you to force signals, registers, or nets at any level of the design hierarchy from within a VHDL architecture (such as a test bench). A `signal_force` works the same as the `force` command with the exception that you cannot issue a repeating force.

See [signal_force](#) for complete details.

signal_release()

The `signal_release()` utility releases any force that was applied to an existing VHDL signal or Verilog register or net. This allows you to release signals, registers, or nets at any level of the design hierarchy from within a VHDL architecture (such as a test bench). A `signal_release` works the same as the `noforce` command.

See [signal_release](#) for complete details.

to_real()

The `to_real()` utility converts the physical type time value into a real value with respect to the current value of simulator resolution. The precision of the converted value is determined by the simulator resolution. For example, if you were converting 1900 fs to a real and the simulator resolution was ps, then the real value would be rounded to 2.0 (that is, 2 ps).

Syntax

```
realval := to_real(timeval);
```

Returns

Name	Type	Description
realval	real	The time value represented as a real with respect to the simulator resolution

Arguments

Name	Type	Description
timeval	time	The value of the physical type time

Related functions

- [get_resolution](#)
- [to_time\(\)](#)

Example

If the simulator resolution is set to ps, and you enter the following function:

```
realval := to_real(12.99 ns);
```

then the value returned to `realval` would be 12990.0. If you wanted the returned value to be in units of nanoseconds (ns) instead, you would use the [get_resolution](#) function to recalculate the value:

```
realval := 1e+9 * (to_real(12.99 ns)) * get_resolution();
```

If you wanted the returned value to be in units of femtoseconds (fs), you would enter the function this way:

```
realval := 1e+15 * (to_real(12.99 ns)) * get_resolution();
```

to_time()

The `to_time()` utility converts a real value into a time value with respect to the current simulator resolution. The precision of the converted value is determined by the simulator resolution. For example, if you converted 5.9 to a time and the simulator resolution was 1 ps, then the time value would be rounded to 6 ps.

Syntax

```
timeval := to_time(realval);
```

Returns

Name	Type	Description
timeval	time	The real value represented as a physical type time with respect to the simulator resolution

Arguments

Name	Type	Description
realval	real	The value of the type real

Related functions

- [get_resolution](#)
- [to_real\(\)](#)

Example

If the simulator resolution is set to 1 ps, and you enter the following function:

```
timeval := to_time(72.49);
```

then the value returned to `timeval` would be 72 ps.

Modeling Memory

If you want to model a memory with VHDL using signals, you may encounter either of the following common problems with simulation:

- Memory allocation error, which typically means the simulator ran out of memory and failed to allocate enough storage.

- Very long times to load, elaborate, or run.

These problems usually result from the fact that signals consume a substantial amount of memory (many dozens of bytes per bit), all of which must be loaded or initialized before your simulation starts.

As an alternative, you can model a memory design using variables or protected types instead of signals, which provides the following performance benefits:

- Reduced storage required to model the memory, by as much as one or two orders of magnitude
- Reduced startup and run times
- Elimination of associated memory allocation errors

Examples of Different Memory Models

[Example 7-1](#) shown below uses different VHDL architectures for the entity named memory to provide the following models for storing RAM:

- `bad_style_87` — uses a VHDL signal
- `style_87` — uses variables in the memory process
- `style_93` — uses variables in the architecture

For large memories, the run time for architecture `bad_style_87` is many times longer than the other two and uses much more memory. Because of this, you should avoid using VHDL signals to model memory.

To implement this model, you will need functions that convert vectors to integers. To use it, you will probably need to convert integers to vectors.

Converting an Integer Into a `bit_vector`

The following code shows how to convert an integer variable into a `bit_vector`.

```
library ieee;
use ieee.numeric_bit.ALL;

entity test is
end test;

architecture only of test is
    signal s1 : bit_vector(7 downto 0);
    signal int : integer := 45;
begin
    p:process
    begin
        wait for 10 ns;
        s1 <= bit_vector(to_signed(int,8));
    end process p;
end only;
```

Examples Using VHDL1987, VHDL1993, VHDL2002 Architectures

- [Example 7-1](#) contains two VHDL architectures that demonstrate recommended memory models: style_93 uses shared variables as part of a process, style_87 uses For comparison, a third architecture, bad_style_87, shows the use of signals.

The style_87 and style_93 architectures work with equal efficiency for this example. However, VHDL 1993 offers additional flexibility because the RAM storage can be shared among multiple processes. In the example, a second process is shown that initializes the memory; you could add other processes to create a multi-ported memory.

- [Example 7-2](#) is a package (named conversions) that is included by the memory model in [Example 7-1](#).
- For completeness, [Example 7-3](#) shows protected types using VHDL 2002. Note that using protected types offers no advantage over shared variables.

Example 7-1. Memory Model Using VHDL87 and VHDL93 Architectures

Example functions are provided below in package “conversions.”

```
-----
-- Source:      memory.vhd
-- Component:   VHDL synchronous, single-port RAM
-- Remarks:     Provides three different architectures
-----

library ieee;
use ieee.std_logic_1164.all;
use work.conversions.all;
```

```
entity memory is
  generic(add_bits : integer := 12;
          data_bits : integer := 32);
  port(add_in : in std_ulogic_vector(add_bits-1 downto 0);
        data_in : in std_ulogic_vector(data_bits-1 downto 0);
        data_out : out std_ulogic_vector(data_bits-1 downto 0);
        cs, mwrite : in std_ulogic;
        do_init : in std_ulogic);
  subtype word is std_ulogic_vector(data_bits-1 downto 0);
  constant nwords : integer := 2 ** add_bits;
  type ram_type is array(0 to nwords-1) of word;
end;

architecture style_93 of memory is
  -----
  shared variable ram : ram_type;
  -----

begin
memory:
process (cs)
  variable address : natural;
  begin
    if rising_edge(cs) then
      address := sylv_to_natural(add_in);
      if (mwrite = '1') then
        ram(address) := data_in;
      end if;
      data_out <= ram(address);
    end if;
  end process memory;
-- illustrates a second process using the shared variable
initialize:
process (do_init)
  variable address : natural;
  begin
    if rising_edge(do_init) then
      for address in 0 to nwords-1 loop
        ram(address) := data_in;
      end loop;
    end if;
  end process initialize;
end architecture style_93;
```

```
architecture style_87 of memory is
begin
memory:
process (cs)
-----
variable ram : ram_type;
-----
variable address : natural;
begin
    if rising_edge(cs) then
        address := sylv_to_natural(add_in);
        if (mwrite = '1') then
            ram(address) := data_in;
        end if;
        data_out <= ram(address);
    end if;
end process;
end style_87;

architecture bad_style_87 of memory is
-----
signal ram : ram_type;
-----
begin
memory:
process (cs)
variable address : natural := 0;
begin
    if rising_edge(cs) then
        address := sylv_to_natural(add_in);
        if (mwrite = '1') then
            ram(address) <= data_in;
            data_out <= data_in;
        else
            data_out <= ram(address);
        end if;
    end if;
end process;
end bad_style_87;
```

Example 7-2. Conversions Package

```
library ieee;
use ieee.std_logic_1164.all;

package conversions is
    function sylv_to_natural(x : std_ulogic_vector) return
        natural;
    function natural_to_sylv(n, bits : natural) return
        std_ulogic_vector;
end conversions;
```

```
package body conversions is

    function sulv_to_natural(x : std_ulogic_vector) return
        natural is
        variable n : natural := 0;
        variable failure : boolean := false;
    begin
        assert (x'high - x'low + 1) <= 31
            report "Range of sulv_to_natural argument exceeds
                natural range"
            severity error;
        for i in x'range loop
            n := n * 2;
            case x(i) is
                when '1' | 'H' => n := n + 1;
                when '0' | 'L' => null;
                when others => failure := true;
            end case;
        end loop;

        assert not failure
            report "sulv_to_natural cannot convert indefinite
                std_ulogic_vector"
            severity error;

        if failure then
            return 0;
        else
            return n;
        end if;
    end sulv_to_natural;

    function natural_to_sulv(n, bits : natural) return
        std_ulogic_vector is
        variable x : std_ulogic_vector(bits-1 downto 0) :=
            (others => '0');
        variable tempn : natural := n;
    begin
        for i in x'reverse_range loop
            if (tempn mod 2) = 1 then
                x(i) := '1';
            end if;
            tempn := tempn / 2;
        end loop;
        return x;
    end natural_to_sulv;

end conversions;
```

Example 7-3. Memory Model Using VHDL02 Architecture

```
-----  
-- Source:      sp_syn_ram_protected.vhd  
-- Component:   VHDL synchronous, single-port RAM  
-- Remarks:     Various VHDL examples: random access memory (RAM)  
-----  
  
LIBRARY ieee;  
USE ieee.std_logic_1164.ALL;  
USE ieee.numeric_std.ALL;  
  
ENTITY sp_syn_ram_protected IS  
    GENERIC (  
        data_width : positive := 8;  
        addr_width  : positive := 3  
    );  
    PORT (  
        inclk      : IN  std_logic;  
        outclk     : IN  std_logic;  
        we         : IN  std_logic;  
        addr       : IN  unsigned(addr_width-1 DOWNTO 0);  
        data_in    : IN  std_logic_vector(data_width-1 DOWNTO 0);  
        data_out   : OUT std_logic_vector(data_width-1 DOWNTO 0)  
    );  
  
END sp_syn_ram_protected;  
  
ARCHITECTURE intarch OF sp_syn_ram_protected IS  
  
    TYPE mem_type IS PROTECTED  
        PROCEDURE write ( data : IN std_logic_vector(data_width-1 downto 0);  
                          addr : IN unsigned(addr_width-1 DOWNTO 0));  
        IMPURE FUNCTION read ( addr : IN unsigned(addr_width-1 DOWNTO 0))  
        RETURN  
            std_logic_vector;  
        END PROTECTED mem_type;  
  
    TYPE mem_type IS PROTECTED BODY  
        TYPE mem_array IS ARRAY (0 TO 2**addr_width-1) OF  
            std_logic_vector(data_width-1 DOWNTO 0);  
        VARIABLE mem : mem_array;  
  
        PROCEDURE write ( data : IN std_logic_vector(data_width-1 downto 0);  
                          addr : IN unsigned(addr_width-1 DOWNTO 0)) IS  
        BEGIN  
            mem(to_integer(addr)) := data;  
        END;  
  
        IMPURE FUNCTION read ( addr : IN unsigned(addr_width-1 DOWNTO 0))  
        RETURN  
            std_logic_vector IS  
        BEGIN  
            return mem(to_integer(addr));  
        END;  
  
    END PROTECTED BODY mem_type;  
  
END intarch;
```



```
    SHARED VARIABLE memory : mem_type;

BEGIN

    ASSERT data_width <= 32
        REPORT "### Illegal data width detected"
        SEVERITY failure;

    control_proc : PROCESS (inclk, outclk)

    BEGIN
        IF (inclk'event AND inclk = '1') THEN
            IF (we = '1') THEN
                memory.write(data_in, addr);
            END IF;
        END IF;

        IF (outclk'event AND outclk = '1') THEN
            data_out <= memory.read(addr);
        END IF;
    END PROCESS;

END intarch;

-----
-- Source:      ram_tb.vhd
-- Component:   VHDL test bench for RAM memory example
-- Remarks:     Simple VHDL example: random access memory (RAM)
-----

LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.numeric_std.ALL;

ENTITY ram_tb IS
END ram_tb;

ARCHITECTURE testbench OF ram_tb IS

    -----
    -- Component declaration single-port RAM
    -----

    COMPONENT sp_syn_ram_protected
        GENERIC (
            data_width : positive := 8;
            addr_width  : positive := 3
        );
        PORT (
            inclk      : IN  std_logic;
            outclk     : IN  std_logic;
            we         : IN  std_logic;
            addr       : IN  unsigned(addr_width-1 DOWNTO 0);
            data_in    : IN  std_logic_vector(data_width-1 DOWNTO 0);
            data_out   : OUT std_logic_vector(data_width-1 DOWNTO 0)
        );
    END COMPONENT;

    -----
```

```
-- Intermediate signals and constants
-----
SIGNAL  addr      : unsigned(19 DOWNT0 0);
SIGNAL  inaddr    : unsigned(3 DOWNT0 0);
SIGNAL  outaddr   : unsigned(3 DOWNT0 0);
SIGNAL  data_in   : unsigned(31 DOWNT0 0);
SIGNAL  data_in1  : std_logic_vector(7 DOWNT0 0);
SIGNAL  data_spl  : std_logic_vector(7 DOWNT0 0);
SIGNAL  we        : std_logic;
SIGNAL  clk       : std_logic;
CONSTANT clk_pd   : time := 100 ns;

BEGIN

-----
-- instantiations of single-port RAM architectures.
-- All architectures behave equivalently, but they
-- have different implementations. The signal-based
-- architecture (rtl) is not a recommended style.
-----
spraml : entity work.sp_syn_ram_protected
  GENERIC MAP (
    data_width => 8,
    addr_width => 12)
  PORT MAP (
    inclk    => clk,
    outclk   => clk,
    we       => we,
    addr     => addr(11 downto 0),
    data_in  => data_in1,
    data_out => data_spl);

-----
-- clock generator
-----
clock_driver : PROCESS
BEGIN
  clk <= '0';
  WAIT FOR clk_pd / 2;
  LOOP
    clk <= '1', '0' AFTER clk_pd / 2;
    WAIT FOR clk_pd;
  END LOOP;
END PROCESS;

-----
-- data-in process
-----
datain_drivers : PROCESS(data_in)
BEGIN
  data_in1 <= std_logic_vector(data_in(7 downto 0));
END PROCESS;

-----
-- simulation control process
-----
ctrl_sim : PROCESS
```

```
BEGIN
  FOR i IN 0 TO 1023 LOOP
    we      <= '1';
    data_in <= to_unsigned(9000 + i, data_in'length);
    addr    <= to_unsigned(i, addr'length);
    inaddr  <= to_unsigned(i, inaddr'length);
    outaddr <= to_unsigned(i, outaddr'length);
    WAIT UNTIL clk'EVENT AND clk = '0';
    WAIT UNTIL clk'EVENT AND clk = '0';

    data_in <= to_unsigned(7 + i, data_in'length);
    addr    <= to_unsigned(1 + i, addr'length);
    inaddr  <= to_unsigned(1 + i, inaddr'length);
    WAIT UNTIL clk'EVENT AND clk = '0';
    WAIT UNTIL clk'EVENT AND clk = '0';

    data_in <= to_unsigned(3, data_in'length);
    addr    <= to_unsigned(2 + i, addr'length);
    inaddr  <= to_unsigned(2 + i, inaddr'length);
    WAIT UNTIL clk'EVENT AND clk = '0';
    WAIT UNTIL clk'EVENT AND clk = '0';

    data_in <= to_unsigned(30330, data_in'length);
    addr    <= to_unsigned(3 + i, addr'length);
    inaddr  <= to_unsigned(3 + i, inaddr'length);
    WAIT UNTIL clk'EVENT AND clk = '0';
    WAIT UNTIL clk'EVENT AND clk = '0';

    we      <= '0';
    addr    <= to_unsigned(i, addr'length);
    outaddr <= to_unsigned(i, outaddr'length);
    WAIT UNTIL clk'EVENT AND clk = '0';
    WAIT UNTIL clk'EVENT AND clk = '0';

    addr    <= to_unsigned(1 + i, addr'length);
    outaddr <= to_unsigned(1 + i, outaddr'length);
    WAIT UNTIL clk'EVENT AND clk = '0';
    WAIT UNTIL clk'EVENT AND clk = '0';

    addr    <= to_unsigned(2 + i, addr'length);
    outaddr <= to_unsigned(2 + i, outaddr'length);
    WAIT UNTIL clk'EVENT AND clk = '0';
    WAIT UNTIL clk'EVENT AND clk = '0';

    addr    <= to_unsigned(3 + i, addr'length);
    outaddr <= to_unsigned(3 + i, outaddr'length);
    WAIT UNTIL clk'EVENT AND clk = '0';
    WAIT UNTIL clk'EVENT AND clk = '0';

    END LOOP;
    ASSERT false
      REPORT "### End of Simulation!"
      SEVERITY failure;
  END PROCESS;

END testbench;
```

Affecting Performance by Cancelling Scheduled Events

Simulation performance is likely to get worse if events are scheduled far into the future but then cancelled before they take effect. This situation acts like a memory leak and slows down simulation.

In VHDL, this situation can occur several ways. The most common are waits with time-out clauses and projected waveforms in signal assignments.

The following code shows a wait with a time-out:

```
signals synch : bit := '0';
...
p: process
begin
    wait for 10 ms until synch = 1;
end process;

synch <= not synch after 10 ns;
```

At time 0, process *p* makes an event for time 10ms. When *synch* goes to 1 at 10 ns, the event at 10 ms is marked as cancelled but not deleted, and a new event is scheduled at 10ms + 10ns. The cancelled events are not reclaimed until time 10ms is reached and the cancelled event is processed. As a result there will be 500000 (10ms/20ns) cancelled but un-deleted events. Once 10ms is reached, memory will no longer increase because the simulator will be reclaiming events as fast as they are added.

For projected waveforms the following would behave the same way:

```
signals synch : bit := '0';
...
p: process(synch)
begin
    output <= '0', '1' after 10ms;
end process;

synch <= not synch after 10 ns;
```

Chapter 8

Verilog and SystemVerilog Simulation

This chapter describes how to compile and simulate Verilog and SystemVerilog designs with ModelSim. This chapter covers the following topics:

- [Basic Verilog Usage](#) — A brief outline of the steps for using Verilog in a ModelSim design.
- [Verilog Compilation](#) — Information on the requirements for compiling and optimizing Verilog designs and libraries.
- [Verilog Simulation](#) — Information on the requirements for running simulation.
- [Cell Libraries](#) — Criteria for using Verilog cell libraries from ASIC and FPGA vendors that are compatible with ModelSim.
- [System Tasks and Functions](#) — System tasks and functions that are built into the simulator.
- [Compiler Directives](#) — Verilog compiler directives supported for ModelSim.
- [Sparse Memory Modeling](#) — Information on how to enable sparse memory models in a design. Sparse memories are a mechanism for allocating storage for memory elements only when they are needed.
- [Verilog PLI/VPI and SystemVerilog DPI](#) — Verilog and SystemVerilog interfaces that you can use to define tasks and functions that communicate with the simulator through a C procedural interface.



Standards, Nomenclature, and Conventions

ModelSim implements the Verilog and SystemVerilog languages as defined by the following standards:

- IEEE 1364-2005 and 1364-1995 (Verilog)
- IEEE 1800-2007 and 1800-2005 (SystemVerilog)

Note



ModelSim supports partial implementation of SystemVerilog IEEE Std 1800-2005. For release-specific information on currently supported implementation, refer to the following text file located in the ModelSim installation directory:

`<install_dir>/docs/technotes/sysvlog.note`

SystemVerilog is built “on top of” IEEE Std 1364 for the Verilog HDL and improves the productivity, readability, and reusability of Verilog-based code. The language enhancements in SystemVerilog provide more concise hardware descriptions, while still providing an easy route with existing tools into current hardware implementation flows. The enhancements also provide extensive support for directed and constrained random testbench development, coverage-driven verification, and assertion-based verification.

The standard for SystemVerilog specifies extensions for a higher level of abstraction for modeling and verification with the Verilog hardware description language (HDL). This standard includes design specification methods, embedded assertions language, testbench language including coverage and assertions application programming interface (API), and a direct programming interface (DPI).

In this chapter, the following terms apply:

- “Verilog” refers to IEEE Std 1364 for the Verilog HDL.
- “Verilog-2001” refers to IEEE Std 1364-2001 for the Verilog HDL.
- “Verilog-1995” refers to IEEE Std 1364-1995 for the Verilog HDL.
- “SystemVerilog” refers to the extensions to the Verilog standard (IEEE Std 1364) as defined in IEEE Std 1800-2007.

Basic Verilog Usage

Simulating Verilog designs with ModelSim consists of the following general steps:

1. Compile your Verilog code into one or more libraries using the [vlog](#) command. See [Verilog Compilation](#) for details.
2. (Optional) Elaborate and optimize your design using the [vopt](#) command. For more information, refer to Chapter 4, [Optimizing Designs with vopt](#) and [Optimization Considerations for Verilog Designs](#).
3. Load your design with the [vsim](#) command. Refer to [Verilog Simulation](#).
4. Simulate the loaded design and debug as needed.

Verilog Compilation

The first time you compile a design there is a two-step process:

1. Create a working library with `vlib` or select **File > New > Library**.
2. Compile the design using `vlog` or select **Compile > Compile**.

Creating a Working Library

Before you can compile your design, you must create a library in which to store the compilation results. Use the `vlib` command or select **File > New > Library** to create a new library. For example:

```
vlib work
```

This creates a library named **work**. By default compilation results are stored in the **work** library.

The **work** library is actually a subdirectory named *work*. This subdirectory contains a special file named *_info*. Do not create libraries using UNIX commands – always use the `vlib` command.

See [Design Libraries](#) for additional information on working with libraries.

Invoking the Verilog Compiler

The `vlog` command invokes the Verilog compiler, which compiles Verilog source code into retargetable, executable code. You can simulate your design on any supported platform without having to recompile your design; the library format is also compatible across all platforms.

As the design compiles, the resulting object code for modules and user-defined primitives (UDPs) is generated into a library. As noted above, the compiler places results into the work library by default. You can specify an alternate library with the `-work` argument of the `vlog` command.

Example 8-1. Invocation of the Verilog Compiler

The following example shows how to use the `vlog` command to invoke the Verilog compiler:

```
vlog top.v +libext+.v+.u -y vlog_lib
```

After compiling *top.v*, `vlog` searches the *vlog_lib* library for files with modules with the same name as primitives referenced, but undefined in *top.v*. The use of `+libext+.v+.u` implies

filenames with a *.v* or *.u* suffix (any combination of suffixes may be used). Only referenced definitions are compiled.

Parsing SystemVerilog Keywords

With standard Verilog files (<filename>.v), **vlog** does not automatically parse SystemVerilog keywords. SystemVerilog keywords are parsed when either of the following situations exists:

- Any file within the design contains the *.sv* file extension
- You use the *-sv* argument with the **vlog** command

The following examples of the **vlog** command show how to enable SystemVerilog features and keywords in ModelSim:

```
vlog testbench.sv top.v memory.v cache.v
```

```
vlog -sv testbench.v proc.v
```

In the first example, the *.sv* extension for *testbench* automatically causes ModelSim to parse SystemVerilog keywords. In the second example, the *-sv* argument enables SystemVerilog features and keywords.

Though a primary goal of the SystemVerilog standardization efforts has been to ensure full backward compatibility with the Verilog standard, there is an issue with keywords. SystemVerilog adds several new reserved keywords to the Verilog language (see Table B-1 in Annex B of the 1800-2005 SystemVerilog standard). If your design uses one of these keywords as a regular identifier for a variable, module, task, or function, then your design will not compile in ModelSim.

Recognizing SystemVerilog Files by File Name Extension

If you use the *-sv* argument with the **vlog** command, then ModelSim assumes that all input files are SystemVerilog, regardless of their respective filename extensions.

If you do not use the *-sv* argument with the **vlog** command, then ModelSim assumes that only files with the extension *.sv*, *.svh*, or *.svp* are SystemVerilog.

File extensions of include files

Similarly, if you do not use the *-sv* argument while reading in a file that uses an ``include` statement to specify an include file, then the file extension of the include file is ignored and the language is assumed to be the same as the file containing the ``include`. For example, if you do not use the *-sv* argument:

If *a.v* included *b.sv*, then *b.sv* would be read as a Verilog file.

If *c.sv* included *d.v*, then *d.v* would be read as a SystemVerilog file.

File extension settings in modelsim.ini

You can define which file extensions indicate SystemVerilog files with the `SVFileExtensions` variable in the `modelsim.ini` file. By default, this variable is defined in `modelsim.ini` as follows:

```
; SVFileExtensions = sv svp svh
```

For example, the following command:

```
vlog a.v b.sv c.svh d.v
```

reads in `a.v` and `d.v` as a Verilog files and reads in `b.sv` and `c.svh` as SystemVerilog files.

File types affecting compilation units

Note that whether a file is Verilog or SystemVerilog can affect when ModelSim changes from one compilation unit to another.

By default, ModelSim instructs the compiler to treat all files within a compilation command line as separate compilation units (single-file compilation unit mode, which is the equivalent of using `vlog -sfcu`).

```
vlog a.v aa.v b.sv c.svh d.v
```

ModelSim would group these source files into three compilation units:

Files in first unit — `a.v`, `aa.v`, `b.sv`

File in second unit — `c.svh`

File in third unit — `d.v`

This behavior is governed by two basic rules:

- Anything read in is added to the current compilation unit.
- A compilation unit ends at the close of a SystemVerilog file.

Incremental Compilation

ModelSim supports incremental compilation of Verilog designs—there is no requirement to compile an entire design in one invocation of the compiler.

You are not required to compile your design in any particular order (unless you are using SystemVerilog packages; see Note below) because all module and UDP instantiations and external hierarchical references are resolved when the design is loaded by the simulator.

Note



Compilation order may matter when using SystemVerilog packages. As stated in the IEEE std 1800-2005 LRM, section entitled *Referencing data in packages*, which states: “Packages must exist in order for the items they define to be recognized by the scopes in which they are imported.”

Incremental compilation is made possible by deferring these bindings, and as a result some errors cannot be detected during compilation. Commonly, these errors include: modules that were referenced but not compiled, incorrect port connections, and incorrect hierarchical references.

Example 8-2. Incremental Compilation Example

Contents of testbench.sv

```
module testbench;
    timeunit 1ns;
    timeprecision 10ps;
    bit d=1, clk = 0;
    wire q;
    initial
        for (int cycles=0; cycles < 100; cycles++)
            #100 clk = !clk;

    design dut(q, d, clk);
endmodule
```

Contents of design.v:

```
module design(output bit q, input bit d, clk);
    timeunit 1ns;
    timeprecision 10ps;
    always @(posedge clk)
        q = d;
endmodule
```

Compile the design incrementally as follows:

```
ModelSim> vlog testbench.sv
```

```
.
# Top level modules:
```

```
# testbench
```

```
ModelSim> vlog -sv test1.v
```

```
.
# Top level modules:
```

```
# dut
```

Note that the compiler lists each module as a top-level module, although, ultimately, only *testbench* is a top-level module. If a module is not referenced by another module compiled in the same invocation of the compiler, then it is listed as a top-level module. This is just an informative message that you can ignore during incremental compilation.

The message is more useful when you compile an entire design in one invocation of the compiler and need to know the top-level module names for the simulator. For example,

```
% vlog top.v and2.v or2.v
-- Compiling module top
-- Compiling module and2
-- Compiling module or2

Top level modules:
  top
```

Automatic Incremental Compilation with `-incr`

The most efficient method of incremental compilation is to manually compile only the modules that have changed. However, this is not always convenient, especially if your source files have compiler directive interdependencies (such as macros). In this case, you may prefer to compile your entire design along with the `-incr` argument. This causes the compiler to automatically determine which modules have changed and generate code only for those modules.

The following is an example of how to compile a design with automatic incremental compilation:

```
% vlog -incr top.v and2.v or2.v
-- Compiling module top
-- Compiling module and2
-- Compiling module or2

Top level modules:
  top
```

Now, suppose that you modify the functionality of the `or2` module:

```
% vlog -incr top.v and2.v or2.v
-- Skipping module top
-- Skipping module and2
-- Compiling module or2

Top level modules:
  top
```

The compiler informs you that it skipped the modules `top` and `and2`, and compiled `or2`.

Automatic incremental compilation is intelligent about when to compile a module. For example, changing a comment in your source code does not result in a recompile; however, changing the compiler command line arguments results in a recompile of all modules.

Note



Changes to your source code that do not change functionality but that do affect source code line numbers (such as adding a comment line) *will* cause all affected modules to be recompiled. This happens because debug information must be kept current so that ModelSim can trace back to the correct areas of the source code.

Library Usage

All modules and UDPs in a Verilog design must be compiled into one or more libraries. One library is usually sufficient for a simple design, but you may want to organize your modules into various libraries for a complex design. If your design uses different modules having the same name, then you are required to put those modules in different libraries because design unit names must be unique within a library.

The following is an example of how you may organize your ASIC cells into one library and the rest of your design into another:

```
% vlib work
% vlib asiclib
% vlog -work asiclib and2.v or2.v
-- Compiling module and2
-- Compiling module or2

Top level modules:
    and2
    or2
% vlog top.v
-- Compiling module top

Top level modules:
    top
```

Note that the first compilation uses the **-work asiclib** argument to instruct the compiler to place the results in the **asiclib** library rather than the default **work** library.

Library Search Rules for vlog

Since instantiation bindings are not determined at compile time, you must instruct the simulator to search your libraries when loading the design. The top-level modules are loaded from the library named **work** unless you prefix the modules with the **<library>.** option. All other Verilog instantiations are resolved in the following order:

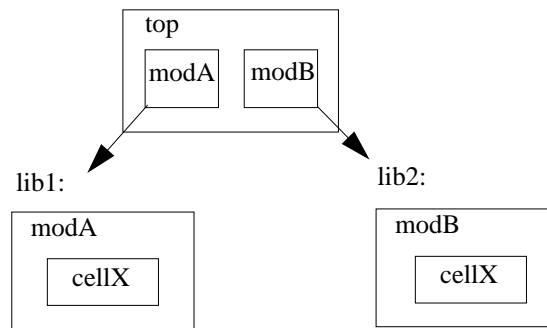
- Search libraries specified with **-Lf** arguments in the order they appear on the command line.
- Search the library specified in the [Verilog-XL uselib Compiler Directive](#) section.
- Search libraries specified with **-L** arguments in the order they appear on the command line.
- Search the **work** library.
- Search the library explicitly named in the special escaped identifier instance name.

Handling Sub-Modules with Common Names

Sometimes in one design you need to reference two different modules that have the same name. This situation can occur if you have hierarchical modules organized into separate libraries, and you have commonly-named sub-modules in the libraries that have different definitions. This may happen if you are using vendor-supplied libraries.

For example, say you have the following design configuration:

Example 8-3. Sub-Modules with Common Names



The normal library search rules fail in this situation. For example, if you load the design as follows:

```
vsim -L lib1 -L lib2 top
```

both instantiations of *cellX* resolve to the *lib1* version of *cellX*. On the other hand, if you specify *-L lib2 -L lib1*, both instantiations of *cellX* resolve to the *lib2* version of *cellX*.

To handle this situation, ModelSim implements a special interpretation of the expression *-L work*. When you specify *-L work* first in the search library arguments you are directing **vsim** to search for the instantiated module or UDP in the library that contains the module that does the instantiation.

In the example above you would invoke vsim as follows:

```
vsim -L work -L lib1 -L lib2 top
```

SystemVerilog Multi-File Compilation

Declarations in Compilation Unit Scope

SystemVerilog allows the declaration of types, variables, functions, tasks, and other constructs in compilation unit scope (\$unit). The visibility of declarations in \$unit scope does not extend outside the current compilation unit. Thus, it is important to understand how compilation units are defined by the tool during compilation.

By default, `vlog` operates in Single File Compilation Unit mode (SFCU). This means the visibility of declarations in `$unit` scope terminates at the end of each source file. Visibility does not carry forward from one file to another, except when a module, interface, or package declaration begins in one file and ends in another file. In that case, the compilation unit spans from the file containing the beginning of the declaration to the file containing the end of the declaration.

`vlog` also supports a non-default behavior called Multi File Compilation Unit mode (MFCU). In MFCU mode, `vlog` compiles all files given on the command line into one compilation unit. You can invoke `vlog` in MFCU mode as follows:

- For a specific compilation -- with the `-mfcu` argument to `vlog`.
- For all compilations -- by setting the variable `MultiFileCompilationUnit = 1` in the `modelsim.ini` file.

By using either of these methods, you allow declarations in `$unit` scope to remain in effect throughout the compilation of all files.

In case you have made MFCU the default behavior by setting `MultiFileCompilationUnit = 1` in your `modelsim.ini` file, it is possible to override the default behavior on specific compilations by using the `-sfcu` argument to `vlog`.

Macro Definitions and Compiler Directives in Compilation Unit Scope

According to the SystemVerilog IEEE Std 1800-2005 LRM, the visibility of macro definitions and compiler directives span the lifetime of a single compilation unit. By default, this means the definitions of macros and settings of compiler directives terminate at the end of each source file. They do not carry forward from one file to another, except when a module, interface, or package declaration begins in one file and ends in another file. In that case, the compilation unit spans from the file containing the beginning of the definition to the file containing the end of the definition.

See [Declarations in Compilation Unit Scope](#) for instructions on how to control `vlog`'s handling of compilation units.

Note



Compiler directives revert to their default values at the end of a compilation unit.

If a compiler directive is specified as an option to the compiler, this setting is used for all compilation units present in the current compilation.

Verilog-XL Compatible Compiler Arguments

The compiler arguments listed below are equivalent to Verilog-XL arguments and may ease the porting of a design to ModelSim. See the [vlog](#) command for a description of each argument.

```
+define+<macro_name> [=<macro_text> ]
+delay_mode_distributed
+delay_mode_path
+delay_mode_unit
+delay_mode_zero
-f <filename>
+incdir+<directory>
+mindelays
+maxdelays
+nowarn<mnemonic>
+typdelays
-u
```

Arguments Supporting Source Libraries

The compiler arguments listed below support source libraries in the same manner as Verilog-XL. See the [vlog](#) command for a description of each argument.

Note that these source libraries are very different from the libraries that the ModelSim compiler uses to store compilation results. You may find it convenient to use these arguments if you are porting a design to ModelSim or if you are familiar with these arguments and prefer to use them.

Source libraries are searched after the source files on the command line are compiled. If there are any unresolved references to modules or UDPs, then the compiler searches the source libraries to satisfy them. The modules compiled from source libraries may in turn have additional unresolved references that cause the source libraries to be searched again. This process is repeated until all references are resolved or until no new unresolved references are found. Source libraries are searched in the order they appear on the command line.

```
-v <filename>
-y <directory>
+libext+<suffix>
+librescan
+nolibcell
-R [<simargs>]
```

Verilog-XL `uselib` Compiler Directive

The ``uselib` compiler directive is an alternative source library management scheme to the `-v`, `-y`, and `+libext` compiler arguments. It has the advantage that a design may reference different modules having the same name. You compile designs that contain ``uselib` directive statements using the `-compile_uselibs` argument (described below) to [vlog](#).

The syntax for the ``uselib` directive is:

```
`uselib <library_reference>...
```

where <library_reference> can be one or more of the following:

- **dir=<library_directory>**, which is equivalent to the command line argument:

```
-y <library_directory>
```
- **file=<library_file>**, which is equivalent to the command line argument:

```
-v <library_file>
```
- **libext=<file_extension>**, which is equivalent to the command line argument:

```
+libext+<file_extension>
```
- **lib=<library_name>**, which references a library for instantiated objects, specifically modules, interfaces and program blocks, but not packages. You must ensure the correct mappings are set up if the library does not exist in the current working directory. The **-compile_uselibs** argument does not affect this usage of **`uselib**.

For example, the following directive

```
`uselib dir=/h/vendorA libext=.v
```

is equivalent to the following command line arguments:

```
-y /h/vendorA +libext+.v
```

Since the **`uselib** directives are embedded in the Verilog source code, there is more flexibility in defining the source libraries for the instantiations in the design. The appearance of a **`uselib** directive in the source code explicitly defines how instantiations that follow it are resolved, completely overriding any previous **`uselib** directives.

An important feature of **`uselib** is to allow a design to reference multiple modules having the same name, therefore independent compilation of the source libraries referenced by the **`uselib** directives is required.

Each source library should be compiled into its own object library. The compilation of the code containing the **`uselib** directives only records which object libraries to search for each module instantiation when the design is loaded by the simulator.

Because the **`uselib** directive is intended to reference source libraries, the simulator must infer the object libraries from the library references. The rule is to assume an object library named **work** in the directory defined in the library reference:

```
dir=<library_directory>
```

or the directory containing the file in the library reference

```
file=<library_file>
```


The simulator will ignore a library reference `libext=<file_extension>`. For example, the following ``uselib` directives infer the same object library:

```
`uselib dir=/h/vendorA
`uselib file=/h/vendorA/libcells.v
```

In both cases the simulator assumes that the library source is compiled into the object library:

```
/h/vendorA/work
```

The simulator also extends the ``uselib` directive to explicitly specify the object library with the library reference `lib=<library_name>`. For example:

```
`uselib lib=/h/vendorA/work
```

The library name can be a complete path to a library, or it can be a logical library name defined with the `vmap` command.

-compile_uselibs Argument

Use the **-compile_uselibs** argument to `vlog` to reference ``uselib` directives. The argument finds the source files referenced in the directive, compiles them into automatically created object libraries, and updates the `modelsim.ini` file with the logical mappings to the libraries.

When using **-compile_uselibs**, ModelSim determines into which directory to compile the object libraries by choosing, in order, from the following three values:

- The directory name specified by the **-compile_uselibs** argument. For example,

```
-compile_uselibs=./mydir
```
- The directory specified by the `MTI_USELIB_DIR` environment variable (see [Environment Variables](#))
- A directory named `mti_uselibs` that is created in the current working directory

The following code fragment and compiler invocation show how two different modules that have the same name can be instantiated within the same design:

```
module top;
  `uselib dir=/h/vendorA libext=.v
  NAND2 u1(n1, n2, n3);
  `uselib dir=/h/vendorB libext=.v
  NAND2 u2(n4, n5, n6);
endmodule
```

vlog -compile_uselibs top

This allows the NAND2 module to have different definitions in the vendorA and vendorB libraries.

uselib is Persistent

As mentioned above, the appearance of a ``uselib` directive in the source code explicitly defines how instantiations that follow it are resolved. This may result in unexpected consequences. For example, consider the following compile command:

```
vlog -compile_uselibs dut.v srtr.v
```

Assume that *dut.v* contains a ``uselib` directive. Since *srtr.v* is compiled after *dut.v*, the ``uselib` directive is still in effect. When *srtr* is loaded it is using the ``uselib` directive from *dut.v* to decide where to locate modules. If this is not what you intend, then you need to put an empty ``uselib` at the end of *dut.v* to "close" the previous ``uselib` statement.

Verilog Configurations

The Verilog 2001 specification added configurations. Configurations specify how a design is "assembled" during the elaboration phase of simulation. Configurations actually consist of two pieces: the library mapping and the configuration itself. The library mapping is used at compile time to determine into which libraries the source files are to be compiled. Here is an example of a simple library map file:

```
library work      ../top.v;  
library rtlLib   lrm_ex_top.v;  
library gateLib  lrm_ex_adder.vg;  
library aLib     lrm_ex_adder.v;
```

Here is an example of a library map file that uses `-incdir`:

```
library lib1 src_dir/*.v -incdir ../include_dir2, ../, my_incdir;
```

The name of the library map file is arbitrary. You specify the library map file using the `-libmap` argument to the `vlog` command. Alternatively, you can specify the file name as the first item on the `vlog` command line, and the compiler reads it as a library map file.

The library map file must be compiled along with the Verilog source files. Multiple map files are allowed but each must be preceded by the `-libmap` argument.

The library map file and the configuration can exist in the same or different files. If they are separate, only the map file needs the `-libmap` argument. The configuration is treated as any other Verilog source file.

Configurations and the Library Named work

The library named "work" is treated specially by ModelSim (see [The Library Named "work"](#) for details) for Verilog configurations.

Consider the following code example:

```
config cfg;
```

```
design top;
instance top.u1 use work.u1;
endconfig
```

In this case, `work.u1` indicates to load `u1` from the current library.

If you want to create a configuration that loads an instance from a library other than the default work library, you can `c`, as follows:

1. Make sure the library has been created using the `vlib` command. For example:

```
vlib mylib
```

2. Define this library (`mylib`) as the new current (working) library:

```
vlog -work mylib
```

3. Load instance `u1` from the current library, which is now `mylib`:

```
config cfg;
design top;
instance top.u1 use mylib.u1;
endconfig
```

Verilog Generate Statements

ModelSim implements the rules adopted for Verilog 2005, because the Verilog 2001 rules for generate statements had numerous inconsistencies and ambiguities. Most of the 2005 rules are backwards compatible, but there is one key difference related to name visibility.

Name Visibility in Generate Statements

Consider the following code example:

```
module m;
  parameter p = 1;

  generate
    if (p)
      integer x = 1;
    else
      real x = 2.0;
    endgenerate

  initial $display(x);
endmodule
```

This example is legal under 2001 rules. However, it is illegal under the 2005 rules and causes an error in ModelSim. Under the new rules, you cannot hierarchically reference a name in an anonymous scope from outside that scope. In the example above, `x` does not propagate its visibility upwards, and each condition alternative is considered to be an anonymous scope.

For this example to simulate properly in ModelSim, change it to the following:

```
module m;
  parameter p = 1;

  if (p) begin:s
    integer x = 1;
  end
  else begin:s
    real x = 2.0;
  end

  initial $display(s.x);
endmodule
```

Because the scope is named in this example (`begin:s`), normal hierarchical resolution rules apply and the code runs without error.

In addition, note that the keyword pair `generate - endgenerate` is optional under the 2005 rules and are excluded in the second example.

Initializing Registers and Memories

For Verilog designs you can initialize registers and memories with specific values or randomly generated values. This functionality is controlled from the `vlog` and `vsim` command lines with the following switches:

- Registers: `vlog +initreg` and `vsim +initreg`
- Memories: `vlog +initmem` and `vsim +initmem`

Initialization Concepts

- **Random stability** — From run to run, it is reasonable to expect that simulation results will be consistent with the same seed value, even when the design is recompiled or different optimization switches are specified.

However, if the design changes in any way, random stability can not be ensured. These design changes include:

- Changing the source code (except for comment editing).
- Changing parameter values with `vopt -G` or `vsim -G`. This forces a different topology during design elaboration.
- Changing a `+define` switch such that different source code is compiled.

For sequential UDPs, the simulator guarantees repeatable initial values only if the design is compiled and run with the same `vlog`, `vopt`, and `vsim` options.

- **Sequential UDPs** — An initial statement in a sequential UDP overrides all `+initreg` functionality.

Limitations

- The following are not initialized with +initmem or +initreg:
 - Variables in dynamic types, dynamic arrays, queues, or associative arrays.
 - Unpacked structs, or unpacked or tagged unions.

Requirements

- Prepare your libraries with vlib and vmap as you would normally.

Initializing with Specific Values — Enabled During Compilation

1. Compile the design unit with the +initreg or +initmem switches to the vlog command. Refer to the vlog command reference page for descriptions of the following options.
 - a. Specify which datatypes should be initialized: +{r | b | e | u}.
 - b. Specify the initialization value: +{0 | 1 | X | Z}.
2. Simulate as you would normally.

Initializing with Specific Values — Enabled During Optimization

1. Compile as you would normally
2. Optimize the design with the +initreg or +initmem switches to the vopt command. Refer to the vopt command reference page for a description of the following options.
 - a. Specify which datatypes should be initialized: +{r | b | e | u}.
 - b. Specify the initialization value: +{0 | 1 | X | Z}.
 - c. Specify design unit name: +<selection>
3. Simulate as you would normally.

Initializing with Random Values — Enabled During Compilation

1. Compile the design unit with the +initreg or +initmem switches to the vlog command. Refer to the vlog command reference page for descriptions of the following options.
 - a. Specify which datatypes should be initialized: +{r | b | e | u}.
 - b. Do not specify the initialization value. This enables the specification of a random seed during simulation.
2. Simulate as you would normally, except for adding the +initmem+<seed> or +initreg+<seed> switches. Refer to the vsim command reference page for a description of this switch. The random values will only include 0 or 1.

If no `+initreg` is present on the `vsim` command line, a random seed of 0 is used during initialization.

Initializing with Random Values — Enabled During Optimization

1. Compile as you would normally
2. Optimize the design with the `+initreg` or `+initmem` switches to the `vopt` command. Refer to the `vopt` command reference page for a description of the following options.
 - a. Specify which datatypes should be initialized: `+{r | b | e | u}`.
 - b. Do not specify the initialization value. This enables the specification of a random seed during simulation.
 - c. Specify design unit name: `+<selection>`
3. Simulate as you would normally, except for adding the `+initmem+<seed>` or `+initreg+<seed>` switches. Refer to the `vsim` command reference page for a description of this switch. The random values will only include 0 or 1.

If no `+initreg` is present on the `vsim` command line, a random seed of 0 is used during initialization.

Verilog Simulation

A Verilog design is ready for simulation after it has been compiled with **vlog** and possibly optimized with **vopt**. For more information on Verilog optimizations, see [Chapter 4, Optimizing Designs with vopt](#) and [Optimization Considerations for Verilog Designs](#). The simulator may then be invoked with the names of the top-level modules (many designs contain only one top-level module) or the name you assigned to the optimized version of the design. For example, if your top-level modules are "testbench" and "globals", then invoke the simulator as follows:

```
vsim testbench globals
```

After the simulator loads the top-level modules, it iteratively loads the instantiated modules and UDPs in the design hierarchy, linking the design together by connecting the ports and resolving hierarchical references. By default all modules and UDPs are loaded from the library named **work**. Modules and UDPs from other libraries can be specified using the **-L** or **-Lf** arguments to **vsim** (see [Library Usage](#) for details).

On successful loading of the design, the simulation time is set to zero, and you must enter a **run** command to begin simulation. Commonly, you enter **run -all** to run until there are no more simulation events or until **\$finish** is executed in the Verilog code. You can also run for specific time periods (for example, run 100 ns). Enter the **quit** command to exit the simulator.

Simulator Resolution Limit (Verilog)

The simulator internally represents time as a 64-bit integer in units equivalent to the smallest unit of simulation time (also known as the simulator resolution limit). The resolution limit defaults to the smallest time units that you specify among all of the ``timescale` compiler directives in the design.

Here is an example of a ``timescale` directive:

```
`timescale 1 ns / 100 ps
```

The first number (1 ns) is the time units; the second number (100 ps) is the time precision, which is the rounding factor for the specified time units. The directive above causes time values to be read as nanoseconds and rounded to the nearest 100 picoseconds.

Time units and precision can also be specified with SystemVerilog keywords as follows:

```
timeunit 1 ns  
timeprecision 100 ps
```

Modules Without Timescale Directives

Unexpected behavior may occur if your design contains some modules with timescale directives and others without. The time units for modules without a timescale directive default to the simulator resolution.

Example

Assume you have the two modules shown in [Table 8-1](#).

Table 8-1. Example Modules—With and Without Timescale Directive

Module 1 (with directive)	Module 2 (without directive)
<pre> `timescale 1 ns / 10 ps module mod1 (set); output set; reg set; parameter d = 1.55; initial begin set = 1'bz; #d set = 1'b0; #d set = 1'b1; end endmodule </pre>	<pre> module mod2 (set); output set; reg set; parameter d = 1.55; initial begin set = 1'bz; #d set = 1'b0; #d set = 1'b1; end endmodule </pre>

Case 1 — Run the **vsim** command in the following order:

```
vsim mod2 mod1
```

Module 1 sets the simulator resolution to 10 ps. Module 2 has no timescale directive, so the time units default to the simulator resolution, in this case 10 ps. If you looked at */mod1/set* and */mod2/set* in the Wave window, you would see that Module 1 transitions every 1.55 ns as expected (because of the 1 ns time unit in the timescale directive). However, in Module 2, *set* transitions every 20 ps. That is because the delay of 1.55 in Module 2 is read as 15.5 ps, which is rounded up to 20 ps.

ModelSim issues the following warning message during elaboration:

```
** Warning: (vsim-3010) [TSCALE] - Module 'mod1' has a `timescale
directive in effect, but previous modules do not.
```

Case 2 — Run the **vsim** command in the following order:

```
vsim mod1 mod2
```

Module 2 sets the simulator resolution to its default (10 ps), so the simulation results would be the same. However, ModelSim issues a different warning message:

```
** Warning: (vsim-3009) [TSCALE] - Module 'mod2' does not have a
`timescale directive in effect, but previous modules do.
```


Note

You should always investigate these warning messages to make sure that the timing of your design operates as intended.

Case 3 — If the design consists of modules with no ``timescale` directives, then the time units default to the value specified by the [Resolution](#) variable in the `modelsim.ini` file. (The variable is set to 1 ns by default.)

-timescale Option

The **-timescale** option can be used with the **vlog** and **vopt** commands to specify the default timescale in effect during compilation for modules that do not have an explicit ``timescale` directive. The format of the **-timescale** argument is the same as that of the ``timescale` directive:

```
-timescale <time_units>/<time_units>
```

where `<time_units>` is `<n> <units>`. The value of `<n>` must be 1, 10, or 100. The value of `<units>` must be fs, ps, ns, us, ms, or s. In addition, the `<time_units>` must be greater than or equal to the `<time_precision>`.

For example:

```
-timescale "1ns / 1ps"
```

The argument above needs quotes because it contains white space.

Multiple Timescale Directives

As alluded to above, your design can have multiple timescale directives. The timescale directive takes effect where it appears in a source file and applies to all source files which follow in the same **vlog** command. Separately compiled modules can also have different timescales. The simulator determines the smallest timescale of all the modules in a design and uses that as the simulator resolution.

timescale, -t, and Rounding

The optional **vsim** argument **-t** sets the simulator resolution limit for the overall simulation. If the resolution set by **-t** is larger than the precision set in a module, the time values in that module are rounded up. If the resolution set by **-t** is smaller than the precision of the module, the precision of that module remains whatever is specified by the ``timescale` directive. Consider the following code:

```
`timescale 1 ns / 100 ps  
  
module foo;  
  
    initial  
        #12.536 $display
```

The list below shows three possibilities for **-t** and how the delays in the module are handled in each case:

- **-t** not set
The delay is rounded to 12.5 as directed by the module's 'timescale directive.
- **-t** is set to 1 fs
The delay is rounded to 12.5. Again, the module's precision is determined by the 'timescale directive. ModelSim does not override the module's precision.
- **-t** is set to 1 ns
The delay will be rounded to 13. The module's precision is determined by the **-t** setting. ModelSim can only round the module's time values because the entire simulation is operating at 1 ns.

Choosing the Resolution for Verilog

You should choose the coarsest resolution limit possible that does not result in undesired rounding of your delays. The time precision should not be unnecessarily small because it limits the maximum simulation time limit, and it degrades performance in some cases.

Event Ordering in Verilog Designs

Event-based simulators such as ModelSim may process multiple events at a given simulation time. The Verilog language is defined such that you cannot explicitly control the order in which simultaneous events are processed. Unfortunately, some designs rely on a particular event order, and these designs may behave differently than you expect.

Event Queues

Section 11 of the IEEE Std 1364-2005 LRM defines several event queues that determine the order in which events are evaluated. At the current simulation time, the simulator has the following pending events:

- active events
- inactive events
- non-blocking assignment update events

- monitor events
- future events
 - inactive events
 - non-blocking assignment update events

The LRM dictates that events are processed as follows – 1) all active events are processed; 2) the inactive events are moved to the active event queue and then processed; 3) the non-blocking events are moved to the active event queue and then processed; 4) the monitor events are moved to the active queue and then processed; 5) simulation advances to the next time where there is an inactive event or a non-blocking assignment update event.

Within the active event queue, the events can be processed in any order, and new active events can be added to the queue in any order. In other words, you *cannot* control event order within the active queue. The example below illustrates potential ramifications of this situation.

Say you have these four statements:

1. always@(q) p = q;
2. always @(q) p2 = not q;
3. always @(p or p2) clk = p and p2;
4. always @(posedge clk)

and current values as follows: q = 0, p = 0, p2=1

The tables below show two of the many valid evaluations of these statements. Evaluation events are denoted by a number where the number is the statement to be evaluated. Update events are denoted <name>(old->new) where <name> indicates the reg being updated and new is the updated value.\

Table 8-2. Evaluation 1 of always Statements

Event being processed	Active event queue
	q(0 -> 1)
q(0 -> 1)	1, 2
1	p(0 -> 1), 2
p(0 -> 1)	3, 2
3	clk(0 -> 1), 2
clk(0 -> 1)	4, 2
4	2
2	p2(1 -> 0)

Table 8-2. Evaluation 1 of always Statements (cont.)

Event being processed	Active event queue
p2(1 -> 0)	3
3	clk(1 -> 0)
clk(1 -> 0)	<empty>

Table 8-3. Evaluation 2 of always Statement

Event being processed	Active event queue
	q(0 -> 1)
q(0 -> 1)	1, 2
1	p(0 -> 1), 2
2	p2(1 -> 0), p(0 -> 1)
p(0 -> 1)	3, p2(1 -> 0)
p2(1 -> 0)	3
3	<empty> (clk does not change)

Again, both evaluations are valid. However, in Evaluation 1, *clk* has a glitch on it; in Evaluation 2, *clk* does not. This indicates that the design has a zero-delay race condition on *clk*.

Controlling Event Queues with Blocking or Non-Blocking Assignments

The only control you have over event order is to assign an event to a particular queue. You do this by using blocking or non-blocking assignments.

Blocking Assignments

Blocking assignments place an event in the active, inactive, or future queues depending on what type of delay they have:

- a blocking assignment without a delay goes in the active queue
- a blocking assignment with an explicit delay of 0 goes in the inactive queue
- a blocking assignment with a non-zero delay goes in the future queue

Non-Blocking Assignments

A non-blocking assignment goes into either the non-blocking assignment update event queue or the future non-blocking assignment update event queue. (Non-blocking assignments with no delays and those with explicit zero delays are treated the same.)

Non-blocking assignments should be used only for outputs of flip-flops. This insures that all outputs of flip-flops do not change until after all flip-flops have been evaluated. Attempting to use non-blocking assignments in combinational logic paths to remove race conditions may only cause more problems. (In the preceding example, changing all statements to non-blocking assignments would not remove the race condition.) This includes using non-blocking assignments in the generation of gated clocks.

The following is an example of how to properly use non-blocking assignments.

```
gen1: always @(master)
    clk1 = master;

gen2: always @(clk1)
    clk2 = clk1;

f1 : always @(posedge clk1)
    begin
        q1 <= d1;
    end

f2:  always @(posedge clk2)
    begin
        q2 <= q1;
    end
```

If written this way, a value on *d1* always takes two clock cycles to get from *d1* to *q2*. If you change *clk1 = master* and *clk2 = clk1* to non-blocking assignments or *q2 <= q1* and *q1 <= d1* to blocking assignments, then *d1* may get to *q2* in less than two clock cycles.

Debugging Event Order Issues

Since many models have been developed on Verilog-XL, ModelSim tries to duplicate Verilog-XL event ordering to ease the porting of those models to ModelSim. However, ModelSim does not match Verilog-XL event ordering in all cases, and if a model ported to ModelSim does not behave as expected, then you should suspect that there are event order dependencies.

ModelSim helps you track down event order dependencies with the following compiler arguments: **-compat**, **-hazards**, and **-keep_delta**.

See the [vlog](#) command for descriptions of **-compat** and **-hazards**.

Hazard Detection

The `-hazards` argument to `vsim` detects event order hazards involving simultaneous reading and writing of the same register in concurrently executing processes. `vsim` detects the following kinds of hazards:

- **WRITE/WRITE** — Two processes writing to the same variable at the same time.
- **READ/WRITE** — One process reading a variable at the same time it is being written to by another process. ModelSim calls this a **READ/WRITE** hazard if it executed the read first.
- **WRITE/READ** — Same as a **READ/WRITE** hazard except that ModelSim executed the write first.

`vsim` issues an error message when it detects a hazard. The message pinpoints the variable and the two processes involved. You can have the simulator break on the statement where the hazard is detected by setting the **break on assertion** level to **Error**.

To enable hazard detection you must invoke `vlog` with the `-hazards` argument when you compile your source code and you must also invoke `vsim` with the `-hazards` argument when you simulate.

Note



Enabling `-hazards` implicitly enables the `-compat` argument. As a result, using this argument may affect your simulation results.

Hazard Detection and Optimization Levels

In certain cases hazard detection results are affected by the optimization level used in the simulation. Some optimizations change the read/write operations performed on a variable if the transformation is determined to yield equivalent results. Because the hazard detection algorithm cannot determine whether the read/write operations can affect the simulation results, the optimizations can result in different hazard detection results. Generally, the optimizations reduce the number of false hazards by eliminating unnecessary reads and writes, but there are also optimizations that can produce additional false hazards.

Limitations of Hazard Detection

- Reads and writes involving bit and part selects of vectors are not considered for hazard detection. The overhead of tracking the overlap between the bit and part selects is too high.
- A **WRITE/WRITE** hazard is flagged even if the same value is written by both processes.
- A **WRITE/READ** or **READ/WRITE** hazard is flagged even if the write does not modify the variable's value.

- Glitches on nets caused by non-guaranteed event ordering are not detected.
- A non-blocking assignment is not treated as a WRITE for hazard detection purposes. This is because non-blocking assignments are not normally involved in hazards. (In fact, they should be used to avoid hazards.)
- Hazards caused by simultaneous forces are not detected.

Debugging Signal Segmentation Violations

If you attempt to access a SystemVerilog object that has not been constructed with the **new** operator, you will receive a fatal error called a signal segmentation violation (SIGSEGV). For example, the following code produces a SIGSEGV fatal error:

```
class C;
  int x;
endclass

C obj;
initial obj.x = 5;
```

This attempts to initialize a property of *obj*, but *obj* has not been constructed. The code is missing the following:

```
C obj = new;
```

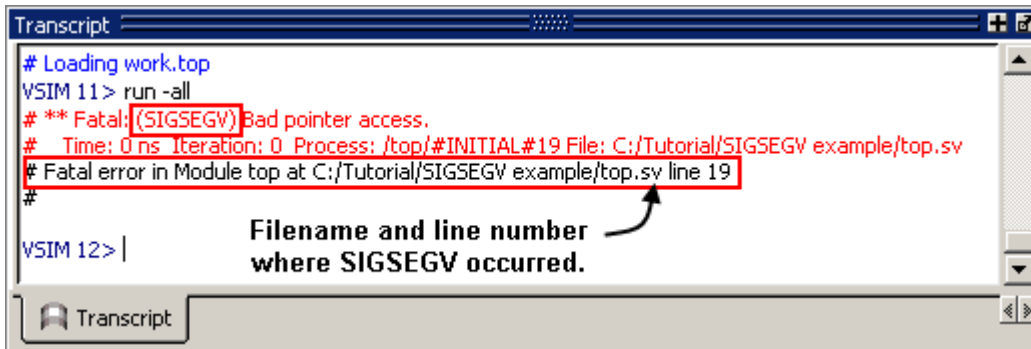
The **new** operator performs three distinct operations:

- Allocates storage for an object of type C
- Calls the “new” method in the class or uses a default method if the class does not define “new”
- Assigns the handle of the newly constructed object to “*obj*”

If the object handle *obj* is not initialized with **new**, there will be nothing to reference. ModelSim sets the variable to the value **null** and the SIGSEGV fatal error will occur.

To debug a SIGSEGV error, first look in the transcript. [Figure 8-1](#) shows an example of a SIGSEGV error message in the Transcript window.

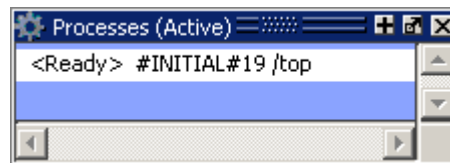
Figure 8-1. Fatal Signal Segmentation Violation (SIGSEGV)



The Fatal error message identifies the filename and line number where the code violation occurred (in this example, the file is *top.sv* and the line number is 38).

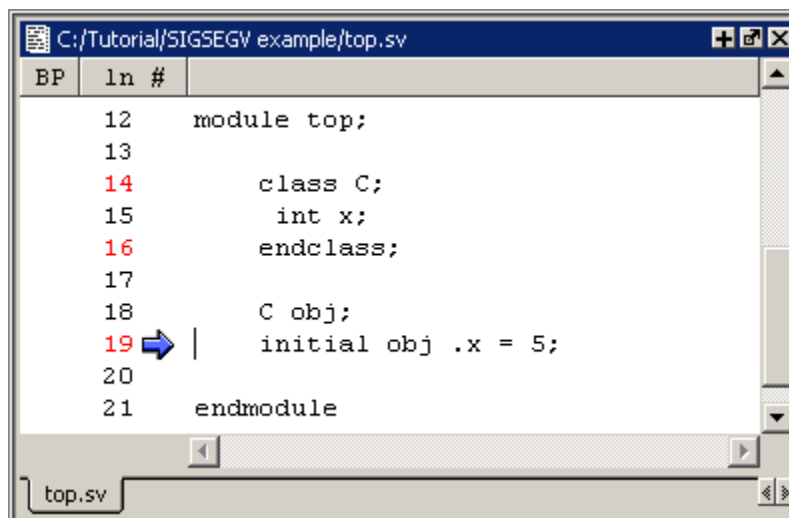
ModelSim sets the active scope to the location where the error occurred. In the Processes window, the current process is highlighted (Figure 8-2).

Figure 8-2. Current Process Where Error Occurred



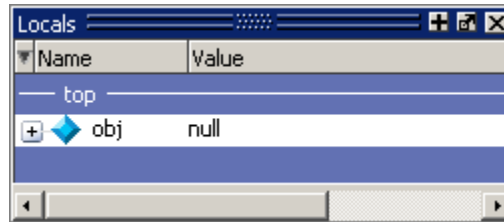
Double-click the highlighted process to open a Source window. A blue arrow will point to the statement where the simulation stopped executing (Figure 8-3).

Figure 8-3. Blue Arrow Indicates Where Code Stopped Executing



You may then look for *null* values in the ModelSim Locals window (Figure 8-4), which displays data objects declared in the current, or local, scope of the active process.

Figure 8-4. null Values in the Locals Window



The *null* value in Figure 8-4 indicates that the object handle for *obj* was not properly constructed with the **new** operator.

Negative Timing Checks

ModelSim automatically detects optimized cells with negative timing checks and causes timing checks to be performed on the delayed versions of input ports (used when there are negative timing check limits). This is the equivalent of applying the `+delayed_timing_checks` switch with the `vsim` command.

`vsim +delayed_timing_checks`

Appropriately applying `+delayed_timing_checks` will significantly improve simulation performance.

To turn off this feature, specify `+no_autodtc` with `vsim`.

Negative Timing Check Limits

By default, ModelSim supports negative timing check limits in Verilog `$setphold` and `$recrem` system tasks. Using the `+no_neg_tcheck` argument with the `vsim` command causes all negative timing check limits to be set to zero.

Models that support negative timing check limits must be written properly if they are to be evaluated correctly. These timing checks specify delayed versions of the input ports, which are used for functional evaluation. The correct syntax for `$setphold` and `$recrem` is as follows.

`$setphold`

Syntax

```
$setphold(clk_event, data_event, setup_limit, hold_limit, [notifier], [tstamp_cond],  
          [tcheck_cond], [delayed_clk], [delayed_data])
```

Arguments

- The *clk_event* argument is required. It is a transition in a clock signal that establishes the reference time for tracking timing violations on the *data_event*. Since `$setphold` combines the functionality of the `$setup` and `$hold` system tasks, the *clk_event* sets the lower bound event for `$hold` and the upper bound event for `$setup`.

- The *data_event* argument is required. It is a transition of a data signal that initiates the timing check. The *data_event* sets the upper bound event for \$hold and the lower bound limit for \$setup.
- The *setup_limit* argument is required. It is a constant expression or specparam that specifies the minimum interval between the *data_event* and the *clk_event*. Any change to the data signal within this interval results in a timing violation.
- The *hold_limit* argument is required. It is a constant expression or specparam that specifies the interval between the *clk_event* and the *data_event*. Any change to the data signal within this interval results in a timing violation.
- The *notifier* argument is optional. It is a register whose value is updated whenever a timing violation occurs. The *notifier* can be used to define responses to timing violations.
- The *tstamp_cond* argument is optional. It conditions the *data_event* for the setup check and the *clk_event* for the hold check. This alternate method of conditioning precludes specifying conditions in the *clk_event* and *data_event* arguments.
- The *tcheck_cond* argument is optional. It conditions the *data_event* for the hold check and the *clk_event* for the setup check. This alternate method of conditioning precludes specifying conditions in the *clk_event* and *data_event* arguments.
- The *delayed_clk* argument is optional. It is a net that is continuously assigned the value of the net specified in the *clk_event*. The delay is determined by the simulator and may be non-zero depending on all the timing check limits.
- The *delayed_data* argument is optional. It is a net that is continuously assigned the value of the net specified in the *data_event*. The delay is determined by the simulator and may be non-zero depending on all the timing check limits.

You can specify negative times for either the *setup_limit* or the *hold_limit*, but the sum of the two arguments must be zero or greater. If this condition is not met, ModelSim zeroes the negative limit during elaboration or SDF annotation. To see messages about this kind of problem, use the **+ntc_warn** argument with the **vsim** command. A typical warning looks like the following:

```
** Warning: (vsim-3616) cells.v(x): Instance 'dff0' - Bad $setuphold
constraints: 5 ns and -6 ns. Negative limit(s) set to zero.
```

The *delayed_clk* and *delayed_data* arguments are provided to ease the modeling of devices that may have negative timing constraints. The model's logic should reference the *delayed_clk* and *delayed_data* nets in place of the normal *clk* and *data* nets. This ensures that the correct data is latched in the presence of negative constraints. The simulator automatically calculates the delays for *delayed_clk* and *delayed_data* such that the correct data is latched as long as a timing constraint has not been violated. See [Using Delayed Inputs for Timing Checks](#) for more information.

Optional arguments not included in the task must be indicated as null arguments by using commas. For example:

```
$setuphold(posedge CLK, D, 2, 4, , , tcheck_cond);
```

The \$setuphold task does not specify *notifier* or *tstamp_cond* but does include a *tcheck_cond* argument. Notice that there are no commas after the *tcheck_cond* argument. Using one or more commas after the last argument results in an error.

Note

Do not condition a \$setuphold timing check using the *tstamp_cond* or *tcheck_cond* arguments and a conditioned event. If this is attempted, only the parameters in the *tstamp_cond* or *tcheck_cond* arguments will be effective, and a warning will be issued.

\$recrem

Syntax

```
$recrem(control_event, data_event, recovery_limit, removal_limit, [notifier], [tstamp_cond],  
        [tcheck_cond], [delayed_ctrl, [delayed_data])
```

Arguments

- The *control_event* argument is required. It is an asynchronous control signal with an edge identifier to indicate the release from an active state.
- The *data_event* argument is required. It is clock or gate signal with an edge identifier to indicate the active edge of the clock or the closing edge of the gate.
- The *recovery_limit* argument is required. It is the minimum interval between the release of the asynchronous control signal and the active edge of the clock event. Any change to a signal within this interval results in a timing violation.
- The *removal_limit* argument is required. It is the minimum interval between the active edge of the clock event and the release of the asynchronous control signal. Any change to a signal within this interval results in a timing violation.
- The *notifier* argument is optional. It is a register whose value is updated whenever a timing violation occurs. The *notifier* can be used to define responses to timing violations.
- The *tstamp_cond* argument is optional. It conditions the *data_event* for the removal check and the *control_event* for the recovery check. This alternate method of conditioning precludes specifying conditions in the *control_event* and *data_event* arguments.
- The *tcheck_cond* argument is optional. It conditions the *data_event* for the recovery check and the *clk_event* for the removal check. This alternate method of conditioning precludes specifying conditions in the *control_event* and *data_event* arguments.

- The *delayed_ctrl* argument is optional. It is a net that is continuously assigned the value of the net specified in the *control_event*. The delay is determined by the simulator and may be non-zero depending on all the timing check limits.
- The *delayed_data* argument is optional. It is a net that is continuously assigned the value of the net specified in the *data_event*. The delay is determined by the simulator and may be non-zero depending on all the timing check limits.

You can specify negative times for either the *recovery_limit* or the *removal_limit*, but the sum of the two arguments must be zero or greater. If this condition is not met, ModelSim zeroes the negative limit during elaboration or SDF annotation. To see messages about this kind of problem, use the **+ntc_warn** argument with the **vsim** command.

The *delayed_clk* and *delayed_data* arguments are provided to ease the modeling of devices that may have negative timing constraints. The model's logic should reference the *delayed_clk* and *delayed_data* nets in place of the normal *control* and *data* nets. This ensures that the correct data is latched in the presence of negative constraints. The simulator automatically calculates the delays for *delayed_clk* and *delayed_data* such that the correct data is latched as long as a timing constraint has not been violated.

Optional arguments not included in the task must be indicated as null arguments by using commas. For example:

```
$recrem(posedge CLK, D, 2, 4, , , tcheck_cond);
```

The \$recrem task does not specify *notifier* or *tstamp_cond* but does include a *tcheck_cond* argument. Notice that there are no commas after the *tcheck_cond* argument. Using one or more commas after the last argument results in an error.

Negative Timing Constraint Algorithm

The ModelSim negative timing constraint algorithm attempts to find a set of delays such that the data net is valid when the clock or control nets transition and the timing checks are satisfied. The algorithm is iterative because a set of delays that satisfies all timing checks for a pair of inputs can cause mis-ordering of another pair (where both pairs of inputs share a common input). When a set of delays that satisfies all timing checks is found, the delays are said to converge.

When none of the delay sets cause convergence, the algorithm pessimistically changes the timing check limits to force convergence. Basically, the algorithm zeroes the smallest negative \$setup/\$recovery limit. If a negative \$setup/\$recovery doesn't exist, then the algorithm zeros the smallest negative \$hold/\$removal limit. After zeroing a negative limit, the delay calculation procedure is repeated. If the delays do not converge, the algorithm zeros another negative limit, repeating the process until convergence is found.

For example, in this timing check,

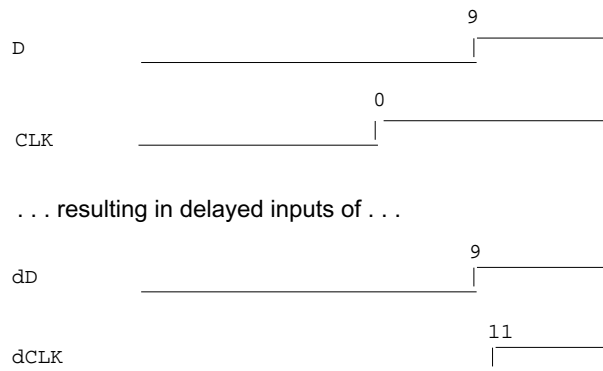
```
$setuphold(posedge CLK, D, -10, 20, notifier,, , dCLK, dD);
```

dCLK is the delayed version of the input *CLK* and *dD* is the delayed version of *D*. By default, the timing checks are performed on the inputs while the model's functional evaluation uses the delayed versions of the inputs. This posedge D-Flipflop module has a negative setup limit of -10 time units, which allows posedge *CLK* to occur up to 10 time units before the stable value of *D* is latched.



Without delaying *CLK* by 11, an old value for *D* could be latched. Note that an additional time unit of delay is added to prevent race conditions.

The inputs look like this:



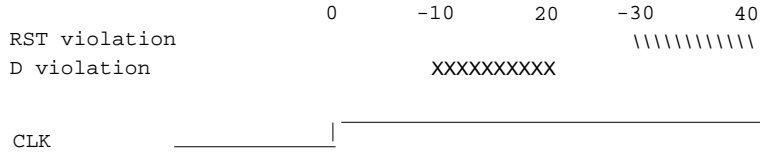
Because the posedge *CLK* transition is delayed by the amount of the negative setup limit (plus one time unit to prevent race conditions) no timing violation is reported and the new value of *D* is latched.

However, the effect of this delay could also affect other inputs with a specified timing relationship to *CLK*. The simulator is responsible for calculating the delay between all inputs and their delayed versions. The complete set of delays (delay solution convergence) must consider all timing check limits together so that whenever timing is met the correct data value is latched.

Consider the following timing checks specified relative to *CLK*:

\$setuphold(posedge CLK, D, -10, 20, notifier,,, dCLK, dD);

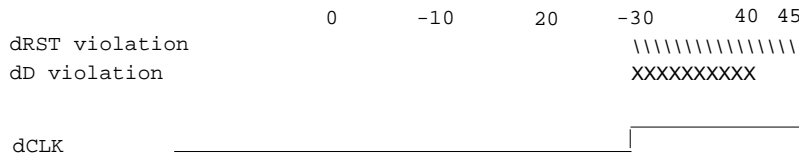
\$setuphold(posedge CLK, negedge RST, -40, 50, notifier,,, dCLK, dRST);



To solve the timing checks specified relative to *CLK* the following delay values are necessary:

	Rising	Falling
<i>dCLK</i>	31	31
<i>dD</i>	20	20
<i>dRST</i>	0	0

The simulator's intermediate delay solution shifts the violation regions to overlap the reference events.

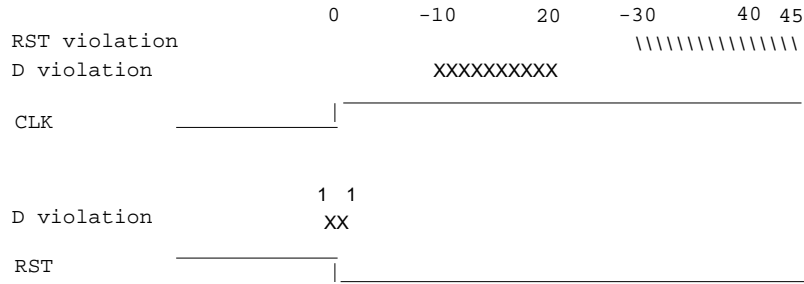


Notice that no timing is specified relative to *negedge CLK*, but the *dCLK* falling delay is set to the *dCLK* rising delay to minimize pulse rejection on *dCLK*. Pulse rejection that occurs due to delayed input delays is reported by:

```
"WARNING[3819] : Scheduled event on delay net dCLK was cancelled"
```

Now, consider the following case where a new timing check is added between *D* and *RST* and the simulator cannot find a delay solution. Some timing checks are set to zero. In this case, the new timing check is not annotated from an SDF file and a default \$setuphold limit of 1, 1 is used:

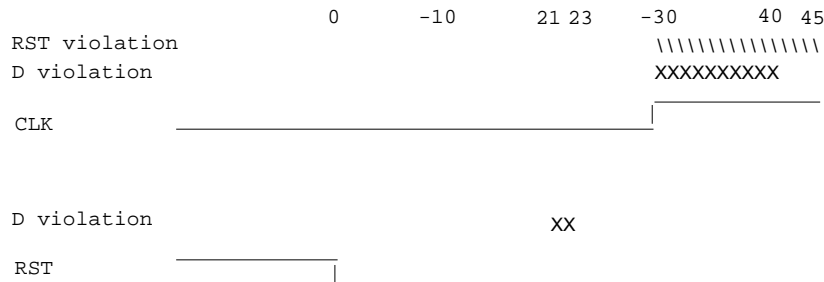
```
$setuphold(posedge CLK, D, -10, 20, notifier,,, dCLK, dD);
$setuphold(posedge CLK, negedge RST, -40, 50, notifier,,, dCLK, dRST);
$setuphold(negedge RST, D, 1, 1, notifier,,, dRST, dD);
```



As illustrated earlier, to solve timing checks on *CLK*, delays of 20 and 31 time units were necessary on *dD* and *dCLK*, respectively.

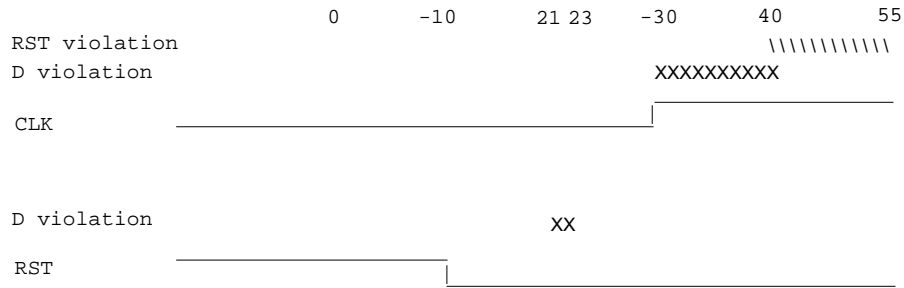
	Rising	Falling
<i>dCLK</i>	31	31
<i>dD</i>	20	20
<i>dRST</i>	0	0

The simulator's intermediate delay solution is:



But this is not consistent with the timing check specified between *RST* and *D*. The falling *RST* signal can be delayed by additional 10, but that is still not enough for the delay solution to converge.

	Rising	Falling
<i>dCLK</i>	31	31
<i>dD</i>	20	20
<i>dRST</i>	0	10



As stated above, if a delay solution cannot be determined with the specified timing check limits the smallest negative \$setup/\$recovery limit is zeroed and the calculation of delays repeated. If no negative \$setup/\$recovery limits exist, then the smallest negative \$hold/\$removal limit is zeroed. This process is repeated until a delay solution is found.

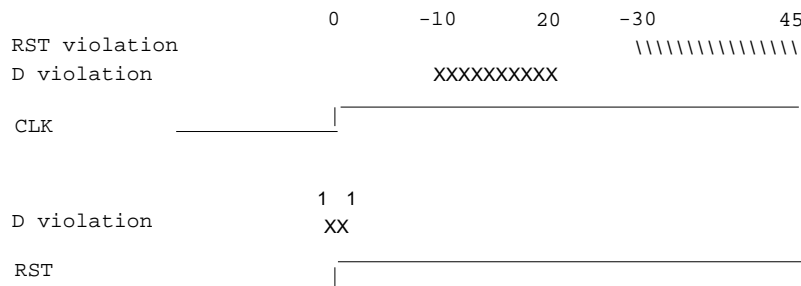
If a timing check in the design was zeroed because a delay solution was not found, a summary message like the following will be issued:

```
# ** Warning: (vsim-3316) No solution possible for some delayed timing
check nets. 1 negative limits were zeroed. Use +ntc_warn for more info.
```

Invoking `vsim` with the `+ntc_warn` option identifies the timing check that is being zeroed.

Finally consider the case where the *RST* and *D* timing check is specified on the posedge *RST*.

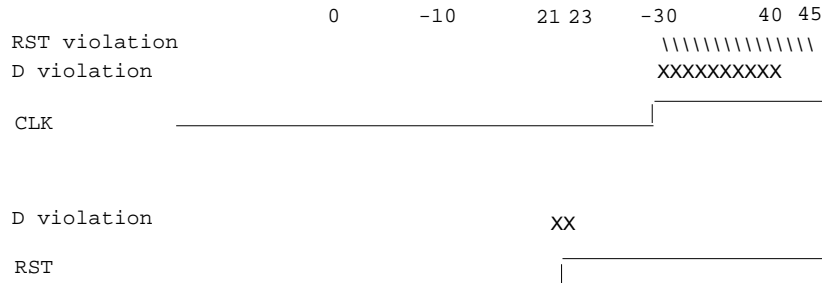
```
$setuphold(posedge CLK, D, -10, 20, notifier,,, dCLK, dD);
$setuphold(posedge CLK, negedge RST, -40, 50, notifier,,, dCLK, dRST);
$setuphold(posedge RST, D, 1, 1, notifier,,, dRST, dD);
```



In this case the delay solution converges when an rising delay on *dRST* is used.

	Rising	Falling
<i>dCLK</i>	31	31

	Rising	Falling
<i>dD</i>	20	20
<i>dRST</i>	20	10



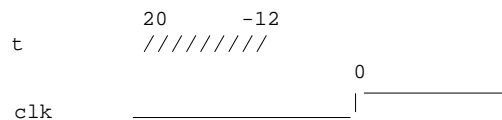
Using Delayed Inputs for Timing Checks

By default ModelSim performs timing checks on inputs specified in the timing check. If you want timing checks performed on the delayed inputs, use the **+delayed_timing_checks** argument to [vsim](#).

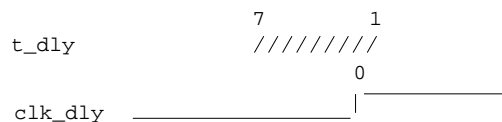
Consider an example. This timing check:

```
$setuphold(posedge clk, posedge t, 20, -12, NOTIFIER,,, clk_dly, t_dly);
```

reports a timing violation when posedge *t* occurs in the violation region:



With the **+delayed_timing_checks** argument, the violation region between the delayed inputs is:



Although the check is performed on the delayed inputs, the timing check violation message is adjusted to reference the undelayed inputs. Only the report time of the violation message is noticeably different between the delayed and undelayed timing checks.

By far the greatest difference between these modes is evident when there are conditions on a delayed check event because the condition is not implicitly delayed. Also, timing checks

specified without explicit delayed signals are delayed, if necessary, when they reference an input that is delayed for a negative timing check limit.

Other simulators perform timing checks on the delayed inputs. To be compatible, ModelSim supports both methods.

Verilog-XL Compatible Simulator Arguments

The simulator arguments listed below are equivalent to Verilog-XL arguments and may ease the porting of a design to ModelSim. See the [vsim](#) command for a description of each argument.

```
+alt_path_delays
-l <filename>
+maxdelays
+mindelays
+multisource_int_delays
+no_cancelled_e_msg
+no_neg_tchk
+no_notifier
+no_path_edge
+no_pulse_msg
-no_risefall_delaynets
+no_show_cancelled_e
+nosdfwarn
+nowarn<mnemonic>
+ntc_warn
+pulse_e/<percent>
+pulse_e_style_ondetect
+pulse_e_style_onevent
+pulse_int_e/<percent>
+pulse_int_r/<percent>
+pulse_r/<percent>
+sdf_nocheck_celltype
+sdf_verbose
+show_cancelled_e
+transport_int_delays
+transport_path_delays
+typdelays
```

Using Escaped Identifiers

ModelSim recognizes and maintains Verilog escaped identifier syntax. Prior to version 6.3, Verilog escaped identifiers were converted to VHDL-style extended identifiers with a backslash at the end of the identifier. Verilog escaped identifiers then appeared as VHDL extended identifiers in tool output and command line interface (CLI) commands. For example, a Verilog escaped identifier like the following:

```
\/top/dut/03
```

had to be displayed as follows:

```
\/top/dut/03\
```

Starting in version 6.3, all object names inside the simulator appear identical to their names in original HDL source files.

Sometimes, in mixed language designs, hierarchical identifiers might refer to both VHDL extended identifiers and Verilog escaped identifiers in the same fullpath. For example, `top\VHDL*ext\Vlog*ext/bottom` (assuming the `PathSeparator` variable is set to `'/'`), or `top.\VHDL*ext.\Vlog*ext.bottom` (assuming the `PathSeparator` variable is set to `'.'`) Any fullpath that appears as user input to the simulator (for example, on the `vsim` command line, in a `.do` file, on the `vopt` command line, and so forth) should be composed of components with escaped identifier syntax appropriate to its language kind.

A `modelsim.ini` variable called [GenerousIdentifierParsing](#) can control parsing of identifiers. input to the tool. If this variable is on (the variable is on by default: value = 1), either VHDL extended identifiers or Verilog escaped identifier syntax may be used for objects of either language kind. This provides backward compatibility with older `.do` files, which often contain pure VHDL extended identifier syntax, even for escaped identifiers in Verilog design regions.

Note that SDF files are always parsed in "generous mode." `SignalSpy` function arguments are also parsed in "generous mode."

On the `vsim` command line, the language-correct escaped identifier syntax should be used for top-level module names. Using incorrect escape syntax on the command line works in the incremental/debug flow, but not in the default optimized flow (see [Optimizing Designs with vopt](#)). This limitation may be removed in a future release.

Tcl and Escaped Identifiers

In Tcl, the backslash is one of a number of characters that have a special meaning. For example,

```
\n
```

creates a new line.

When a Tcl command is used in the command line interface, the TCL backslash should be escaped by adding another backslash. For example:

```
force -freeze /top/ix/iy/\yw\[1]\ 10 0, 01 {50 ns} -r 100
```

The Verilog identifier, in this example, is `\yw[1]`. Here, backslashes are used to escape the square brackets (`[]`), which have a special meaning in Tcl.

For a more detailed description of special characters in Tcl and how backslashes should be used with those characters, click **Help > Tcl Syntax** in the menu bar, or simply open the `docs/tcl_help_html/TclCmd` directory in your QuestaSim installation.

Cell Libraries

Mentor Graphics has passed the Verilog test bench from the ASIC Council and achieved the “Library Tested and Approved” designation from Si2 Labs. This test bench is designed to ensure Verilog timing accuracy and functionality and is the first significant hurdle to complete on the way to achieving full ASIC vendor support. As a consequence, many ASIC and FPGA vendors’ Verilog cell libraries are compatible with ModelSim Verilog.

The cell models generally contain Verilog “specify blocks” that describe the path delays and timing constraints for the cells. See Section 14 in the IEEE Std 1364-2005 for details on specify blocks, and Section 15 for details on timing constraints. ModelSim Verilog fully implements specify blocks and timing constraints as defined in IEEE Std 1364 along with some Verilog-XL compatible extensions.

SDF Timing Annotation

ModelSim Verilog supports timing annotation from Standard Delay Format (SDF) files. See [Standard Delay Format \(SDF\) Timing Annotation](#) for details.

Delay Modes

Verilog models may contain both distributed delays and path delays. The delays on primitives, UDPs, and continuous assignments are the distributed delays, whereas the port-to-port delays specified in specify blocks are the path delays. These delays interact to determine the actual delay observed. Most Verilog cells use path delays exclusively, with the distributed delays set to zero. For example,

```
module and2(y, a, b);
  input a, b;
  output y;
  and(y, a, b);
  specify
    (a => y) = 5;
    (b => y) = 5;
  endspecify
endmodule
```

In this two-input AND gate cell, the distributed delay for the AND primitive is zero, and the actual delays observed on the module ports are taken from the path delays. This is typical for most cells, but a complex cell may require non-zero distributed delays to work properly. Even so, these delays are usually small enough that the path delays take priority over the distributed delays. The rule is that if a module contains both path delays and distributed delays, then the larger of the two delays for each path shall be used (as defined by the IEEE Std 1364). This is the default behavior, but you can specify alternate delay modes with compiler directives and arguments. These arguments and directives are compatible with Verilog-XL. Compiler delay mode arguments take precedence over delay mode directives in the source code.

Distributed Delay Mode

In distributed delay mode, the specify path delays are ignored in favor of the distributed delays. You can specify this delay mode with the **+delay_mode_distributed** compiler argument or the **`delay_mode_distributed** compiler directive.

Path Delay Mode

In path delay mode, the distributed delays are set to zero in any module that contains a path delay. You can specify this delay mode with the **+delay_mode_path** compiler argument or the **`delay_mode_path** compiler directive.

Unit Delay Mode

In unit delay mode, the non-zero distributed delays are set to one unit of simulation resolution (determined by the minimum `time_precision` argument in all `'timescale` directives in your design or the value specified with the `-t` argument to `vsim`), and the specify path delays and timing constraints are ignored. You can specify this delay mode with the **+delay_mode_unit** compiler argument or the **`delay_mode_unit** compiler directive.

Zero Delay Mode

In zero delay mode, the distributed delays are set to zero, and the specify path delays and timing constraints are ignored. You can specify this delay mode with the **+delay_mode_zero** compiler argument or the **`delay_mode_zero** compiler directive.

System Tasks and Functions

ModelSim supports system tasks and functions as follows:

- All system tasks and functions defined in IEEE Std 1364
- Some system tasks and functions defined in SystemVerilog IEEE std 1800-2005 LRM
- Several system tasks and functions that are specific to ModelSim
- Several non-standard, Verilog-XL system tasks

The system tasks and functions listed in this section are built into the simulator, although some designs depend on user-defined system tasks implemented with the Programming Language Interface (PLI), Verilog Procedural Interface (VPI), or the SystemVerilog DPI (Direct Programming Interface). If the simulator issues warnings regarding undefined system tasks or functions, then it is likely that these tasks or functions are defined by a PLI/VPI application that must be loaded by the simulator.

IEEE Std 1364 System Tasks and Functions

The following supported system tasks and functions are described in detail in the IEEE Std 1364.

Note



The [change](#) command can be used to modify local variables in Verilog and SystemVerilog tasks and functions.

Table 8-4. IEEE Std 1364 System Tasks and Functions - 1

Timescale tasks	Simulator control tasks	Simulation time functions	Command line input
\$prinntimescale	\$finish	\$realtime	\$test\$plusargs
\$timeformat	\$stop	\$stime \$time	\$value\$plusargs

Table 8-5. IEEE Std 1364 System Tasks and Functions - 2

Probabilistic distribution functions	Conversion functions	Stochastic analysis tasks	Timing check tasks
\$dist_chi_square	\$bitstoreal	\$q_add	\$hold
\$dist_erlang	\$itor	\$q_exam	\$nochange
\$dist_exponential	\$realtobits	\$q_full	\$period
\$dist_normal	\$rtoi	\$q_initialize	\$recovery
\$dist_poisson	\$signed	\$q_remove	\$setup
\$dist_t	\$unsigned		\$setuphold
\$dist_uniform			\$skew
\$random			\$width ¹
			\$removal
			\$recrem

1. Verilog-XL ignores the threshold argument even though it is part of the Verilog spec. ModelSim does not ignore this argument. Be careful that you do not set the threshold argument greater-than-or-equal to the limit argument as that essentially disables the \$width check. Also, note that you cannot override the threshold argument by using SDF annotation.

Table 8-6. IEEE Std 1364 System Tasks

Display tasks	PLA modeling tasks	Value change dump (VCD) file tasks
\$display	\$async\$and\$array	\$dumpall
\$displayb	\$async\$nand\$array	\$dumpfile
\$displayh	\$async\$or\$array	\$dumpflush
\$displayo	\$async\$nor\$array	\$dumplimit
\$monitor	\$async\$and\$plane	\$dumpoff
\$monitorb	\$async\$nand\$plane	\$dumpon
\$monitorh	\$async\$or\$plane	\$dumpvars
\$monitoro	\$async\$nor\$plane	\$dumpportson
\$monitoroff	\$sync\$and\$array	\$dumpportsoff
\$monitoron	\$sync\$nand\$array	\$dumpportsall
\$strobe	\$sync\$or\$array	\$dumpportsflush
\$strobeb	\$sync\$nor\$array	\$dumpports
\$strobeh	\$sync\$and\$plane	\$dumpportslimit
\$strobeo	\$sync\$nand\$plane	
\$write	\$sync\$or\$plane	
\$writeb	\$sync\$nor\$plane	
\$writeh		
\$writeo		

Table 8-7. IEEE Std 1364 File I/O Tasks

File I/O tasks		
\$fclose	\$fmonitoro	\$fwriteh
\$fdisplay	\$fopen	\$fwriteo
\$fdisplayb	\$fread	\$readmemb
\$fdisplayh	\$fscanf	\$readmemh
\$fdisplayo	\$fseek	\$rewind
\$feof	\$fstrobe	\$sdf_annotate

Table 8-7. IEEE Std 1364 File I/O Tasks (cont.)

File I/O tasks

\$ferror	\$fstrobeb	\$sformat
\$fflush	\$fstrobeh	\$sscanf
\$fgetc	\$fstrobeo	\$swrite
\$fgets	\$ftell	\$swriteb
\$fmonitor	\$fwrite	\$swriteh
\$fmonitorb	\$fwriteb	\$swriteo
\$fmonitorh		\$sungetc

SystemVerilog System Tasks and Functions

The following ModelSim-supported system tasks and functions are described in detail in the SystemVerilog IEEE Std 1800-2005 LRM.

Table 8-8. SystemVerilog System Tasks and Functions - 1

Expression size function	Range function
\$bits	\$isunbounded

Table 8-9. SystemVerilog System Tasks and Functions - 2

Shortreal conversions	Array querying functions
\$shortrealbits	\$dimensions
\$bitstoshortreal	\$left
	\$right
	\$low
	\$high
	\$increment
	\$size

Table 8-10. SystemVerilog System Tasks and Functions - 4

Reading packed data functions	Writing packed data functions	Other functions
\$readmemb	\$writememb	\$root
\$readmemh	\$writememh	\$unit

System Tasks and Functions Specific to the Tool

The following system tasks and functions are specific to ModelSim. They are not included in the IEEE Std 1364, nor are they likely supported in other simulators. Their use may limit the portability of your code.

Table 8-11. Tool-Specific Verilog System Tasks and Functions

\$coverage_save	\$disable_signal_spy
\$messagelog	\$enable_signal_spy
\$psprintf()	\$init_signal_driver
\$sdf_done	\$init_signal_spy
	\$signal_force
	\$signal_release

[\\$coverage_save](#)

Syntax

`$coverage_save(<filename>, [<instancepath>], [<xml_output>])`

Description

The `$coverage_save()` system function saves only Code Coverage information to a file during a batch run that typically would terminate with the `$finish` call. It also returns a “1” to indicate that the coverage information was saved successfully or a “0” to indicate an error (unable to open file, instance name not found, and so forth.)

If you do not specify `<instancepath>`, ModelSim saves all coverage data in the current design to the specified file. If you do specify `<instancepath>`, ModelSim saves data on that instance, and all instances below it (recursively), to the specified file.

If set to 1, the `[<xml_output>]` argument specifies that the output be saved in XML format.

See [Code Coverage](#) for more information on Code Coverage.

\$messagelog

Syntax

```
$messagelog({"<message>", <value>...}[, ...]);
```

Arguments

- <message> — Your message, enclosed in quotes ("), using text and specifiers to define the output.
- <value> — A scope, object, or literal value that corresponds to the specifiers in the <message>. You must specify one <value> for each specifier in the <message>.

Specifiers

The \$messagelog task supports all specifiers available with the \$display system task. For more information about \$display, refer to section 17.1 of the IEEE std 1364-2005.

The following specifiers are specific to \$messagelog.

Note



The format of these custom specifiers differ from the \$display specifiers. Specifically, “%:” denotes a \$messagelog specifier and the letter denotes the type of specifier.

- %:C — Group/Category
A string argument, enclosed in quotes ("). This attribute defines a group or category used by the message system. If you do not specify %:C, the message system logs **User** as the default.
- %:F — Filename
A string argument specifying a simple filename, relative path to a filename, or a full path to a filename. In the case of a simple filename or relative path to a filename, the tool uses what you specify in the message output, but internally uses the current directory to complete these paths to form a full path: this allows the message viewer to link to the specified file.
If you do not include %:F, the tool automatically logs the value of the filename in which the \$messagelog is called.
If you do include %:R, %:F, or %:L, or a combination of any two of these, the tool does not automatically log values for the undefined specifier(s).
- %:I — Message ID
A string argument. The Message Viewer displays this value in the ID column. This attribute is not used internally, therefore you do not need to be concerned about uniqueness or conflict with other message IDs.
- %:L — Line number
An integer argument.

If you do not include `:%L`, the tool automatically logs the value of the line number on which the `$messagelog` is called.

If you do include `:%R`, `:%F`, or `:%L`, or a combination of any two of these, the tool does not automatically log values for the undefined specifier(s).

- `:%O` — Object/Signal Name

A hierarchical reference to a variable or net, such as `sig1` or `top.sigx[0]`. You can specify multiple `:%O` for each `$messagelog`, which effectively forms a list of attributes of that kind, for example:

```
$messagelog("The signals are %:O, %:O, and %:O.",
           sig1, top.sigx[0], ar [3].sig);
```

- `:%R` — Instance/Region name

A hierarchical reference to a scope, such as `top.sub1` or `sub1`. You can also specify a string argument, such as `"top.mychild"`, where the identifier inside the quotes does not need to correlate with an actual scope, it can be an artificial scope.

If you do not include `:%R`, the tool automatically logs the instance or region in which the `$messagelog` is called.

If you do include `:%R`, `:%F`, or `:%L`, or a combination of any two of these, the tool does not automatically log values for the undefined specifier(s).

- `:%S` — Severity Level

A case-insensitive string argument, enclosed in quotes (""), that is one of the following:

Note — This is the default if you do not specify `:%S`

Warning

Error

Fatal

Info — The error message system recognizes this as a Note

Message — The error message system recognizes this as a Note

- `:%V` — Verbosity Rating

An integer argument, where the default is zero (0). The verbosity rating allows you to specify a field you can use to sort or filter messages in the Message Viewer. In most cases you specify that this attribute is not printed, using the tilde (`~`) character.

Description

- Non-printing attributes (`~`) — You can specify that an attribute value is not to be printed in the transcribed message by placing the tilde (`~`) character after the percent (`%`) character, for example:

```
$messagelog("%:~S Do not print the Severity Level", "Warning");
```

However, the value of `:%S` is logged for use in the Message Viewer.

- Logging of simulation time — For each call to \$messagelog, the simulation time is logged, however the simulation time is not considered an attribute of the message system. This time is available in the Message Viewer.
- Minimum field-width specifiers — are accepted before each specifier character, for example:

```
%:0I  
%:10I
```

- Left-right justification specifier (-) — is accepted as it is for \$display.
- Macros — You can use the macros ‘__LINE__ (returns line number information) and ‘__FILE__ (returns filename information) when creating your \$messagelog tasks. For example:

```
module top;  
  
function void wrapper(string file, int line);  
    $messagelog("Hello: The caller was at %:F,%:0L", file, line);  
endfunction  
  
initial begin  
    wrapper(`__FILE__, `__LINE__);  
    wrapper(`__FILE__, `__LINE__);  
end  
  
endmodule
```

which would produce the following output

```
# Hello: The caller was at test.sv,7  
# Hello: The caller was at test.sv,8
```

Examples

- The following \$messagelog task:

```
$messagelog("hello world");
```

transcripts the message:

```
hello world
```

while logging all default attributes, but does not log a category.

- The following \$messagelog task:

```
$messagelog("%:~S%0t: PCI-X burst read started in transactor %:R",  
"Note", $time - 50, top.sysfixture.pcix);
```

transcripts the message:

```
150: PCI-X burst read started in transactor top.sysfixture.pcix
```

while silently logging the severity level of “Note”, and uses a direct reference to the Verilog scope for the %:R specifier, and does not log any attributes for %:F (filename) or %:L (line number).

- The following \$messagelog task:

```
$messagelog("%:~V%S %:C-%:I,%:L: Unexpected AHB interrupt received
in transactor %:R", 1, "Error", "AHB", "UNEXPINTRPT", `__LINE__,
ahbtop.c190);
```

transcripts the message:

```
** Error: AHB-UNEXPINTRPT,238: Unexpected AHB interrupt received in
transactor ahbtop.c190
```

where the verbosity level (%:V) is “1”, severity level (%:S) is “Error”, the category (%:C) is “AHB”, and the message identifier (%:I) is “UNEXPINTRPT”. There is a direct reference for the region (%:R) and the macro ‘__LINE__’ is used for line number (%:L), resulting in no attribute logged for %:F (filename).

\$sprintf()

Syntax

```
$sprintf()
```

Description

The \$sprintf() system function behaves like the \$format() file I/O task except that the string result is passed back to the user as the function return value for \$sprintf(), not placed in the first argument as for \$format(). Thus \$sprintf() can be used where a string is valid. Note that at this time, unlike other system tasks and functions, \$sprintf() cannot be overridden by a user-defined system function in the PLI.

\$sdf_done

Syntax

```
$sdf_done
```

Description

This task is a "cleanup" function that removes internal buffers, called MIPDs, that have a delay value of zero. These MIPDs are inserted in response to the -v2k_int_delay argument to the [vsim](#) command. In general, the simulator automatically removes all zero delay MIPDs. However, if you have \$sdf_annotate() calls in your design that are not getting executed, the zero-delay MIPDs are not removed. Adding the \$sdf_done task after your last \$sdf_annotate() removes any zero-delay MIPDs that have been created.

Verilog-XL Compatible System Tasks and Functions

ModelSim supports a number of Verilog-XL specific system tasks and functions.

Supported Tasks and Functions Mentioned in IEEE Std 1364

The following supported system tasks and functions, though not part of the IEEE standard, are described in an annex of the IEEE Std 1364.

\$countdrivers
\$getpattern
\$readmemb
\$readmemh

Supported Tasks and Functions Not Described in IEEE Std 1364

The following system tasks are also provided for compatibility with Verilog-XL, though they are not described in the IEEE Std 1364.

\$deposit(variable, value);

This system task sets a Verilog register or net to the specified value. **variable** is the register or net to be changed; **value** is the new value for the register or net. The value remains until there is a subsequent driver transaction or another \$deposit task for the same register or net. This system task operates identically to the ModelSim **force -deposit** command.

\$disable_warnings("<keyword>"[,<module_instance>...]);

This system task instructs ModelSim to disable warnings about timing check violations or triregs that acquire a value of 'X' due to charge decay. <keyword> may be **decay** or **timing**. You can specify one or more module instance names. If you do not specify a module instance, ModelSim disables warnings for the entire simulation.

\$enable_warnings("<keyword>"[,<module_instance>...]);

This system task enables warnings about timing check violations or triregs that acquire a value of 'X' due to charge decay. <keyword> may be **decay** or **timing**. You can specify one or more module instance names. If you do not specify a module_instance, ModelSim enables warnings for the entire simulation.

\$system("command");

This system function takes a literal string argument, executes the specified operating system command, and displays the status of the underlying OS process. Double quotes are required for the OS command. For example, to list the contents of the working directory on Unix:

```
$system("ls -l");
```

Return value of the **\$system** function is a 32-bit integer that is set to the exit status code of the underlying OS process.

Note

There is a known issue in the return value of this system function on the win32 platform. If the OS command is built with a cygwin compiler, the exit status code may not be reported correctly when an exception is thrown, and thus the return code may be wrong. The workaround is to avoid building the application using cygwin or to use the switch **-mno-cygwin** in cygwin the gcc command line.

\$systemf(list_of_args)

This system function can take any number of arguments. The list_of_args is treated exactly the same as with the \$display() function. The OS command that runs is the final output from \$display() given the same list_of_args. Return value of the \$systemf function is a 32-bit integer that is set to the exit status code of the underlying OS process.

Note

There is a known issue in the return value of this system function on the win32 platform. If the OS command is built with a cygwin compiler, the exit status code may not be reported correctly when an exception is thrown, and thus the return code may be wrong. The workaround is to avoid building the application using cygwin or to use the switch **-mno-cygwin** in cygwin the gcc command line.

Supported Tasks that Have Been Extended

The \$setuphold and \$recrem system tasks have been extended to provide additional functionality for negative timing constraints and an alternate method of conditioning, as in Verilog-XL. See [Negative Timing Check Limits](#).

Unsupported Verilog-XL System Tasks

The following system tasks are Verilog-XL system tasks that are not implemented in ModelSim Verilog, but have equivalent simulator commands.

\$input("filename")

This system task reads commands from the specified filename. The equivalent simulator command is **do <filename>**.

\$list[(hierarchical_name)]

This system task lists the source code for the specified scope. The equivalent functionality is provided by selecting a module in the Structure (sim) window. The corresponding source code is displayed in a Source window.

\$reset

This system task resets the simulation back to its time 0 state. The equivalent simulator command is **restart**.

\$restart("filename")

This system task sets the simulation to the state specified by filename, saved in a previous call to \$save. The equivalent simulator command is **restore <filename>**.

\$save("filename")

This system task saves the current simulation state to the file specified by filename. The equivalent simulator command is **checkpoint <filename>**.

\$scope(hierarchical_name)

This system task sets the interactive scope to the scope specified by hierarchical_name. The equivalent simulator command is **environment <pathname>**.

\$showscopes

This system task displays a list of scopes defined in the current interactive scope. The equivalent simulator command is **show**.

\$showvars

This system task displays a list of registers and nets defined in the current interactive scope. The equivalent simulator command is **show**.

Compiler Directives

ModelSim Verilog supports all of the compiler directives defined in the IEEE Std 1364, some Verilog-XL compiler directives, and some that are proprietary.

Many of the compiler directives (such as ``timescale`) take effect at the point they are defined in the source code and stay in effect until the directive is redefined or until it is reset to its default by a ``resetall` directive. The effect of compiler directives spans source files, so the order of source files on the compilation command line could be significant. For example, if you have a file that defines some common macros for the entire design, then you might need to place it first in the list of files to be compiled.

The ``resetall` directive affects only the following directives by resetting them back to their default settings (this information is not provided in the IEEE Std 1364):

```
`celldefine  
'default_decay_time  
'default_nettype  
'delay_mode_distributed  
'delay_mode_path  
'delay_mode_unit  
'delay_mode_zero  
'protect  
'timescale  
'unconnected_drive  
'uselib
```


ModelSim Verilog implicitly defines the following macro:

```
`define MODEL_TECH
```

IEEE Std 1364 Compiler Directives

The following compiler directives are described in detail in the IEEE Std 1364.

```
`celldefine  
`default_nettype  
`define  
`else  
`elsif  
`endcelldefine  
`endif  
`ifdef  
`ifndef  
`include  
`line  
`nounconnected_drive  
`resetall  
`timescale  
`unconnected_drive  
`undef
```

Compiler Directives for vlog

The following directives are specific to ModelSim and are not compatible with other simulators.

```
`protect ... `endprotect
```

This directive pair allows you to encrypt selected regions of your source code. The code in **`protect** regions has all debug information stripped out. This behaves exactly as if using:

```
vlog -nodebug=ports+pli
```

except that it applies to selected regions of code rather than the whole file. This enables usage scenarios such as making module ports, parameters, and specify blocks publicly visible while keeping the implementation private.

The **`protect** directive is ignored by default unless you use the `+protect` argument to `vlog`. Once compiled, the original source file is copied to a new file in the current work directory. The name of the new file is the same as the original file with a "p" appended to the suffix. For example, "top.v" is copied to "top.vp". This new file can be delivered and used as a replacement for the original source file.

A usage scenario might be that a vendor uses the **`protect** / **`endprotect** directives on a module or a portion of a module in a file named *encrypt.v*. They compile it with `vlog +protect encrypt.v` to produce a new file named *encrypt.vp*. You can compile *encrypt.vp* just like any other verilog file. The protection is not compatible between

tools, so the vendor must ship you a different *encrypt.vp* than they ship to some who uses a different simulator.

You can use **vlog +protect=<filename>** to create an encrypted output file, with the designated filename, in the current directory (not in the *work* directory, as in the default case where [=<filename>] is not specified). For example:

```
vlog test.v +protect=test.vp
```

If the filename is specified in this manner, all source files on the command line are concatenated together into a single output file. Any ``include` files are also inserted into the output file.

``protect` and ``endprotect` directives cannot be nested.

If errors are detected in a protected region, the error message always reports the first line of the protected block.

``include`

If any ``include` directives occur within a protected region, the compiler generates a copy of the include file with a *.vp* suffix and protects the entire contents of the include file. However, when you use `vlog +protect` to generate encrypted files, the original source files must all be complete Verilog modules or packages. Compiler errors result if you attempt to perform compilation of a set of parameter declarations within a module.

You can avoid such errors by creating a dummy module that includes the parameter declarations. For example, if you have a file that contains your parameter declarations and a file that uses those parameters, you can do the following:

```
module dummy;  
    `protect  
    `include "params.v" // contains various parameters  
    `include "tasks.v" // uses parameters defined in params.v  
    `endprotect  
endmodule
```

Then, compile the dummy module with the `+protect` switch to generate an encrypted output file with no compile errors.

```
vlog +protect dummy
```

After compilation, the work library contains encrypted versions of *params.v* and *tasts.v*, called *params.vp* and *tasks.vp*. You may then copy these encrypted files out of the work directory to more convenient locations. These encrypted files can be included within your design files; for example:

```
module main  
    `include "params.vp"  
    `include "tasks.vp"  
    ...  
endmodule
```

Though other simulators have a ``protect` directive, the algorithm ModelSim uses to encrypt source files is different. Hence, even though an uncompiled source file with ``protect` is compatible with another simulator, once the source is compiled in ModelSim, you could not simulate it elsewhere.

Verilog-XL Compatible Compiler Directives

The following compiler directives are provided for compatibility with Verilog-XL.

``default_decay_time <time>`

This directive specifies the default decay time to be used in trireg net declarations that do not explicitly declare a decay time. The decay time can be expressed as a real or integer number, or as "infinite" to specify that the charge never decays.

``delay_mode_distributed`

This directive disables path delays in favor of distributed delays. See [Delay Modes](#) for details.

``delay_mode_path`

This directive sets distributed delays to zero in favor of path delays. See [Delay Modes](#) for details.

``delay_mode_unit`

This directive sets path delays to zero and non-zero distributed delays to one time unit. See [Delay Modes](#) for details.

``delay_mode_zero`

This directive sets path delays and distributed delays to zero. See [Delay Modes](#) for details.

``uselib`

This directive is an alternative to the `-v`, `-y`, and `+libext` source library compiler arguments. See [Verilog-XL uselib Compiler Directive](#) for details.

The following Verilog-XL compiler directives are silently ignored by ModelSim Verilog. Many of these directives are irrelevant to ModelSim Verilog, but may appear in code being ported from Verilog-XL.

```
`accelerate
`autoexpand_vectornets
`disable_portfaults
`enable_portfaults
`expand_vectornets
`noaccelerate
`noexpand_vectornets
`noremove_gatenames
`noremove_netnames
`nosuppress_faults
`remove_gatenames
`remove_netnames
`suppress_faults
```

The following Verilog-XL compiler directives produce warning messages in ModelSim Verilog. These are not implemented in ModelSim Verilog, and any code containing these directives may behave differently in ModelSim Verilog than in Verilog-XL.

```
`default_trireg_strength
`sIGNED
`unsigned
```

Sparse Memory Modeling

Sparse memories are a mechanism for allocating storage for memory elements only when they are needed. You mark which memories should be treated as sparse, and ModelSim dynamically allocates memory for the accessed addresses during simulation.

Sparse memories are more efficient in terms of memory consumption, but access times to sparse memory elements during simulation are slower. Thus, sparse memory modeling should be used only on memories whose active addresses are "few and far between."

There are two methods of enabling sparse memories:

- “Manually” by inserting attributes or meta-comments in your code
- Automatically by setting the [SparseMemThreshold](#) variable in the *modelsim.ini* file

Manually Marking Sparse Memories

You can mark memories in your code as sparse using either the *mti_sparse* attribute or the *sparse* meta-comment. For example:

```
(* mti_sparse *) reg mem [0:1023]; // Using attribute
reg /*sparse*/ [0:7] mem [0:1023]; // Using meta-comment
```

The meta-comment syntax is supported for compatibility with other simulators.

You can identify memories as “not sparse” by using the +nosparse switch to [vlog](#) or [vopt](#).

Automatically Enabling Sparse Memories

Using the `SparseMemThreshold` .ini variable, you can instruct ModelSim to mark as sparse any memory that is a certain size. Consider this example:

If `SparseMemThreshold = 2048` then

```
reg mem[0:2047]; // will be marked as sparse automatically
reg mem[0:2046]; // will not be marked as sparse
```

The variable `SparseMemThreshold` is set, by default, to 1048576.

Combining Automatic and Manual Modes

Because `mti_sparse` is a Verilog 2001 attribute that accepts values, you can enable automatic sparse memory modeling but still control individual memories within your code. Consider this example:

If `SparseMemThreshold = 2048` then

```
reg mem[0:2047]; // will be marked as sparse automatically
reg mem[0:2046]; // will not be marked as sparse
```

However, you can override this automatic behavior using `mti_sparse` with a value:

```
(* mti_sparse = 0 *) reg mem[0:2047];
// will *not* be marked as sparse even though SparseMemThreshold = 2048

(* mti_sparse = 1*) reg mem[0:2046];
// will be marked as sparse even though SparseMemThreshold = 2048
```

Priority of Sparse Memories

The following list describes the priority in which memories are labeled as sparse or not sparse:

1. `vlog` or `vopt +nosparse[+]` — These memories are marked as "not sparse", where `vlog` options override `vopt` options.
2. metacomment `/* sparse */` or attribute `(* mti_sparse *)` — These memories are marked "sparse" or "not sparse" depending on the attribute value.
3. `SparseMemThreshold` .ini variable — Memories as deep as or deeper than this threshold are marked as sparse.

Determining Which Memories Were Implemented as Sparse

To identify which memories were implemented as sparse, use this command:

write report -l

The `write report` command lists summary information about the design, including sparse memory handling. You would issue this command if you are not certain whether a memory was successfully implemented as sparse or not. For example, you might add a `/*sparse*/` metacomment above a multi-D SystemVerilog memory, which is not supported. In that case, the simulation will function correctly, but ModelSim will use a non-sparse implementation of the memory.

If you are planning to optimize your design with `vopt`, be sure to use the `+acc` argument in order to make the sparse memory visible, thus allowing the `write report -l` command to report the sparse memory.

Limitations

There are certain limitations that exist with sparse memories:

- Sparse memories can have only one packed dimension. For example:

```
reg [0:3] [2:3] mem [0:1023]
```

has two packed dimensions and cannot be marked as sparse.

- Sparse memories can have only one unpacked dimension. For example:

```
reg [0:1] mem [0:1][0:1023]
```

has two unpacked dimensions and cannot be marked as sparse.

- Dynamic and associative arrays cannot be marked as sparse.
- Memories defined within a structure cannot be marked as sparse.
- PLI functions that get the pointer to the value of a memory will not work with sparse memories. For example, using the `tf_nodeinfo()` function to implement `$fread` or `$fwrite` will not work, because ModelSim returns a NULL pointer for `tf_nodeinfo()` in the case of sparse memories.
- Memories that have parameterized dimensions like the following example:

```
parameter MYDEPTH = 2048;  
reg [31:0] mem [0:MYDEPTH-1];
```

cannot be processed as a sparse memory *unless* the design has been optimized with the `vopt` command. In optimized designs, the memory is implemented as a sparse memory, and all parameter overrides to that `MYDEPTH` parameter are treated correctly.

Verilog PLI/VPI and SystemVerilog DPI

ModelSim supports the use of the Verilog PLI (Programming Language Interface) and VPI (Verilog Procedural Interface) and the SystemVerilog DPI (Direct Programming Interface).

These interfaces provide a mechanism for defining tasks and functions that communicate with the simulator through a C procedural interface. For more information on the ModelSim implementation, refer to [Verilog Interfaces to C](#).

Standards, Nomenclature, and Conventions

The QuestSim implementation of the Verilog VPI is based on the following standards:

- IEEE 1364-2005 and 1364-2001 (Verilog)
- IEEE 1800-2005 (SystemVerilog)

ModelSim supports partial implementation of the Verilog VPI. For release-specific information on currently supported implementation, refer to the following text file located in the ModelSim installation directory:

`<install_dir>/docs/technotes/Verilog_VPI.note`

Chapter 9

SystemC Simulation

This chapter describes how to compile and simulate SystemC designs with ModelSim. ModelSim implements the SystemC language based on the Open SystemC Initiative (OSCI) proof-of-concept SystemC simulator. This includes the Transaction Level Modeling (TLM) Library, Release 2.0. It is recommended that you obtain the OSCI functional specification, or the latest version of the *IEEE Standard SystemC Language Reference Manual* (IEEE Std 1666-2005).

Note



The functionality described in this chapter requires a systemc license feature in your ModelSim license file. To obtain this feature, please contact your Mentor Graphics sales representative.

In addition to the functionality described in the OSCI specification, ModelSim for SystemC includes the following features:

- Single common Graphic Interface for SystemC and HDL languages.
- Extensive support for mixing SystemC, VHDL, Verilog, and SystemVerilog in the same design (SDF annotation for HDL only). For detailed information on mixing SystemC with HDL see [Mixed-Language Simulation](#).

Supported Platforms and Compiler Versions

SystemC runs on a subset of ModelSim supported platforms. The table below shows the currently supported platforms and compiler versions:

Table 9-1. Supported Platforms for SystemC

Platform	Supported compiler versions	32-bit support	64-bit support
Intel and AMD x86-based architectures (32- and 64-bit) SUSE Linux Enterprise Server 9.0, 9.1, 10 Red Hat Enterprise Linux 3, 4, 5	gcc 4.0.2, gcc 4.1.2 VCO is linux (32-bit binary) VCO is linux_x86_64 (64-bit binary)	yes	yes
Solaris 8, 9, and 10	gcc 4.1.2	yes	no
Solaris 10 on x86	gcc 4.1.2	yes	yes

Table 9-1. Supported Platforms for SystemC

Platform	Supported compiler versions	32-bit support	64-bit support
Windows XP and Vista ¹	Minimalist GNU for Windows (MinGW) gcc 4.2.1	yes	no

1. SystemC supported on this platform with gcc-4.2.1-mingw32.

Note



ModelSim SystemC has been tested with the gcc versions provided in the install tree. It is strongly recommended to use the gcc version that came with your installation—customized versions of gcc may cause problems.

Building gcc with Custom Configuration Options

The gcc configuration for ModelSim has been qualified only for default options. If you use advanced gcc configuration options, ModelSim may not work with those options.

To use a custom gcc build, set the [CppPath](#) variable in the *modelsim.ini* file. This variable specifies the pathname to the compiler binary you intend to use.

When using a custom gcc, ModelSim requires that you build the custom gcc with several specific configuration options. These vary on a per-platform basis, as shown in the following table:

Table 9-2. Custom gcc Platform Requirements

Platform	Mandatory configuration options
Linux	none
Solaris	--with-gnu-ld --with-ld=/path/to/binutils-2.16/bin/ld --with-gnu-as --with-as=/path/to/binutils-2.16/bin/as
Solaris x86	--with-ld=/usr/ccs/bin/ld --with-gnu-as --with-as=/path/to/binutils-2.16/bin/as Cannot build gcc-4.x on sunos5x86 with gnu ld use /usr/ccs/bin/ld. GNU as (assembler) must be used to build the compiler.
Win32 (MinGW)	--with-gnu-as --with-gnu-ld

- `sjlj-exceptions` or `setjump longjump` exceptions do not work with SystemC. It can cause problems with catching exceptions thrown from `SC_THREAD` and `SC_CTHREAD`.

- Always build the compiler with `--disable-sjlj-exceptions` and never with `--enable-sjlj-exceptions`.
- `binutils-2.17` and `binutils-2.18` do not work. Do not attempt to use those on win32 at least.

If you do not have a GNU `binutils2.16` assembler and linker, you can use the `as` and `ld` programs. They are located inside the `gcc` in directory:

`<install_dir>/lib/gcc-lib/<gnuplatform>/<ver>`

The location of the `as` and `ld` executables has changed since `gcc-3.4`. For all `gcc-4.x` releases, `as` and `ld` are located in:

`<install_dir>/libexec/gcc/<gnuplatform>/<ver>`

By default ModelSim also uses the following options when configuring built-in `gcc`:

- `--disable-nls`
- `--enable-languages=c,c++`

These are not mandatory, but they do reduce the size of the `gcc` installation.

Usage Flow for SystemC-Only Designs

ModelSim allows users to simulate SystemC, either alone or in combination with other VHDL/Verilog modules. The following is an overview of the usage flow for strictly SystemC designs. More detailed instructions are presented in the sections that follow.

1. Create and map the working design library with the **`vlib`** and **`vmap`** statements, as appropriate to your needs.
2. If you are simulating `sc_main()` as the top-level, skip to step 3.

If you are simulating a SystemC top-level module instead, then modify the SystemC source code to export the top level SystemC design unit(s) using the `SC_MODULE_EXPORT` macro. See [Modifying SystemC Source Code](#) for details on how to convert `sc_main()` to an equivalent module.

3. Analyze the SystemC source using the `sccom` command, which invokes the native C++ compiler to create the C++ object files in the design library.

See [Using sccom in Addition to the Raw C++ Compiler](#) for information on when you are required to use **`sccom`** as opposed to another C++ compiler.

4. Perform a final link of the C++ source using `sccom -link`. This process creates a shared object file in the current work library which will be loaded by **`vsim`** at runtime.

`sccom -link` must be re-run before simulation if any new **`sccom`** compiles were performed.

5. Load the design into the simulator using the standard ModelSim `vsim` command.
6. Run the simulation using the `run` command, entered at the `VSIM>` command prompt.
7. Debug the design using ModelSim GUI features, including the Source and Wave windows.

Binding to Verilog or SystemVerilog Designs

The SystemVerilog **bind** construct allows you to bind a Verilog or SystemVerilog design unit to a SystemC module. This is especially useful for binding SystemVerilog assertions to your SystemC, VHDL, Verilog and mixed designs during verification. See [Using SystemVerilog bind Construct in Mixed-Language Designs](#).

Limitations of Bind Support for SystemC

There exists certain restrictions on actual expressions when binding to SystemC targets. If the target of a bind is a SystemC module or an instance of a SystemC module, expressions and literals are not supported as actuals. These include, but are not limited to,

- bitwise binary expressions using operators `&`, `|`, `~`, `^` and `^~`
- concatenation expression
- bit select and part select expressions
- variable/constant

Compiling SystemC Files

To compile SystemC designs, you must:

- create a design library
- modify SystemC source code if using design units as top-level
- run `sccom` SystemC compiler
- run SystemC linker (`sccom -link`)

Creating a Design Library for SystemC

Use `vlib` to create a new library in which to store the compilation results. For example:

```
vlib work
```

This creates a library named **work**. By default, compilation results are stored in the **work** library.

The **work** library is actually a subdirectory named `work`. This subdirectory contains a special file named `_info`.

Note



Do not create libraries using UNIX commands—always use the `vlib` command.

See [Design Libraries](#) for additional information on working with libraries.

Converting `sc_main()` to a Module

Since it is natural for simulators to elaborate design-unit(s) as tops, it is recommended that you use design units as your top-level rather than relying on `sc_main` based elaboration and simulation. There are a few limitations and requirements for running a `sc_main()` based simulation.

If you have a `sc_main()` based design and would like to convert it to a design-unit based one, a few modifications must be applied to your SystemC source code. To see example code containing the code modifications detailed in [Modifying SystemC Source Code](#), see [Code Modification Examples](#).

Exporting All Top Level SystemC Modules

For SystemC designs, you must export all top level modules in your design to ModelSim. You do this with the `SC_MODULE_EXPORT(<sc_module_name>)` macro. SystemC templates are not supported as top level or boundary modules. See [Templatized SystemC Modules](#). The `sc_module_name` is the name of the top level module to be simulated in ModelSim. You must specify this macro in a C++ source (`.cpp`) file. If the macro is contained in a header file instead of a C++ source file, an error may result.

Invoking the SystemC Compiler

ModelSim compiles one or more SystemC design units with a single invocation of `sccom`, the SystemC compiler. The design units are compiled in the order that they appear on the command line. For SystemC designs, all design units must be compiled just as they would be for any C++ compilation. An example of an `sccom` command might be:

```
sccom -I ../myincludes mytop.cpp mydut.cpp
```

Compiling Optimized and/or Debug Code

By default, `sccom` invokes the C++ compiler (`g++` or `aCC`) without any optimizations. If desired, you can enter any `g++/aCC` optimization arguments at the `sccom` command line.

Also, source level debug of SystemC code is not available by default in ModelSim. To compile your SystemC code for source level debugging in ModelSim, use the `g++/aCC -g` argument on the `sccom` command line.

Reducing Compilation Time for Non-Debug Simulations

If the SystemC objects in the design need not be visible in the ModelSim simulation database, you can save compilation time by running `sccom` with the `-nodebug` argument. This bypasses the parser which creates the ModelSim debug database. However, all files containing an `SC_MODULE_EXPORT()` macro call must NOT be compiled with the `sccom -nodebug` argument, otherwise the design fails to load.

This approach is useful if you are running a design in regression mode, or creating a library (.a) from the object files (.o) created by `sccom`, to be linked later with the SystemC shared object.

Specifying an Alternate g++ Installation

We recommend using the version of `g++` that is shipped with ModelSim on its various supported platforms. However, if you want to use your own installation, you can do so by setting the `CppPath` variable in the `modelsim.ini` file to the `g++` executable location.

For example, if your `g++` executable is installed in `/u/abc/gcc-4.2.1/bin`, then you would set the variable as follows:

```
CppPath /u/abc/gcc-4.2.1/bin/g++
```

Maintaining Portability Between OSCI and the Simulator

If you intend to simulate on both ModelSim and the OSCI proof-of-concept SystemC simulator, you can use the `MTI_SYSTEMC` macro to execute the ModelSim specific code in your design only when running ModelSim. `Sccom` defines this macro by default during compile time.

Using the original and modified code shown in the example shown in [Example 9-8](#), you might write the code as follows:

```
#ifndef MTI_SYSTEMC //If using the ModelSim simulator, sccom compiles this
SC_MODULE(mytop)
{
    sc_signal<bool> mysig;
    mymod mod;

    SC_CTOR(mytop)
        : mysig("mysig"),
          mod("mod")
    {
        mod.outp(mysig);
    }
};
```

```
SC_MODULE_EXPORT(top);

#else //Otherwise, it compiles this
int sc_main(int argc, char* argv[])
{
    sc_signal<bool> mysig;
    mymod mod("mod");
    mod.outp(mysig);

    sc_start(100, SC_NS);
}
#endif
```

Switching Platforms and Compilation

Compiled SystemC libraries are platform-dependent. If you move between platforms, you must remove all SystemC files from the working library and then recompile your SystemC source files. To remove SystemC files from the working directory, use the `vdel` command with the `-allsystemc` argument.

If you attempt to load a design that was compiled on a different platform, an error such as the following occurs:

```
# vsim work.test_ringbuf
# Loading work/systemc.so
# ** Error: (vsim-3197) Load of "work/systemc.so" failed:
work/systemc.so: ELF file data encoding not little-endian.
# ** Error: (vsim-3676) Could not load shared library
work/systemc.so for SystemC module 'test_ringbuf'.
# Error loading design
```

You can type **verror 3197** at the `vsim` command prompt and get details about what caused the error and how to fix it.

Using sccom in Addition to the Raw C++ Compiler

When compiling complex C/C++ test bench environments, it is common to compile code with many separate runs of the compiler. Often, you may compile code into archives (.a files), and then link the archives at the last minute using the `-L` and `-l` link options.

When using SystemC, you may also want to compile a portion of your C design using raw `g++` or `aCC` instead of `sccom`. (Perhaps you have some legacy code or some non-SystemC utility code that you want to avoid compiling with `sccom`.) You can do this; however, some cautions and rules apply.

Rules for sccom Use

The rules governing when and how you must use `sccom` are as follows:

- You must compile all code that references SystemC types or objects using `sccom`.

- When using **sccom**, you should not use the **-I** compiler option to point the compiler at any search directories containing OSCI or any other vendor supplied SystemC header files. **sccom** does this for you accurately and automatically.
- If you do use the raw C++ compiler to compile C/C++ functionality into archives or shared objects, you must then link your design using the **-L** and **-l** options with the **sccom -link** command. These options effectively pull the non-SystemC C/C++ code into a simulation image that is used at runtime.

Failure to follow the above rules can result in link-time or elaboration-time errors due to mismatches between the OSCI or any other vendor supplied SystemC header files and the ModelSim SystemC header files.

Rules for Using Raw g++ to Compile Non-SystemC C/C++ Code

If you use raw g++ to compile your non-systemC C/C++ code, the following rules apply:

1. The **-fPIC** option to g++ should be used during compilation with **sccom**.
2. For C++ code, you must use the built-in g++ delivered with ModelSim, or (if using a custom g++) use the one you built and specified with the **CppPath** variable in the *modelsim.ini* file.

Otherwise binary incompatibilities may arise between code compiled by **sccom** and code compiled by raw g++.

Compiling Changed Files Only (Incremental Compilation)

You can use **sccom -incr** to enable automatic incremental compilation so that only changed files are compiled. This allows ModelSim to determine which source files have changed and recompile only those source files.

A changed file is re-compiled in the following cases:

- Its pre-processor output is different from the last time it was successfully compiled (see [Note](#) below). This includes changes in included header files and to the source code itself.
- You invoke **sccom** with a different set of command-line options that have an impact on the gcc command line. Preserving all settings for the gcc command ensures that ModelSim re-compiles source files when a different version of gcc is used or when a platform changes.

Note

Pre-processor output is used because it prevents compilation on a file with the following types of changes:

- Access or modification time (touch)
 - Changes to comments—except changes to the source code that affect line numbers (such as adding a comment line) will cause all affected files to be recompiled. This occurs to keep debug information current so that ModelSim can trace back to the correct areas of the source code.
-

Example

The following example shows how to compile a SystemC design with automatic incremental compilation.

1. Run `sccom -incr` on three files and re-link all compiled files in the design.

```
% sccom -incr top.cpp and2.cpp or2.cpp
Model Technology ModelSim SE sccom DEV compiler 2003.05 Mar  2 2008
Exported modules:
    top
% sccom -incr -link
Model Technology ModelSim SE sccom DEV compiler 2003.05 Mar  2 2008
```

2. After changing functional content of the top module, re-compile and re-link.

```
% sccom -incr top.cpp and2.cpp or2.cpp
Model Technology ModelSim SE sccom DEV compiler 2003.05 Mar  2 2008

-- Skipping file and2.cpp
-- Skipping file or2.cpp

Exported modules:
    top

% sccom -incr -link
Model Technology ModelSim SE sccom DEV compiler 2003.05 Mar  2 2008
```

3. Link again without actually changing any file.

```
% sccom -incr -link
Model Technology ModelSim SE sccom DEV compiler 2003.05 Mar  2 2008
-- Skipping linking
```

Note

You must compile all included libraries (using `-lib`) with `-incr` for automatic incremental compilation to work in linking mode. Failing to do so generates an error.

Limitations

- Automatic incremental compile is only supported for source files compiled with sccom. ModelSim does not track files for changes if they are compiled directly using a C++ compiler.
- Physically moving the library that holds a shared object forces re-creating that shared object next time. This applies only to the directories holding the shared object, not to the libraries that hold object files.
- If the SystemC source file includes a static library, then any change in that static library will not cause ModelSim to recompile the source file.
- If a design file consists of more than one SystemC module, changing even one module causes ModelSim to recompile the entire source file (and all the modules contained in it), regardless of whether the other modules were changed or not.
- Automatic incremental archiving is not supported (if you use the `-archive` argument, the `-incr` argument has no effect).

Issues with C++ Templates

Templatized SystemC Modules

Templatized SystemC modules are not supported for use in the following locations:

- the top level of the design
- the boundary between SystemC and higher level HDL modules (for instance, the top level of the SystemC branch)

To convert a top level templatized SystemC module, you can either specialize the module to remove the template, or you can create a wrapper module that you can use as the top module.

For example, assume you have the following templatized SystemC module:

```
template <class T>
class top : public sc_module
{
    sc_signal<T> sig1;
    ...
};
```

You can specialize the module by setting `T = int`, thereby removing the template, as follows:

```
class top : public sc_module
{
    sc_signal<int> sig 1;
    ...
};
```

Or, alternatively, you could write a wrapper to be used over the template module:

```
class modelsim_top : public sc_module
{
    top<int> actual_top;
    ...
};

SC_MODULE_EXPORT(modelsim_top);
```

Organizing Templated Code

Suppose you have a class template, and it contains a certain number of member functions. All those member functions must be visible to the compiler when it compiles any instance of the class. For class templates, the C++ compiler generates code for each unique instance of the class template. Unless the compiler can read the full implementation of the class template, it cannot generate code for it, which leaves the invisible parts as undefined. Since it is legal to have undefined symbols in a *.so* file, **sccom -link** will not produce any errors or warnings. To make functions visible to the compiler, you must move them to the *.h* file.

Generating SystemC Verification Extensions

The data introspection for SystemC verification (SCV) depends on partial template specialization of a template called `scv_extensions`. This template extends data objects with the abstract interface `scv_extensions_if`. Each specialization of the `scv_extensions` template implements the `scv_extensions_if` interface in a way appropriate to the type in the template parameter.

This section introduces a utility (`sccom -dumpscvext`) that automatically generates SCV extensions for any given type of data object.

Usage

You must include the declaration of all types (for which you want extensions to be generated) in a header file.

For example, assume you want to generate extensions for `packet_t`.

1. Define a header file similar to the following:

```
typedef struct {
    int packet_type;
    int src;
    int dest;
    int payload;
}packet_t;
```

2. Creates a C++ file (*.cpp*) that includes all the header files that have all the type declarations and define a global variable for each type you want to extend.

Result: The C++ file for the above type looks like this:

```
#include "test.h"
packet_t pack;
```

3. For class templates, you need to instantiate each specialization.

For example, if `packet_t` were a class template, you could do something like this:

```
packet_t<int> pack1;
packet_t<long> pack2;
...
```

4. Run the `sccom -dumpscvext` command to dump SCV extensions for all the types for whom global variables have been defined in the C++ file.

sccom -dumpscvext mypacket.cpp

where `mypacket.cpp` is the name of the C++ file containing global variable definitions.

Result: The generated extensions are displayed in stdout (similar to the way `scgenmod` dumps a foreign module declaration).

Note



You must define global variables for all types for which extensions need to be generated. The `sccom -dumpscvext` command will cause an error out if it cannot find any global variables defined in the supplied C++ file.

The command also automatically inserts the following header in `mypacket.cpp` with the generated extensions:

```
#ifndef TYPENAME_H
#define TYPENAME_H
#include "scv.h"
<generated extensions>

#endif
```

Note



If extensions are generated for more than one type, the type name of the first type will be used as `TYPENAME` in the `ifndef` preprocessor.

Supported Object Types

Table 9-3 shows the target list of simple data types that are supported by the `sccom -dumpscvext` command, along with the extension generated for each type.

Table 9-3. Generated Extensions for Each Object Type

SystemC Data Object Type	Generated Extension
bool	scv_extensions<bool>

Table 9-3. Generated Extensions for Each Object Type

SystemC Data Object Type	Generated Extension
char	scv_extensions<char>
short	scv_extensions<short>
int	scv_extensions<int>
long	scv_extensions<long>
long long	scv_extensions<long long>
unsigned char	scv_extensions<unsigned char>
unsigned short	scv_extensions<unsigned short>
unsigned int	scv_extensions<unsigned int>
unsigned long	scv_extensions<unsigned long>
unsigned long long	scv_extensions<unsigned long long>
float	scv_extensions<float>
double	scv_extensions<double>
string	scv_extensions<string>
pointer	scv_extensions<T*>
array	scv_extensions<T[N]>
sc_string	scv_extensions<sc_string>
sc_bit	scv_extensions<sc_bit>
sc_logic	scv_extensions<sc_logic>
sc_int	scv_extensions<sc_int<W>>
sc_uint	scv_extensions<sc_uint<W>>
sc_bigint	scv_extensions<sc_bigint<W>>
sc_biguint	scv_extensions<sc_biguint<W>>
sc_bv	scv_extensions<sc_bv<W>>
sc_lv	scv_extensions<sc_lv<W>>

SCV Extensions for User-specified Types

This section explains the rules for generating SCV extensions for user-specified types such as structures, unions, classes, and enums.

Structures and Classes

Note the following set of rules for generating a SCV extensions for a structure or class:

- Generated extensions start with macro `SCV_EXTENSIONS()`, and typename is the name of the user-specified type.
- All types in the generated extension are public and follow the same mapping table as simple types.
- Private members of the struct/class are ignored unless the extensions class is made a friend of the user-specified type. In the latter case, all private members of the class are made public in the generated extension.
- Generated extensions contain a constructor defined by the macro `SCV_EXTENSIONS_CTOR()`, and typename is the name of the user-specified type.
- A `SCV_FIELD` entry is added in constructor for each generated extension.

The following examples demonstrate the generation process for a structure and class types.

Example 9-1. Generating SCV Extensions for a Structure

```
/* SystemC type */

struct packet_t {
    sc_uint<8> addr;
    sc_uint<12> data;
};

/* Generated SCV Extention */

SCV_EXTENSIONS(packet_t) {
    public:
        scv_extensions< sc_uint<8> > addr;
        scv_extensions< sc_uint<12> > data;

        SCV_EXTENSIONS_CTOR(packet_t) {
            SCV_FIELD(addr);
            SCV_FIELD(data);
        }
};
```

Example 9-2. Generating SCV Extensions for a Class without Friend (Private Data Not Generated)

```
/* SystemC type */

class restricted_t {
    public:
        sc_uint<8> public_data;
    private:
        sc_uint<8> private_data;
```

```
};

/* Generated SCV Extension */

SCV_EXTENSIONS(restricted_t) {
    public:
        scv_extensions< sc_uint<8> > public_data;

        SCV_EXTENSIONS_CTOR(restricted_t) {
            SCV_FIELD(public_data);
        }
};
```

Example 9-3. Generating SCV Extensions for a Class with Friend (Private Data Generated)

```
/* SystemC type */

class restricted_t {
    friend class scv_extensions<restricted_t>;

    public:
        sc_uint<8> public_data;
    private:
        sc_uint<8> private_data;
};

/* Generated SCV Extension */

SCV_EXTENSIONS(restricted_t) {
    public:
        scv_extensions< sc_uint<8> > public_data;
        scv_extensions< sc_uint<8> > private_data;

        SCV_EXTENSIONS_CTOR(restricted_t) {
            SCV_FIELD(public_data);
            SCV_FIELD(private_data);
        }
};
```

Enums

Note the following set of rules for generating a SCV extensions for enumerated types:

- Generated extensions start with macro `SCV_ENUM_EXTENSIONS()`, and typename is the name of the enumerated type.
- Generated extensions consists of only a constructor defined by the macro `SCV_ENUM_CTOR()`, and typename is the name of the user-specified type.
- A `SCV_ENUM` entry are added in constructor for each element of the enumerated type.

The following example demonstrates the generation process for an enumerated type.

Example 9-4. Generating SCV Extensions for an Enumerated Type

```
/* SystemC type */
enum instruction_t { ADD, SUB = 201 };

/* Generated SCV Extension */

SCV_ENUM_EXTENSIONS(instruction_t) {
    public:

    SCV_ENUM_CTOR(instruction_t) {
        SCV_ENUM(ADD);
        SCV_ENUM(SUB);
    }
};
```

Mentor Dynamic Extensions

The OSCI-SCV library has been modified to support Mentor Dynamic Extensions, which allow the following:

- [Named Constraints](#)
- [Dynamic Enabling and Disabling of Named Constraints](#)
- [Constrained Randomization of the Data Type for Standard Vectors](#)
- [Randomly Sized Fixed-Max Arrays](#)

Named Constraints

The open SCV API supports the following macros for creating constraint data expression initializers data member fields of a user-defined constraint, based on a derivation of class `scv_constraint_base`:

```
#define SCV_CONSTRAINT(expr)
#define SCV_SOFT_CONSTRAINT(expr)
```

The first defines a hard constraint and the second defines a soft constraint.

The following example shows a user-defined constraint that uses these macros in the SCV constraint constructor macro, `SCV_CONSTRAINT_CTOR()`.

Example 9-5. User-Defined Constraint

```
class EtherFrameConstraintT : virtual public scv_constraint_base {
public:
    scv_smart_ptr<unsigned> Type;
    scv_smart_ptr<unsigned long long> DestAddr;
    scv_smart_ptr<unsigned long long> SrcAddr;
    scv_smart_ptr<unsigned> CRC;
    scv_smart_ptr<EtherFramePayloadT> Payload;
```



```
SCV_CONSTRAINT_CTOR( EtherFrameConstraintT ){
    printf( "Start initializing EtherFrameConstraint ...\n" );
    SCV_CONSTRAINT( Type() == (SDF_BYTE << 8 | SDF_BYTE) );
    SCV_CONSTRAINT( DestAddr() != SrcAddr() );
    SCV_CONSTRAINT( DestAddr() < 0xffLL ); // Limit to 48 bits
    SCV_CONSTRAINT( SrcAddr() < 0xffLL ); // Limit to 48 bits
}
};
```

To augment these macros, the following macro allows a constraint field to be named:

```
#define SCV_NAMED_CONSTRAINT(type, name, expr)
```

which uses the following arguments:

- `type` — the type of the constraint (HARD/SOFT), specified as `scv_constraint_expr::scv_constraint_type`.
- `name` — the actual name given to the constraint.
- `expr` — the expression argument that is passed exactly as in the existing macros `SCV_CONSTRAINT()` and `SCV_SOFT_CONSTRAINT()`.

To support the constraint type (hard or soft), the following class is defined with an enum type that you can use specify type:

```
class scv_constraint_expr {
public:
    typedef enum { HARD, SOFT } scv_constraint_type;
    scv_constraint_expr(
        const char* name, scv_constraint_type type, scv_expression e,
        const char* file = "unknown", int line = 0 );

    const char *name() const;
    const char *file() const;
    int line() const;

    void disable();
    void enable();
    bool is_disabled() const;
};
```

When the constraint is created, the file name and line # are captured in the class `scv_constraint_expr` object so that it can be provided later to parts of the internal SCV implementation for reporting purposes, such as error messages. You can do this by referencing the ANSI C `FILE` and `LINE` directives at the point where the name constraint is constructed.

Accessors `::name()`, `::file()`, and `::line()` are provided to class `scv_constraint_expr` as shown above to provide this information for messaging, if needed.

Dynamic Enabling and Disabling of Named Constraints

You can enable and disable constraints that have been created with names in accordance with the naming macro described in [Named Constraints](#) (above). To support this feature, class `scv_constraint_base` contains the following methods:

```
class scv_constraint_base {
    ...
public:
    ...
    bool disable_constraint( const char* name );
    bool enable_constraint( const char* name );
    ...
};
```

You can use these methods to enable or disable any named constraint field in a user-defined constraint object derived from class `scv_constraint_base`. The implementation of class `scv_constraint_base` can use names as lookup keys to an internal table of class `scv_constraint_expr` objects. Once looked up, you can call the `::enable()` or `::disable()` method on those objects appropriately.

Constrained Randomization of the Data Type for Standard Vectors

The data type for standard vectors (`std::vector`) has a data introspection capability in the same way that fixed arrays and other primitive data types do. This means you can define SCV extensions for vectors by specifying `scv_extensions< vector >` in a manner similar to what is supported for arrays: `scv_extensions< T[N] >`.

In addition to being able to randomize all elements of a C++ STL `std::vector`, the SCV constraint solver can randomize the number of elements of a `std::vector` (its size) to an arbitrary value.

Further, you can constrain this randomization of vector size simply by calling `vector_size.keep_only()` on the `::vector_size` member of the `scv_extensions< vector >` class. The `::keep_only()` method can be given a range of values that size can assume.

Randomly Sized Fixed-Max Arrays

This randomly sized "fixed-max" feature for array types was originally provided to test preliminary implementations of randomization support for the `std::vector` data type. However, it is also useful feature for randomization of the number of elements in an array up to a fixed maximum size denoted by the template `N` parameter of `scv_extensions< T[N] >`.

It is fully backward compatible with existing support for array (`scv_extensions< T[N] >`) support in the current open SCV API; randomization of size is disabled by default for backward compatibility, but you can enable it as needed. Default operation is for all `N` elements to be randomized as is done in the open SCV API.

Further, you can constrain this randomization simply by calling `vector_size.keep_only()` on the `::vector_size` member of the `scv_extensions< T[N] >` class. The `::keep_only()` method can be given a range of values that size can assume.

Linking the Compiled Source

Once the design has been compiled, you must link it using the `sccom` command with the **-link** argument.

The **sccom -link** command collects the object files created in the different design libraries, and uses them to build a shared library (.so) in the current work library or the library specified by the **-work** option. If you have changed your SystemC source code and recompiled it using **sccom**, then you must relink the design by running **sccom -link** before invoking **vsim**. Otherwise, your changes to the code are not recognized by the simulator. Remember that any dependent .a or .o files should be listed on the **sccom -link** command line before the .a or .o on which it depends. For more details on dependencies and other syntax issues, see [sccom](#).

Simulating SystemC Designs

After compiling the SystemC source code, you can simulate your design with `vsim`.

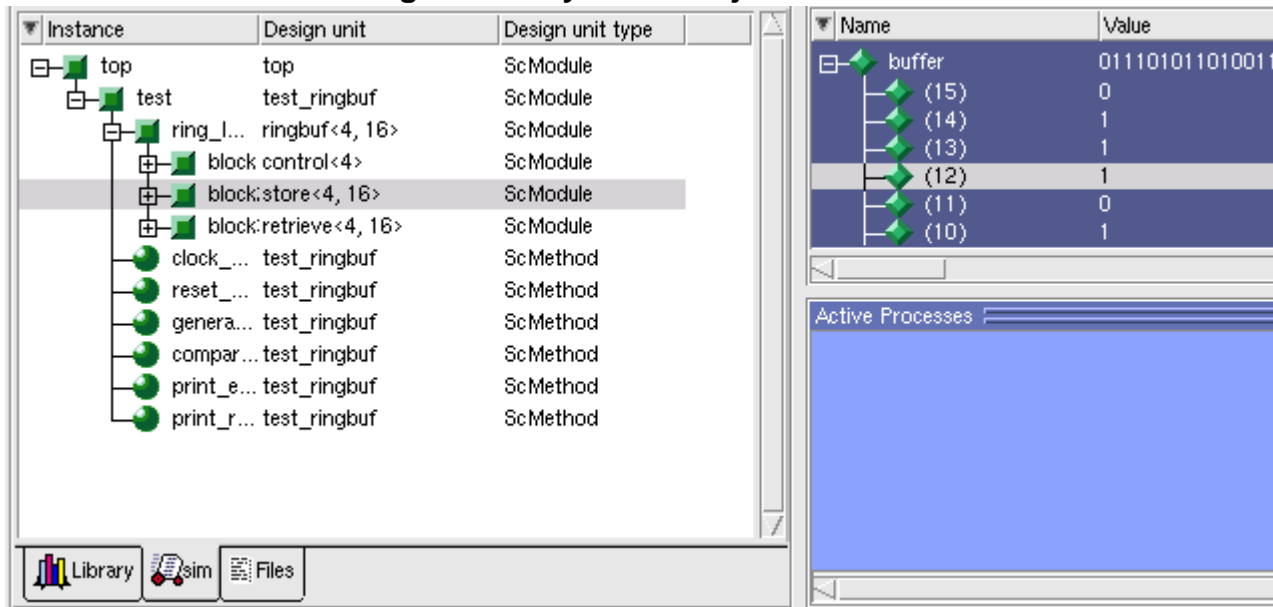
Loading the Design

For SystemC, invoke `vsim` with the top-level module of the design. This example invokes `vsim` on a design named `top`:

```
vsim top
```

When the GUI comes up, you can expand the hierarchy of the design to view the SystemC modules. SystemC objects are denoted by green icons (see [Design Object Icons and Their Meaning](#) for more information).

Figure 9-1. SystemC Objects in GUI



To simulate from a command shell, without the GUI, invoke vsim with the -c option:

```
vsim -c <top_level_module>
```

For instructions on how to run a design with sc_main() as the top level, see [Using sc_main as Top Level](#).

Running Simulation

Run the simulation using the [run](#) command or select one of the **Simulate > Run** options from the menu bar.

SystemC Time Unit and Simulator Resolution

This section applies to SystemC only simulations. For simulations of mixed-language designs, the rules for how ModelSim interprets the resolution vary. See [Simulator Resolution Limit](#) for details on mixed-language simulations.

Two related yet distinct concepts are involved with determining the simulation resolution: the SystemC time unit and the simulator resolution. The following table describes the concepts, lists the default values, and defines the methods for setting/overriding the values.

Table 9-4. Time Unit and Simulator Resolution

	Description	Set by default as <i>.ini</i> file	Default value	Override default by
SystemC time unit	The unit of time used in your SystemC source code. You need to set this in cases where your SystemC default time unit is at odds with any other, non-SystemC segments of your design.	ScTimeUnit	1ns	ScTimeUnit <i>.ini</i> file variable or <code>sc_set_default_time_unit()</code> function before an <code>sc_clock</code> or <code>sc_time</code> statement.
Simulator resolution	The smallest unit of time measured by the simulator. If your delays get truncated, set the resolution smaller; this value must be less than or equal to the UserTimeUnit	Resolution	1ns	<code>-t</code> argument to <code>vsim</code> (This overrides all other resolution settings.) or <code>sc_set_time_resolution()</code> function or GUI: Simulate > Start Simulation > Resolution

Available settings for both time unit and resolution are: 1x, 10x, or 100x of fs, ps, ns, us, ms, or sec.

You can view the current simulator resolution by invoking the [report](#) command with the **simulator state** option.

Choosing Your Simulator Resolution

You should choose the coarsest simulator resolution limit possible that does not result in undesired rounding of your delays. However, the time precision should also not be set unnecessarily small, because in some cases performance will be degraded.

When deciding what to set the simulator's resolution to, you must keep in mind the relationship between the simulator's resolution and the SystemC time units specified in the source code. For example, with a time unit usage of:

```
sc_wait(10, SC_PS);
```

a simulator resolution of 10ps would be fine. No rounding off of the ones digits in the time units would occur. However, a specification of:

```
sc_wait(9, SC_PS);
```

would require you to set the resolution limit to 1ps in order to avoid inaccuracies caused by rounding.

Initialization and Cleanup of SystemC State-Based Code

State-based code should not be used in Constructors and Destructors. Constructors and Destructors should be reserved for creating and destroying SystemC design objects, such as `sc_modules` or `sc_signals`. State-based code should also not be used in the elaboration phase callbacks **before_end_of_elaboration()** and **end_of_elaboration()**.

The following virtual functions should be used to initialize and clean up state-based code, such as logfiles or the VCD trace functionality of SystemC. They are virtual methods of the following classes: `sc_port_base`, `sc_module`, `sc_channel`, and `sc_prim_channel`. You can think of them as phase callback routines in the SystemC language:

- `before_end_of_elaboration ()` — Called after all constructors are called, but before port binding.
- `end_of_elaboration ()` — Called at the end of elaboration after port binding.
- `start_of_simulation ()` — Called before simulation starts. Simulation-specific initialization code can be placed in this function.
- `end_of_simulation ()` — Called before ending the current simulation session.

The call sequence for these functions with respect to the SystemC object construction and destruction is as follows:

1. Constructors
2. `before_end_of_elaboration ()`
3. `end_of_elaboration ()`
4. `start_of_simulation ()`
5. `end_of_simulation ()`
6. Destructors

Usage of Callbacks

The **start_of_simulation()** callback is used to initialize any state-based code. The corresponding cleanup code should be placed in the **end_of_simulation()** callback. These callbacks are only called during simulation by **vsim** and thus, are safe.

If you have a design in which some state-based code must be placed in the constructor, destructor, or the elaboration callbacks, you can use the `mti_IsVoptMode()` function to determine if the elaboration is being run by `vopt`. You can use this function to prevent `vopt` from executing any state-based code.

Debugging the Design

You can debug SystemC designs using all the debugging features of ModelSim, with the exception of the Dataflow window. You must have compiled the design using the `sccom -g` argument in order to debug the SystemC objects in your design.

Viewable SystemC Types

Types (<type>) of the objects which may be viewed for debugging are the following:

Types

<code>bool, sc_bit</code>	<code>short, unsigned short</code>
<code>sc_logic</code>	<code>long, unsigned long</code>
<code>sc_bv<width></code>	<code>sc_bigint<width></code>
<code>sc_lv<width></code>	<code>sc_biguint<width></code>
<code>sc_int<width></code>	<code>sc_ufixed<W,I,Q,O,N></code>
<code>sc_uint<width></code>	<code>short, unsigned short</code>
<code>sc_fix</code>	<code>long long, unsigned long long</code>
<code>sc_fix_fast</code>	<code>float</code>
<code>sc_fixed<W,I,Q,O,N></code>	<code>double</code>
<code>sc_fixed_fast<W,I,Q,O,N></code>	<code>enum</code>
<code>sc_ufix</code>	<code>pointer</code>
<code>sc_ufix_fast</code>	<code>array</code>
<code>sc_ufixed</code>	<code>class</code>
<code>sc_ufixed_fast</code>	<code>struct</code>
<code>sc_signed</code>	<code>union</code>
<code>sc_unsigned</code>	<code>ac_int</code>
<code>char, unsigned char</code>	<code>ac_fixed</code>
<code>int, unsigned int</code>	

Viewable SystemC Objects

Objects which may be viewed in SystemC for debugging purposes are as shown in the following table.

Table 9-5. Viewable SystemC Objects

Channels	Ports	Variables	Aggregates
sc_clock (a hierarchical channel) sc_event sc_export sc_mutex sc_fifo<type> sc_signal<type> sc_signal_rv<width> sc_signal_resolved tlm_fifo<type> User defined channels derived from sc_prim_channel	sc_in<type> sc_out<type> sc_inout<type> sc_in_rv<width> sc_out_rv<width> sc_inout_rv<width> sc_in_resolved sc_out_resolved sc_inout_resolved sc_in_clk sc_out_clk sc_inout_clk sc_fifo_in sc_fifo_out User defined ports derived from sc_port<> which is : <ul style="list-style-type: none"> • connected to a built-in channel • connected to a user-defined channel derived from an sc_prim_channel¹ 	Module member variables of all C++ and SystemC built-in types (listed in the Types list below) are supported.	Aggregates of SystemC signals or ports. Only three types of aggregates are supported for debug: <ul style="list-style-type: none"> struct class array

1. You must use a special macro to make these ports viewable for debugging. For details See [MTI_SC_PORT_ENABLE_DEBUG](#).

MTI_SC_PORT_ENABLE_DEBUG

A user-defined port which is not connected to a built-in primitive channel is not viewable for debugging by default. You can make the port viewable if the actual channel connected to the port is a channel derived from an sc_prim_channel. If it is, you can add the macro MTI_SC_PORT_ENABLE_DEBUG to the channel class' public declaration area, as shown in this example:

```
class my_channel: public sc_prim_channel
{
...
public:
```



```
MTI_SC_PORT_ENABLE_DEBUG
```

```
};
```

Waveform Compare with SystemC

Waveform compare supports the viewing of SystemC signals and variables. You can compare SystemC objects to SystemC, Verilog or VHDL objects.

For pure SystemC compares, you can compare any two signals that match type and size exactly; for C/C++ types and some SystemC types, sign is ignored for compares. Thus, you can compare char to unsigned char or sc_signed to sc_unsigned. All SystemC fixed-point types may be mixed as long as the total number of bits and the number of integer bits match.

Mixed-language compares are supported as listed in the following table:

Table 9-6. Mixed-language Compares

C/C++ types	bool, char, unsigned char short, unsigned short int, unsigned int long, unsigned long
SystemC types	sc_bit, sc_bv, sc_logic, sc_lv sc_int, sc_uint sc_bigint, sc_biguint sc_signed, sc_unsigned
Verilog types	net, reg
VHDL types	bit, bit_vector, boolean, std_logic, std_logic_vector

The number of elements must match for vectors; specific indexes are ignored.

Debugging Source-Level Code

In order to debug your SystemC source code, you must compile the design for debug using the **-g** C++ compiler option. You can add this option directly to the [sccom](#) command line on a per run basis, with a command such as:

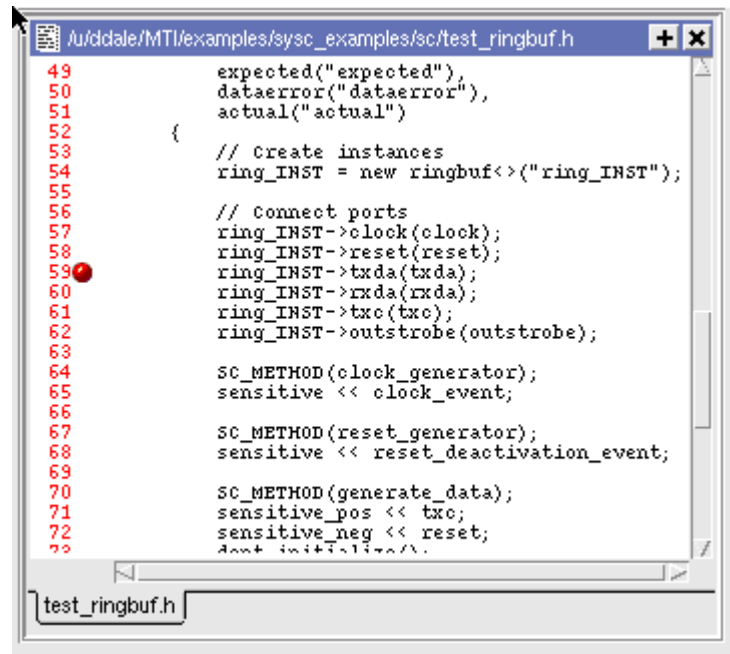
```
sccom mytop -g
```

Or, if you plan to use it every time you run the compiler, you can specify it in the *modelsim.ini* file with the [CppOptions](#) variable. See [modelsim.ini Variables](#) for more information.

The source code debugger, [C Debug](#), is automatically invoked when the design is compiled for debug in this way.

Figure 9-2 shows an example of how to set breakpoints in a Source window (Line 59) and single-step through your SystemC/C++ source code.

Figure 9-2. Breakpoint in SystemC Source



```
49     expected("expected"),
50     dataerror("dataerror"),
51     actual("actual")
52     {
53         // Create instances
54         ring_INST = new ringbuf<>("ring_INST");
55
56         // Connect ports
57         ring_INST->clock(clock);
58         ring_INST->reset(reset);
59         ring_INST->txda(txda);
60         ring_INST->rxda(rxda);
61         ring_INST->txc(txc);
62         ring_INST->outstrobe(outstrobe);
63
64         SC_METHOD(clock_generator);
65         sensitive << clock_event;
66
67         SC_METHOD(reset_generator);
68         sensitive << reset_deactivation_event;
69
70         SC_METHOD(generate_data);
71         sensitive_pos << txc;
72         sensitive_neg << reset;
73     }
```

Note



To allow source annotation, use the `-nodbgSYM` argument for the `sccom` command:

sccom -nodbgSYM

This disables the generation of symbols for the debugging database in the library.

Stepping Out From OSCI Library Functions

When you are using C Debug to single-step through the SystemC code, you may find that stepping through the code often ends up going inside SystemC library routines. This can be a distraction from debugging your actual code.

By default, auto-stepping out of the library for debugging is enabled, which means stepping into the library is not allowed (`cdbg allow_lib_step off`). So, if you step into a library function, execution will automatically return to your code.

You can use the `cdbg` command to disable this behavior:

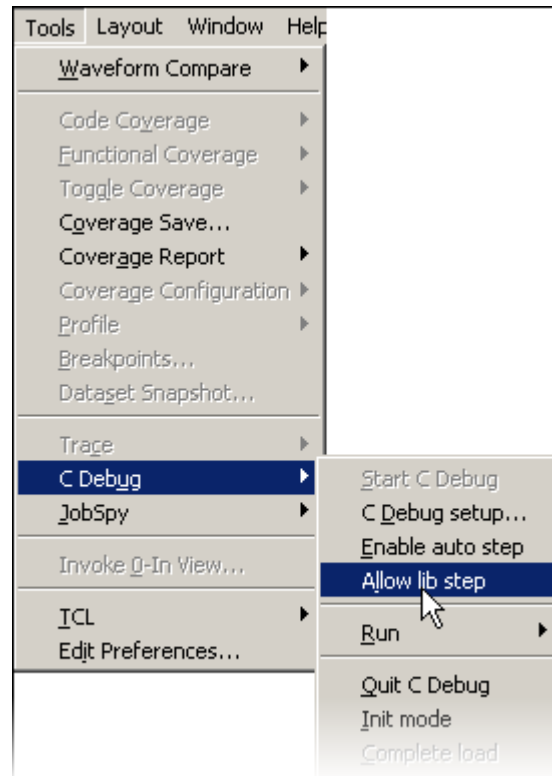
cdbg allow_lib_step on

Now, execution will not automatically step out from library functions, but it will step into the library code.

The `allow_lib_step` argument to the `cdbg` command takes a value of "on" or "off."

You can also perform this action in the GUI by selecting **Tools > CDebug > Allow lib step** from the menus (Figure 9-3).

Figure 9-3. Setting the Allow lib step Function



For example, assume that the debugger has stepped to a library function call. If this were the only library function call in the current line, execution would go the next line in your code (there would be no need for the “step out” action). However, if there are more function calls in the current line, execution comes back to the same line, and the next 'step -over' operation goes to the next line in your code. So the debugging operation always stays in your code, regardless of where it steps.

Setting Constructor/Destructor Breakpoints

You can set breakpoints in constructors and destructors of SystemC objects. Constructor breakpoints need to be set before SystemC shared library is loaded. You can set breakpoints using either the Cdebug Init mode or Automated Constructor breakpoint flow.

Cdebug Init mode

1. Start Cdebug before loading the design.

- a. Select **Tools > CDebug > Start CDebug** from the menus or use the following command:
cdbg debug_on
2. Turn on the Cdebug Init mode.
 - a. Select **Tools > CDebug > Init mode** from the menus or use the following command:
cdbg init_mode_setup
3. Load the design.

ModelSim will stop after loading the shared library.
4. Set breakpoints on constructors.

Automated Constructor breakpoint flow

1. Start ModelSim in the GUI or batch mode.
 - a. Type **vsim** at a UNIX shell prompt (**vsim -c** for batch mode) or double-click the ModelSim icon in Windows.

If the Welcome to ModelSim dialog appears, click **Close**.
2. Set the breakpoints using the following command.
bp -c [<filename>:<line> | <function_name>]

NOTE: You can also set breakpoints by opening a file in source window and clicking on a line number.
3. Load the design by entering the **vsim** command. ModelSim automatically stops after loading the shared library and sets all the constructor breakpoints. You can set additional constructor breakpoints here.
4. The **run -continue** command elaborates the design and stops the simulation at the constructor breakpoint.

You can also set destructor breakpoints using these same steps in either the Cdebug Init mode or the Automated Constructor breakpoint flow; or, after the design is loaded. If you set destructor breakpoints before loading the design, then ModelSim keeps all the breakpoints enabled even after design is loaded.

When you set a destructor breakpoint, ModelSim automatically sets up in **Stop on quit** mode (see [Debugging Functions when Quitting Simulation](#)). The debugger will stop at the breakpoint after you issue the **quit -f** command in ModelSim. This allows you to step through and examine the code. Run the **run -continue** command when you have finished examining the C code.

Because the **Stop on quit** mode is set up, when simulation completes, ModelSim automatically quits C-debugger and the GUI (whether or not a C breakpoint was hit and you return to the VSIM> prompt).

Instance Based Breakpointing

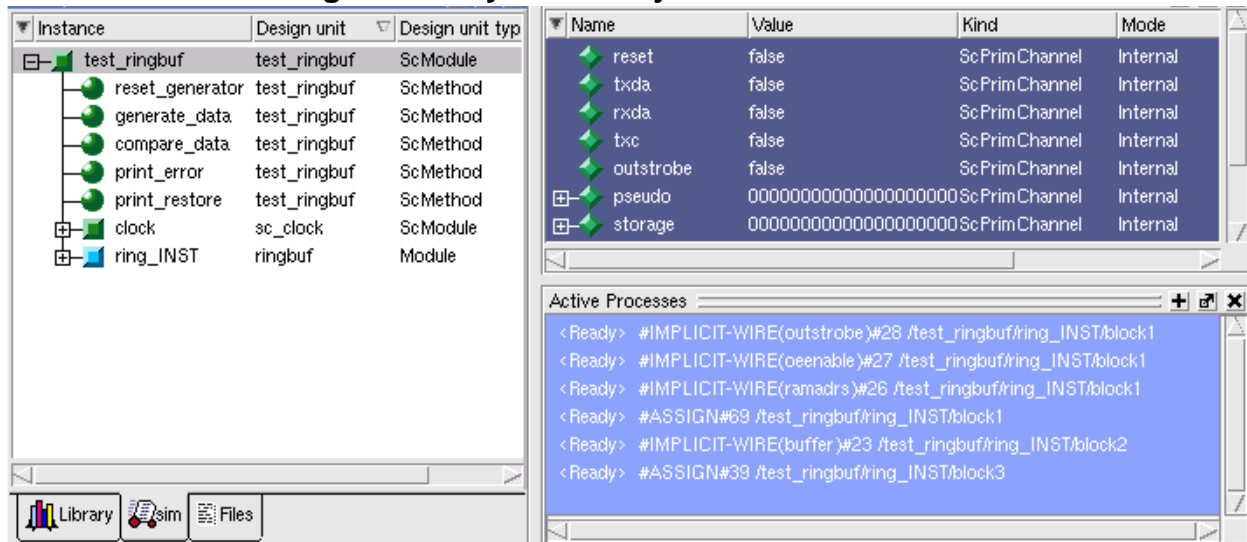
To set a SystemC breakpoints so it applies only to a specified instance, use the `-inst` argument to the `bp` command:

```
bp <filename>:<line#> -inst <instance>
```

Viewing SystemC Objects in GUI

You can view and expand SystemC objects in the Objects window and processes in the Processes pane, as shown in [Figure 9-4](#).

Figure 9-4. SystemC Objects and Processes



SystemC Object and Type Display

This section contains information on how ModelSim displays certain objects and types, as they may differ from other simulators.

Support for Globals and Statics

Globals and statics are supported for ModelSim debugging purposes, however some additional naming conventions must be followed to make them viewable.

Naming Requirement

In order to make a global viewable for debugging purposes, the name given must match the declared signal name. An example:

```
sc_signal<bool> clock("clock");
```

For statics to be viewable, the name given must be fully qualified, with the module name and declared name, as follows:

```
<module_name>::<declared_name>
```

For example, the static data member "count" is viewable in the following code excerpt:

```
SC_MODULE(top)
{
    static sc_signal<float> count; //static data member
    ....
}
sc_signal<float> top::count("top::count"); //static named in quotes
```

Viewing Global and Static Signals

ModelSim translates C++ scopes into a hierarchical arrangement. Since globals and statics exist at a level above ModelSim's scope, ModelSim must add a top level, **sc_root**, to all global and static signals. Thus, to view these static or global signals in ModelSim, you need to add **sc_root** to the hierarchical name for the signal. In the case of the above examples, the debugging statements for examining "top/count" (a static) and "clock" (a global) would be:

```
VSIM> examine /sc_root/top/count  
VSIM> examine /sc_root/clock
```

Support for Aggregates

ModelSim supports aggregates of SystemC signals or ports. Three types of aggregates are supported: structures, classes, and arrays. Unions are not supported for debug. An aggregate of signals or ports will be shown as a signal of aggregate type. For example, an aggregate such as:

```
sc_signal <sc_logic> a[3];
```

is equivalent to:

```
sc_signal <sc_lv<3>> a;
```

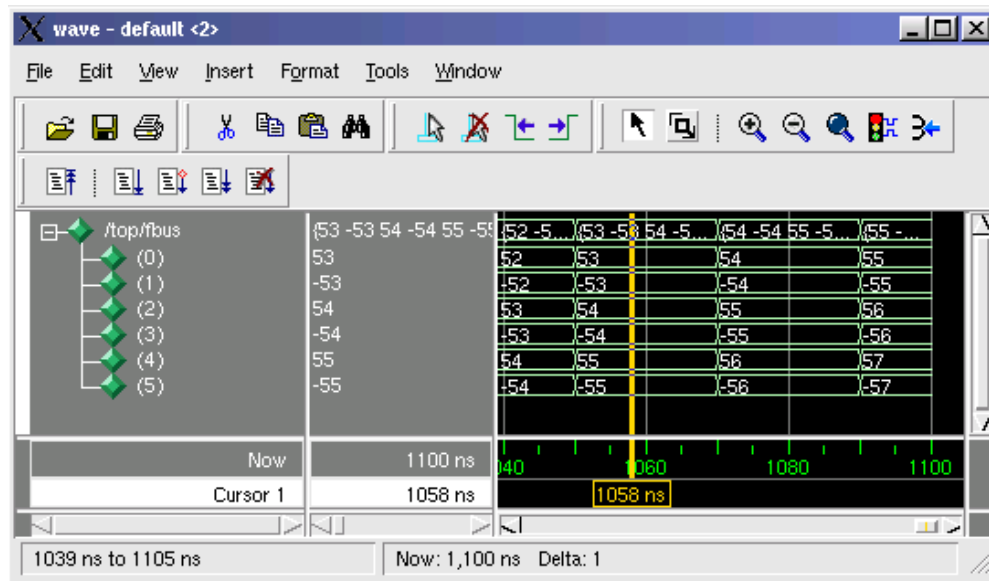
for debug purposes. ModelSim shows one signal - object "a" - in both cases.

The following aggregate

```
sc_signal <float> fbus [6];
```

when viewed in the Wave window, would appear shown in [Figure 9-5](#).

Figure 9-5. Aggregates in Wave Window



SystemC Dynamic Module Array

ModelSim supports SystemC dynamic module arrays. An example of using a dynamic module array:

```
module **mod_inst;
mod_inst = new module*[2];
mod_inst[0] = new module("mod_inst[0]");
mod_inst[1] = new module("mod_inst[1]");
```

Limitations

- The instance names of modules containing dynamic arrays must match the corresponding C++ variables, such as “mod_inst[0]” and “mod_inst[1]” in the example above. If not named correctly, the module instances simulate correctly, but are not debuggable.

Viewing FIFOs

In ModelSim, the values contained in an `sc_fifo` appear in a definite order. The top-most or left-most value is always the next to be read from the FIFO. Elements of the FIFO that are not in use are not displayed.

Example of a signal where the FIFO has five elements:

```
# examine f_char
# {}
VSIM 4> # run 10
VSIM 6> # examine f_char
```

```
# A
VSIM 8> # run 10
VSIM 10> # examine f_char
# {A B}
VSIM 12> # run 10
VSIM 14> # examine f_char
# {A B C}
VSIM 16> # run 10
VSIM 18> # examine f_char
# {A B C D}
VSIM 20> # run 10
VSIM 22> # examine f_char
# {A B C D E}
VSIM 24> # run 10
VSIM 26> # examine f_char
# {B C D E}
VSIM 28> # run 10
VSIM 30> # examine f_char
# {C D E}
VSIM 32> # run 10
VSIM 34> # examine f_char
# {D E}
```

Viewing SystemC Memories

The ModelSim tool detects and displays SystemC memories. A memory is defined as any member variable of a SystemC module which is defined as an array of the following type:

unsigned char	sc_bit (of 2-D or more arrays only)
unsigned short	sc_logic (of 2-D or more arrays only)
unsigned int	sc_lv<N>
unsigned long	sc_bv<N>
unsigned long long	sc_int<N>
char	sc_uint<N>
short	sc_bigint<N>
int	sc_biguint<N>
float	sc_signed
double	sc_unsigned
enum	

Properly Recognizing Derived Module Class Pointers

If you declare a pointer as a base class pointer, but actually assign a derived class object to it, ModelSim still treats it as a base class pointer instead of a derived class pointer, as you intended. As such, it would be unavailable for debug. To make it available for debug, you must

use the **mti_set_typename** member function to instruct that it should be treated as a derived class pointer.

To correctly associate the derived class type with an instance:

1. Use the member function **mti_set_typename** and apply it to the modules. Pass the actual derived class name to the function when an instance is constructed, as shown in [Example 9-6](#).

Example 9-6. Use of **mti_set_typename**

```
SC_MODULE(top) {  
    base_mod* inst;  
  
    SC_CTOR(top) {  
        if (some_condition) {  
            inst = new dl_mod("dl_inst");  
            inst->mti_set_typename("dl_mod");  
        } else {  
            inst = new d2_mod("d2_inst");  
            inst->mti_set_typename("d2_mod");  
        }  
    }  
};
```



Tip: In this example, the class names are simple names, which may not be the case if the type is a class template with lots of template parameters. Look up the name in `<work>/moduleinfo.sc` file, if you are unsure of the exact names.

Here is the code for which the above `SC_MODULE` was modified:

```
class base_mod : public sc_module {  
    sc_signal<int> base_sig;  
    int          base_var;  
  
    ...  
};  
  
class dl_mod : public base_mod {  
    sc_signal<int> dl_sig;  
    int          dl_var;  
  
    ...  
};  
  
class d2_mod : public base_mod {
```

```
    sc_signal<int> d2_sig;  
    int           d2_var;  
  
    ...  
};  
  
SC_MODULE(top) {  
    base_mod* inst;  
  
    SC_CTOR(top) {  
        if (some_condition)  
            inst = new dl_mod("dl_inst");  
        else  
            inst = new d2_mod("d2_inst");  
    }  
};
```

In this unmodified code, the **sccom** compiler could only see the declarative region of a module, so it thinks "inst" is a pointer to the "base_mod" module. After elaboration, the GUI would only show "base_sig" and "base_var" in the Objects window for the instance "inst".

You really wanted to see all the variables and signals of that derived class. However, since you didn't associate the proper derived class type with the instance "inst", the signals and variables of the derived class are not debuggable, even though they exist in the kernel.

The solution is to associate the derived class type with the instance, as shown in the modified SC_MODULE above.

Custom Debugging of SystemC Channels and Variables

ModelSim offers a string-based debug solution for various simulation objects which are considered undebuggable by the SystemC compiler **sccom**. Through it, you can gain easy access for debugging to the following:

- SystemC variables of a user-defined type
- Built-in channels of a user defined type
- Built-in ports of a user defined type
- User defined channels and ports

This custom interface can be also used to debug objects that may be supported for debug natively by the simulator, but whose native debug view is too cumbersome.

Supported SystemC Objects

The custom debug interface provides debug support for the following SystemC objects (T is a user defined type, or a user-defined channel or port):

```
T
sc_signal<T>
sc_fifo<T>
tlm_fifo<T>
sc_in<T>
sc_out<T>
sc_inout<T>
```

Usage

To provide custom debug for any object:

1. Register a callback function — one for each instance of that object — with the simulator. Specify the maximum length of the string buffer to be reserved for an object instance. See [Registration and Callback Function Syntax](#).
2. The simulator calls the callback function, with the appropriate arguments, when it needs the latest value of the object.

The registration function can be called from the phase callback function **before_end_of_elaboration()**, or anytime before this function during the elaboration phase of the simulator.

3. The ModelSim simulator passes the callback function a pre-allocated string of a length specified during registration. The callback function must write the value of the object in that string, and it must be null terminated (`\0`).
4. The ModelSim simulator takes the string returned by the callback function as-is and displays it in the Objects window, Wave window, and CLI commands (such as `examine`). The `describe` command on custom debug objects simply reports that the object is a custom debug object of the specified length.

The macro used to register an object for debugging is `SC_MTI_REGISTER_CUSTOM_DEBUG`. Occasionally, ModelSim fails to register an object because it determines that the object cannot be debugged. In such cases, an error message is issued to that effect. If this occurs, use the `SC_MTI_REGISTER_NAMED_CUSTOM_DEBUG` to both name and register the object for debugging.

Registration and Callback Function Syntax

Registration:

```
void SC_MTI_REGISTER_CUSTOM_DEBUG
    (void* obj, size_t value_len,
     mtiCustomDebugCB cb_func);

void SC_MTI_REGISTER_NAMED_CUSTOM_DEBUG
```

```
(void* obj, size_t value_len,  
 mtiCustomDebugCB cb_func, const char* name);
```

Callback:

```
typedef void (*mtiCustomDebugCB)(void* obj, char* value, char  
 format_char);
```

- **obj** — the handle to the object being debugged
- **value_len** — the maximum length of the debug string to be reserved for this object
- **cb_func** — the callback function to be called by the simulator for the latest value of the object being debugged
- **name** — the name of the object being debugged
- **value** — A pointer to the string value buffer in which the callback must write the string value of the object being debugged
- **format_char** — the expected format of the value: ascii ('a'), binary ('b'), decimal ('d'), hex ('h'), or octal ('o')

The callback function does not return anything.

Example 9-7. Using the Custom Interface on Different Objects

Consider an arbitrary user-defined type T as follows:

```
class myclass {  
  
private:  
  
    int x;  
    int y;  
  
public:  
    void get_string_value(char format_str, char* mti_value);  
    size_t get_value_length();  
  
    ...  
};
```

Variable of type T would be:

```
void mti_myclass_debug_cb(void* var, char* mti_value, char format_str)  
{  
    myclass* real_var = RCAST<myclass*>var;  
    real_var.get_string_value(format_str, mti_value);  
}  
  
SC_MODULE(test) {
```

```

myclass var1;
myclass* var2;

SC_CTOR(test) {
    SC_MTI_REGISTER_CUSTOM_DEBUG(
        &var1,
        var1.get_value_length(),
        mti_myclass_debug_cb);

    SC_MTI_REGISTER_CUSTOM_DEBUG(
        var2,
        var2->get_value_length(),
        mti_myclass_debug_cb);
}
};

```

sc_signal, sc_fifo and tlm_fifo of type T and Associated Ports would be:

```

void mti_myclass_debug_cb(void* var, char* mti_value, char format_str)
{
    myclass* real_var = RCAST<myclass*>var;
    real_var.get_string_value(format_str, mti_value);
}

SC_MODULE(test) {

    sc_signal<myclass> sig1;
    sc_signal<myclass> *sig2;
    sc_fifo<myclass> fifo;

    SC_CTOR(test) {
        myclass temp;

        SC_MTI_REGISTER_CUSTOM_DEBUG(
            &sig1,
            temp.get_value_length(),
            mti_myclass_debug_cb);

        SC_MTI_REGISTER_CUSTOM_DEBUG(
            sig2,
            temp.get_value_length(),
            mti_myclass_debug_cb);

        SC_MTI_REGISTER_CUSTOM_DEBUG(
            &fifo,
            temp.get_value_length(),
            mti_myclass_debug_cb);
    }
};

```

As shown in [Example 9-7](#), although the callback function is registered on a `sc_signal<T>` or a `sc_fifo<T>` object, the callback is called on the T object, instead of the channel itself. We call the callback on T because `sc_signal<T>` has two sets of values, current and new value and `sc_fifo` can have more than one element in the fifo. The callback is called on each element of the fifo that is valid at any given time. For an `sc_signal<T>` the callback is called only on the current value, not the new value.

By registering the primitive channel `sc_signal<T>` for custom debug, any standard port connected to it (`sc_in<T>`, `sc_out<T>`, `sc_inout<T>`, `sc_fifo_in<T>`, and so forth) automatically is available for custom debug. It is illegal to register any built-in ports for custom debug separately.

User Defined Primitive Channels and Ports

The callback and registration mechanism for a user-defined channel derived from `sc_prim_channel` are no different than a variable of an user-defined type. Please see the section on variables of type T in [Example 9-7](#) for more details on the registration and callback mechanism for such objects.

You have two choices available to you for making user defined ports debuggable:

- Automatic debug of any port connected to a primitive channel

Any port that is connected to a channel derived from `sc_prim_channel` is automatically debuggable only if the connected channel is debuggable either natively or using custom debug. To enable this automatic debugging capability, use the following macro in the channel class:

```
MTI_SC_PORT_ENABLE_DEBUG
```

In this case, you may not separately register the port for custom debug.

- Specific port registration

Register the port separately for custom debug. To do this, simply register the specific port, without using the macro. The callback and registration mechanism is the same as a variable of type T.

Hierarchical Channels/Ports Connected to Hierarchical Channels

Hierarchical channels are basically modules, and appear in the structure pane in ModelSim. Since they are part of the design hierarchy, custom debug cannot be supported for hierarchical channels. Ports connected to hierarchical channels, however, though not supported for debug natively in ModelSim, are supported for debug with the custom interface.

Any port object registered for custom debug is treated as a variable of a user defined type. Please see [Example 9-7](#), variables of type T, for more details on the registration and callback mechanism for such objects.

Any Other Channels and Ports Connected to Such Channels

It is legal in SystemC to create a channel that implements an interface and is not derived either from `sc_channel` or `sc_prim_channel`. Take the following, for example:

```
class mychannel : public myinterface {}
```

```
class myport : public sc_port<myinterface> {}
```

Channels and ports of this category are supported for debug natively in ModelSim. ModelSim treats them as variables of type T. These channels and ports can be registered for custom debug. The registration and callback mechanism is the same as for a variable of type T, as shown in [Example 9-7](#) above.

Modifying SystemC Source Code

If your design does not have `sc_main()` at the top level, several modifications must be applied to your original SystemC source code. To see example code containing the modifications listed below, see [Code Modification Examples](#).

Converting `sc_main()` to a Module

Unless your design has `sc_main()` at the top level, in order for ModelSim to run the SystemC/C++ source code, you must replace the control function of `sc_main()` with a constructor, `SC_CTOR()`, placed within a module at the top level of the design (see `mytop` in [Example 9-8](#)). In addition:

- any test bench code inside `sc_main()` should be moved to a process, normally an `SC_THREAD` process.
- all C++ variables in `sc_main()`, including SystemC primitive channels, ports, and modules, must be defined as members of `sc_module`. Therefore, initialization must take place in the `SC_CTOR`. For example, all `sc_clock()` and `sc_signal()` initializations must be moved into the constructor.

Replacing `sc_start()` Function with Run Command and Options

ModelSim uses the `run` command and its options in place of the `sc_start()` function. If `sc_main()` has multiple `sc_start()` calls mixed in with the test bench code, then use an `SC_THREAD()` with wait statements to emulate the same behavior. An example of this is shown in [“Code Modification Examples”](#) on page 384.

Removing Calls to `sc_initialize()`

`vsim` calls `sc_initialize()` by default at the end of elaboration, so calls to `sc_initialize()` are unnecessary.

Code Modification Examples

Example 9-8. Converting sc_main to a Module

The following is a simple example of how to convert `sc_main` to a module and elaborate it with `vsim`.

Table 9-7. Simple Conversion - sc_main to Module

Original OSCI code #1 (partial)	Modified code #1 (partial)
<pre>int sc_main(int argc, char* argv[]) { sc_signal<bool> mysig; mymod mod("mod"); mod.outp(mysig); sc_start(100, SC_NS); }</pre>	<pre>SC_MODULE(mytop) { sc_signal<bool> mysig; mymod mod; SC_CTOR(mytop) : mysig("mysig"), mod("mod") { mod.outp(mysig); } }; SC_MODULE_EXPORT(mytop);</pre>

The run command equivalent to the `sc_start(100, SC_NS)` statement is:

run 100 ns

Example 9-9. Using `sc_main` and Signal Assignments

This next example is slightly more complex, illustrating the use of `sc_main()` and signal assignments, and how you would get the same behavior using ModelSim.

Table 9-8. Using `sc_main` and Signal Assignments

OSCI code #2 (partial)	Modified code #2 (partial)
<pre>int sc_main(int, char**) { sc_signal<bool> reset; counter_top top("top"); sc_clock CLK("CLK", 10, SC_NS, 0.5, 0.0, SC_NS, false); top.reset(reset); reset.write(1); sc_start(5, SC_NS); reset.write(0); sc_start(100, SC_NS); reset.write(1); sc_start(5, SC_NS); reset.write(0); sc_start(100, SC_NS); }</pre>	<pre>SC_MODULE(new_top) { sc_signal<bool> reset; counter_top top; sc_clock CLK; void sc_main_body(); SC_CTOR(new_top) : reset("reset"), top("top") CLK("CLK", 10, SC_NS, 0.5, 0.0, SC_NS, false) { top.reset(reset); SC_THREAD(sc_main_body); } }; void new_top::sc_main_body() { reset.write(1); wait(5, SC_NS); reset.write(0); wait(100, SC_NS); reset.write(1); wait(5, SC_NS); reset.write(0); wait(100, SC_NS); sc_stop(); } SC_MODULE_EXPORT(new_top);</pre>

Example 9-10. Using an SCV Transaction Database

One last example illustrates the correct way to modify a design using an SCV transaction database. ModelSim requires that the transaction database be created before calling the constructors on the design subelements. The example is as follows:

Table 9-9. Modifications Using SCV Transaction Database

Original OSCI code # 3 (partial)	Modified ModelSim code #3 (partial)
<pre>int sc_main(int argc, char* argv[]) { scv_startup(); scv_tr_text_init(); scv_tr_db db("my_db"); scv_tr_db db::set_default_db(&db); sc_clock clk ("clk",20,0.5,0,true); sc_signal<bool> rw; test t("t"); t.clk(clk);; t.rw(rw); sc_start(100); }</pre>	<pre>SC_MODULE(top) { sc_signal<bool>* rw; test* t; SC_CTOR(top) { scv_startup(); scv_tr_text_init() scv_tr_db* db = new scv_tr_db("my_db"); scv_tr_db::set_default_db(db);; clk = new sc_clock("clk",20,0.5,0,true); rw = new sc_signal<bool> ("rw"); t = new test("t"); } }; SC_MODULE_EXPORT(new_top);</pre>

Take care to preserve the order of functions called in **sc_main()** of the original code.

Sub-elements cannot be placed in the initializer list, since the constructor body must be executed prior to their construction. Therefore, the sub-elements must be made pointer types, created with "new" in the SC_CTOR() module.

Using sc_main as Top Level

ModelSim executes sc_main() as a thread process.

Example 9-11. Simple SystemC-only sc_main()

```
int
sc_main(int, char*[])
{
    design_top t1 = new design_top("t1");
    sc_start(-1);
    delete t1;
    return 1;
}
```

Prerequisites

- Must be running ModelSim 6.3 or higher.

Procedure

To simulate in ModelSim using `sc_main()` as the top-level in your design:

1. Run `vsim` with `sc_main` as the top-level module:

```
vsim -c sc_main
```

2. Explicitly name all simulation objects for mixed-language designs, or to enable debug support of objects created by `sc_main()`. Pass the declared name as a constructor arguments, as follows:

```
sc_signal<int> sig("sig");
top_module* top = new top("top");
```



Tip: For SystemC-only designs, the simulation runs even if debug support is not enabled. Mixed language designs, however, will not elaborate if explicit naming is not performed in `sc_main()`. ModelSim issues an error message to this effect.

3. Optionally, override the default stack size (10Mb) for `sc_main()` in the `modelsim.ini` file:

```
ScMainStackSize 1 Gb
```

See [ScMainStackSize](#) variable for more information.

Concepts

- ModelSim executes `sc_main()` in two parts:
 - The code before the first call to `sc_start()` — executed during the construction phase of all other design tops.
 - The code after the first `sc_start()` or any other subsequent `sc_start()`'s — executed based on the `sc_start()` arguments.

The overall simulation is controlled by the ModelSim prompt and the `sc_start()` call does not proceed unless an appropriate **run** command is issued from the ModelSim prompt. `sc_start()` always yields to ModelSim for the time specified in its argument. Example:

```
int
sc_main(int, char*[])
{
    top t1("t1");
    sc_signal<int> reset("reset");
    t1.reset(reset);
    t2->reset(reset);
    sc_start(100, SC_NS); <----- 1st part executed during
                                construction. Yield to the kernel
                                for 100 ns.
```

```

    reset = 1;           <----- Executed only if
                        run 100 ns or more is issued
                        from batch or GUI prompt.

    sc_start(100, SC_NS); <----- Yield to the kernel for another
                        100 ns

    return 1;           <----- Executed only if
                        the simulation is run for
                        more than 200 ns.
}

```

sc_start(-1) in the OSCI simulator means that the simulation is run until the time it is halted by sc_stop(), or because there were no future events scheduled at that time. The sc_start(-1) in means that sc_main() is yielding to the ModelSim simulator until the current simulation session finishes.

- Avoid sc_main() going out of scope — Since sc_main() is run as a thread, it must not go out of scope or delete any simulation objects while the current simulation session is running. The current simulation session is active unless a quit, restart, sc_stop, \$finish, or assert is executed, or a new design is loaded. To avoid sc_main() from going out of scope or deleting any simulation objects, sc_main() must yield control to the ModelSim simulation kernel before calling any delete and before returning from sc_main. In ModelSim, sc_start(-1) gives control to the ModelSim kernel until the current simulation session is exited. Any code after the sc_start(-1) is executed when the current simulation ends.

```

int
sc_main(int, char*[])
{
    top t1("t1");
    top* t2 = new top("t2");
    sc_signal<int> reset("reset");
    t1.reset(reset);
    t2->reset(reset);
    sc_start(100, SC_NS); <----- 1st part executed during
                        construction. yield to the kernel
                        for 100 ns.

    reset = 1;           <----- Will be executed only if
                        run 100 ns or more is issued
                        from batch or GUI prompt.

    sc_start(100, SC_NS); <----- Yield to the kernel for another 100 ns

    sc_start(-1);       <----- Will cause sc_main() to
                        suspend until the end of
                        the current simulation session

    delete t2;          <----- Will be executed at the
                        end of the current simulation
                        session.

    return 1;
}

```

If the run command specified at the simulation prompt before ending the current simulation session exceeds the cumulative `sc_start()` times inside `sc_main()`, the simulation continues to run on design elements instantiated both by `sc_main()` and outside of `sc_main()`. For example, in this case, if `sc_main()` instantiates an `sc_clock`, the clock will continue to tick if the simulation runs beyond `sc_main()`.

On the other hand, if the current simulation ends before the cumulative `sc_start()` times inside `sc_main`, the remainder of the `sc_main` will be executed before quitting the current simulation session if the `ScMainFinishOnQuit` variable is set to 1 in the `modelsim.ini` file. If this variable is set to 0, the remainder of `sc_main` will not be executed. The default value for this variable is 1. One drawback of not completely running `sc_main()` is that memory leaks might occur for objects created by `sc_main`. Also, it is possible that simulation stimulus and execution of the test bench will not be complete, and thus the simulation results will not be valid.

- `sc_cycle(sc_time)` is deprecated in SystemC 2.2. A suggested alternative to `sc_cycle` is `sc_start(sc_time)`. In case of a cycle accurate design, this will yield the same behavior. ModelSim will always convert `sc_cycle()` to `sc_start()` with a note.
- `sc_initialize()` is also deprecated in SystemC 2.2. The replacement for `sc_initialize()` is `sc_start(SC_ZERO_TIME)`. ModelSim treats `sc_initialize()` as `sc_start(SC_ZERO_TIME)`.
- ModelSim treats `sc_main()` as a top-level module and creates a hierarchy called `sc_main()` for it. Any simulation object created by `sc_main()` will be created under the `sc_main()` hierarchy in ModelSim. For example, for the `sc_main()` described above, the following hierarchy will be created:

```

/
|
|-- sc_main
|   |-- t1
|   |-- t2
|   |-- reset

```

Differences Between the Simulator and OSCI

ModelSim is based upon the OSCI proof-of-concept SystemC simulator. However, there are some minor but key differences to be aware of:

- The default time resolution of the simulator is 1ps. For **vsim** it is 1ns. You can change the value for time resolution by using the **vsim** command with the **-t** option or by modifying the value of the `Resolution` variable in the `modelsim.ini` file.
- The **run** command in ModelSim is equivalent to `sc_start()`. In the SystemC simulator, `sc_start()` runs the simulation for the duration of time specified by its argument. In ModelSim the **run** command runs the simulation for the amount of time specified by its argument.

- The `sc_cycle()`, and `sc_start()` functions are not supported in ModelSim.
- The default name for `sc_object()` is bound to the actual C object name. However, this name binding only occurs after all `sc_object` constructors are executed. As a result, any `name()` function call placed inside a constructor will not pick up the actual C object name.
- The value returned by the `name()` method prefixes OSCI-compliant hierarchical paths with "sc_main", which is ModelSim's implicit SystemC root object. For example, for the following example code:

```
#include "systemc.h"

SC_MODULE(bloc)
{
    SC_CTOR(bloc) {}
};

SC_MODULE(top)
{
    bloc bl ;
    SC_CTOR(top) : bl("bl") { cout << bl.name() << endl ; }
};

int sc_main(int argc, char* argv[])
{
    top top_i("top_i");
    sc_start(0, SC_NS);
    return 0;
}
```

the OSCI returns:

```
top_i.bl
```

and ModelSim returns:

```
sc_main.top_i.bl
```

Fixed-Point Types

Contrary to OSCI, ModelSim compiles the SystemC kernel with support for fixed-point types. If you want to compile your own SystemC code to enable that support, you must first define the compile time macro `SC_INCLUDE_FX`. You can do this in one of two ways:

- Enter the `g++/aCC` argument `-DSC_INCLUDE_FX` on the `sccom` command line, such as:

```
sccom -DSC_INCLUDE_FX top.cpp
```

- Add a define statement to the C++ source code before the inclusion of the `systemc.h`, as shown below:

```
#define SC_INCLUDE_FX
#include "systemc.h"
```

Algorithmic C Datatype Support

ModelSim supports native debug for the Algorithmic-C data types **ac_int** and **ac_fixed**. The Algorithmic C data types are used in Catapult C Synthesis, a tool that generates optimized RTL from algorithms written as sequential ANSI-standard C/C++ specifications. These data types are synthesizable and run faster than their SystemC counterparts `sc_bigint`, `sc_biguint`, `sc_fixed` and `sc_ufixed`.

To use these data types in the simulator, you must obtain the datatype package and specify the path containing the Algorithmic C header files with the `-I` argument on the `sccom` command line:

```
sccom -I <path_to_AC_headers> top.cpp
```

To enable native debug support for these datatypes, you must also specify the `-DSC_INCLUDE_MTI_AC` argument on the `sccom` command line.

```
sccom -DSC_INCLUDE_MTI_AC -I <path_to_AC_headers> top.cpp
```

Native debug is only supported for Version 1.2 and above. If you do not specify `-DSC_INCLUDE_MTI_AC`, the GUI displays the C++ layout of the datatype classes.

Support for cin

The ModelSim simulator has a limited support for the C++ standard input `cin`. To enable support for `cin`, the design source files must be compiled with `-DUSE_MTI_CIN` `sccom` option. For example:

```
sccom -DUSE_MTI_CIN top.cpp
```

Limitations

ModelSim does not support `cin` when it is passed as a function parameter of type `istream`. This is true for both C++ functions and member functions of a user-defined class/struct.

For example, the following `cin` usage is not supported:

```
void getInput(istream& is)
{
    int input_data;
    ...
    is >> input_data;
    ....
}
getinput(cin);
```

A workaround for this case, the source code needs to be modified as shown below:

```
void getinput()
{
    int input_data;
    ...
    cin >> input_data;
    ....
}
getinput();
```

OSCI 2.2 Feature Implementation Details

Support for OSCI TLM Library

ModelSim includes the header files and examples from the **OSCI SystemC TLM** (Transaction Level Modeling) Library Standard version 2.0. The TLM library can be used with simulation, and requires no extra switches or files. TLM objects are not debuggable, with the exception of `tlm_fifo`.

Examples and documentation are located in *install_dir/examples/systemc/tlm*. The TLM header files (*tlm_*.h*) are located in *include/systemc*.

Phase Callback

The following functions are supported for phase callbacks:

- `before_end_of_elaboration()`
- `start_of_simulation()`
- `end_of_simulation()`

For more information regarding the use of these functions, see [Initialization and Cleanup of SystemC State-Based Code](#).

Accessing Command-Line Arguments

The following global functions allow you to gain access to command-line arguments:

- `sc_argc()` — Returns the number of arguments specified on the `vsim` command line with the `-sc_arg` argument. This function can be invoked from anywhere within SystemC code.
- `sc_argv()` — Returns the arguments specified on the `vsim` command line with the `-sc_arg` argument. This function can be invoked from anywhere within SystemC code.

Example:

When **vsim** is invoked with the following command line:

```
vsim -sc_arg "-a" -c -sc_arg "-b -c" -t ns -sc_arg -d
```

`sc_argc()` and `sc_argv()` will behave as follows:

```
int argc;  
const char * const * argv;  
  
argc = sc_argc();  
argv = sc_argv();
```

The number of arguments (`argc`) is now 4.

```
argv[0] is "vopt" // if running vopt explicitly  
argv[0] is "vsim" // if not  
argv[1] is "-a"  
argv[2] is "-b -c"  
argv[3] is "-d"
```

sc_stop Behavior

When encountered during the simulation run in batch mode, the `sc_stop()` function stops the current simulation and causes ModelSim to exit. In GUI mode, a dialog box appears asking you to confirm the exit. This is the default operation of `sc_stop()`. If you want to change the default behavior of `sc_stop`, you can change the setting of the [OnFinish](#) variable in the `modelsim.ini` file. To change the behavior interactively, use the `-onfinish` argument to the `vsim` command.

Construction Parameters for SystemC Types

The information in this section applies only to SystemC signals, ports, variables, or fifos that use one of the following fixed-point types:

```
sc_signed  
sc_unsigned  
sc_fix  
sc_fix_fast  
sc_ufix  
sc_ufix_fast
```

These are the only SystemC types that have construction time parameters. The default size for these types is 32. If you require values other than the default parameters, you need to read this section.

If you are using one of these types in a SystemC signal, port, fifo, or an aggregate of one of these (such as an array of `sc_signal`), you cannot pass the size parameters to the type. This is a limitation imposed by the C++ language. Instead, SystemC provides a global default size (32) that you can control.

For `sc_signed` and `sc_unsigned`, you need to use the two objects, `sc_length_param` and `sc_length_context`, and you need to use them in an unusual way. If you just want the default vector length, simply do this:

```
SC_MODULE(dut) {
    sc_signal<sc_signed> s1;
    sc_signal<sc_signed> s2;
    SC_CTOR(dut)
        : s1("s1"), s2("s2")
        {
        }
}
```

For a single setting, such as using five-bit vectors, your module and its constructor would look like the following:

```
SC_MODULE(dut) {
    sc_length_param l;
    sc_length_context c;
    sc_signal<sc_signed> s1;
    sc_signal<sc_signed> s2;
    SC_CTOR(dut)
        : l(5), c(l), s1("s1"), s2("s2")
        {
        }
}
```

Notice that the constructor initialization list sets up the length parameter first, assigns the length parameter to the context object, and then constructs the two signals. You **DO** pass the name to the signal constructor, but the name is passed to the signal object, not to the underlying type. There is no way to reach the underlying type directly. Instead, the default constructors for `sc_signed` and `sc_unsigned` reach out to the global area and get the currently defined length parameter—the one you just set.

If you need to have signals or ports with different vector sizes, you need to include a pair of parameter and context objects for each different size. For example, the following uses a five-bit vector and an eight-bit vector:

```
SC_MODULE(dut) {
    sc_length_param l1;
    sc_length_context c1;
    sc_signal<sc_signed> s1;
    sc_signal<sc_signed> s2;

    sc_length_param l2;
    sc_length_context c2;
    sc_signal<sc_signed> u1;
    sc_signal<sc_signed> u2;
```

```
SC_CTOR(dut)
: l1(5), c1(11), s1("s1"), s2("s2"),
  l2(8), c2(12), u1("u1"), u2("u2")
{
}
}
```

With simple variables of this type, you reuse the context object. However, you must have the extra parameter and context objects when you are using them in a constructor-initialization list because the compiler does not allow repeating an item in that list.

The four fixed-point types that use construction parameters work exactly the same way, except that they use the objects `sc_fxtype_contxt` and `sc_fxtype_params` to do the work. Also, there are more parameters you can set for fixed-point numbers. Assuming you want to set only the length of the number and the number of fractional bits, the following example is similar to the preceding example, modified for fixed-point numbers:

```
SC_MODULE(dut) {
  sc_fxtype_params p1;
  sc_fxtype_contxt c1;
  sc_signal<sc_fix> s1;
  sc_signal<sc_fix> s2;
  sc_fxtype_params p2;
  sc_fxtype_contxt c2;
  sc_signal<sc_ufix> u1;
  sc_signal<sc_ufix> u2;
  SC_CTOR(dut)
  : p1(5,0), c1(p1), s1("s1"), s2("s2"),
    p2(8,5), c2(p2), u1("u1"), u2("u2")
  {
  }
}
```

Troubleshooting SystemC Errors

In the process of modifying your SystemC design to run on ModelSim, you may encounter several common errors. This section highlights some actions you can take to correct such errors.

Unexplained Behaviors During Loading or Runtime

If your SystemC simulation behaves in otherwise unexplainable ways, you should determine whether you need to adjust the stack space ModelSim allocates for threads in your design. The required size for a stack depends on the depth of functions on that stack and the number of bytes they require for automatic (local) variables.

By default the SystemC stack size is 10,000 bytes per thread.

You may have one or more threads needing a larger stack size. If so, call the SystemC function `set_stack_size()` and adjust the stack to accommodate your needs. Note that you can ask for too much stack space and have unexplained behavior as well.

Errors During Loading

When simulating your SystemC design, you might get a "failed to load sc lib" message because of an undefined symbol, looking something like this:

```
# Loading /home/cmg/newport2_systemc/chip/vhdl/work/systemc.so
# ** Error: (vsim-3197) Load of
"/home/cmg/newport2_systemc/chip/vhdl/work/systemc.so" failed: ld.so.1:
/home/icds_nut/modelsim/5.8a/sunos5/vsimk: fatal: relocation error: file
/home/cmg/newport2_systemc/chip/vhdl/work/systemc.so: symbol
_Z28host_respond_to_vhdl_requestPm:
referenced symbol not found.
# ** Error: (vsim-3676) Could not load shared library
/home/cmg/newport2_systemc/chip/vhdl/work/systemc.so for SystemC module
'host_xtor'.
```

Source of Undefined Symbol Message

The causes for such an error could be:

- missing definition of a function/variable
- missing type
- object file or library containing the defined symbol is not linked
- mixing of C and C++ compilers to compile a testcase
- using SystemC 2.2 header files from other vendors
- bad link order specified in `scom -link`
- multiply-defined symbols

Missing Definition

If the undefined symbol is a C function in your code or a library you are linking with, be sure that you declared it as an extern "C" function:

```
extern "C" void myFunc();
```

This should appear in any header files include in your C++ sources compiled by **scom**. It tells the compiler to expect a regular C function; otherwise the compiler decorates the name for C++ and then the symbol can't be found.

Also, be sure that you actually linked with an object file that fully defines the symbol. You can use the "nm" utility on Unix platforms to test your SystemC object files and any libraries you link with your SystemC sources. For example, assume you ran the following commands:

```
scom test.cpp  
scom -link libSupport.a
```

If there is an unresolved symbol and it is not defined in your sources, it should be correctly defined in any linked libraries:

```
nm libSupport.a | grep "mySymbol"
```

Missing Type

When you get errors during design elaboration, be sure that all the items in your SystemC design hierarchy, including parent elements, are declared in the declarative region of a module. If not, **sccom** ignores them.

For example, we have a design containing SystemC over VHDL. The following declaration of a child module "test" inside the constructor module of the code is not allowed and will produce an error:

```
SC_MODULE(Export)
{
    SC_CTOR(Export)
    {
        test *testInst;
        testInst = new test("test");
    }
};
```

The error results from the fact that the SystemC parse operation will not see any of the children of "test". Nor will any debug information be attached to it. Thus, the signal has no type information and can not be bound to the VHDL port.

The solution is to move the element declaration into the declarative region of the module.

Using SystemC 2.2 Header Files Supplied by Other Vendors

SystemC 2.2 includes version control for SystemC header files. If you compile your SystemC design using a SystemC 2.2 header file that was distributed by other vendors, and then you run **sccom -link** to link the design, an error similar to the following may result upon loading the design:

```
** Error: (vsim-3197) Load of "work/systemc.so" failed: work/systemc.so:
undefined symbol: _ZN20sc_api_version_2_1_0C1Ev.
```

To resolve the error, recompile the design using **sccom**. Make sure any include paths read by **sccom** do not point to a SystemC 2.2 installation. By default, **sccom** automatically picks up the ModelSim SystemC header files.

Misplaced -link Option

The order in which you place the **-link** option within the **sccom -link** command is critical. There is a big difference between the following two commands:

sccom -link liblocal.a

and

sccom liblocal.a -link

The first command ensures that your SystemC object files are seen by the linker before the library "liblocal.a" and the second command ensures that "liblocal.a" is seen first. Some linkers can look for undefined symbols in libraries that follow the undefined reference while others can look both ways. For more information on command syntax and dependencies, see [sccom](#).

Multiple Symbol Definitions

The most common type of error found during **sccom -link** operation is the multiple symbol definition error. The error message looks something like this:

```
work/sc/gensrc/test_ringbuf.o: In function
`test_ringbuf::clock_generator(void)':
work/sc/gensrc/test_ringbuf.o(.text+0x4): multiple definition of
`test_ringbuf::clock_generator(void)'
work/sc/test_ringbuf.o(.text+0x4): first defined here
```

This error arises when the same global symbol is present in more than one *.o* file. There are two common causes of this problem:

- A stale *.o* file in the working directory with conflicting symbol names.

In this first case, just remove the stale files with the following command:

```
vdel -lib <lib_path> -allsystemc
```

- Incorrect definition of symbols in header files.

In the second case, if you have an out-of-line function (one that isn't preceded by the "inline" keyword) or a variable defined (for instance, not just referenced or prototyped, but truly defined) in a *.h* file, you can't include that *.h* file in more than one *.cpp* file.

Text in *.h* files is included into *.cpp* files by the C++ preprocessor. By the time the compiler sees the text, it's just as if you had typed the entire text from the *.h* file into the *.cpp* file. So a *.h* file included into two *.cpp* files results in lots of duplicate text being processed by the C++ compiler when it starts up. Include guards are a common technique to avoid duplicate text problems.

If an *.h* file has an out-of-line function defined, and that *.h* file is included into two *.c* files, then the out-of-line function symbol will be defined in the two corresponding *.o* files. This leads to a multiple symbol definition error during **sccom -link**.

To solve this problem, add the "inline" keyword to give the function "internal linkage". This makes the function internal to the *.o* file, and prevents the function's symbol from colliding with a symbol in another *.o* file.

For free functions or variables, you could modify the function definition by adding the "static" keyword instead of "inline", although "inline" is better for efficiency.

Sometimes compilers do not honor the "inline" keyword. In such cases, you should move your function(s) from a header file into an out-of-line implementation in a *.cpp* file.

Chapter 10

Mixed-Language Simulation

ModelSim single-kernel simulation allows you to simulate designs that are written in VHDL, Verilog, SystemVerilog, and SystemC. While design units must be entirely of one language type, any design unit may instantiate design units from another language. Any instance in the design hierarchy may be a design unit from another language without restriction. In addition, ModelSim supports a procedural interface between SystemC and SystemVerilog, so you may make calls between these languages at the procedural level.

Basic Mixed-Language Flow

Simulating mixed-language designs with ModelSim includes these general steps:

1. Compile HDL source code using `vcom` or `vlog`. Compile SystemC C++ source code using `scom`. Compile all modules in the design following order-of-compile rules.
 - For SystemC designs with HDL instances — Create a SystemC foreign module declaration for all Verilog/SystemVerilog and VHDL instances (see [SystemC Foreign Module \(Verilog\) Declaration](#) or [SystemC Foreign Module \(VHDL\) Declaration](#)).
 - For Verilog/SystemVerilog/VHDL designs with SystemC instances — Export any SystemC instances that will be directly instantiated by the other language using the `SC_MODULE_EXPORT` macro. Exported SystemC modules can be instantiated just as you would instantiate any Verilog/SystemVerilog/VHDL module or design unit.
 - For binding Verilog design units to VHDL or Verilog design units or SystemC modules — See “[Using SystemVerilog bind Construct in Mixed-Language Designs](#).” When using `bind` in compilation unit scope, use the `-cname` argument with the `vlog` command (see [Handling Bind Statements in the Compilation Unit Scope](#)).
 - For VHDL that instantiates Verilog — Do not use `-nodebug=ports` during compilation of the Verilog modules because VHDL will not have the necessary access to the port information.
2. For designs containing SystemC — Link all objects in the design using `scom -link`.
3. Elaborate and optimize your design using the `vopt` command. See [Optimizing Mixed Designs](#).
4. Simulate the design with the `vsim` command.

5. Run and debug your design.

Separate Compilers with Common Design Libraries

VHDL source code is compiled by `vcom` and the resulting compiled design units (entities, architectures, configurations, and packages) are stored in the working library. Likewise, Verilog/SystemVerilog source code is compiled by `vlog` and the resulting design units (modules and UDPs) are stored in the working library.

SystemC/C++ source code is compiled with the `sccom` command. The resulting object code is compiled into the working library.

Design libraries can store any combination of design units from any of the supported languages, provided the design unit names do not overlap (VHDL design unit names are changed to lower case). See [Design Libraries](#) for more information about library management.

Using Hierarchical References

ModelSim supports the IEEE 1076-2008 standard "external name" syntax that allows you to make hierarchical references from VHDL to VHDL. Currently, these references can cross Verilog boundaries but must begin and end in VHDL. (The target of an external name must be a VHDL object.)

The external names syntax allows references to be made to signals, constants, or variables:

```
<<SIGNAL external_pathname : subtype_indication>>  
<<CONSTANT external_pathname : subtype_indication>>  
<<VARIABLE external_pathname : subtype_indication>>  
  
external_pathname <=  
    absolute_pathname | relative_pathname | package_pathname
```

Notice that the standard requires the entire syntax be enclosed in double angle brackets, `<<>>`. It also requires that you specify the type of the object you are referencing.

Here are some examples of external references:

```
REPORT "Test Pin = " & integer'image(<<SIGNAL .tb.dut.i0.tp : natural>>)  
    SEVERITY note;  
  
Q <= <<SIGNAL .tb.dut.i0.tp : std_log_vector(3 DOWNT0 0)>>;  
  
ALIAS test_pin IS <<SIGNAL .tb.dut.i0.tp : std_log_vector(3 DOWNT0 0)>>;  
    ...  
test_pin(3) <= '1';  
Q(0) <= test_pin(0);
```

To use this capability, compile your VHDL source for the IEEE 1076-2008 syntax as follows:

vcom -2008 design.vhd testbench.vhd

Note



The 1076-2002 syntax is the compiler's default.

The order of elaboration for Verilog to Verilog references that cross VHDL boundaries does not matter. However, the ability to reference from Verilog to VHDL or VHDL to Verilog is not yet supported in any version of ModelSim.

SystemVerilog binds in VHDL scopes are translated to "equivalent" VHDL so any restrictions on VHDL external names apply to the hierarchical references in the bind statement (that is, the target must be a VHDL object.) Since binds are done after all other instances within a scope there should not produce ordering issues.

Access Limitations in Mixed-Language Designs

You *cannot* directly read or change a SystemC object with a hierarchical reference within a mixed-language design. Further, you cannot directly access a Verilog/SystemVerilog object up or down the hierarchy if there is an interceding SystemC block.

To access obstructed SystemC objects, propagate the value through the ports of all design units in the hierarchy or use the control/observe functions. You can use either of the following member functions of `sc_signal` to control and observe hierarchical signals in a design:

- `control_foreign_signal()`
- `observe_foreign_signal()`

For more information on the use of control and observe, see "[Hierarchical References In Mixed HDL and SystemC Designs](#)".

Using SystemVerilog bind Construct in Mixed-Language Designs

The SystemVerilog **bind** construct allows you to bind a Verilog design unit to another Verilog design unit or to a VHDL design unit or to a SystemC module. This is especially useful for binding SystemVerilog assertions to your SystemC, VHDL, Verilog and mixed designs during verification.

Binding one design unit to another is a simple process of creating a module that you want to bind to a target design unit, then writing a bind statement. For example, if you want to bind a SystemVerilog assertion module to a VHDL design, do the following:

1. Write assertions inside a Verilog module.
2. Designate a target VHDL entity or a VHDL entity/architecture pair.

3. Bind the assertion module to the target with a **bind** statement.

The procedure for binding a SystemVerilog assertion module to a SystemC module is similar except that in step 2 you designate a target top level SystemC module or an instance of a SystemC module in the SystemC design hierarchy.

Modules, programs, or interfaces can be bound to:

- all instances of a target SystemC module
- a specific instance of the target SystemC module
- all instances that use a certain architecture in the target module

Binding to a configuration is not allowed.

Syntax of bind Statement

To bind a SystemVerilog assertion module to a VHDL design, the syntax of the **bind** statement is:

```
bind <target_entity/architecture_name> <assertion_module_name>  
<instance_name> <port connections>
```

For binding to a SystemC module, the syntax is:

```
bind <target SystemC module/full hierpath of an instance of a SystemC  
module> <assertion_module_name> <instance_name> <port connections>
```

This **bind** statement will create an instance of the assertion module inside the target VHDL entity/architecture or SystemC module with the specified instance name and port connections. When the target is a VHDL entity, the **bind** instance is created under the last compiled architecture. Note that the instance being bound cannot contain another **bind** statement. In addition, a bound instance can make hierarchical reference into the design.

What Can Be Bound

The following list provides examples of what can be bound.

- Bind to all instances of a VHDL entity.

```
bind e bind_du inst(p1, p2);
```
- Bind to all instances of a VHDL entity & architecture.

```
bind \e(a) bind_du inst(p1, p2);
```
- Bind to multiple VHDL instances.

```
bind test.dut.inst1 bind_du inst(p1, p2);  
bind test.dut.inst2 bind_du inst(p1, p2);
```

```
bind test.dut.inst3 bind_du inst(p1, p2);
```

- Bind to a single VHDL instance.

```
bind test.dut.inst1 bind_du inst(p1, p2);
```

- Bind to an instance where the instance path includes a for generate scope.

```
bind test.dut/forgen__4/inst1 bind_du inst(p1, p2);
```

- Bind to all instances of a VHDL entity and architecture in a library.

```
bind \mylib.e(a) bind_du inst(p1, p2);
```

- Bind to all instances of a SystemC module.

```
bind sc_mod bind_du inst(p1, p2);
```

- Bind to multiple SystemC module instances.

```
bind test.dut.sc_inst1 bind_du inst(p1, p2);
bind test.dut.sc_inst2 bind_du inst(p1, p2);
bind test.dut.sc_inst3 bind_du inst(p1, p2);
```

- Bind to a single SystemC module instance.

```
bind test.dut.sc_inst1 bind_du inst(p1, p2);
```

Hierarchical References

The ModelSim Signal Spy™ technology provides hierarchical access to bound SystemVerilog objects from VHDL objects. SystemVerilog modules also can access bound VHDL objects using Signal Spy, and they can access bounded Verilog objects using standard Verilog hierarchical references. See the [Signal Spy](#) chapter for more information on the use of Signal Spy.

Mapping of Types

All SystemVerilog data types supported at the SV-VHDL boundary are supported while binding to VHDL target scopes. This includes hierarchical references in actual expressions *if* they terminate in a VHDL scope. These data-types follow the same type-mapping rules followed at the SV-VHDL mixed-language boundary for direct instantiation. See [Mapping Data Types](#).

All the types supported at the SystemC-SystemVerilog mixed language boundary are also supported when binding to a SystemC target. Please refer to [Verilog or SystemVerilog and SystemC Signal Interaction And Mappings](#) for a complete list of all supported types.

Using SV Bind With or Without vopt

SV **bind**, when using **vopt**, is fully compatible with IEEE-1800 LRM.

When you use SV **bind** without **vopt** (either by using the **-novopt** switch with **vsim** or by setting the **VoptFlow** variable to 0 in the *modelsim.ini* file), the actual expression in a **bind** port map must be simple names (including hierarchical names if the target is a Verilog design unit) and Verilog literals. For example:

```
bind target checker inst(req, ack, 1'b1)
```

is a legal expression; whereas,

```
bind target checker inst(req | ack, {req1, req2})
```

is illegal because the actual expressions are neither simple names nor literals.

Additional restrictions on actual expressions exist for both Verilog and VHDL. For example, if the target of **bind** is a VHDL design unit or an instance of a VHDL design unit, the following types of actual expressions are supported only with **vopt**:

- bitwise binary expressions using operators **&**, **|**, **~**, **^** and **^~**
- concatenation expression
- bit select and part select expressions
- any variable/constant visible in the target scope including those defined in packages
- hierarchical references to VHDL signals/constants/variables

See [Optimizing Designs with vopt](#) for further details.

Binding to VHDL Enumerated Types

SystemVerilog infers an enumeration concept similar to VHDL enumerated types. In VHDL, the enumerated names are assigned to a fixed enumerated value, starting left-most with the value 0. In SystemVerilog, you can also explicitly define the enumerated values. As a result, the **bind** construct can be used for port mapping of VHDL enumerated types to Verilog port vectors.

Port mapping is supported for both input and output ports. The integer value of the enum is first converted to a bit vector before connecting to a Verilog formal port. Note that you cannot connect enum value on port actual – it has to be signal. In addition, port vectors can be of any size less than or equal to 32.

This kind of port mapping between VHDL enum and Verilog vector is only allowed when the Verilog is instantiated under VHDL through the **bind** construct and is not supported for normal instances.

The allowed VHDL types for port mapping to SystemVerilog port vectors are:

Table 10-1. VHDL Types Mapped To SystemVerilog Port Vectors

bit	std_logic	vl_logic
bit_vector	std_logic_vector	vl_logic_vector

See also, [Sharing User-Defined Types](#).

Example of Binding to VHDL Enumerated Types

Suppose you want to use SVA to monitor a VHDL finite state machine that uses enumerated types. With ModelSim, you can directly map VHDL enumerated types to SystemVerilog enumerated types. The same type-sharing rules are followed, which are applicable for direct instantiations at the SV-VHDL mixed-language boundary (see [Sharing User-Defined Types](#)).

Consider the following enumerated type defined in a VHDL package:

```
--/*-----pack.vhd-----*/
package pack is
    type fsm_state is(idle, send_bypass,
        load0,send0, load1,send1, load2,send2,
        load3,send3, load4,send4, load5,send5,
        load6,send6, load7,send7, load8,send8,
        load9,send9, load10,send10,
        load_bypass, wait_idle);
end package;
```

To use this at the SystemVerilog-VHDL mixed-language boundary, you must compile this package with the `-mixedsvvh` option for the `vcom` command:

```
vcom -mixedsvvh pack.vhd
```

You can include this package in your VHDL target, like a normal VHDL package:

```
use work.pack.all;
...
signal int_state : fsm_state;
signal nxt_state : fsm_state;
...
```

This package can also be imported in the SystemVerilog module containing the properties to be monitored, as if it were a SystemVerilog package.

```
import pack::*;
...
input port:
module interleaver_props (
    input clk, in_hs, out_hs,
    input fsm_state int_state
);
...
```

```

// Check for sync byte at the start of a every packet property
pkt_start_check;
- @(posedge clk) (int_state == idle && in_hs) -> (sync_in_valid);
endproperty
...

```

Now, suppose you want to implement functional coverage of the VHDL finite state machine states. With ModelSim, you can bind any SystemVerilog functionality, such as functional coverage, into a VHDL object:

```

...
covergroup sm_cvg @(posedge clk);
  coverpoint int_state
  {
    bins idle_bin = {idle};
    bins load_bins = {load_bypass, load0, load9, load10};
    bins send_bins = {send_bypass, send0, send9, send10};
    bins others = {wait_idle};
    option.at_least = 500;
  }
  coverpoint in_hs;
  in_hsXint_state: cross in_hs, int_state;
endgroup

sm_cvg sm_cvg_cl = new;
...

```

As with monitoring VHDL components, you create a wrapper to connect the SVA to the VHDL component:

```

module interleaver_binds;
...
// Bind interleaver_props to a specific interleaver instance
// and call this instantiate interleaver_props_bind
bind interleaver_m0 interleaver_props interleaver_props_bind (
  // connect the SystemVerilog ports to VHDL ports (clk)
  // and to the internal signal (int_state)
  .clk(clk), ..
  .int_state(int_state)
);
...
endmodule

```

Again, you can use either of two options to perform the actual binding in ModelSim — instantiation or the loading of multiple top modules into the simulator.

```
vsim interleaver_tester interleaver_binds
```

Binding to a VHDL Instance

ModelSim also supports the binding of SystemVerilog into VHDL design units that are defined by generate or configuration statements.

Consider the following VHDL code:

```
architecture Structure of Test is
    signal A, B, C : std_logic_vector(0 to 3);
    ...
begin
    TOP : for i in 0 to 3 generate
        First : if i = 0 generate
            - configure it..
            for all : thing use entity work.thing(architecture_ONE);
        begin
            Q    : thing port map (A(0), B(0), C(0));
        end generate;

        Second : for i in 1 to 3 generate
            - configure it..
            for all : thing use entity work.thing(architecture_TWO);
        begin
            Q    : thing port map ( A(i), B(i), C(i) );
        end generate;
    end generate;
end Structure;
```

The following SystemVerilog program defines the assertion:

```
program SVA (input c, a, b);
...
sequence s1;
    @(posedge c) a ##1 b ;
endsequence
cover property (s1);
...
endprogram
```

To tie the SystemVerilog cover directive to the VHDL component, you can use a wrapper module such as the following:

```
module sva_wrapper;
    bind test.top__2.second__1.q    // Bind a specific instance
    SVA                             // to SVA and call this
    sva_bind                         // instantiation sva_bind
    ( .a(A), .b(B), .c(C) );       // Connect the SystemVerilog ports
                                    // to VHDL ports (A, B and C)
endmodule
```

You can instantiate sva_wrapper in the top level or simply load multiple top modules into the simulator:

```
vlib work
vlog *.sv
vcom *.vhd
vsim test sva_wrapper
```

This binds the SystemVerilog program, SVA, to the specific instance defined by the generate and configuration statements.

You can control the format of generate statement labels by using the [GenerateFormat](#) variable in the *modelsim.ini* file.

Handling Bind Statements in the Compilation Unit Scope

Bind statements are allowed in module, interface, and program blocks, and may exist in the compilation unit scope. ModelSim treats the compilation unit scope (\$unit) as a package – internally wrapping the content of \$unit into a package.

Before [vsim](#) elaborates a module it elaborates all packages upon which that module depends. In other words, it elaborates a \$unit package before a module in the compilation unit scope.

It should be noted that when the **bind** statement is in the compilation unit scope, the **bind** only becomes effective when \$unit package gets elaborated by [vsim](#). In addition, the package gets elaborated only when a design unit that depends on that package gets elaborated. So if you have a file in a compilation unit scope that contains only **bind** statements, you can compile that file by itself, but the **bind** statements will never be elaborated. A warning to this effect is generated by [vlog](#) if **bind** statements are found in the compilation unit scope.

The **-cuname** argument for [vlog](#) gives a user-defined name to a specified compilation \$unit package (which, in the absence of **-cuname**, is some implicitly generated name). You must provide this named compilation unit package with the [vsim](#) command as the top level design unit in order to force elaboration.

The **-cuname** argument is used only in conjunction with the **-mfcu** argument, which instructs the compiler to treat all files within a compilation command line as a single compilation unit.

Example 10-1. Binding with -cuname and -mfcu Arguments

Suppose you have a SystemVerilog module, called *checker.sv*, that contains an assertion for checking a counter:

```
module checker(clk, reset, cnt);
  parameter SIZE = 4;
  input clk;
  input reset;
  input [SIZE-1:0] cnt;
  property check_count;
    @(posedge clk)
    !reset | => cnt == ($past(cnt) + 1);
  endproperty
  assert property (check_count);
endmodule
```

You want to **bind** that to a counter module named *counter.sv*.

```

module counter(clk, reset, cnt);
parameter SIZE = 8;
input clk;
input reset;
output [SIZE-1:0] cnt;
reg [SIZE-1:0] cnt;
always @(posedge clk)
begin
    if (reset == 1'b1)
        cnt = 0;
    else
        cnt = cnt + 1;
end
endmodule

```

The **bind** statement is in a file named *bind.sv*, which will reside in the compilation unit scope.

```
bind counter checker #(SIZE) checker_inst(clk, reset, cnt);
```

This statement instructs ModelSim to create an instance of *checker* in the target module, *counter.sv*.

The final component of this design is a test bench, named *tb.sv*.

```

module testbench;
reg clk, reset;
wire [15:0] cnt;
counter #(16) inst(clk, reset, cnt);
initial
begin
    clk = 1'b0;
    reset = 1'b1;
    #500 reset = 1'b0;
    #1000 $finish;
end
always #50 clk = ~clk;
endmodule

```

If the *bind.sv* file is compiled by itself (vlog bind.sv), you will receive a Warning like this one:

```
** Warning: 'bind' found in a compilation unit scope that either does not
contain any design units or only contains design units that are
instantiated by 'bind'. The 'bind' instance will not be elaborated.
```

To fix this problem, use the `-cname` argument with `vlog` as follows:

```
vlog -cname bind_pkg -mfcu bind.sv
```

Then simulate the design with:

```
vsim testbench bind_pkg
```

If you are using the `vlog -R` or `qverilog` commands to compile and simulate the design, this binding issue is handled properly automatically.

Limitations to Bind Support for SystemC

There exists certain restrictions on actual expressions when binding to SystemC targets. If the target of a bind is a SystemC module or an instance of a SystemC module, expressions and literals are not supported as actuals. These include, but are not limited to,

- bitwise binary expressions using operators `&`, `|`, `~`, `^` and `^~`
- concatenation expression
- bit select and part select expressions
- variable/constant

Optimizing Mixed Designs

The `vopt` command performs global optimizations to improve simulator performance. You run `vopt` on the top-level design unit. See [Optimizing Designs with vopt](#) for further details.

Simulator Resolution Limit

In a mixed-language design with only one top, the resolution of the top design unit is applied to the whole design. If the root of the mixed design is VHDL, then VHDL simulator resolution rules are used (see [Simulator Resolution Limit for VHDL](#) for VHDL details). If the root of the mixed design is Verilog or SystemVerilog, Verilog rules are used (see [Simulator Resolution Limit \(Verilog\)](#) for details). If the root is SystemC, then SystemC rules are used (see [SystemC Time Unit and Simulator Resolution](#) for details).

In the case of a mixed-language design with multiple tops, the following algorithm is used:

- If VHDL or SystemC modules are present, then the Verilog resolution is ignored. An error is issued if the Verilog resolution is finer than the chosen one.
- If both VHDL and SystemC are present, then the resolution is chosen based on which design unit is elaborated first. For example:

```
vsim sc_top vhdl_top -do vsim.do
```

In this case, the SystemC resolution (default 1 ns) is chosen.

```
vsim vhdl_top sc_top -do vsim.do
```

In this case, the VHDL resolution is chosen.

- All resolutions specified in the source files are ignored if `vsim` is invoked with the `-t` option. When set, this overrides all other resolutions.

Runtime Modeling Semantics

The ModelSim simulator is compliant with all pertinent Language Reference Manuals. To achieve this compliance, the sequence of operations in one simulation iteration (that is, delta cycle) is as follows:

- SystemC processes are run
- Signal updates are made
- HDL processes are run

The above scheduling semantics are required to satisfy both the SystemC and the HDL LRM. Namely, all processes triggered by an event in a SystemC primitive channel shall wake up at the beginning of the following delta. All processes triggered by an event on an HDL signal shall wake up at the end of the current delta. For a signal chain that crosses the language boundary, this means that processes on the SystemC side get woken up one delta later than processes on the HDL side. Consequently, one delta of skew will be introduced between such processes. However, if the processes are communicating with each other, correct system behavior will still result.

Hierarchical References to SystemVerilog

Hierarchical references to SystemVerilog properties/sequences is supported with the following restrictions.

- Clock and disable iff expressions cannot have a formal.
- Method 'matched' not supported on a hierarchically referenced sequence

Hierarchical References In Mixed HDL and SystemC Designs

A SystemC signal (including `sc_signal`, `sc_buffer`, `sc_signal_resolved`, and `sc_signal_rv`) can control or observe an HDL signal using two member functions of `sc_signal`:

```
bool control_foreign_signal(const char* name);
bool observe_foreign_signal(const char* name);
```

The argument (`const char* name`) is a full hierarchical path to an HDL signal or port. These functions always returns "true" for all cases (even if the call failed). However, an error is issued if the call could not be completed due to any reason. See tables for Verilog/SystemVerilog ([Data Type Mapping from SystemC to Verilog or SystemVerilog](#)) and VHDL ([Data Type Mapping Between SystemC and VHDL](#)) to view a list of types supported at the mixed language boundary. If it is a supported boundary type, it is supported for hierarchical references.

Note



SystemC control/observe always return “true” for all cases (even if the call failed).

Control

When a SystemC signal calls **control_foreign_signal()** on an HDL signal, the HDL signal is considered a fanout of the SystemC signal. This means that every value change of the SystemC signal is propagated to the HDL signal. If there is a pre-existing driver on the HDL signal which has been controlled, the value of the HDL signal is the resolved value of the existing driver and the SystemC signal. This value remains in effect until a subsequent driver transaction occurs on the HDL signal, following the semantics of the **force -deposit** command.

Observe

When a SystemC signal calls **observe_foreign_signal()** on an HDL signal, the SystemC signal is considered a fanout of the HDL signal. This means that every value change of the HDL signal is propagated to the SystemC signal. If there is a pre-existing driver on the SystemC signal which has been observed, the value is changed to reflect that of the HDL signal. This value remains in effect until a subsequent driver transaction occurs on the SystemC signal, following the semantics of the **force -deposit** command.

Example:

```
SC_MODULE(test_ringbuf)
{
    sc_signal<bool> observe_sig;
    sc_signal<sc_lv<4> > control_sig;

    // HDL module instance
    ringbuf* ring_INST;

    SC_CTOR(test_ringbuf)
    {
        ring_INST = new ringbuf("ring_INST", "ringbuf");
        .....

        observe_sig.observe_foreign_signal("/test_ringbuf/ring_INST/block1_INST/buffers(0)");

        control_sig.control_foreign_signal("/test_ringbuf/ring_INST/block1_INST/sig");
    }
};
```

Signal Connections Between Mixed HDL and SystemC Designs

You can use the `scv_connect()` API function to connect a SystemC signal (including `sc_signal`, `sc_buffer`, `sc_signal_resolved`, and `sc_signal_rv`) to an HDL signal.

Note



The behavior of `scv_connect()` is identical to the behavior of the [Control](#) and [Observe](#) functions, described above in [Hierarchical References In Mixed HDL and SystemC Designs](#).

The `scv_connect()` API is provided by the SystemC Verification Standard and is defined as follows:

```
/* Function to connect an sc_signal object to an HDL signal. */
template < typename T> void scv_connect(
    sc_signal<T> & signal,
    const char * hdl_signal,
    scv_hdl_direction d = SCV_OUTPUT,
    unsigned hdl_sim_inst = 0
);

/* Function to connect an sc_signal_resolved object to an HDL signal. */
void scv_connect(
    sc_signal_resolved& signal,
    const char * hdl_signal,
    scv_hdl_direction d = SCV_OUTPUT,
    unsigned hdl_sim_inst = 0
);

/* Function connects an sc_signal_rv object to an HDL signal. */
template < int W> void scv_connect(
    sc_signal_rv<W>& signal,
    const char * hdl_signal,
    scv_hdl_direction d = SCV_OUTPUT,
    unsigned hdl_sim_inst = 0
);
```

where

- `signal` is an `sc_signal`, `sc_signal_resolved` or `sc_signal_rv` object
- `hdl_signal` is the full hierarchical path to an HDL signal or port
- `d` is the direction of the connection given by enum `scv_hdl_direction`
- `hdl_sim_inst` is not supported—any value given for this argument will be ignored

```
enum scv_hdl_direction {
```

```

    SCV_INPUT = 1, /* HDL is the only driver */
    SCV_OUTPUT = 2 /* SystemC is the only driver */
};

```

Supported Types

The `scv_connect()` function supports all datatypes supported at the SystemC-HDL mixed-language boundaries. Refer to the tables for Verilog/SystemVerilog ([Data Type Mapping from SystemC to Verilog or SystemVerilog](#)) and VHDL ([Data Type Mapping Between SystemC and VHDL](#)) to view a list of types supported at the mixed language boundary. If it is a supported boundary type, it is supported for hierarchical references.

Mapping Data Types

Cross-language (HDL) instantiation does not require additional effort on your part. As ModelSim loads a design, it detects cross-language instantiations because it can determine the language type of each design unit as it is loaded from a library. ModelSim then performs the necessary adaptations and data type conversions automatically. SystemC and HDL cross-language instantiation requires minor modification of SystemC source code (addition of `SC_MODULE_EXPORT`, `sc_foreign_module`, and so forth).

A VHDL instantiation of Verilog may associate VHDL signals and values with Verilog ports and parameters. Likewise, a Verilog instantiation of VHDL may associate Verilog nets and values with VHDL ports and generics. This is also true for SystemC and VHDL/Verilog/SystemVerilog ports.

Mixed-language mappings for ModelSim:

- [Verilog and SystemVerilog to VHDL Mappings](#)
- [VHDL To Verilog and SystemVerilog Mappings](#)
- [Verilog or SystemVerilog and SystemC Signal Interaction And Mappings](#)
- [VHDL and SystemC Signal Interaction And Mappings](#)
- [Verilog or SystemVerilog and SystemC Signal Interaction And Mappings](#)

Verilog and SystemVerilog to VHDL Mappings

[Table 10-2](#) shows the mapping of data types from SystemVerilog to VHDL.

Table 10-2. SystemVerilog-to-VHDL Data Types Mapping

SystemVerilog Type	VHDL Type		Comments
	Primary mapping	Secondary mapping	
bit	bit	std_logic	2 state scalar data type

Table 10-2. SystemVerilog-to-VHDL Data Types Mapping

SystemVerilog Type	VHDL Type		Comments
	Primary mapping	Secondary mapping	
logic	std_logic	bit	4 state scalar data type
reg	std_logic	bit	4 state scalar data type
wire	std_logic	bit	A scalar wire
bit vector	bit_vector	std_logic_vector	A signed/unsigned, packed/unpacked single dimensional bit vector
reg vector	std_logic_vector	bit_vector	A signed/unsigned, packed/unpacked single dimensional logic vector
wire vector	std_logic_vector	bit_vector	A signed/unsigned, packed/unpacked single dimensional multi-bit wire
logic vector	std_logic_vector	bit_vector	A signed/unsigned, packed/unpacked single dimensional logic vector
integer	integer		4-state data type, 32 bit signed integer
integer unsigned	integer		4-state data type, 32 bit unsigned integer
int	integer		2-state data type, 32 bit signed integer
shortint	integer		2-state data type, 16 bit signed integer
longint	integer		2-state data type, 64 bit signed integer
int unsigned	integer		2-state data type, 32 bit unsigned integer
shortint unsigned	integer		2-state data type, 16 bit unsigned integer
longint unsigned	integer		2-state data type, 64 bit unsigned integer
byte	integer		2-state data type, 8 bit signed integer or ASCII character

Table 10-2. SystemVerilog-to-VHDL Data Types Mapping

SystemVerilog Type	VHDL Type		Comments
	Primary mapping	Secondary mapping	
byte unsigned	integer		2-state data type, 8 bit unsigned integer or ASCII character
enum	enum		SV enums of only 2-state int base type supported
struct	record		unpacked structure
packed struct	record	std_logic_vector bit_vector	packed structure
real	real		2-state data type, 64-bit real number
shortreal	real		2-state data type, 32-bit real number
multi-D arrays	multi-D arrays		multi-dimensional arrays of supported types

Verilog Parameters

The type of a Verilog parameter is determined by its initial value.

Table 10-3. Verilog Parameter to VHDL Mapping

Verilog type	VHDL type
integer	integer
real	real
string	string
packed vector	std_logic_vector bit_vector

Verilog Ports

Table 10-4 lists the allowed VHDL types for ports connected to Verilog nets and for signals connected to Verilog ports. Note that you can use the wildcard syntax convention (.*) when instantiating Verilog ports where the instance port name matches the connecting port name and their data types are equivalent.

Table 10-4. Allowed VHDL Types for Verilog Ports

bit	std_ulogic
-----	------------

bit_vector	std_logic_vector
enum	std_ulogic_vector
integer	vl_logic
natural	vl_ulogic
positive	vl_logic_vector
record	vl_ulogic_vector
std_logic	multi-dimensional arrays

The vl_logic type is an enumeration that defines the full state set for Verilog nets, including ambiguous strengths. The bit and std_logic types are convenient for most applications, but the vl_logic type is provided in case you need access to the full Verilog state set. For example, you may wish to convert between vl_logic and your own user-defined type. The vl_logic type is defined in the vl_types package in the pre-compiled **verilog** library. This library is provided in the installation directory along with the other pre-compiled libraries (**std** and **ieee**). The vl_logic type is defined in the following file installed with ModelSim:

```
<install_dir>/vhdl_src/verilog/vltypes.vhd
```

Verilog States

Verilog states are mapped to std_logic and bit as follows:

Table 10-5. Verilog States Mapped to std_logic and bit

Verilog	std_logic	bit
HiZ	'Z'	'0'
Sm0	'L'	'0'
Sm1	'H'	'1'
SmX	'W'	'0'
Me0	'L'	'0'
Me1	'H'	'1'
MeX	'W'	'0'
We0	'L'	'0'
We1	'H'	'1'
WeX	'W'	'0'
La0	'L'	'0'
La1	'H'	'1'

Table 10-5. Verilog States Mapped to std_logic and bit

Verilog	std_logic	bit
LaX	'W'	'0'
Pu0	'L'	'0'
Pu1	'H'	'1'
PuX	'W'	'0'
St0	'0'	'0'
St1	'1'	'1'
StX	'X'	'0'
Su0	'0'	'0'
Su1	'1'	'1'
SuX	'X'	'0'

For Verilog states with ambiguous strength:

- bit receives '0'
- std_logic receives 'X' if either the 0 or 1 strength component is greater than or equal to strong strength
- std_logic receives 'W' if both the 0 and 1 strength components are less than strong strength

VHDL To Verilog and SystemVerilog Mappings

The following table illustrates mapping of data types from VHDL to SystemVerilog.

Table 10-6. VHDL to SystemVerilog Data Types Mapping

VHDL Type	SystemVerilog Type		Comments
	Primary mapping	Secondary mapping	
bit	bit	reg, logic	2-state scalar data type
std_logic	reg	bit, logic	4-state scalar data type
bit_vector	bit vector	reg vector, wire vector, logic vector, struct packed	A signed/unsigned, packed/unpacked bit vector
std_logic_vector	reg vector	bit_vector, wire vector, logic vector, struct packed	A signed/unsigned, packed/unpacked logic vector

Table 10-6. VHDL to SystemVerilog Data Types Mapping (cont.)

VHDL Type	SystemVerilog Type		Comments
	Primary mapping	Secondary mapping	
integer	int	integer, shortint, longint, int unsigned, shortint unsigned, longint unsigned, byte, byte unsigned	2-state data type, 32 bit signed integer
enum	enum		VHDL enumeration types
record	struct	packed struct	VHDL records
real	real	shortreal	2-state data type, 64-bit real number
multi-D arrays	multi-D arrays		multi-dimensional arrays of supported types

VHDL Generics

Table 10-7 shows the mapping of VHDL Generics to Verilog types.

Table 10-7. VHDL Generics to Verilog Mapping

VHDL type	Verilog type
integer, real, time, physical, enumeration	integer or real
string	string literal
bit, st_logic, bit_vector, std_logic_vector, vl_logic, vl_logic_vector ¹	packed vector

1. Note that Verilog vectors (such as 3'b011) that can be represented as an integer value are mapped to generic of integer type (to preserve backward compatibility). Only vectors whose values cannot be represented as integers (such as 3'b0xx) are mapped to generics of this type.

When a scalar type receives a real value, the real is converted to an integer by truncating the decimal portion.

Type time is treated specially: the Verilog number is converted to a time value according to the **'timescale** directive of the module.

Physical and enumeration types receive a value that corresponds to the position number indicated by the Verilog number. In VHDL this is equivalent to T'VAL(P), where T is the type, VAL is the predefined function attribute that returns a value given a position number, and P is the position number.

VHDL type bit is mapped to Verilog states as shown in [Table 10-8](#):

Table 10-8. Mapping VHDL bit to Verilog States

VHDL bit	Verilog State
'0'	St0
'1'	St1

VHDL type std_logic is mapped to Verilog states as shown in [Table 10-9](#):

Table 10-9. Mapping VHDL std_logic Type to Verilog States

VHDL std_logic	Verilog State
'U'	StX
'X'	StX
'0'	St0
'1'	St1
'Z'	HiZ
'W'	PuX
'L'	Pu0
'H'	Pu1
'_'	StX

Verilog or SystemVerilog and SystemC Signal Interaction And Mappings

SystemC design units are interconnected via hierarchical and primitive channels. An `sc_signal<>` is one type of primitive channel. The following section discusses how various SystemC channel types map to Verilog wires when connected to each other across the language boundary.

Channel and Port Type Mapping

The following port type mapping table lists all channels. Three types of primitive channels and one hierarchical channel are supported on the language boundary (SystemC modules connected to Verilog modules).

Table 10-10. Channel and Port Type Mapping

Channels	Ports	Verilog mapping
sc_signal<T>	sc_in<T> sc_out<T>sc_inout<T>	Depends on type T. See table entitled Data Type Mapping from SystemC to Verilog or SystemVerilog .
sc_signal_rv<W>	sc_in_rv<W> sc_out_rv<W> sc_inout_rv<W>	wire [W-1:0]
sc_signal_resolved	sc_in_resolved sc_out_resolved sc_inout_resolved	wire [W-1:0]
sc_clock	sc_in_clk sc_out_clk sc_inout_clk	wire
sc_mutex	N/A	Not supported on language boundary
sc_fifo	sc_fifo_in sc_fifo_out	Not supported on language boundary
sc_semaphore	N/A	Not supported on language boundary
sc_buffer	N/A	Not supported on language boundary
user-defined	user-defined	Not supported on language boundary ¹

1. User defined SystemC channels and ports derived from built-in SystemC primitive channels and ports can be connected to HDL signals. The built-in SystemC primitive channel or port must be already supported at the mixed-language boundary for the derived class connection to work.

A SystemC sc_out port connected to an HDL signal higher up in the design hierarchy is treated as a pure output port. A read() operation on such an sc_out port might give incorrect values. Use an sc_inout port to do both read() and write() operations.

Data Type Mapping from SystemC to Verilog or SystemVerilog

Table 10-11 shows the correspondence of SystemC data types to SystemVerilog data types.

Table 10-11. Data Type Mapping – SystemC to Verilog or SystemVerilog

SystemC Type	SystemVerilog Primary Mapping	SystemVerilog Secondary Mapping
enum ¹	enum	-
bool	bit	logic wire
char	byte	bit [7:0] logic [7:0] wire [7:0]
unsigned char	byte unsigned	bit [7:0] logic [7:0] wire [7:0]
short	shortint	bit [15:0] logic [15:0] wire [15:0]
unsigned short	shortint unsigned	bit [15:0] logic [15:0] wire [15:0]
int	int	integer bit [31:0] logic [31:0] wire [31:0]
unsigned int	int unsigned	integer unsigned bit [31:0] logic [31:0] wire [31:0]
long	longint (for 64 bit) int (for 32 bit)	bit [W-1:0] logic [W-1:0] wire [W-1:0], where W=64 on 64-bit W=32 on 32-bit
unsigned long	longint unsigned (64-bit) int unsigned (32-bit)	bit [W-1:0] logic [W-1:0] wire [W-1:0], where W=64 on 64-bit W=32 on 32-bit

Table 10-11. Data Type Mapping – SystemC to Verilog or SystemVerilog

SystemC Type	SystemVerilog Primary Mapping	SystemVerilog Secondary Mapping
long long	longint	bit [63:0] logic [63:0] wire [63:0]
unsigned long long	longint unsigned	bit [63:0] logic [63:0] wire [63:0]
sc_bit	bit	logic wire
sc_logic	logic	bit wire
sc_bv	bit [W-1:0]	logic [W-1:0] wire [W-1:0]
sc_lv	logic [W-1:0]	bit [W-1:0] wire [W-1:0]
float	shortreal	N/A
double	real	N/A
struct ^{2,3}	struct	struct packed
union ²	packed union	N/A
sc_int<W> / sc_signed ²	shortint (if W=16) int (if W=32) longint (if W=64) bit [W-1:0] (otherwise)	logic [W-1:0] wire [W-1:0]
sc_uint<W> / sc_unsigned	shortint unsigned (if W=16) int unsigned (if W=32) longint unsigned (if W=64) bit [W-1:0] (otherwise)	logic [W-1:0] wire [W-1:0]
sc_bigint<W>	bit [W-1:0]	logic [W-1:0] wire [W-1:0]
sc_biguint<W>	bit [W-1:0]	logic [W-1:0] wire [W-1:0]
sc_fixed<W,I,Q,O,N> sc_ufixed<W,I,Q,O,N>	bit [W-1:0]	logic [W-1:0] wire [W-1:0]
sc_fixed_fast<W,I,Q,O,N> sc_ufixed_fast<W,I,Q,O,N>	bit [W-1:0]	logic [W-1:0] wire [W-1:0]
sc_fix sc_ufix	bit [WL-1:0] ⁴	logic [W-1:0] wire [W-1:0]

Table 10-11. Data Type Mapping – SystemC to Verilog or SystemVerilog

SystemC Type	SystemVerilog Primary Mapping	SystemVerilog Secondary Mapping
sc_fix_fast sc_ufix_fast	bit [WL-1:0]	logic [W-1:0] wire [W-1:0]

1. Refer to [enum, struct, and union at SC-SV Mixed-Language Boundary](#) for more information on these complex types.
2. To make a port of type sc_signed or sc_unsigned of word length other than the default (32), you must use sc_length_param and sc_length_context to set the word length. For more information, see [Construction Parameters for SystemC Types](#).
3. Supports real and shortreal as field types.
4. WL (word length) is the total number of bits used in the type. It is specified during runtime. To make a port of type sc_fix, sc_ufix, sc_fix_fast, or sc_ufix_fast of word length other than the default(32), you must use sc_fxtype_params and sc_fxtype_context to set the word length. For more information, see [Construction Parameters for SystemC Types](#).

Data Type Mapping from Verilog or SystemVerilog to SystemC

Table 10-12 shows the correspondence of Verilog/SystemVerilog data types to SystemC data types.

Table 10-12. Data Type Mapping – Verilog or SystemVerilog to SystemC

Verilog/ SystemVerilog Type	SystemC Primary Mapping	SystemC Secondary Mapping
bit	bool	sc_bit sc_logic
logic	sc_logic	sc_bit bool
reg	sc_logic	sc_bit bool
bit vector	sc_bv<W>	sc_lv<W> sc_int<W> sc_uint<W>
logic vector	sc_lv<W>	sc_bv<W> sc_int<W> sc_uint<W>
reg vector	sc_lv<W>	sc_bv<W> sc_int<W> sc_uint<W>
wire vector	sc_lv<W>	sc_bv<W> sc_int<W> sc_uint<W>
wire	sc_logic	sc_bit bool
integer	sc_lv<32>	int sc_int<32>
integer unsigned	sc_lv<32>	unsigned int sc_uint<32> sc_bv<32>
int	int	sc_lv<32> sc_int<32> sc_bv<32>
shortint	short	sc_lv<16> sc_int<16> sc_bv<16>

Table 10-12. Data Type Mapping – Verilog or SystemVerilog to SystemC

Verilog/ SystemVerilog Type	SystemC Primary Mapping	SystemC Secondary Mapping
longint	long long	sc_lv<64> sc_int<64> sc_bv<64> long (for 64-bit)
longint unsigned	unsigned long long	sc_lv<64> sc_uint<64> sc_bv<64> unsigned long (for 64-bit)
byte	char	sc_lv<8> sc_int<8> sc_bv<8>
byte unsigned	unsigned char	sc_lv<8> sc_uint<8> sc_bv<8>
enum ¹	enum	-
struct ¹	struct	-
packed struct	struct	
packed union ^{1, 2}	union	-
real ²	double	-
shortreal ²	float	-
multi-D array ^{2, 3}	multi-D array	-

1. Refer to [enum, struct, and union at SC-SV Mixed-Language Boundary](#) for more information on these complex types.
2. Unpacked and tagged unions are not supported at the SC-SV mixed language boundary.
3. Classes, multi-dimensional arrays, unpacked/tagged unions, strings and handles are not supported for SystemC control/observe.

enum, struct, and union at SC-SV Mixed-Language Boundary

The following guidelines apply to the use of enumerations, structures and unions at the SystemC/SystemVerilog mixed language boundary.

Enumerations

A SystemVerilog enum may be used at the SystemC - SystemVerilog language boundary if it meets the following criteria:

- Base type of the SystemVerilog enum must be int (32-bit 2-state integer).

- The value of enum elements are not ambiguous and are equal to the value of the corresponding value of enum elements on the SystemC side.

Enums with different strings are allowed at the language boundary as long as the values on both sides are identical.

- SystemVerilog enums with 'range of enumeration elements' are allowed provided the corresponding enum is correctly defined (manually) on the SystemC side.

Unions and Structures

You can use a SystemVerilog union or structure at a SystemC-SystemVerilog boundary if it meets the following criteria:

- The type of all elements of the union/structure is one of the supported types.
- The type of the corresponding elements of the SystemC union/structure follow the supported type mapping for variable ports on the SC-SV language boundary. See [Channel and Port Type Mapping](#) for mapping information.
- The number and order of elements in the definition of structures on SystemVerilog and SystemC side is the same.

For unions, the order of elements may be different, but the number of elements must be the same.

- Union must be packed and untagged. While both packed and unpacked structures are supported, only packed unions are supported at the SystemC-SystemVerilog language boundary.

Port Direction

Verilog port directions are mapped to SystemC as shown in [Table 10-13](#). Note that you can use the wildcard syntax convention (.*) when instantiating Verilog ports where the instance port name matches the connecting port name and their data types are equivalent.

Table 10-13. Mapping Verilog Port Directions to SystemC

Verilog	SystemC
input	sc_in<T> sc_in_resolved sc_in_rv<W>
output	sc_out<T> sc_out_resolved sc_out_rv<W>
inout	sc_inout<T> sc_inout_resolved sc_inout_rv<W>

Verilog to SystemC State Mappings

Verilog states are mapped to `sc_logic`, `sc_bit`, and `bool` as shown in [Table 10-14](#).

Table 10-14. Mapping Verilog States to SystemC States

Verilog	sc_logic	sc_bit	bool
HiZ	'Z'	'0'	false
Sm0	'0'	'0'	false
Sm1	'1'	'1'	true
SmX	'X'	'0'	false
Me0	'0'	'0'	false
Me1	'1'	'1'	true
MeX	'X'	'0'	false
We0	'0'	'0'	false
We1	'1'	'1'	true
WeX	'X'	'0'	false
La0	'0'	'0'	false
La1	'1'	'1'	true
LaX	'X'	'0'	false
Pu0	'0'	'0'	false
Pu1	'1'	'1'	true
PuX	'X'	'0'	false
St0	'0'	'0'	false
St1	'1'	'1'	true
StX	'X'	'0'	false
Su0	'0'	'0'	false
Su1	'1'	'1'	true
SuX	'X'	'0'	false

For Verilog states with ambiguous strength:

- `sc_bit` receives '1' if the value component is 1, else it receives '0'
- `bool` receives true if the value component is 1, else it receives false
- `sc_logic` receives 'X' if the value component is X, H, or L

- `sc_logic` receives '0' if the value component is 0
- `sc_logic` receives '1' if the value component is 1

SystemC to Verilog State Mappings

SystemC type `bool` is mapped to Verilog states as shown in [Table 10-15](#):

Table 10-15. Mapping SystemC `bool` to Verilog States

bool	Verilog
false	St0
true	St1

SystemC type `sc_bit` is mapped to Verilog states as shown in [Table 10-16](#):

Table 10-16. Mapping SystemC `sc_bit` to Verilog States

sc_bit	Verilog
'0'	St0
'1'	St1

SystemC type `sc_logic` is mapped to Verilog states as shown in [Table 10-17](#):

Table 10-17. Mapping SystemC `sc_logic` to Verilog States

sc_logic	Verilog
'0'	St0
'1'	St1
'Z'	HiZ
'X'	StX

VHDL and SystemC Signal Interaction And Mappings

SystemC has a more complex signal-level interconnect scheme than VHDL. Design units are interconnected with hierarchical and primitive channels. An `sc_signal<>` is one type of primitive channel. The following section discusses how various SystemC channel types map to VHDL types when connected to each other across the language boundary.

Port Type Mapping

Table 10-18 lists port type mappings for all channels. Three types of primitive channels and one hierarchical channel are supported on the language boundary (SystemC modules connected to VHDL modules).

Table 10-18. SystemC Port Type Mapping

Channels	Ports	VHDL mapping
sc_signal<T>	sc_in<T> sc_out<T> sc_inout<T>	Depends on type T. See table entitled Data Type Mapping Between SystemC and VHDL .
sc_signal_rv<W>	sc_in_rv<W> sc_out_rv<W> sc_inout_rv<W>	std_logic_vector(W-1 downto 0)
sc_signal_resolved	sc_in_resolved sc_out_resolved sc_inout_resolved	std_logic
sc_clock	sc_in_clk sc_out_clk sc_inout_clk	bit/std_logic/boolean
sc_mutex	N/A	Not supported on language boundary
sc_fifo	sc_fifo_in sc_fifo_out	Not supported on language boundary
sc_semaphore	N/A	Not supported on language boundary
sc_buffer	N/A	Not supported on language boundary
user-defined	user-defined	Not supported on language boundary ¹

1. User defined SystemC channels and ports derived from built-in SystemC primitive channels and ports can be connected to HDL signals. The built-in SystemC primitive channel or port must be already supported at the mixed-language boundary for the derived class connection to work.

A SystemC sc_out port connected to an HDL signal higher up in the design hierarchy is treated as a pure output port. A read() operation on such an sc_out port might give incorrect values. Use an sc_inout port to do both read() and write() operations.

Data Type Mapping Between SystemC and VHDL

Table 10-19 lists the mapping between SystemC `sc_signal` types and VHDL types.

Table 10-19. Mapping Between SystemC `sc_signal` and VHDL Types

SystemC	VHDL
bool, sc_bit	bit/std_logic/boolean
sc_logic	std_logic
sc_bv<W>	bit_vector(W-1 downto 0)
sc_lv<W>	std_logic_vector(W-1 downto 0)
sc_bv<32>, sc_lv<32>	integer
sc_bv<64>, sc_lv<64>	real
sc_int<W>, sc_uint<W>	bit_vector(W-1 downto 0) std_logic_vector(W -1 downto 0)
sc_bigint<W>, sc_biguint<W>	bit_vector(W-1 downto 0) std_logic_vector(W-1 downto 0)
sc_fixed<W,I,Q,O,N>, sc_ufixed<W,I,Q,O,N>	bit_vector(W-1 downto 0) std_logic_vector(W-1 downto 0)
sc_fixed_fast<W,I,Q,O,N>, sc_ufixed_fast<W,I,Q,O,N>	bit_vector(W-1 downto 0) std_logic_vector(W-1 downto 0)
¹ sc_fix, ¹ sc_ufix	bit_vector(WL-1 downto 0) std_logic_vector(WL- 1 downto 0)
¹ sc_fix_fast, ¹ sc_ufix_fast	bit_vector(WL-1 downto 0) std_logic_vector(WL- 1 downto 0)
² sc_signed, ² sc_unsigned	bit_vector(WL-1 downto 0) std_logic_vector(WL- 1 downto 0)
char, unsigned char	bit_vector(7 downto 0) std_logic_vector(7 downto 0)
short, unsigned short	bit_vector(15 downto 0) std_logic_vector(15 downto 0)
int, unsigned int	bit_vector(31 downto 0) std_logic_vector(7 downto 0)
long, unsigned long	bit_vector(31 downto 0) std_logic_vector(31 downto 0)
long long, unsigned long long	bit_vector(63 downto 0) std_logic_vector(63 downto 0)

Table 10-19. Mapping Between SystemC `sc_signal` and VHDL Types (cont.)

SystemC	VHDL
float	bit_vector(31 downto 0) std_logic_vector(31 downto 0)
double	bit_vector(63 downto 0) std_logic_vector(63 downto 0) real
struct	record
enum	enum
record ³	record element_declaration {element_declaration} end record [record_type_simple_name]
signal array ⁴	type signal_name array (constraint_definition) of signal_type
Not supported on language boundary (no equivalent SystemC type)	multi-D array
pointer	Not supported on language boundary (no equivalent VHDL type)
class	Not supported on language boundary (no equivalent VHDL type)
union	Not supported on language boundary (no equivalent VHDL type)
bit_fields	Not supported on language boundary (no equivalent VHDL type)
Not supported on language boundary (no equivalent SystemC type)	access
Not supported on language boundary (no equivalent SystemC type)	protected

1. WL (word length) is the total number of bits used in the type. It is specified during runtime. To make a port of type `sc_fix`, `sc_ufix`, `sc_fix_fast`, or `sc_ufix_fast` of word length other than the default(32), you must use `sc_fxtype_params` and `sc_fxtype_context` to set the word length. For more information, see [Construction Parameters for SystemC Types](#).
2. To make a port of type `sc_signed` or `sc_unsigned` of word length other than the default (32), you must use `sc_length_param` and `sc_length_context` to set the word length. For more information, see [Construction Parameters for SystemC Types](#).
3. Including nested records.
4. SystemC signal arrays are supported only for cases where VHDL instantiates a SystemC module—not vice versa.

Type Checking—Records

Two records at the SystemC-VHDL mixed-language boundary will be equivalent if all of the following conditions hold true for them:

- The number and order of elements in the definition of records on VHDL and SystemC side is the same.
- Size of each field of one record is exactly same as the size of the corresponding field in the second record.
- Type of each field of both the records is supported at the SystemC-VHDL boundary.
- Mapping between corresponding field types is permitted at the SystemC-VHDL boundary.

Type Checking—Enums

Two enumerated types at the SystemC-VHDL mixed-language boundary will be equivalent if all of the following conditions hold true for them:

- The number of elements of both enums is the same.
- The element values of both enums is the same. SystemC allows enums to have noncontinuous enum values, but VHDL allows only consecutive enum values (starting from 0) for enums. As such, this check limits the element values of SystemC enums to be consecutive integers starting from 0.
- A warning message will occur if the enum labels (enum strings) for both the enums at the SystemC-VHDL boundary are different but their values are the same.

Type Checking—Signal Arrays

SystemC signal arrays can be connected to VHDL array only if both the following conditions hold true for them:

- The number of elements in the SystemC signal array and the VHDL array is the same.
- Mapping between the type of SystemC signal array and the type of the element of the VHDL array is permitted at the SystemC-VHDL boundary.

Note



SystemC signal arrays are supported only for cases where VHDL instantiates a SystemC module—not vice versa.

Port Direction Mapping

VHDL port directions are mapped to SystemC as shown in [Table 10-20](#):

Table 10-20. Mapping VHDL Port Directions to SystemC

VHDL	SystemC
in	sc_in<T>, sc_in_resolved, sc_in_rv<W>
out	sc_out<T>, sc_out_resolved, sc_out_rv<W>
inout	sc_inout<T>, sc_inout_resolved, sc_inout_rv<W>
buffer	sc_out<T>, sc_out_resolved, sc_out_rv<W>

Note



VHDL constants are supported for port connections at a VHDL-SystemC boundary.

VHDL to SystemC State Mapping

VHDL states are mapped to sc_logic, sc_bit, and bool as shown in [Table 10-21](#):

Table 10-21. Mapping VHDL std_logic States to SystemC States

std_logic	sc_logic	sc_bit	bool
'U'	'X'	'0'	false
'X'	'X'	'0'	false
'0'	'0'	'0'	false
'1'	'1'	'1'	true
'Z'	'Z'	'0'	false
'W'	'X'	'0'	false
'L'	'0'	'0'	false
'H'	'1'	'1'	true
'-'	'X'	'0'	false

SystemC to VHDL State Mapping

SystemC type `bool` is mapped to VHDL boolean as shown in [Table 10-22](#):

Table 10-22. Mapping SystemC `bool` to VHDL Boolean States

bool	VHDL
false	false
true	true

SystemC type `sc_bit` is mapped to VHDL bit as shown in [Table 10-23](#):

Table 10-23. Mapping SystemC `sc_bit` to VHDL bit

sc_bit	VHDL
'0'	'0'
'1'	'1'

SystemC type `sc_logic` is mapped to VHDL `std_logic` states as shown in [Table 10-24](#):

Table 10-24. Mapping SystemC `sc_logic` to VHDL `std_logic`

sc_logic	std_logic
'0'	'0'
'1'	'1'
'Z'	'Z'
'X'	'X'

VHDL Instantiating Verilog or SystemVerilog

Once you have generated a component declaration for a Verilog module, you can instantiate the component just like any other VHDL component. You can reference a Verilog module in the entity aspect of a component configuration—all you need to do is specify a module name instead of an entity name. You can also specify an optional secondary name for an optimized sub-module.

Further, you can reference a Verilog configuration in the configuration aspect of a VHDL component configuration—just specify a Verilog configuration name instead of a VHDL configuration name.

Verilog/SystemVerilog Instantiation Criteria Within VHDL

A Verilog design unit may be instantiated within VHDL if it meets the following criteria:

- The design unit is a module or configuration. UDPs are not allowed.
- The ports are named ports of type: reg, logic, bit, one-dimensional arrays of reg/logic/bit, integer, int, shortint, longint, byte, integer unsigned, int unsigned, shortint unsigned, longint unsigned, byte unsigned. (See also, [Modules with Unnamed Ports](#)).

Component Declaration for VHDL Instantiating Verilog

A Verilog module that is compiled into a library can be referenced from a VHDL design as though the module is a VHDL entity. Likewise, a Verilog configuration can be referenced as though it were a VHDL configuration.

You can extract the interface to the module from the library in the form of a component declaration by running [vgencomp](#). Given a library and module name, the vgencomp command writes a component declaration to standard output.

The default component port types are:

- std_logic
- std_logic_vector

Optionally, you can choose one of the following:

- bit and bit_vector
- vl_logic and vl_logic_vector

VHDL and Verilog Identifiers

The VHDL identifiers for the component name, port names, and generic names are the same as Verilog and SystemVerilog identifiers for the module name, port names, and parameter names. Except for the cases noted below, ModelSim does nothing to the Verilog identifier when it generates the entity.

ModelSim converts Verilog identifiers to VHDL 1076-1993 extended identifiers in three cases:

- The Verilog identifier is not a valid VHDL 1076-1987 identifier.
- You compile the Verilog module with the **-93** argument. One exception is a valid, lowercase identifier (for instance, topmod). Valid, lowercase identifiers will not be converted even if you compile with **-93**.

- The Verilog identifier is not unique when case is ignored. For example, if you have TopMod and topmod in the same module, ModelSim will convert the former to \TopMod\.

vgencomp Component Declaration when VHDL Instantiates Verilog

`vgencomp` generates a component declaration according to these rules:

- Generic Clause

A generic clause is generated if the module has parameters. A corresponding generic is defined for each parameter that has an initial value that does not depend on any other parameters.

The generic type is determined by the parameter's initial value as follows:

Parameter value	Generic type
integer	integer
real	real
string literal	string

The default value of the generic is the same as the parameter's initial value. For example:

Verilog parameter	VHDL generic
parameter p1 = 1 - 3;	p1 : integer := -2;
parameter p2 = 3.0;	p2 : real := 3.000000;
parameter p3 = "Hello";	p3 : string := "Hello";

- Port Clause

A port clause is generated if the module has ports. A corresponding VHDL port is defined for each named Verilog port.

You can set the VHDL port type to `bit`, `std_logic`, or `vl_logic`. If the Verilog port has a range, then the VHDL port type is `bit_vector`, `std_logic_vector`, or `vl_logic_vector`. If the range does not depend on parameters, then the vector type will be constrained accordingly, otherwise it will be unconstrained. For example:

Verilog port	VHDL port
input p1;	p1 : in std_logic;
output [7:0] p2;	p2 : out std_logic_vector(7 downto 0);
output [4:7] p3;	p3 : out std_logic_vector(4 to 7);

Verilog port	VHDL port
inout [W-1:0] p4;	p4 : inout std_logic_vector;

Configuration declarations are allowed to reference Verilog modules in the entity aspects of component configurations. However, the configuration declaration cannot extend into a Verilog instance to configure the instantiations within the Verilog module.

Modules with Bidirectional Pass Switches

Modules that have bidirectional pass switches (tran primitives) internally connected to their ports are not fully supported when the module is instantiated by VHDL. This is due to limitations imposed by the requirements of VHDL signal resolution.

However, full bidirectional operation is supported if the following requirements are met:

- The Verilog port is declared with mode inout.
- The connected VHDL signal is of type or subtype std_logic.
- The connected port hierarchy above the VHDL signal does not cross any other mixed language boundaries, and the top-level signal is also of type or subtype std_logic.

In all other cases, the following warning is issued at elaboration and the simulation of the Verilog port may produce incorrect results if the design actually drives in both directions across the port:

**** Warning: (vsim-3011) testfile(4): [TRAN] - Verilog net 'n' with bidirectional tran primitives might not function correctly when connected to a VHDL signal.**

If you use the port solely in a unidirectional manner, then you should explicitly declare it as either input or output (whichever matches the direction of the signal flow).

Modules with Unnamed Ports

Verilog allows modules to have unnamed ports, whereas VHDL requires that all ports have names. If any of the Verilog ports are unnamed, then all are considered to be unnamed, and it is not possible to create a matching VHDL component. In such cases, the module may not be instantiated from VHDL.

Unnamed ports occur when the module port list contains bit-selects, part-selects, or concatenations, as in the following example:

```
module m(a[3:0], b[1], b[0], {c,d});
  input [3:0] a;
  input [1:0] b;
  input c, d;
endmodule
```


Note that `a[3:0]` is considered to be unnamed even though it is a full part-select. A common mistake is to include the vector bounds in the port list, which has the undesired side effect of making the ports unnamed (which prevents you from connecting by name even in an all-Verilog design).

Most modules having unnamed ports can be easily rewritten to explicitly name the ports, thus allowing the module to be instantiated from VHDL. Consider the following example:

```
module m(y[1], y[0], a[1], a[0]);
    output [1:0] y;
    input [1:0] a;
endmodule
```

Here is the same module rewritten with explicit port names added:

```
module m(.y1(y[1]), .y0(y[0]), .a1(a[1]), .a0(a[0]));
    output [1:0] y;
    input [1:0] a;
endmodule
```

Empty Ports

Verilog modules may have "empty" ports, which are also unnamed, but they are treated differently from other unnamed ports. If the only unnamed ports are empty, then the other ports may still be connected to by name, as in the following example:

```
module m(a, , b);
    input a, b;
endmodule
```

Although this module has an empty port between ports `a` and `b`, the named ports in the module can still be connected to or from VHDL.

Verilog or SystemVerilog Instantiating VHDL

You can reference a VHDL entity or configuration from Verilog or SystemVerilog as though the design unit is a module or a configuration of the same name.

VHDL Instantiation Criteria Within Verilog

You can instantiate a VHDL design unit within Verilog or SystemVerilog if it meets the following criteria:

- The design unit is an entity/architecture pair or a configuration.
- The entity ports are of type: `bit`, `bit_vector`, `enum`, `integer`, `natural`, `positive`, `real`, `shortreal`, `std_logic`, `std_ulogic`, `std_logic_vector`, `std_ulogic_vector`, `vl_ulogic`,

vl_logic_vector, or their subtypes; unconstrained arrays; nested records; and records with fields of type integer, real, enum, and multi-dimensional arrays.

The port clause may have any mix of these types. Multi-dimensional arrays of these support types are also supported.

- The generics are of type bit, bit_vector, integer, real, std_logic, std_logic_vector, vl_logic, vl_logic_vector, time, physical, enumeration, or string.

String is the only composite type allowed.

Entity and Architecture Names and Escaped Identifiers

An entity name is not case-sensitive in Verilog instantiations. The entity default architecture is selected from the work library unless specified otherwise. Since instantiation bindings are not determined at compile time in Verilog, you must instruct the simulator to search your libraries when loading the design. See [Library Usage](#) for more information.

Alternatively, you can employ the escaped identifier to provide an extended form of instantiation:

```
\mylib.entity(arch) ul (a, b, c);  
\mylib.entity ul (a, b, c);  
\entity(arch) ul (a, b, c);
```

If the escaped identifier takes the form of one of the above and is not the name of a design unit in the work library, then the instantiation is broken down as follows:

- library = mylib
- design unit = entity
- architecture = arch

Named Port Associations

Port associations may be named or positional. Use the same port names and port positions that appear in the entity.

Named port associations are not case sensitive unless a VHDL port name is an extended identifier (1076-1993). If the VHDL port name is an extended identifier, the association is case-sensitive, and the leading and trailing backslashes of the VHDL identifier are removed before comparison.

Generic Associations

Generic associations are provided via the module instance parameter value list. List the values in the same order that the generics appear in the entity. Parameter assignment to generics is not case sensitive.

The **defparam** statement is not allowed for setting generic values.

SDF Annotation

A mixed VHDL/Verilog design can also be annotated with SDF. See [SDF for Mixed VHDL and Verilog Designs](#) for more information.

Sharing User-Defined Types

Using a Common VHDL Package

With the “import” construct of SystemVerilog, you can implement user-defined types (records, enums, alias, subtypes, types, and multi-dimensional arrays) and constants from VHDL in a SystemVerilog design. (Anything other than these types is not supported.) For example:

```
import vh_pack::vh_type
```

In order to import a VHDL package into SystemVerilog, you must compile it using the **-mixedsvvh** argument with the **vcom** command (refer to [Usage Notes](#), below).

Note

The following types must be defined in a common package if you want to use them at the SystemVerilog-VHDL boundary:

- Records
- Enumerations
- One-dimensional array of bit, std_logic, std_ulogic, integer, natural, positive, real & time
- Multi-dimensional arrays and array of arrays of all supported types
- Subtypes of all supported types
- Alias of records, enums and arrays only
- Types (static ranges only)

Also, be sure to use vcom -mixedsvvh when compiling the common package.

ModelSim supports VHDL constants of all types currently supported at the VHDL-SV mixed language boundary as shown in [Table 10-6](#).

Deferred constants are not supported. Only static expressions are supported as constant values.

Table 10-25 shows the mapping of literals from VHDL to SystemVerilog.

Table 10-25. Mapping Literals from VHDL to SystemVerilog

VHDL	SystemVerilog
'0' (Forcing 0)	'0'
'L' (Weak 0)	'0'
'1' (Forcing 1)	'1'
'H' (Weak 1)	'1'
'U' (Uninitialized)	'X'
'X' (Forcing Unknown)	'X'
'W' (Weak Unknown)	'X'
'-' (Don't care)	'X'
'Z' (High Impedance)	'Z'

Table 10-26 lists all supported types inside VHDL Records.

Table 10-26. Supported Types Inside VHDL Records

VHDL Type	SystemVerilog Type
bit, boolean	bit
std_logic	logic
std_ulogic	logic
bit_vector	bit vector
std_logic_vector, std_ulogic_vector, signed, unsigned	logic vector
integer, natural, positive	int
real	real
record	structure
multi-D arrays, array of arrays	multi-d arrays

Usage Notes

When using a common VHDL package at a SystemVerilog-VHDL boundary, compile the VHDL package with the **-mixedsvvh** argument with the **vcom** command, as follows:

```
vcom -mixedsvvh [[b | l | r] | i] <vhdl_package>
```

where

- b — treats all scalars and vectors in the package as SystemVerilog bit type
- l — treats all scalars and vectors in the package as SystemVerilog logic type
- r — treats all scalars and vectors in the package as SystemVerilog reg type
- i — ignores the range specified with VHDL integer types

When you compile a VHDL package with **-mixedsvvh**, the package can be included in a SystemVerilog design as if it were defined in SystemVerilog itself.

Note

If you do not specify b, l, or r with **-mixedsvvh**, then the default treatment of data types is applied:

- VHDL `bit_vector` is treated as SystemVerilog bit vector and
 - VHDL `std_logic_vector`, `std_ulogic_vector`, and `vl_logic_vector` are treated as SystemVerilog logic vectors
-

Example

Consider the following VHDL package that you want to use at a SystemVerilog-VHDL boundary:

```
--/*-----pack.vhd-----*/
package pack is
  type st_pack is record
    a: bit_vector (3 downto 0);
    b: bit;
    c: integer;
  end record;
  constant c : st_pack := (a=>"0110", b=>'0', c=>4);
end package;
```

You must compile this package with the **-mixedsvvh** argument for **vcom**:

vcom -mixedsvvh pack.vhd

This package can now be imported in the SystemVerilog design, as if it were a SystemVerilog package.

```
--/*-----VHDL_entity-----*/
use work.pack.all;
entity top is
end entity;
architecture arch of top is
  component bot
    port(in1 : in st_pack;
         in2 : bit_vector(1 to c.c);
         out1 : out st_pack);
  end component;
```

```
begin
end arch;

/*-----SV_file-----*/
import pack::*; // including the VHDL package in SV
module bot(input st_pack in1, input bit [1:c.c] in2, output st_pack out1);
endmodule
```

Using a Common SystemVerilog Package

With the “use” construct of VHDL, you can implement user-defined types (structures, enums, and multi-dimensional arrays) from SystemVerilog in a VHDL design. (Anything other than these types is not supported.) For example:

```
use work.sv_pack.sv_type
```

In order to include a SystemVerilog package in VHDL, you must compile it using the **-mixedsvvh** argument of the **vlog** command (refer to [Usage Notes](#), below).

Note



The following types must be defined in a common package if you want to use them at the SystemVerilog-VHDL boundary:

- Structures
- Enumerations with base type as 32-bit 2-state integer
- Multi-dimensional arrays of all supported types

Also, be sure to use **vcom -mixedsvvh** when compiling the common package.

[Table 10-27](#) lists all supported types inside SystemVerilog structures.

Table 10-27. Supported Types Inside SystemVerilog Structure

SystemVerilog Type	VHDL Type	Comments
bit	bit	bit types
logic, reg	std_logic	multi-valued types
enum	enum	SV enums of only 2-state int base type supported
struct	record	unpacked structure
packed struct	record	packed structure
real	real	2-state data type, 64-bit real number
shortreal	real	2-state data type, 32-bit real number
multi-D arrays	multi-D arrays	multi-dimensional arrays of supported types
byte, int, shortint, longint	integer	integer types

Usage Notes

When using a common SystemVerilog package at a SV-VHDL boundary, you should compile the SystemVerilog package with the **-mixedsvvh** argument of the **vlog** command, as follows:

```
vlog -mixedsvvh [b | s | v] <sv_package>
```

where

b treats all scalars/vectors in the package as VHDL bit/bit_vector

s treats all scalars/vectors in the package as VHDL std_logic/std_logic_vector

v treats all scalars/vectors in the package as VHDL vl_logic/vl_logic_vector

When you compile a SystemVerilog package with **-mixedsvvh**, the package can be included in a VHDL design as if it were defined in VHDL itself.

Note



If you do not specify **b**, **s**, or **v** with **-mixedsvvh**, the default treatment of data types is applied.

Example

The following SystemVerilog package contains a type named `st_pack`, which you want to use at the SV-VHDL mixed-language boundary.

```
/*-----pack.sv-----*/  
package pack;  
  typedef struct {  
    bit [3:0] a;  
    bit b;  
  } st_pack;  
endpackage
```

To use this package (and type) at a SystemVerilog-VHDL boundary, you must compile it using **vlog -mixedsvvh**:

```
vlog -mixedsvvh pack.sv
```

You can now include this package (`st_pack`) in the VHDL design, as if it were a VHDL package:

```
--/*-----VHDL_file-----*/  
use work.pack.all; -- including the SV package in VHDL  
  
entity top is  
end entity;  
  
architecture arch of top is  
  component bot  
  port(  
    in1 : in st_pack; -- using type from the SV package.  
  )  
end architecture
```

```
        out1 : out st_pack);  
    end component;  
  
    signal sin1, sout1 : st_pack;  
begin  
    ...  
end arch;  
  
/*-----SV Module-----*/  
import pack::*;  
  
module bot(input st_pack in1, output st_pack out1);  
    ...  
endmodule
```

SystemC Instantiating Verilog or SystemVerilog

To instantiate Verilog or SystemVerilog modules into a SystemC design, you must first create a [SystemC Foreign Module \(Verilog\) Declaration](#) for each Verilog/SystemVerilog module. Once you have created the foreign module declaration, you can instantiate the foreign module just like any other SystemC module.

Verilog Instantiation Criteria Within SystemC

A Verilog/SystemVerilog design unit may be instantiated within SystemC if it meets the following criteria:

- The design unit is a module (UDPs and Verilog primitives are not allowed).
- The ports are named ports (Verilog allows unnamed ports).
- The Verilog/SystemVerilog module name must be a valid C++ identifier.
- The ports are not connected to bidirectional pass switches (it is not possible to handle pass switches in SystemC).

A Verilog/SystemVerilog module that is compiled into a library can be instantiated in a SystemC design as though the module were a SystemC module by passing the Verilog/SystemVerilog module name to the foreign module constructor. For an illustration of this, see [Example 10-2](#).

SystemC and Verilog Identifiers

The SystemC identifiers for the module name and port names are the same as the Verilog identifiers for the module name and port names. Verilog identifiers must be valid C++ identifiers. SystemC and Verilog are both case-sensitive. ModelSim does nothing to the SystemC identifiers when it generates the module.

Verilog Configuration Support

You can use a Verilog configuration to configure a Verilog module instantiated in SystemC. The Verilog configuration must be elaborated (with `vsim` or `vopt`) as a top-level design unit, or be part of another top-level VHDL or Verilog configuration.

SystemC Foreign Module (Verilog) Declaration

In cases where you want to run a mixed simulation with SystemC and Verilog/SystemVerilog, you must generate and declare a foreign module that stands in for each Verilog module instantiated under SystemC. You can create foreign modules in one of two ways:

- Run **scgenmod**, a utility that automatically generates your foreign module declaration (much like **vgencomp** generates a component declaration).
- Modify your SystemC source code manually.

After you have analyzed the design, you can generate a foreign module declaration by using [scgenmod](#) as follows:

```
scgenmod mod1
```

where *mod1* can be any name of a Verilog module. A foreign module declaration for the specified module is written to stdout.

Guidelines for Manual Creation of Foreign Module Declaration

Apply the following guidelines to the creation of foreign modules. A foreign module:

- Contains ports corresponding to Verilog ports. These ports must be explicitly named in the constructor initializer list of the foreign module.
- Must not contain any internal design elements such as child instances, primitive channels, or processes.
- Must pass a secondary constructor argument denoting the module's HDL name to the `sc_foreign_module` base class constructor. For Verilog, the HDL name is simply the Verilog module name corresponding to the foreign module, or `[<lib>].<module>`.
- Allows inclusion of parameterized modules. Refer to [Parameter Support for SystemC Instantiating Verilog](#) for details.

Example 10-2. SystemC Instantiating Verilog - 1

A sample Verilog module to be instantiated in a SystemC design is:

```
module vcounter (clock, topcount, count);  
    input clock;  
    input topcount;  
    output count;
```

```
    reg count;  
    ...  
endmodule
```

The SystemC foreign module declaration for the above Verilog module is:

```
class counter : public sc_foreign_module {  
    public:  
        sc_in<bool> clock;  
        sc_in<sc_logic> topcount;  
        sc_out<sc_logic> count;  
    counter(sc_module_name nm)  
        : sc_foreign_module(nm, "lib.vcounter"),  
        clock("clock"),  
        topcount("topcount"),  
        count("count")  
        {}  
};
```

The Verilog module is then instantiated in the SystemC source as follows:

```
counter dut("dut");
```

where the constructor argument (*dut*) is the instance name of the Verilog module.

Example 10-3. SystemC Instantiating Verilog - 2

Another variation of the SystemC foreign module declaration for the same Verilog module might be:

```
class counter : public sc_foreign_module {  
    public:  
        ...  
    counter(sc_module_name nm, char* hdl_name)  
        : sc_foreign_module(nm, hdl_name),  
        clock("clock"),  
        ...  
    {}  
};
```

The instantiation of this module would be:

```
counter dut("dut", "lib.counter");
```

Parameter Support for SystemC Instantiating Verilog

Since the SystemC language has no concept of parameters, parameterized values must be passed from a SystemC parent to a Verilog child through the SystemC foreign module (*sc_foreign_module*). See [SystemC Foreign Module \(Verilog\) Declaration](#) for information regarding the creation of *sc_foreign_module*.

Passing Parameters to `sc_foreign_module` (Verilog)

To instantiate a Verilog module containing parameterized values into the SystemC design, you can use one of two methods, depending on whether the parameter is an integer. If the parameter is an integer, you have two choices: passing as a template argument to the foreign module or as a constructor argument to the foreign module. Non-integer parameters must be passed to the foreign module using constructor arguments.

Passing Integer and Non-Integer Parameters as Constructor Arguments

Both integer and non-integer parameters can be passed by specifying two parameters to the `sc_foreign_module` constructor: the number of parameters (`int num_generics`), and the parameter list (`const char* generic_list`). The `generic_list` is listed as an array of `const char*`.

If you create your foreign module manually (see [Guidelines for Manual Creation of Foreign Module Declaration](#)), you must also pass the parameter information to the `sc_foreign_module` constructor. If you use `scgenmod` to create the foreign module declaration, the parameter information is detected in the HDL child and is incorporated automatically.

Example 10-4. Sample Foreign Module Declaration, with Constructor Arguments for Parameters

Following [Example 10-2](#), the following parameter information would be passed to the SystemC foreign module declaration:

```
class counter : public sc_foreign_module {
public:
    sc_in<bool> clk;
    ...
counter(sc_module_name nm, char* hdl_name
        int num_generics, const char** generic_list)
    : sc_foreign_module (nm),
    {elaborate_foreign_module(hdl_name, num_generics, generic_list);}
};
```

Example 10-5. Passing Parameters as Constructor Arguments - 1

Verilog module:

```
module counter (clk, count)

    parameter integer_param = 4;
    parameter real_param = 2.9;
    parameter str_param = "ERROR";

    output [7:0] count;
    input clk;

    ...
```

```
endmodule
```

Foreign module (created by the command: **scgenmod counter**):

```
class counter : public sc_foreign_module
{
public:
    sc_in<sc_logic> clk;
    sc_out<sc_lv<8> > count;

    counter(sc_module_name nm, const char* hdl_name
            int num_generics, const char** generic_list)
        : sc_foreign_module(nm),
          clk("clk"),
          count("count")
    {
        elaborate_foreign_module(hdl_name, num_generics, generic_list);
    }
    ~counter()
    {}
};
```

Instantiation of the foreign module in SystemC:

```
SC_MODULE(top) {

    counter* counter_inst_1; // Instantiate counter with counter_size = 20

    SC_CTOR(top)
    {
        const char* generic_list[3];
        generic_list[0] = strdup("integer_param=16");
        generic_list[1] = strdup("real_param=2.6");
        generic_list[2] = strdup("str_param=\"Hello\"");

        //Pass all parameter overrides using foreign module constructor args
        counter_inst_1 = new counter("c_inst", "work.counter", 3, \
generic_list);

        // Cleanup the memory allocated for the generic list
        for (int i = 0; i < 3; i++;)
            free((char*)generic_list[i]);
    }
};
```

Passing Integer Parameters as Template Arguments

Integer parameters can be passed as template arguments to a foreign module. Doing so enables port sizes of Verilog modules to be configured using the integer template arguments. Use the `-createtemplate` option to `scgenmod` to generate a class template foreign module.

Example 10-6. SystemC Instantiating Verilog, Passing Integer Parameters as Template Arguments

Verilog module:

```
module counter (clk, count)

    parameter counter_size = 4;

    output [counter_size - 1 : 0] count;
    input clk;

    ...

endmodule
```

Foreign module (created by the command: **scgenmod -createtemplate counter**):

```
template <int counter_size = 4>
class counter : public sc_foreign_module
{
public:
    sc_in<sc_logic> clk;
    sc_out<sc_lv<counter_size-1 + 1> > count;

    counter(sc_module_name nm, const char* hdl_name)
        : sc_foreign_module(nm),
          clk("clk"),
          count("count")
    {
        this->add_parameter("counter_size", counter_size);
        elaborate_foreign_module(hdl_name);
    }
    ~counter()
    {}

};
```

Instantiation of the foreign module in SystemC:

```
SC_MODULE(top) {

    counter<20> counter_inst_1;
        // Instantiates counter with counter_size = 20
    counter      counter_inst_2;
        // Instantiates counter with default counter_size = 4

    SC_CTOR(top)
        : counter_inst_1(cinst_1, "work.counter"),
          counter_inst_2(cinst_2, "work.counter")
    {}

};
```

Example 10-7. Passing Integer Parameters as Template Arguments and Non-integer Parameters as Constructor Arguments

Verilog module:

```
module counter (clk, count)

    parameter counter_size = 4;
    parameter real_param = 2.9;
    parameter str_param = "ERROR";

    output [counter_size - 1 : 0] count;
    input clk;

    ...

endmodule
```

Foreign module (created by command: **scgenmod -createtemplate counter**):

```
template <int counter_size = 4>
class counter : public sc_foreign_module
{
public:
    sc_in<sc_logic> clk;
    sc_out<sc_lv<counter_size-1 + 1> > count;

    counter(sc_module_name nm, const char* hdl_name
            int num_generics, const char** generic_list)
        : sc_foreign_module(nm),
          clk("clk"),
          count("count")
    {
        this->add_parameter("counter_size", counter_size);
        elaborate_foreign_module(hdl_name, num_generics, generic_list);
    }
    ~counter()
    {}

};
```

Instantiation of the foreign module in SystemC:

```
SC_MODULE(top) {

    // Instantiate counter with counter_size = 20
    counter<20>* counter_inst_1;

    SC_CTOR(top)
    {
        const char* generic_list[2];
        generic_list[0] = strdup("real_param=2.6");
        generic_list[1] = strdup("str_param=\"Hello\"");

        //
```

```
// The integer parameter override is already passed as template
// argument. Pass the overrides for the non-integer parameters
// using the foreign module constructor arguments.
//
counter_inst_1 = new counter<20>("c_inst", "work.counter", 2, \
generic_list);

// Cleanup the memory allocated for the generic list
for (int i = 0; i < 2; i++;)
    free((char*)generic_list[i]);
}
};
```

Verilog or SystemVerilog Instantiating SystemC

You can reference a SystemC module from Verilog/SystemVerilog as though the design unit is a module of the same name.

SystemC Instantiation Criteria for Verilog

A SystemC module can be instantiated in Verilog/SystemVerilog if it meets the following criteria:

- SystemC module names are case-sensitive. The module name at the SystemC instantiation site must match exactly with the actual SystemC module name.
- SystemC modules are exported using the `SC_MODULE_EXPORT` macro. See [Exporting SystemC Modules for Verilog](#).
- The module ports are as listed in the table shown in [Channel and Port Type Mapping](#).
- Port data type mapping must match exactly. See the table in [Data Type Mapping from SystemC to Verilog or SystemVerilog](#).

Port associations may be named or positional. Use the same port names and port positions that appear in the SystemC module declaration. Named port associations are case sensitive.

Exporting SystemC Modules for Verilog

To be able to instantiate a SystemC module from Verilog/SystemVerilog (or use a SystemC module as a top level module), the module must be exported.

Assume a SystemC module named *transceiver* exists, and that it is declared in header file *transceiver.h*. Then the module is exported by placing the following code in a *.cpp* file:

```
#include "transceiver.h"
SC_MODULE_EXPORT(transceiver);
```

Parameter Support for Verilog Instantiating SystemC

Passing Parameters from Verilog to SystemC

To pass actual parameter values, simply use the native Verilog/SystemVerilog parameter override syntax. Parameters are passed to SystemC via the module instance parameter value list.

In addition to int, real, and string, ModelSim supports parameters with a bit range.

Named parameter association must be used for all Verilog/SystemVerilog modules that instantiate SystemC.

Retrieving Parameter Values

To retrieve parameter override information from Verilog/SystemVerilog, you can use the following functions:

```
int sc_get_param(const char* param_name, int& param_value);
int sc_get_param(const char* param_name, double& param_value);
int sc_get_param(const char* param_name, sc_string& param_value, char
format_char = 'a');
```

The first argument to `sc_get_param` defines the parameter name, the second defines the parameter value. For retrieving string values, ModelSim also provides a third optional argument, `format_char`. It is used to specify the format for displaying the retrieved string. The format can be ASCII ("a" or "A"), binary ("b" or "B"), decimal ("d" or "D"), octal ("o" or "O"), or hexadecimal ("h" or "H"). ASCII is the default. These functions return a 1 if successful, otherwise they return a 0.

Alternatively, you can use the following forms of the above functions in the constructor initializer list:

```
int sc_get_int_param(const char* param_name, int* is_successful);
double sc_get_real_param(const char* param_name, int* is_successful);
sc_string sc_get_string_param(const char* param_name, char format_char =
'a', int* is_successful);
```

Example 10-8. Verilog/SystemVerilog Instantiating SystemC, Parameter Information

Here is a complete example, ring buffer, including all files necessary for simulation.


```

// test_ringbuf.v

`timescale 1ns / 1ps
module test_ringbuf();
    reg clock;
    ...
    parameter int_param = 4;
    parameter real_param = 2.6;
    parameter str_param = "Hello World";
    parameter [7:0] reg_param = 'b001100xz;

    // Instantiate SystemC module
    ringbuf #(.int_param(int_param),
             .real_param(real_param),
             .str_param(str_param),
             .reg_param(reg_param))
            chip(.clock(clock),
               ...
               ... };
endmodule
-----

// ringbuf.h
#ifndef INCLUDED_RINGBUF
#define INCLUDED_RINGBUF

#include <systemc.h>
#include "control.h"
...

SC_MODULE(ringbuf)
{
public:
    // Module ports
    sc_in clock;
    ...
    ...

    SC_CTOR(ringbuf)
        : clock("clock"),
        ...
        ...
    {
        int int_param = 0;
        if (sc_get_param("int_param", &int_param))
            cout << "int_param" << int_param << endl;

        double real_param = 0.0;
        int is_successful = 0;
        real_param = sc_get_real_param("real_param", &is_successful);
        if (is_successful)
            cout << "real_param" << real_param << endl;

        std::string str_param;
        str_param = sc_get_string_param("str_param", 'a', &is_successful);
        if (is_successful)
            cout << "str_param=" << str_param.c_str() << endl;
    }
};

```

```
        str::string reg_param;
        if (sc_get_param("reg_param", 'b'))
            cout << "reg_param=" << reg_param.c_str() << endl;
    }

    ~ringbuf() {}
};

#endif
```

```
-----

// ringbuf.cpp
#include "ringbuf.h"

SC_MODULE_EXPORT(ringbuf);
```

To run the simulation, you would enter the following commands:

```
vlib work
sccom ringbuf.cpp
vlog test_ringbuf.v
sccom -link
vsim test_ringbuf
```

The simulation would return the following:

```
# int_param=4
# real_param=2.6
# str_param=Hello World
# reg_param=001100xz
```

SystemC Instantiating VHDL

To instantiate VHDL design units into a SystemC design, you must first generate a [SystemC Foreign Module \(Verilog\) Declaration](#) for each VHDL design unit you want to instantiate. Once you have generated the foreign module declaration, you can instantiate the foreign module just like any other SystemC module.

VHDL Instantiation Criteria Within SystemC

A VHDL design unit may be instantiated from SystemC if it meets the following criteria:

- The design unit is an entity/architecture pair or a configuration.
- The entity ports are of type bit, bit_vector, real, std_logic, std_logic_vector, std_ulogic, std_ulogic_vector, or their subtypes. The port clause may have any mix of these types. Only locally static subtypes are allowed.

Port associations may be named or positional. Use the same port names and port positions that appear in the entity.

SystemC Foreign Module (VHDL) Declaration

In cases where you want to run a mixed simulation with SystemC and VHDL, you must create and declare a foreign module that stands in for each VHDL design unit instantiated under SystemC. You can create the foreign modules in one of two ways:

- Run **scgenmod**, a utility that automatically generates your foreign module declaration (much like **vgencomp** generates a component declaration).
- Modify your SystemC source code manually.

After you have analyzed the design, you can generate a foreign module declaration by using **scgenmod** as follows:

```
scgenmod mod1
```

where *mod1* is any name of a VHDL entity. A foreign module declaration for the specified entity is written to stdout.

Guidelines for VHDL Complex Types

You can use VHDL complex data types with **scgenmod**. The compatible record/enum is generated, along with the foreign module declaration, subject to the following rules:

- Names of fields of the SystemC structure/enum must be same as those on the VHDL side.
- The data types of fields in the SystemC structure must follow the same type conversion (mapping) rules as normal ports.
- Additional dummy functions (`operator<<`, `sc_trace`, `operator==` functions) must be generated along with the structure definition.

Guidelines for Manual Creation in VHDL

Apply the following guidelines to the creation of foreign modules. A foreign module:

- Contains ports corresponding to VHDL ports. These ports must be explicitly named in the constructor initializer list of the foreign module.
- Must not contain any internal design elements such as child instances, primitive channels, or processes.
- Must pass a secondary constructor argument denoting the module's HDL name to the `sc_foreign_module` base class constructor. For VHDL, the HDL name can be in the format `[<lib>.]<primary>[(<secondary>)]` or `[<lib>.]<conf>`.

- Can contain generics, which are supported for VHDL instantiations in SystemC designs. See [Generic Support for SystemC Instantiating VHDL](#) for more information.

Example 10-9. SystemC Design Instantiating a VHDL Design Unit

A sample VHDL design unit to be instantiated in a SystemC design is:

```
entity counter is
  port (count : buffer bit_vector(8 downto 1);
        clk   : in bit;
        reset : in bit);
end;
architecture only of counter is
  ...
  ...
end only;
```

The SystemC foreign module declaration for the above VHDL module is:

```
class counter : public sc_foreign_module {
public:
  sc_in<bool> clk;
  sc_in<bool> reset;
  sc_out<sc_logic> count;
counter(sc_module_name nm)
  : sc_foreign_module(nm, "work.counter(only)"),
  clk("clk"),
  reset("reset"),
  count("count")
  {}
};
```

The VHDL module is then instantiated in the SystemC source as follows:

```
counter dut("dut");
```

where the constructor argument (*dut*) is the VHDL instance name.

Generic Support for SystemC Instantiating VHDL

Since the SystemC language has no concept of generics, generic values must be passed from a SystemC parent to an HDL child through the SystemC foreign module (`sc_foreign_module`). See [SystemC Foreign Module \(Verilog\) Declaration](#) for information regarding the creation of `sc_foreign_module`.

Passing Generics to `sc_foreign_module` Constructor (VHDL)

To instantiate a VHDL entity containing generics into the SystemC design, you can use one of two methods, depending on whether the generic is an integer. If the generic is an integer, you have two choices: passing as a template argument to the foreign module or as a constructor

argument to the foreign module. Non-integer generics must be passed to the foreign module using constructor arguments.

Passing Integer and Non-Integer Generics as Constructor Arguments

Both integer and non-integer parameters can be passed by specifying two generic parameters to the `sc_foreign_module` constructor: the number of generics (`int num_generics`), and the generic list (`const char* generics_list`). The `generic_list` is listed as an array of `const char*`.

If you create your foreign module manually (see [Guidelines for Manual Creation in VHDL](#)), you must also pass the generic information to the `sc_foreign_module` constructor. If you use **scgenmod** to create the foreign module declaration, the generic information is detected in the HDL child and is incorporated automatically.

Example 10-10. SystemC Instantiating VHDL, Generic Information

Following [Example 10-9](#), the generic information that would be passed to the SystemC foreign module declaration is shown below. The generic parameters passed to the constructor are shown in magenta color:

```
class counter : public sc_foreign_module {
    public:
        sc_in<bool> clk;
        ...
    counter(sc_module_name nm, char* hdl_name
            int num_generics, const char** generic_list)
        : sc_foreign_module(nm),
        {elaborate_foreign_module(hdl_name, num_generics, generic_list);}
};
```

The instantiation is:

```
dut = new counter ("dut", "work.counter", 9, generic_list);
```

Example 10-11. Passing Parameters as Constructor Arguments - 2

VHDL entity:

```
entity counter is
    generic(
        integer_gen : integer := 4,
        real_gen    : real    := 0.0,
        str_gen     : string);
    port(
        clk : in std_logic;
        count : out std_logic_vector(7 downto 0));
end counter;
```

Foreign module (created by the command: **scgenmod counter**):

```
class counter : public sc_foreign_module
```

```
{
public:
    sc_in<sc_logic> clk;
    sc_out<sc_lv<8> > count;

    counter(sc_module_name nm, const char* hdl_name
           int num_generics, const char** generic_list)
        : sc_foreign_module(nm),
          clk("clk"),
          count("count")
        {
            elaborate_foreign_module(hdl_name, num_generics, generic_list);
        }
    ~counter()
    {}

};
```

Instantiation of the foreign module in SystemC:

```
SC_MODULE(top) {

    counter* counter_inst_1; // Instantiate counter with counter_size = 20

    SC_CTOR(top)
    {
        const char* generic_list[3];
        generic_list[0] = strdup("integer_param=16");
        generic_list[1] = strdup("real_param=2.6");
        generic_list[2] = strdup("str_param=\"Hello\"");

        //Pass all parameter overrides using foreign module constructor args
        counter_inst_1 = new counter("c_inst", "work.counter", 3, \
generic_list);

        // Cleanup the memory allocated for the generic list
        for (int i = 0; i < 3; i++;)
            free((char*)generic_list[i]);
    }
};
```

Passing Integer Generics as Template Arguments

Integer generics can be passed as template arguments to a foreign module. Doing so enables port sizes of VHDL modules to be configured using the integer template arguments. Use the `-createtemplate` option to [scgenmod](#) to generate a class template foreign module.

Example 10-12. SystemC Instantiating VHDL, Passing Integer Generics as Template Arguments

VHDL entity:

```
entity counter is
```

```

    generic(counter_size : integer := 4);
    port(
        clk : in std_logic;
        count : out std_logic_vector(counter_size - 1 downto 0));
end counter;

```

Foreign module (created by the command: **scgenmod -createtemplate counter**):

```

template <int counter_size = 4>
class counter : public sc_foreign_module
{
public:
    sc_in<sc_logic> clk;
    sc_out<sc_lv<counter_size-1 + 1> > count;

    counter(sc_module_name nm, const char* hdl_name)
        : sc_foreign_module(nm),
          clk("clk"),
          count("count")
    {
        this->add_parameter("counter_size", counter_size);
        elaborate_foreign_module(hdl_name);
    }
    ~counter()
    {}
}
}

```

Instantiation of the foreign module in SystemC:

```

SC_MODULE(top) {

    counter<20> counter_inst_1;
        // Instantiates counter with counter_size = 20
    counter    counter_inst_2;
        // Instantiates counter with default counter_size = 4

    SC_CTOR(top)
        : counter_inst_1(cinst_1, "work.counter"),
          counter_inst_2(cinst_2, "work.counter")
    {}

};

```

Example 10-13. Passing Integer Generics as Template Arguments and Non-integer Generics as Constructor Arguments

VHDL entity:

```

entity counter is
    generic(counter_size : integer := 4);
    port(
        clk : in std_logic;
        count : out std_logic_vector(counter_size - 1 downto 0));

```

```
end counter;
```

Foreign module (created by the command: **scgenmod -createtemplate counter**):

```
template <int counter_size = 4>
class counter : public sc_foreign_module
{
public:
    sc_in<sc_logic> clk;
    sc_out<sc_lv<counter_size-1 + 1> > count;

    counter(sc_module_name nm, const char* hdl_name
            int num_generics, const char** generic_list)
        : sc_foreign_module(nm),
          clk("clk"),
          count("count")
    {
        this->add_parameter("counter_size", counter_size);
        elaborate_foreign_module(hdl_name, num_generics, generic_list);
    }
    ~counter()
    {}
};
```

Instantiation of the foreign module in SystemC:

```
SC_MODULE(top) {

    // Instantiate counter with counter_size = 20
    counter<20>* counter_inst_1;

    SC_CTOR(top)
    {
        const char* generic_list[2];
        generic_list[0] = strdup("real_param=2.6");
        generic_list[1] = strdup("str_param=\"Hello\"");

        //
        // The integer parameter override is already passed as template
        // argument. Pass the overrides for the non-integer parameters
        // using the foreign module constructor arguments.
        //
        counter_inst_1 = new counter<20>("c_inst", "work.counter", 2, \
generic_list);

        // Cleanup the memory allocated for the generic list
        for (int i = 0; i < 2; i++;)
            free((char*)generic_list[i]);
    }
};
```


VHDL Instantiating SystemC

To instantiate SystemC in a VHDL design, you must create a component declaration for the SystemC module. Once you have generated the component declaration, you can instantiate the SystemC component just like any other VHDL component.

SystemC Instantiation Criteria for VHDL

A SystemC design unit may be instantiated within VHDL if it meets the following criteria:

- SystemC module names are case sensitive. The module name at the SystemC instantiation site must match exactly with the actual SystemC module name.
- The SystemC design unit is exported using the `SC_MODULE_EXPORT` macro.
- The module ports are as listed in the table in [Data Type Mapping Between SystemC and VHDL](#)
- Port data type mapping must match exactly. See the table in [Port Type Mapping](#).

Port associations may be named or positional. Use the same port names and port positions that appear in the SystemC module. Named port associations are case sensitive.

Component Declaration for VHDL Instantiating SystemC

A SystemC design unit can be referenced from a VHDL design as though it is a VHDL entity. The interface to the design unit can be extracted from the library in the form of a component declaration by running **vgencomp**. Given a library and a SystemC module name, **vgencomp** writes a component declaration to standard output.

The default component port types are:

- `std_logic`
- `std_logic_vector`

Optionally, you can choose:

- `bit` and `bit_vector`

VHDL and SystemC Identifiers

The VHDL identifiers for the component name and port names are the same as the SystemC identifiers for the module name and port names. Except for the cases noted below, ModelSim does nothing to the SystemC identifier when it generates the entity.

ModelSim converts the SystemC identifiers to VHDL 1076-1993 extended identifiers in three cases:

- The SystemC identifier is not a valid VHDL 1076-1987 identifier.
- SystemC module is compiled with `scom -93`. One exception is a valid, lowercase identifier (such as `scmod`). Valid, lowercase identifiers are not converted even if you compile the design with `scom -93`.
- The SystemC identifier is not unique when case is ignored. For example, if `ScMod` and `scmod` both appear in the same design, ModelSim will convert the former to `\ScMod\`.

vgencomp Component Declaration when VHDL Instantiates SystemC

`vgencomp` generates a component declaration according to these rules:

- Port Clause

A port clause is generated if the module has ports. A corresponding VHDL port is defined for each named SystemC port.

You can set the VHDL port type to `bit` or `std_logic`. If the SystemC port has a range, then the VHDL port type is `bit_vector` or `std_logic_vector`. For example:

SystemC port	VHDL port
<code>sc_in<sc_logic>p1;</code>	<code>p1 : in std_logic;</code>
<code>sc_out<sc_lv<8>>p2;</code>	<code>p2 : out std_logic_vector(7 downto 0);</code>
<code>sc_inout<sc_lv<8>>p3;</code>	<code>p3 : inout std_logic_vector(7 downto 0)</code>

Configuration declarations are allowed to reference SystemC modules in the entity aspects of component configurations. However, the configuration declaration cannot extend into a SystemC instance to configure the instantiations within the SystemC module.

Exporting SystemC Modules for VHDL

To be able to instantiate a SystemC module within VHDL (or use a SystemC module as a top level module), the module must be exported.

Assume a SystemC module named *transceiver* exists, and that it is declared in header file *transceiver.h*. Then the module is exported by placing the following code in a *.cpp* file:

```
#include "transceiver.h"  
SC_MODULE_EXPORT(transceiver);
```

The **sccom -link** command collects the object files created in the work library, and uses them to build a shared library (.so) in the current work library. If you have changed your SystemC source code and recompiled it using **sccom**, then you must run **sccom -link** before invoking **vsim**. Otherwise your changes to the code are not recognized by the simulator.

Generic Support for VHDL Instantiating SystemC

Support for generics is available in a workaround flow for the current release. For workaround flow details, please refer to *systemc_generics.note* located in the `<install_dir>/modeltech/docs/technotes` directory.

SystemC Procedural Interface to SystemVerilog

SystemC designs can communicate with SystemVerilog through a procedural interface, the SystemVerilog Direct Programming Interface (DPI). In contrast to a hierarchical interface, where communication is advanced through signals and ports, DPI communications consists of task and function calls passing data as arguments. This type of interface can be useful in transaction level modeling, in which bus functional models are widely used.

This section describes the use flow for using the SystemVerilog DPI to call SystemVerilog export functions from SystemC, and to call SystemC import functions from SystemVerilog.

The SystemVerilog LRM describes the details of a DPI C import and export interface. This document describes how to extend the same interface to include SystemC and C++ in general. The import and export keywords used in this document are in accordance with SystemVerilog as described in the SV LRM. An export function or task is defined in SystemVerilog, and is called by C or SystemC. An import task or function is defined in SystemC or C, and is called from SystemVerilog.

Definition of Terms

The following terms are used in this chapter.

- C++ import function

A C++ import function is defined as a free floating C++ function, either in the global or some private namespace. A C++ import function must not have any SystemC types as formal arguments. This function must be made available in the SystemC shared library.

- SystemC Import Function

A SystemC import function must be available in the SystemC shared library, and it can be either of the following:

- A free-floating C++ function, either in the global or private namespace, with formal arguments of SystemC types.

- A SystemC module member function, with or without formal arguments of SystemC types.
- Export Function
A SystemVerilog export function, as defined in the SystemVerilog LRM.

SystemC DPI Usage Flow

The usage flow of SystemC DPI depends on the function modes, whether they are import or export. The import and export calls described in the following sections can be mixed with each other in any order.

SystemC Import Functions

In order to make a SystemC import function callable from SystemVerilog, it needs to be registered from the SystemC code before it can be called from SystemVerilog. This can be thought of as exporting the function outside SystemC, thus making it callable from other languages. The registration must be done by passing a pointer to the function using an API. The registration can be done anywhere in the design but it must be done before the call happens in SystemVerilog, otherwise the call fails with undefined behavior.

Global Functions

A global function can be registered using the API below:

```
int sc_dpi_register_cpp_function(const char* function_name, PTFN  
func_ptr);
```

This function takes two arguments:

- the name of the function, which can be different than the actual function name. This name must match the SystemVerilog import declaration. No two function registered using this API can have the same name: it creates an error if they do.
- a function pointer to the registered function. On successful registration, this function will return a 0. A non-zero return status means an error.

Example 10-14. Global Import Function Registration

```
int scGlobalImport(sc_logic a, sc_lv<9>* b);  
sc_dpi_register_cpp_function("scGlobalImport", scGlobalImport);
```

A macro like the one shown below is provided to make the registration even more simple. In this case the ASCII name of the function will be identical to the name of the function in the source code.

```
SC_DPI_REGISTER_CPP_FUNCTION(scGlobalImport);
```

In the SystemVerilog code, the import function needs to be defined with a special marker ("DPI-SC") that tells the SV compiler that this is an import function defined in the SystemC shared library. The syntax for calling the import function remains the same as described in the SystemVerilog LRM.

Example 10-15. SystemVerilog Global Import Declaration

For the SystemC import function shown in [Example 10-14](#), the SystemVerilog import declaration is as follows:

```
import mti_scdpi::*;
import "DPI-SC" context function int scGlobalImport(
    input sc_logic a, output sc_lv[8:0] b);
```

Please refer to [Module Member Functions](#) and [Calling SystemVerilog Export Tasks / Functions from SystemC](#) for more details on the SystemC import and export task or function declaration syntax.

Module Member Functions

Registering Functions

Module member functions can be registered anytime before they are called from the SystemVerilog code. The following macro can be used to register a non-static member function if the registration is done from a module constructor or a module member function. For a static member function, the registration is accomplished using the interface `SC_DPI_REGISTER_CPP_FUNCTION`, as described in [SystemC Import Functions](#).

```
SC_DPI_REGISTER_CPP_MEMBER_FUNCTION(<function_name>, <func_ptr>);
```

Example:

```
SC_MODULE(top) {
    void sc_func() {
    }

    SC_CTOR(top) {
        SC_DPI_REGISTER_CPP_MEMBER_FUNCTION("sc_func", &top::sc_func);
    }
};
```

Note that in the above case, since the registration is done from the module constructor, the module pointer argument might be redundant. However, the module pointer argument will be required if the macro is used outside a constructor.

To register a member function from a function that is not a member of the module, the following registration function must be used:

```
int sc_dpi_register_cpp_member_function(<function_name>, <module_ptr>,
<func_ptr>);
```

This function takes three arguments. The first argument is the name of the function, which can be different than the actual function name. This is the name that must be used in the SystemVerilog import declaration. The second argument is a reference to the module instance where the function is defined. It is illegal to pass a reference to a class other than a class derived from `sc_module` and will lead to undefined behavior. The third and final argument is a function pointer to the member function being registered. On successful registration, this function will return a 0. A non-zero return status means an error. For example, the member function `run()` of the module "top" in the example above can be registered as follows:

```
sc_module* pTop = new top("top");
sc_dpi_register_cpp_member_function("run", pTop, &top::run);
```

Setting Stack Size for Import Tasks

The tool implicitly creates a SystemC thread to execute the C++ functions declared as SystemVerilog import tasks. The default stack size is 64KBytes and may not be big enough for any C++ functions. To change the default stack size, you can use the interface `sc_dpi_set_stack_size`. You must use this interface right after the registration routine, for example:

```
SC_MODULE(top) {
    void sc_task() {
    }

    SC_CTOR(top) {
        SC_DPI_REGISTER_CPP_MEMBER_FUNCTION("sc_task", &top::sc_task);
        sc_dpi_set_stack_size(1000000); // set stack size to be 1Mbyte.
    }
}
```

For the C++ functions declared as SystemVerilog import functions, you do not need to set the stack size.

Declaring and Calling Member Import Functions in SystemVerilog

The declaration for a member import function in SystemVerilog is similar to the following:

```
import "DPI-SC" context function int scMemberImport(
    input sc_logic a, output sc_lv[8:0] b);
```

Registration of static member functions is identical to the registration of global functions using the API `sc_dpi_register_cpp_function()`.

Only one copy of the overloaded member functions is supported as a DPI import, as DPI can only identify the import function by its name. not by the function parameters.

To enable the registration of member functions, the SystemC source file must be compiled with the `-DMTI_BIND_SC_MEMBER_FUNCTION` macro.

Calling Member Import Functions in a Specific SystemC Scope

A member import function can be registered for multiple module instances, as in the case when registration routine `SC_DPI_REGISTER_CPP_MEMBER_FUNCTION()` is called from inside a SystemC module constructor. At runtime, you must specify the proper scope when the member import function call is initiated from SystemVerilog side. You can use the following two routines to manipulate the SystemC scope before making the member import function call:

```
function string scSetScopeByName(input string sc_scope_name);
```

and

```
function string scGetScopeName();
```

scSetScopeByName() expects the full hierarchical name of a valid SystemC scope as the input. The hierarchical name must use the Verilog-style path separator. The previous scope hierarchical name before setting the new scope will be returned.

scGetScopeName() returns the current SystemC scope for next member import function call.

Since both routines are predefined in ModelSim built-in package **mti_scdpi**, you need to import this package into the proper scope where the two routines are used, using the following statement:

```
import mti_scdpi::*;
```

Example 10-16. Usage of `scSetScopeByName` and `scGetScopeName`

```
//test.cpp:
SC_MODULE(scmod)
{
    void cppImportFn();

    SC_CTOR(scmod)
    {
        .....
        SC_DPI_REGISTER_CPP_MEMBER_FUNCTION("cppImportFn",
&scmod::cppImportFn);
        .....
    }
};

//test.sv:
module top();
```

```
import mti_scdpi::*;    // where scSetScopeByName() and scGetScopeName()
are
defined.

string prev_sc_scope;
string curr_sc_scope;

scmod inst1();    //scope name "top.inst1"
scmod inst2();    //scope name "top.inst2"

import "DPI-SC" function void cppImportFn();

// call DPI-SC import function under scope "top.inst1"
prev_sc_scope = scSetScopeByName("top.inst1");
curr_sc_scope = scGetScopeName();
cppImportFn();

// call DPI-SC import function under scope "top.inst2"
prev_sc_scope = scSetScopeByName("top.inst2");
curr_sc_scope = scGetScopeName();
cppImportFn();

endmodule
```

Calling SystemVerilog Export Tasks / Functions from SystemC

Unless an export call is made from an import function, you must set the scope of the export function explicitly to provide the SystemVerilog context information to the simulator. You do this by calling `svSetScope()` before each export function or task call.

An export function to be called with SystemC arguments must have an export declaration, similar to the following:

```
export "DPI-SC" context function Export;
```

The function declaration must use the SystemC type package, similar to the following:

```
import mti_scdpi::*;
function int Export(input sc_logic a, output sc_bit b);
```

The syntax for calling an export function from SystemC is the same as any other C++ function call.

SystemC Data Type Support in SystemVerilog DPI

The SystemVerilog package “scdpi” must be imported if a SystemC data type is used in the arguments of import and export functions.

```
import mti_scdpi::*
```


The SystemC data type names have been treated as special keywords. Avoid using these keywords for other purposes in your SystemVerilog source files.

The table below shows how each of the SystemC type will be represented in SystemVerilog. This table must be followed strictly for passing arguments of SystemC type. The SystemVerilog typedef statements, listed in the middle column of [Table 10-28](#), are automatically imported whenever the mti_scdpi package is imported.

Table 10-28. SystemC Types as Represented in SystemVerilog

SystemC Type	SV Typedef	Import/Export Declaration
sc_logic	typedef logic sc_logic	sc_logic
sc_bit	typedef bit sc_bit	sc_bit
sc_bv<N>	typedef bit sc_bv	sc_bit[N-1:0]
sc_lv<N>	typedef logic sc_lv	sc_lv[N-1:0]
sc_int<N>	typedef bit sc_int	sc_int[N-1:0]
sc_uint<N>	typedef bit sc_uint	sc_uint[N-1:0]
sc_bigint<N>	typedef bit sc_bigint	sc_bigint[N-1:0]
sc_biguint<N>	typedef bit sc_biguint	sc_biguint[N-1:0]
sc_fixed<W,I,Q,O,N>	typedef bit sc_fixed	sc_fixed[I-1:I-W]
sc_ufixed<W,I,Q,O,N>	typedef bit sc_ufixed	sc_ufixed[I-1:I-W]
sc_fixed_fast<W...>	typedef bit sc_fixed_fast	sc_fixed[I-1:I-W]
sc_ufixed_fast<W...>	typedef bit sc_ufixed_fast	sc_fixed[I-1:I-W]
sc_signed	typedef bit sc_signed	sc_signed[N-1:0]
sc_unsigned	typedef bit sc_unsigned	sc_unsigned[N-1:0]
sc_fix	typedef bit sc_fix	sc_fix[I-1:1-W]
sc_ufix	typedef bit sc_ufix	sc_ufix[I-1:1-W]
sc_fix_fast	typedef bit sc_fix_fast	sc_fix_fast[I-1:1-W]
sc_ufix_fast	typedef bit sc_ufix_fast	sc_ufix_fast[I-1:1-W]

According to the table above, a SystemC argument of type **sc_uint<32>** will be declared as **sc_uint[31:0]** in SystemVerilog “DPI-SC” declaration. Similarly, **sc_lv<9>** would be **sc_lv[8:0]**. to enable the fixed point datatypes, the SystemC source file must be compiled with **-DSC_INCLUDE_FX**.

For fixed-point types the left and right indexes of the SV vector can lead to a negative number. For example, **sc_fixed<3,0>** will translate to **sc_fixed[0-1:0-3]** which is **sc_fixed[-1:-3]**. This representation is used for fixed-point numbers in the ModelSim tool, and must be strictly followed.

For the SystemC types whose size is determined during elaboration, such as **sc_signed** and **sc_unsigned**, a parameterized array must be used on the SV side. The array size parameter value, on the SystemVerilog side, must match correctly with the constructor arguments passed to types such as **sc_signed** and **sc_unsigned** at SystemC elaboration time.

Some examples:

An export declaration with arguments of SystemC type:

```
export "DPI-SC" context function Export;  
  
import mti_scdpi::*;  
function int Export(input sc_logic a, input sc_int[8:0] b);
```

An import function with arguments of SystemC type:

```
import mti_scdpi::*;  
import "DPI-SC" context function int scGlobalImport(  
    input sc_logic a, output sc_lv[8:0] b);
```

An export function with arguments of regular C types:

```
export "DPI-SC" context function Export;  
function int Export(input int a, output int b);
```

Using a Structure to Group Variables

Both SystemC and SystemVerilog support using a *structure*, which is a composite data type that consists of a user-defined group of variables. This grouping capability of a structure provides a convenient way to work with a large number of related variables. The structure lets you use multiple instances of these variables without having to repeat them individually for each instance.

The same typedefs supported for SystemC types as arguments to DPI-SC can be members of structures.

Example — SystemVerilog

The following structure declaration defines a group of five simple variables: direction, flags, data, addr, token_number. The name of the structure is defined as packet_sv.

```
typedef struct {  
    sc_bit          direction;  
    sc_bv[7:0]     flags;  
    sc_lv[63:0]    data;  
    bit[63:0]     addr;  
    int            token_number;  
} packet_sv;
```

You can then use this structure (packet_sv) as a data-type for arguments of DPI-SC, just like any other variable. For example:

```
import "DPI-SC" task svImportTask(input packet_sv pack_in,  
    output packet_sv pack_out);
```

Example — SystemC

An equivalent structure containing corresponding members of SystemC types are available on the SystemC side of the design. The following structure declaration defines a group of five simple variables: `direction`, `flags`, `data`, `addr`, `token_number`. The name of the structure is defined as `packet_sc`.

```
typedef struct {
    sc_bit          direction;
    sc_bv<8>        flags;
    sc_lv<64>        data;
    svBitVecVal     addr[SV_PACKED_DATA_NELEMS(64)];
    int             token_number;
} packet_sc;
```

You can then use this structure (`packet_sc`) as a data-type for arguments of DPI-SC, just like any other variable. For example:

```
import "DPI-SC" task svImportTask(input packet_sc pack_in,
    output packet_sc pack_out);
```

SystemC Function Prototype Header File (`sc_dpiheader.h`)

A SystemC function prototype header file is automatically generated for each SystemVerilog compilation. By default, this header file is named `sc_dpiheader.h`. This header file contains the C function prototype statements consistent with the "DPI-SC" import/export function/task declarations. You can include this file in the SystemC source files where the prototypes are needed for SystemC compiles and use this file as a sanity check for the SystemC function arguments and return type declaration in the SystemC source files.

When the SystemVerilog source files with the usage of "DPI-SC" spans over multiple compiles, the `sc_dpiheader.h` generated from an earlier SystemVerilog compilation will potentially be overwritten by the subsequent compiles. To avoid the name conflict, one can use the `"-scdpiheader"` argument to the `vlog` command to name the header file differently for each compilation. For example the following `vlog` command line will generate a header file called `"top_scdpi.h"`:

```
vlog -scdpiheader top_scdpi.h top.sv
```

Support for Multiple SystemVerilog Libraries

By default, only the DPI-SC usage in current work library is processed at the SystemC link time. If additional SystemVerilog libraries are used that import or export SystemC DPI routines, the names of these libraries must be provided to `sccom` at link time using the `"-dpilib"` argument.

An example of linking with multiple SystemVerilog libraries are:

```
sccom -link -dpilib dpilib1 -dpilib dpilib2 -dpilib dpilib3
```

where dpilib1, dpilib2 and dpilib3 are the logical names of SystemVerilog libraries previously compiled.

An example of a complete compile flow for compiling with multiple libraries is as follows:

```
// compile SV source files for dpilib1
vlog -work dpilib1 -scdpiheader sc_dpiheader1.h ./src/dpilib1_src.sv

// compile SV source files for dpilib2
vlog -work dpilib2 -scdpiheader sc_dpiheader2.h ./src/dpilib2_src.sv

// compile SV source files for dpilib3
vlog -work dpilib3 -scdpiheader sc_dpiheader3.h ./src/dpilib3_src.sv

// SystemC source file compilations that may include all of the above
three header files.
sccom scmod.cpp

// compile other Verilog sources file if there are any.
vlog -work work non_scdpi_source.sv

// final sccom link phase
sccom -link -dpilib dpilib1 -dpilib dpilib2 -dpilib dpilib3
```

SystemC DPI Usage Example

```
-----
hello.v:

module top;

hello c_hello();

import "DPI-SC" context function void sc_func();
export "DPI-SC" task verilog_task;

task verilog_task();
    $display("hello from verilog_task.");
endtask

initial
begin

    sc_func();

    #2000 $finish;
end
endmodule
```

hello.cpp:

```
#include "systemc.h"
#include "sc_dpiheader.h"

SC_MODULE(hello)
{
    void call_verilog_task();
    void sc_func();

    SC_CTOR(hello)
    {
        SC_THREAD(call_verilog_task);

        SC_DPI_REGISTER_CPP_MEMBER_FUNCTION("sc_func", &hello::sc_func);
    }

    ~hello() {};
};

void hello::sc_func()
{
    printf("hello from sc_func().\n");
}

void hello::call_verilog_task()
{
    svSetScope(svGetScopeFromName("top"));

    for(int i = 0; i < 3; ++i)
    {
        verilog_task();
    }
}

SC_MODULE_EXPORT(hello);
```

Compilation:

```
vlog -sv hello.v
sccom -DMTI_BIND_SC_MEMBER_FUNCTION hello.cpp
sccom -link
vsim -c -do "run -all; quit -f" top
```


Chapter 11

Advanced Simulation Techniques

Checkpointing and Restoring Simulations

The `checkpoint` and `restore` commands allow you to save and restore the simulation state within the same invocation of `vsim` or between `vsim` sessions.

Table 11-1. Checkpoint and Restore Commands

Action	Definition	Command used
checkpoint	saves the simulation state	checkpoint <filename>
"warm" restore	restores a checkpoint file saved in a current <code>vsim</code> session	restore <filename>
"cold" restore	restores a checkpoint file saved in a previous invocation of <code>vsim</code>	vsim -restore <filename>

Checkpoint File Contents

The following things are saved with `checkpoint` and restored with the `restore` command:

- `modelsim.ini` settings
- simulation kernel state
- `vsim.wlf` file
- signals listed in the List and Wave windows
- file pointer positions for files opened under VHDL
- file pointer positions for files opened by the Verilog `$fopen` system task
- state of foreign architectures
- state of PLI/VPI/DPI code

Checkpoint Exclusions

You *cannot* checkpoint/restore the following:

- state of macros
- changes made with the command-line interface (such as user-defined Tcl commands)
- state of graphical user interface windows
- toggle statistics

If you use the foreign interface, you will need to add additional function calls in order to use **checkpoint/restore**. See the Foreign Language Interface Reference Manual or [Verilog Interfaces to C](#) for more information.

Controlling Checkpoint File Compression

The checkpoint file is normally compressed. To turn off the compression, use the following command:

```
set CheckpointCompressMode 0
```

To turn compression back on, use this command:

```
set CheckpointCompressMode 1
```

You can also control checkpoint compression using the *modelsim.ini* file in the [vsim] section (use the same 0 or 1 switch):

```
[vsim]  
CheckpointCompressMode = <switch>
```

The Difference Between Checkpoint/Restore and Restart

The [restart](#) command resets the simulator to time zero, clears out any logged waveforms, and closes any files opened under VHDL and the Verilog \$fopen system task. You can get the same effect by first doing a checkpoint at time zero and later doing a restore. Using **restart**, however, is likely to be faster and you don't have to save the checkpoint. To set the simulation state to anything other than time zero, you need to use **checkpoint/restore**.

Using Macros with Restart and Checkpoint/Restore

The [restart](#) command resets and restarts the simulation kernel, and zeros out any user-defined commands, but it does not touch the state of the macro interpreter. This lets you do **restart** commands within macros.

The pause mode indicates that a macro has been interrupted. That condition will not be affected by a restart, and if the restart is done with an interrupted macro, the macro will still be interrupted after the restart.

The situation is similar for using **checkpoint/restore** without quitting ModelSim; that is, doing a [checkpoint](#) and later in the same session doing a [restore](#) of the earlier checkpoint. The **restore**

does not touch the state of the macro interpreter so you may also do **checkpoint** and **restore** commands within macros.

Checkpointing Foreign C Code That Works with Heap Memory

If checkpointing foreign C code (FLI/PLI/VPI/DPI) that works with heap memory, use `mti_Malloc()` rather than raw `malloc()` or `new`. Any memory allocated with `mti_Malloc()` is guaranteed to be restored correctly. Any memory allocated with raw `malloc()` will not be restored correctly, and simulator crashes can result.

Checkpointing a Running Simulation

In general you can invoke a checkpoint command only when the simulation is stopped. If you need to checkpoint without stopping the simulation, you need to write a script that utilizes the [when](#) command and variables from your code to trigger a checkpoint. The example below shows how this might be done with a simple Verilog design.

Keep in mind that the variable(s) in your code must be visible at the simulation time that the checkpoint will occur. Some global optimizations performed by ModelSim may limit variable visibility, and you may need to optimize your design using the `+acc` argument to `vopt`.

You would compile and run the example like this:

```
vlog when.v
vsim -c when -do "do when.do"
```

where *when.do* is:

```
onbreak {
    echo "Resume macro at $now"
    resume
}
quietly set continueSim 1
quietly set whenFired 0
quietly set checkpointCntr 0

when { needToSave = 1 } {
    echo "when Stopping to allow checkpoint at $now"
    set whenFired 1
    stop
}

while {$continueSim} {
    run -all
    if { $whenFired } {
        set whenFired 0
        echo "Out of run command. Do checkpoint here"
        checkpoint cpf.n[incr checkpointCntr].cpt
    }
}
```

and *when.v* is:

```
module when;

    reg clk;
    reg [3:0] cnt;
    reg needToSave;

    initial
    begin
        needToSave = 0;
        clk = 0;
        cnt = 0;
        #1000;
        $display("Done at time %t", $time);
        $finish;
    end

    always #10 clk = ~clk;

    always @(posedge clk)
    begin
        cnt = cnt + 1;
        if (cnt == 4'hF)
            begin
                $display("Need to Save : %b", needToSave);
                needToSave = 1;
            end
    end

    // Need to reset the flag, but must wait a timestep
    // so that the when command has a chance to fire

    always @(posedge needToSave)
        #1 needToSave = 0;
endmodule
```

and the transcript output is:

```
# vsim -do {do when.do} -c when
# //
# Loading work.when
# do when.do
# Need to Save : 0
# when Stopping to allow checkpoint at 290 # Simulation stop requested.
# Resume macro at 290
# Out of run command. Do checkpoint here # Need to Save : 0
# when Stopping to allow checkpoint at 610
# Simulation stop requested.
# Resume macro at 610
# Out of run command. Do checkpoint here # Need to Save : 0
# when Stopping to allow checkpoint at 930
# Simulation stop requested.
# Resume macro at 930
# Out of run command. Do checkpoint here
# Done at time          1000
# ** Note: $finish      : when.v(14)
#   Time: 1 us  Iteration: 0  Instance: /when
```

Simulating with an Elaboration File

The ModelSim compiler generates a library format that is compatible across platforms. This means the simulator can load your design on any supported platform without having to recompile first. Though this architecture offers a benefit, it also comes with a possible

detriment: the simulator has to generate platform-specific code every time you load your design. This impacts the speed with which the design is loaded.

You can generate a loadable image (elaboration file) which can be simulated repeatedly. On subsequent simulations, you load the elaboration file rather than loading the design "from scratch." Elaboration files load quickly.

Why an Elaboration File?

In many cases design loading time is not that important. For example, if you're doing "iterative design," where you simulate the design, modify the source, recompile and resimulate, the load time is just a small part of the overall flow. However, if your design is locked down and only the test vectors are modified between runs, loading time may materially impact overall simulation time, particularly for large designs loading SDF files.

Another reason to use elaboration files is for benchmarking purposes. Other simulator vendors use elaboration files, and they distinguish between elaboration and run times.

One caveat with elaboration files is that they must be created and used in the same environment. The same environment means the same hardware platform, the same OS and patch version, and the same version of any PLI/FLI code loaded in the simulation.

Elaboration File Flow

We recommend the following flow to maximize the benefit of simulating elaboration files.

1. If timing for your design is fixed, include all timing data when you create the elaboration file (using the **-sdf<type> instance=<filename>** argument). If your timing is not fixed in a Verilog design, you'll have to use \$sdf_annotate system tasks. Note that use of \$sdf_annotate causes timing to be applied after elaboration.
2. Apply all normal vsim arguments when you create the elaboration file. Some arguments (primarily related to stimulus) may be superseded later during loading of the elaboration file (see [Modifying Stimulus](#) below).
3. Load the elaboration file along with any arguments that modify the stimulus (see below).

Creating an Elaboration File

Elaboration file creation is performed with the same **vsim** settings or switches as a normal simulation *plus* an elaboration specific argument. The simulation settings are stored in the elaboration file and dictate subsequent simulation behavior. Some of these simulation settings can be modified at elaboration file load time, as detailed below.

To create an elaboration file, use the **-elab <filename>** or **-elab_cont <filename>** argument to [vsim](#).

The **-elab_cont** argument is used to create the elaboration file then continue with the simulation after the elaboration file is created. You can use the **-c** switch with **-elab_cont** to continue the simulation in command-line mode.

Note

Elaboration files can be created in command-line mode *only*. You cannot create an elaboration file while running the ModelSim GUI.

Loading an Elaboration File

To load an elaboration file, use the **-load_elab <filename>** argument to [vsim](#). By default the elaboration file will load in command-line mode or interactive mode depending on the argument (**-c** or **-i**) used during elaboration file creation. If no argument was used during creation, the **-load_elab** argument will default to the interactive mode.

The **vsim** arguments listed below can be used with **-load_elab** to affect the simulation.

```
+<plus_args>
-c or -i
-do <do_file>
-vcdread <filename>
-vcdstim <filename>
-filemap_elab <HDLfilename>=<NEWfilename>
-l <log_file>
-trace_foreign <level>
-quiet
-wlf <filename>
```

Modification of an argument that was specified at elaboration file creation, in most cases, causes the previous value to be replaced with the new value. Usage of the **-quiet** argument at elaboration load causes the mode to be toggled from its elaboration creation setting.

All other **vsim** arguments must be specified when you create the elaboration file, and they cannot be used when you load the elaboration file.

Note

The elaboration file must be loaded under the same environment in which it was created. The same environment means the same hardware platform, the same OS and patch version, the same version of any PLI/FLI code loaded in the simulation, and the same release of ModelSim.

Modifying Stimulus

A primary use of elaboration files is repeatedly simulating the same design with different stimulus. The following mechanisms allow you to modify stimulus for each run.

- Use of the change command to modify parameters or generic values. This affects values only; it has no effect on triggers, compiler directives, or generate statements that reference either a generic or parameter.
- Use of the **-filemap_elab** `<HDLfilename>=<NEWfilename>` argument to establish a map between files named in the elaboration file. The `<HDLfilename>` file name, if it appears in the design as a file name (for example, a VHDL FILE object as well as some Verilog sysfuncs that take file names), is substituted with the `<NEWfilename>` file name. This mapping occurs before environment variable expansion and can't be used to redirect stdin/stdout.
- VCD stimulus files can be specified when you load the elaboration file. Both `vcdread` and `vcdstim` are supported. Specifying a different VCD file when you load the elaboration file supersedes a stimulus file you specify when you create the elaboration file.
- In Verilog, the use of **+args** which are readable by the PLI routine `mc_scan_plusargs()`. **+args** values specified when you create the elaboration file are superseded by **+args** values specified when you load the elaboration file.

Using With the PLI or FLI

PLI models do not require special code to function with an elaboration file as long as the model doesn't create simulation objects in its standard `tf` routines. The `sizetf`, `misctf` and `checktf` calls that occur during elaboration are played back at **-load_elab** to ensure the PLI model is in the correct simulation state. Registered user `tf` routines called from the Verilog HDL will not occur until **-load_elab** is complete and the PLI model's state is restored.

By default, FLI models are activated for checkpoint during elaboration file creation and are activated for restore during elaboration file load. (See the "Using checkpoint/restore with the FLI" section of the Foreign Language Interface Reference manual for more information.) FLI models that support checkpoint/restore will function correctly with elaboration files.

FLI models that don't support checkpoint/restore may work if simulated with the **-elab_defer_fli** argument. When used in tandem with **-elab**, **-elab_defer_fli** defers calls to the FLI model's initialization function until elaboration file load time. Deferring FLI initialization skips the FLI checkpoint/restore activity (callbacks, `mti_IsRestore()`, ...) and may allow these models to simulate correctly. However, deferring FLI initialization also causes FLI models in the design to be initialized in order with the entire design loaded. FLI models that are sensitive to this ordering may still not work correctly even if you use **-elab_defer_fli**.

See the **vsim** command for details on **-elab**, **-elab_cont**, **-elab_defer_fli**, **-compress_elab**, **-filemap_elab**, and **-load_elab**.

Upon first simulating the design, use **vsim -elab <filename> <library_name.design_unit>** to create an elaboration file that will be used in subsequent simulations.

In subsequent simulations you simply load the elaboration file (rather than the design) with **vsim -load_elab <filename>**.

To change the stimulus without recoding, recompiling, and reloading the entire design, ModelSim allows you to map the stimulus file (or files) of the original design unit to an alternate file (or files) with the **-filemap_elab** switch. For example, the VHDL code for initiating stimulus might be:

```
FILE vector_file : text IS IN "vectors";
```

where *vectors* is the stimulus file.

If the alternate stimulus file is named, say, *alt_vectors*, then the correct syntax for changing the stimulus without recoding, recompiling, and reloading the entire design is as follows:

```
vsim -load_elab <filename> -filemap_elab vectors=alt_vectors
```

Chapter 12

Recording and Viewing Transactions

This chapter discusses transactions in ModelSim: what they are, how to successfully record them, and how to view them in the GUI.

Transaction Background	487
What is a Transaction?	488
About the Source Code for Transactions	488
Viewing Transactions in the GUI	491
Viewing Transaction Objects in the Structure Window	493
Viewing Transactions in the Wave Window	493
Viewing a Transaction in the List Window	500
Viewing a Transaction in the Objects Window	501
Transaction Recording Flow	502
Transaction Recording Procedures	510
Recording Transactions in Verilog	510
Recording Transactions in SystemC.....	513
Transaction Recording Guidelines	505
Names of Streams and Substreams.....	506
Stream Logging.....	506
Attribute Type.....	507
Anonymous Attributes	508
Multiple Uses of the Same Attribute	508
Transaction UIDs	507
Relationships in Transactions	508
The Life-cycle of a Transaction	508
Retroactive Recording / Start and End Times.....	509
Start and End Times for Phase Transactions	509
Transaction Handles and Memory Leaks	509
CLI Debugging Command Reference	521
Verilog API System Task Reference	521

Transaction Background

What is a Transaction?	488
About the Source Code for Transactions	488
About Transaction Streams.....	489

What is a Transaction?

A *transaction* is a statement of what the design is doing between one time and another during a simulation run. It is as simple as it is powerful.

While the definition of a transaction may be simple, the word “transaction” itself can be confusing because of its association with Transaction Level Modeling (TLM). In TLM, design units pass messages across interfaces and these messages are typically called transactions.

In ModelSim, the term transaction is used in a broader sense:

- *transaction*

An abstract statement, logged in the WLF file, of what the design was doing at a specific time. The designer writes a transaction in the source code, which is then logged into the WLF file during simulation. Often, transactions represent packets of data moving around between design objects. Transactions allow users to debug and monitor the design at any level of abstraction.

As written in the source code, a transaction at a minimum consists of:

- a name
- a start time
- an end time

With that alone, you could record the transitions of a state machine, summarize the activity on a bus, and so forth. Additionally, transactions may have user-defined *attributes*, such as address, data, status, and so on.

About the Source Code for Transactions

Essentially, you record transactions by writing the transactions into your design code:

- Verilog/SystemVerilog transactions — written using a custom API specifically developed for designs being verified with the ModelSim simulator. The term “Verilog” is used throughout this chapter to indicate both forms of the language (Verilog and SystemVerilog) unless otherwise specified.

See [Recording Transactions in Verilog](#) for details on the tasks involved in recording.

- SystemC transactions — written with the SystemC Verification (SCV) library.

See “[Recording Transactions in SystemC](#)” for details on the tasks involved in recording.

See the SystemC Verification Standard Specification, Version 1.0e for SystemC API syntax for recording transactions.

You create/record transactions through the Verilog or SystemC API calls placed in your design source code. As the simulation progresses, individual transactions are recorded into the WLF file and are available for design debug and performance analysis in both interactive debug and post-simulation debug.

See [CLI Debugging Command Reference](#) for the ModelSim Verilog API recording syntax.

About Transaction Streams

Transactions are recorded on *streams*, much as values are recorded on wires and signals. Streams are debuggable objects: they appear in or may be added to GUI windows such as the Objects pane or Wave windows.

When more than one transaction is recorded on a stream at one time the transactions are said to be “overlapping”. The simulator creates *substreams* as needed so that overlapping transactions on the stream remain distinct (see [Figure 12-1](#)).

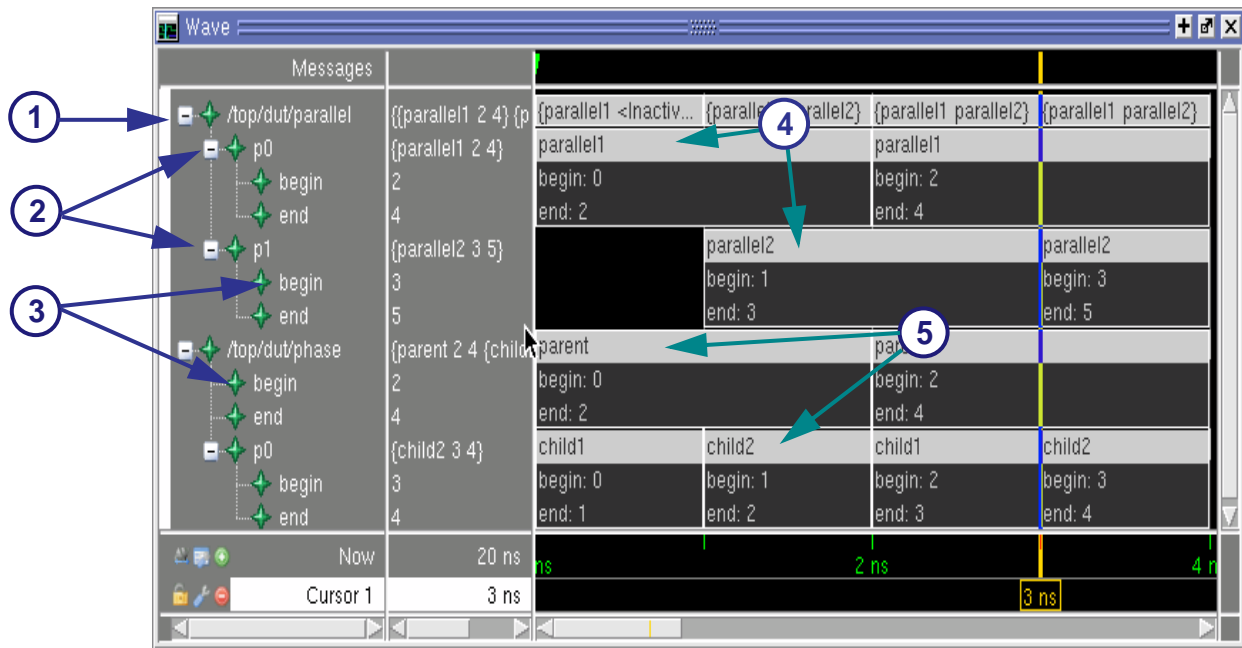
Overlapping transactions appear in the Wave window as they are recorded, either as:

- *parallel* transactions — transactions which overlap, but where no intrinsic relationship exists between the two transactions.
- *phase* transactions — where the overlapping transaction is actually a “child” of the initial transaction.

You specify whether an overlapping transaction is phase or parallel during the recording.

The simulator automatically logs the transactions, making them available for immediate viewing in the GUI. Transactions are best viewed in the Wave window. See [Viewing Transactions in the GUI](#) for procedural details.

Figure 12-1. Transaction Anatomy in Wave Window



Icon	Element
①	Transaction Stream
②	Substream
③	Attributes
④	Parallel transactions
⑤	Phase transactions

Parallel Transactions

The simulator creates a separate substream for each transaction so that they are distinct from each other in the view. Expanding the substream reveals the attributes on those transactions.

i Concept: Substream Creation — Generally, you have no direct control over the creation of substreams; they are created for you during simulation as needed. The rule for substream creation is: A transaction is placed on the first substream that has no active transaction and does not have any transaction in the future of the one being logged.

Phase / Child Transactions

Phase transactions are a special type of overlapping transaction in ModelSim. See [Recording Phase Transactions](#) for information on how to specify the recording of a transaction as a phase of a parent transaction.

The simulator has an alternative way of drawing phase transactions, as they are considered to be “phases” of a parent transaction. For example, consider that a busRead transaction may have several steps or phases. Each of these could be represented as a smaller, overlapping transaction and would appear on a second substream. However, you can indicate that these are phase, and by doing so, you instruct the tool to draw them specially, as shown in [Figure 12-1](#).

Viewing Transactions in the GUI

Once recorded, transactions can be viewed in the following GUI windows: Wave, List, and the Object. Transactions are best viewed in the Wave window, where their appearance is unlike any other objects in the GUI.

Prerequisites

- Transactions must be recorded (written in source code) prior to simulation in order to appear in the GUI.

See “[Recording Transactions in Verilog](#)” and “[Recording Transactions in SystemC](#)” for details.

Transactions Viewing Commonalities

The information contained in this section relates to viewing transactions in all windows and panes where transactions appear. It explains the general viewing behavior that is consistent across the GUI.

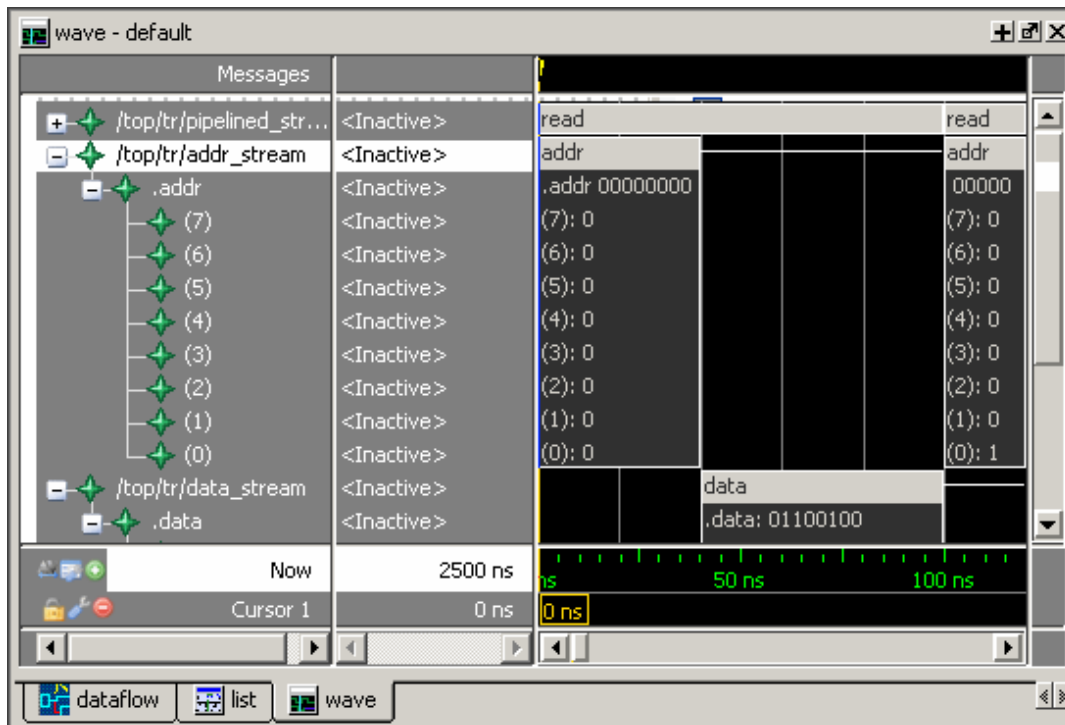
A stream has children and is expandable if:

- there have been transactions defined on it with attributes
- transactions have overlapped on the stream

Unexpanded, such a stream's value includes the names of all current active transactions, for example, "{busRetry busWrite}". The values of any attributes are available only if the stream is expanded to reveal them.

[Figure 12-2](#) shows several streams, one of which has eight sub-streams.

Figure 12-2. Transaction Stream in Wave Window



If no transactions were defined on a particular stream, or none of the transactions have attributes, then the stream is a simple signal with the name of the current transaction as its value.

The <Inactive> value appears under the following conditions:

- When no transaction is active on a stream, the value is "<Inactive>".
- Where an element (attribute and/or sub-stream) exists, but is not used by a transaction, it has the value "<Inactive>".

Attributes and sub-streams are additive in ModelSim. These are added to the stream's basic definition and are kept as part of the stream definition from that point onward. Even if an attribute is not used on some transaction, it remains part of the stream.

SCV allows designs to set explicit, undefined values on begin attributes and end attributes. The simulator shows these as "<Undefined>".

Transaction streams are dynamic objects under the control of the design. During simulation, the design may define new streams, define new transaction kinds, overlap transactions or create phase transactions, add special attributes of all kinds, and so forth. In response, the simulator actively re-creates the objects in the GUI to reflect the most recent changes.

Dynamic changes are always additive: once an element is added to a stream, it remains there in all views. In post-simulation debug, all elements are shown as if they existed from the beginning of the simulation run. For both interactive and post-simulation debug, elements that

did not exist at a particular simulation time are shown as if the "nolog" command had been used; their values are "No_Data".

Viewing Transaction Objects in the Structure Window

Structure windows allow you to navigate through the regions in the design, much as you would use the env command in batch mode. Transactions objects look much like signals or nets in the design hierarchy. When you navigate to a region containing a stream, the stream is visible in the Objects window.

Viewing Transactions in the Wave Window

Prerequisite

- For transactions to be viewable in the Wave window, logging must be enabled at the simulation time when the transaction begins. Logging is automatically enabled for transactions written in SCV and Verilog. Logging can be disabled using the `nolog` command.

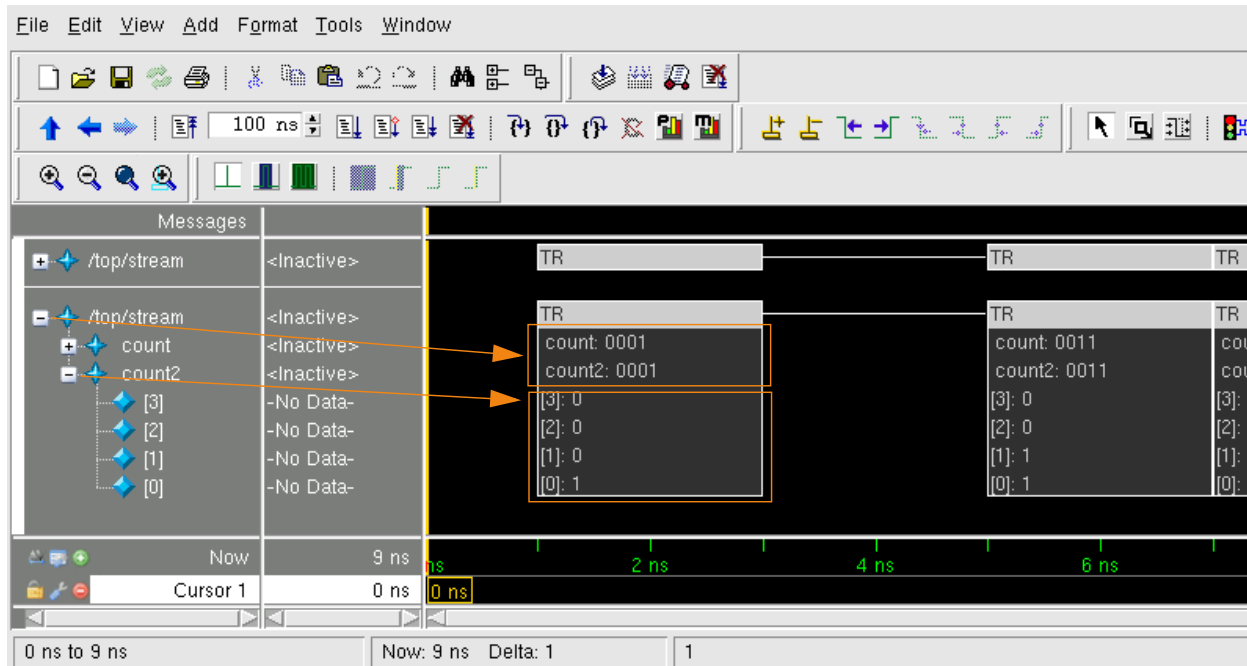
Procedure

1. Run simulation on a design containing transactions.
vsim top; run -all
2. Add transactions to Wave window:
 - Drag and Drop from Object or Structure (sim) windows
 - From the command line:
add wave -expand top/*
3. Select the plus icon next to streams having objects beneath them to reveal substreams and/or any attributes.

The icon for a transaction stream is a four-point star in the color of the source language for the region in which the stream is found (SystemC - green, Verilog - blue).

In the waveform pane, transactions appear as boxes surrounding all the visible values for that transaction. Here's an example of a transaction on a stream with only one sub-stream where the stream is shown in its expanded and collapsed forms:

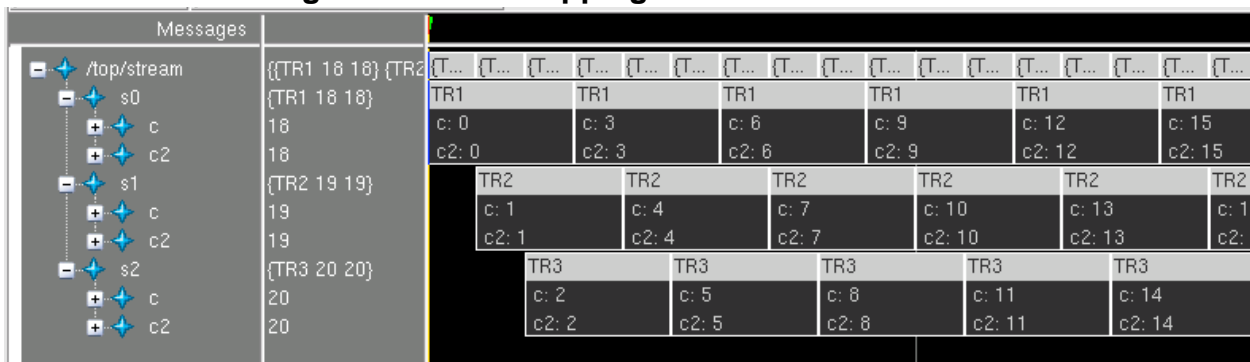
Figure 12-3. Viewing Transactions and Attributes



Each box represents an “instance” of a transaction on the stream. The horizontal line drawn between the first and second transaction indicates a period of either no activity OR a period in which logging has been disabled; there is no way to know which is the case.

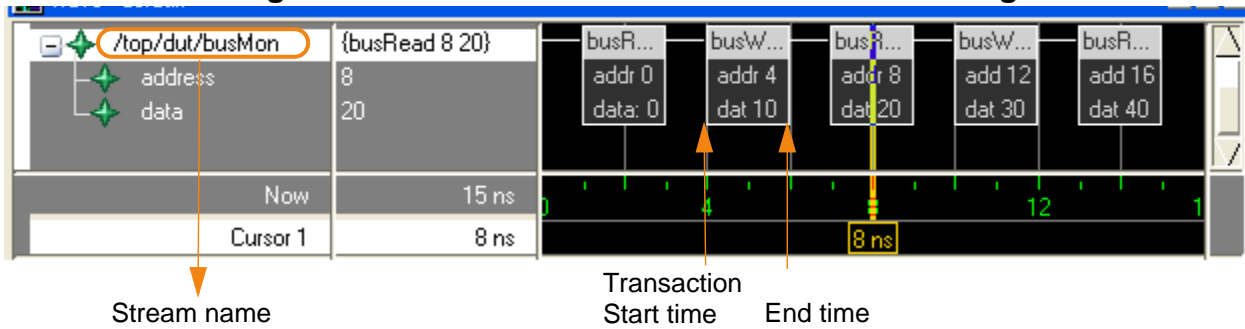
When there are overlapping, parallel transactions, the stream shows overlapping values. Expanding the stream reveals the sub-streams, separating the transactions neatly, as in [Figure 12-4](#). Each sub-stream may expand to reveal attributes or phase sub-streams.

Figure 12-4. Overlapping Parallel Transactions



[Figure 12-5](#) shows a simple transaction stream from a bus monitor. The transactions include simple, user-defined address and data attributes:

Figure 12-5. Transaction in Wave Window - Viewing



The top row of a transaction is the name of transaction. When the transaction stream is expanded, as in Figure 12-5, additional rows are revealed that represent attributes of the transaction.

A transaction is just the individual transaction occurring on a stream. In Figure 12-5, “busW” shown between the two arrows is a single transaction. In the same figure, the transaction stream is the whole row of transactions, tagged with “/top/dut/busMon” as its name.



Tip: For SystemC begin/end attributes — If a begin end attribute was declared by the generator, but the value was not defined, the value appears as “Undefined” in the GUI.

Appearance of Retroactive Transactions in Wave Window

Retroactive recording refers to the recording of a transaction whose start and/or end time occurs before the current simulation time. When these transactions are drawn in the Wave window, more substreams may be shown than you might expect. This is due to the fact that even though there might be a “space” between the two transactions long enough for your retroactive transaction, the tool creates an additional substream to draw that transaction.

Logged Transactions and Retroactive Recording

A transaction is logged in the `.wlf` file if logging is enabled at the simulation time when the design calls `::begin_transaction()` or `$begin_transaction`. The effective start time of the transaction (in other words, the time passed by the design as a parameter to beginning the transaction) is irrelevant. For example, a stream could have logging disabled between T1 and T2 and still record a transaction in that period using retroactive logging after time T2. A transaction is always entirely logged or not logged.

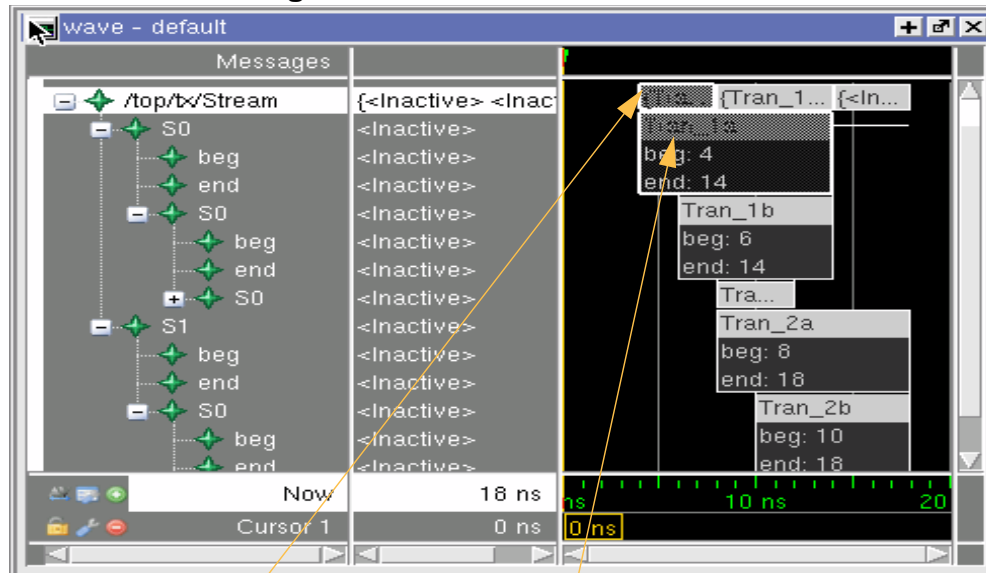
Selecting Transactions or Streams

You can select transactions or streams with a left click of the mouse, or if the transactions are recorded with relations, you can right click for a pop-up menu for various choices.

Selecting transactions or streams with mouse:

- Select an individual transaction: left click on the transaction. When you select a transaction, any substreams of that transaction are selected also. See [Figure 12-6](#).
Left click while holding down the SHIFT key to select multiple transactions/streams.
- Select a transaction stream: left click on the transaction name in the object name area of the Wave window. See [Figure 12-7](#).

Figure 12-6. Selected Transaction



Select transaction...

...the substream transaction
is selected also

Selecting and Viewing Related Transactions

1. Select a single transaction.
2. Right mouse click to bring up pop-up menu with the following choices:
 - Select Related — to select a transaction to which the current transaction is pointing.
 - Select Relating — to select a transaction that is pointing to the current transaction.
 - Select Chain — to select all related and relating transactions for the current transaction. Use this to select an entire causal chain.
 - Select Meta — to select all related and relating transactions for the current transaction. Use this to select any existing branches for the relationship.

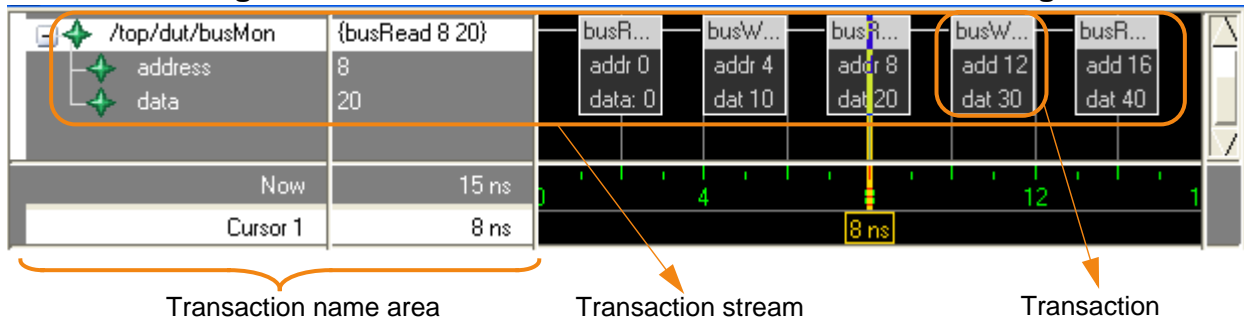
Selecting any of these items brings up a submenu which lists all relationship names that apply.

These pop-up menu items are grayed out if more than one transaction is selected.

Customizing Transaction Appearance

You can customize the appearance of a transaction itself, or for the entire transaction stream (see [Figure 12-7](#)). Further, you can apply these custom settings for either the current Wave window, or all Wave windows.

Figure 12-7. Transaction in Wave Window - Customizing

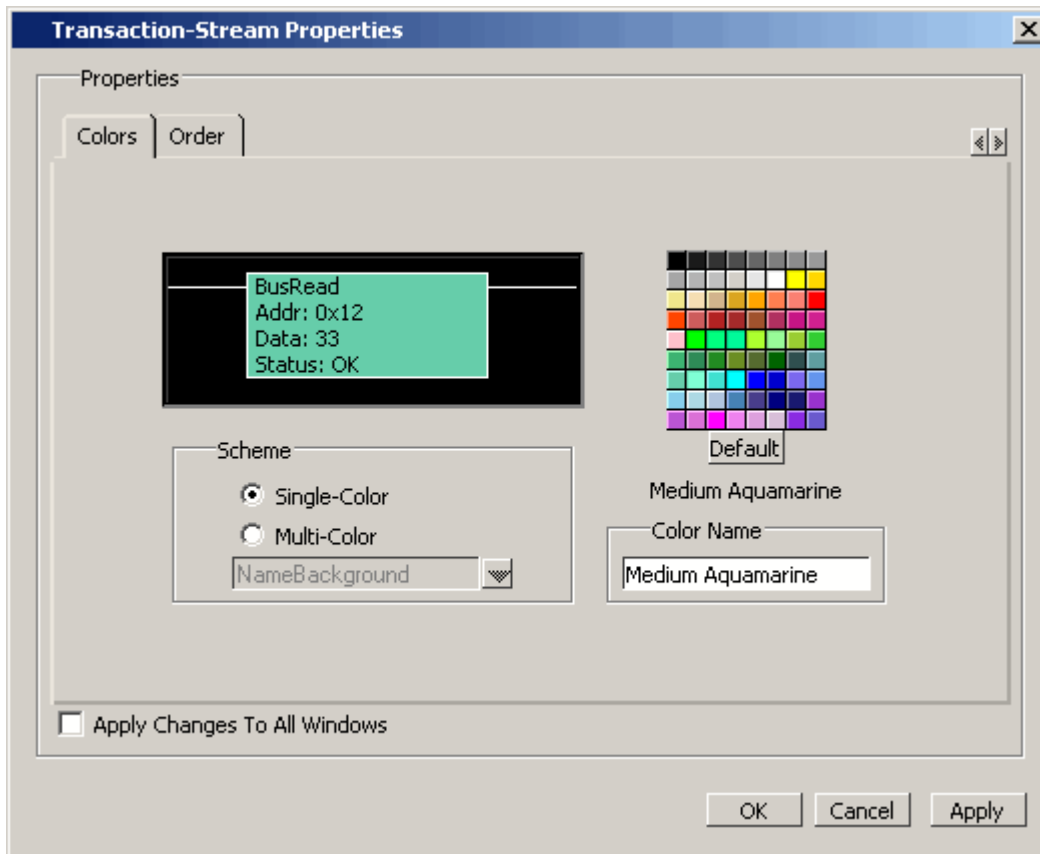


Customizing Color

You can change the color of one or more transactions or streams using the GUI or the `tr color` command.

1. Right-click a transaction or stream name to open a popup menu.
2. Select Transaction Properties to open the Transaction-Stream Properties dialog box ([Figure 12-8](#)).

Figure 12-8. Transaction Stream Properties



3. Select the Colors tab.
4. In the Scheme area of the dialog box, select:
 - Single-Color to apply the color change to all elements of the stream or transaction.
 - Multi-Color to apply different colors to specific elements of the stream or transaction. When you select one of the following elements and select a color, the color is applied to that element:
 - InactiveLine - line between transactions
 - BorderLine - border around the transaction
 - NameBackground - background behind the transaction name text
 - NameText - text for the transaction name
 - AttributeBackground - background behind the attribute text
 - AttributeText - text for attribute
5. Choose a color from the palette or enter a color in the field (for example, light blue) and
6. Select **Apply** to leave dialog box open, or **OK** to apply and close it.

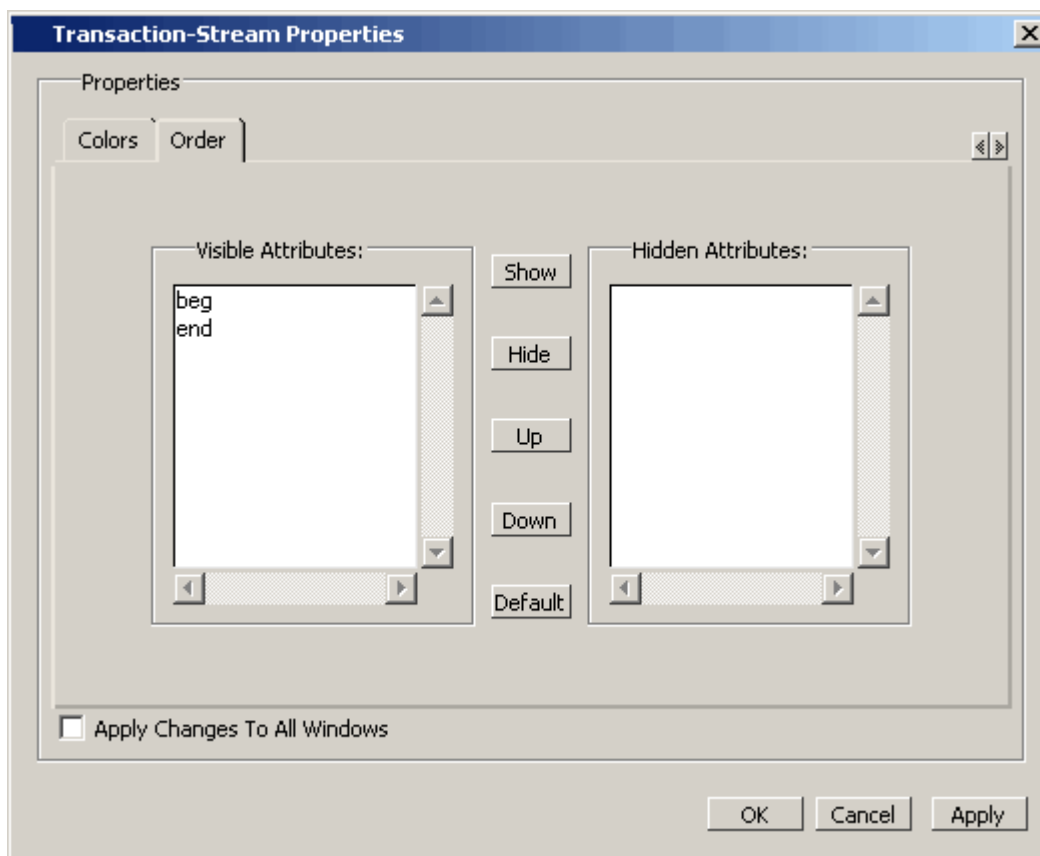
The element, transaction or entire stream of transactions changes to the chosen color.

Customizing Appearance of Attributes

You can change the order of the attributes and hide/show attributes in the stream using the GUI or the `tr order` command.

1. Right-click a transaction or stream name to open a popup menu.
2. Select Transaction Properties to open the Transaction-Stream Properties dialog box .
3. Select the Order tab (Figure 12-9).

Figure 12-9. Changing Appearance of Attributes



4. Select the attribute from the list of visible attributes and select:
 - Show - to display currently hidden attributes in stream
 - Hide - to hide attribute from view in the stream
 - Up - to move attribute up in the stream up
 - Down - to move down
 - Default - to restore original view

5. **Apply** applies change leaving dialog box open; **OK** applies and exits.

Viewing a Transaction in the List Window

Prerequisites

Your design code must contain the transactions for them to be visible in the GUI. See [Recording Transactions in SystemC](#) or [Recording Transactions in Verilog](#) for instructions on transaction recording.

Procedure

1. Run simulation on a design containing transactions.
vsim top; run -all
2. Add transaction objects (transaction streams, sub-streams, attributes and attribute elements) to List window:
 - Drag and Drop from the Object or Structure (sim) windows

Results

When transactions are present in the List window, new rows are written to the List window any time a transaction's state changes. Specifically, rows are printed when a transaction starts or ends and when any attribute changes state, which can occur between time steps or deltas.

Example 12-1. Transactions in List Window

This example shows List output for a stream showing two transaction kinds. Each has a begin attribute, a special attribute and an end attribute in the style of SCV.

```
ns                               /top/abc/busMon
  delta
0 +0                             <Inactive>
1 +0                             <Inactive>
1 +0                             <Inactive>
1 +0      {busRead 1 <Inactive> <Inactive>}
3 +0          {busRead 1 100 <Inactive>}
3 +0          {busRead 1 100 10}
3 +0                             <Inactive>
4 +0                             <Inactive>
4 +0                             <Inactive>
4 +0                             <Inactive>
4 +0      {busWrite 2 <Inactive> <Inactive>}
6 +0          {busWrite 2 200 <Inactive>}
6 +0          {busWrite 2 200 20}
6 +0                             <Inactive>
7 +0                             <Inactive>
7 +0                             <Inactive>
7 +0                             <Inactive>
7 +0      {busRead 3 <Inactive> <Inactive>}
9 +0          {busRead 3 300 <Inactive>}
9 +0          {busRead 3 300 30}
```

9 +0

<Inactive>

In this example, you can see the same time/delta repeating as changes are made to the transaction. For example, at 1(0) a busRead begins with the begin attribute set to the value "1". At time 3(0), the end attribute value "100" arrives. On the next line, also at time 3(0), the special attribute's value of "10" arrives. On the next line the transaction has ended. This is followed by a number of lines showing the "<Inactive>" state as the various attributes change state internally.

Viewing a Transaction in the Objects Window

Prerequisites

- Running a design in which transactions have been written.

Procedure

1. Run simulation on a design containing transactions.

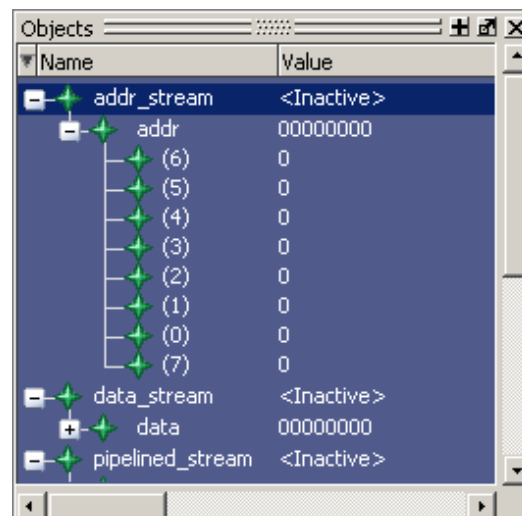
```
vsim top; run -all
```

2. Open the Objects window, if not open by default: View > Objects.

Results

Streams appear in the Objects window as simple or composite signals, depending on the complexity of transactions that have been defined for the stream. The icon for a transaction stream is a four pointed star in the color of source language for the region in which the stream is found (SystemC - green, Verilog - blue, etc.).

Figure 12-10. Transactions in Objects Window



Debugging with Tcl

In order to access attributes of transactions for debugging, you must know the full path to the specific stream, substream or attribute you wish to access. After you set the path to the transaction, you can use Tcl to analyze your transactions. A full path (using the Verilog path delimiter) to an attribute would be:

```
<stream>.<substream>[<substream...>].<attribute>
```

An example of setting the path to the attribute of a transaction is as follows:

1. Set the names of streams created using TCL. For example:

```
set streamName "top.stream1"
```

ModelSim names the sub-streams which are auto generated in the following format name, <first_initial_of_stream><number_of_substream>, so you would set the substream name as:

```
set subStream "s0"
```

2. Set the attribute name you want to access, such as:

```
set attributeName "myInteger"
```

Once you have set the stream, substream, and attribute names, you can access the variable value at any specified time. A sample examine command using the attribute in the above example might be:

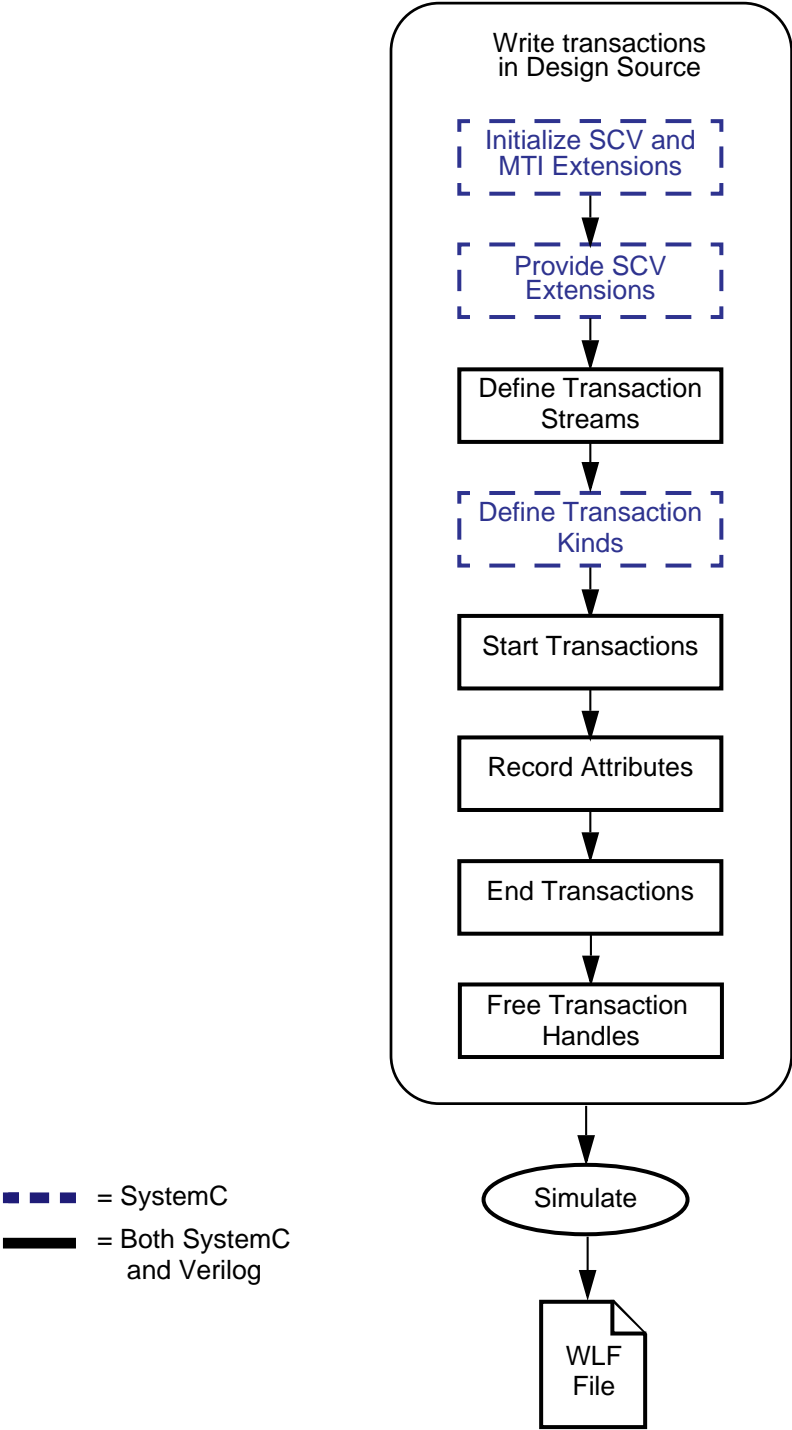
```
exa -t 30 $streamName.$subStream.$attributeName
```

You can place commands such as these into a Tcl script and use it to parse the .wlf database.

Transaction Recording Flow

The basic steps for recording transactions can be summarized in [Figure 12-11](#).

Figure 12-11. Recording Transactions



The SystemC tasks and Verilog API calls used in these steps are listed in [Figure 12-1](#).

Table 12-1. System Tasks and API for Recording Transactions

Action	SystemC - System Task Used	Verilog - ModelSim API Used
Initializing SCV and MTI extensions — Required - SCV only. See Initializing SCV and Creating WLF Database Object	scv_startup()	N/A
Creating database tied to WLF — Required for SCV only. See Initializing SCV and Creating WLF Database Object	scv_tr_db() scv_tr_wlf_init()	N/A
Provide SCV extensions — Required for SCV only. ¹ See Creating Transaction Generators	scv_tr_stream()	N/A
Define transaction streams — Required. SC - See Defining a transaction stream V - See Defining a transaction stream	scv_tr_generator()	\$create_transaction_stream
Define transaction kinds — Required for SVC only. See Defining a transaction kind (This step is Optional.)	See SCV documentation	N/A
Start the transaction — Required. SC - See Starting a Transaction V - See Starting a Transaction	::begin_transaction()	\$begin_transaction
Record attributes — Optional. SC - See Recording Special Attributes V - See Recording an Attribute	::record_attribute()	\$add_attribute
End the transaction — Required. SC - See Ending a Transaction V - See Ending a Transaction	::end_transaction()	\$end_transaction
Free the transaction handle — Required for Verilog. SC - See Freeing a Transaction Handle V - See Freeing the Transaction Handle	Freed automatically when transaction goes out of scope	\$free_transaction
Specify relationships between transactions — Optional. SC - See Freeing a Transaction Handle V - See Specifying Relationships	::add_relation()	\$add_relation or \$begin_transaction

Table 12-1. System Tasks and API for Recording Transactions

Action	SystemC - System Task Used	Verilog - ModelSim API Used
Specify begin and/or end times of transactions — Optional. SC - See Specifying Transaction Start and End Times V - See Specifying Transaction Start and End Times	::begin_transaction() and ::end_transaction()	\$begin_transaction and \$end_transaction
Control database logging — Optional. See Stream Logging	log / nolog and ::set_recording()	log / nolog
Simulate the design — Required in order to view transactions.	vsim <top>	vsim <top>

1. Required only for SCV user-defined types used as attributes.

Transaction Recording Guidelines

This section outlines the rules and guidelines that apply to all transaction recording, regardless of the language in which the transaction is recorded. Read these guidelines prior to recording transactions for a general understanding of recording transactions for viewing in ModelSim:

Names of Streams and Substreams	506
Stream Logging	506
Transaction UIDs	507
Attribute Type	507
Anonymous Attributes	508
Multiple Uses of the Same Attribute	508
Relationships in Transactions	508
The Life-cycle of a Transaction	508
Retroactive Recording / Start and End Times	509
Start and End Times for Phase Transactions	509
Transaction Handles and Memory Leaks	509

For language-specific instructions and deviations from these general truths, see:

- [Recording Transactions in Verilog](#)
- [Recording Transactions in SystemC](#)

For SCV specific limitations and implementation details, see [SCV Limitations](#).

Limitations

- The checkpoint/restore commands are not supported for transactions.

- Transactions appearing in a .wlf file that was created with 6.3 are not viewable in later versions. You must rerun the simulator in version 6.4 or above for them to be viewable.

For SCV specific limitations and implementation details, see [SCV Limitations](#).

Names of Streams and Substreams



Important: A space in any name (whether a database, stream, transaction, or attribute) requires the name be enclosed by escaped or extended identifiers.

You must provide a name for streams so that they can be referenced for debug. Anonymous streams are not allowed. Any legal Verilog or C language identifiers are recommended for naming, since these are guaranteed to be supported for debug, though the tool imposes no restrictions on names.

Note



The simulator issues a warning for a non-standard name.

Full or Relative Pathnames

When creating a transaction stream, you can specify a full path to the region in which you want the transaction stream to appear. Assuming that the specified path leads to an existing region in the design hierarchy, that request is honored. No regions are created in the process.

You can also specify a relative path, using the tool to search upward from the calling region in the hierarchy as determined automatically by the simulator. The region where a transaction stream appears is determined according to the placement of the call to create the stream (`$create_transaction_stream` or `scv_tr_stream`). For most designs, the transaction stream is placed just where you would want it to be. However, for some SystemVerilog and OVM class-based designs, the placement may not be appropriate. In these cases, full path specifications are usually safest.

Substream Names

The tool names substreams automatically. The name of any substream is the first character of the parent's name followed by a simple index number. The first substream has the index zero. If the parent stream has a non-standard name, such as one that starts with a numeral or a space, you may have difficulty with debug.

Stream Logging

By default, when your design creates a stream, logging is enabled for that stream providing that the logging is enabled at the simulation time when the design calls `::begin_transaction()`. The

effective start time of the transaction (the time passed by the design as a parameter to `::begin transaction()`) does not matter. For example, a stream could have logging disabled between T1 and T2 and still record a transaction in that period using retroactive logging after time T2. A transaction is always entirely logged or entirely ignored. You can disable the logging on transaction streams with the `nolog` command.

There is no way in the ModelSim tool to distinguish a stream whose logging has been disabled from one that is merely inactive.

Transaction UIDs

Each transaction, when created during simulation, is assigned a 64-bit serial number. This serial number, along with the logical name of the dataset in which the transaction exists, comprises the transaction's UID (unique identifier). Within the simulation run, this number is unique.

The `"tr uid"` and `"tr color"` commands use the UID to specify a specific transaction within a particular dataset in which it exists. UIDs also allow for any transaction to refer to any other transaction.

Use examples:

```
tr color -nametext "light blue" {sim 10023}
```

```
tr color -namebg red {myData 209832}
```

The first example represents a transaction in the current simulation, since `"sim"` is always the name of the current simulation dataset. The second example is a transaction from a WLF file opened with the logical name `"myData"`.

Attribute Type

- For any given stream, ModelSim associates each attribute with a type for that attribute. When ModelSim records an attribute, it looks at the attribute name to see if there is already an attribute of that name and type. An attribute is new if the name does not match an existing attribute of the stream or if the name matches but the type does not. ModelSim permits the name to be reused for a different data type, but the debug system forces this to act like two different attributes. For example, there will be two different rows in the wave display for the same attribute name.
- For any given stream, the attribute's type is fixed the first time you use the attribute. Thereafter, you can not change the type of that attribute on that stream. If you try, the simulator issues a fatal error.
- Overloading an attribute name is allowed, but ModelSim issues a warning since debug actions (like part select) may be impossible.

Multiple Uses of the Same Attribute

There is nothing to prevent your design from setting the same attribute (same type) many times during the transaction. However, the ModelSim tool records only the last value of the attribute prior to the end of the transaction.

Once any attribute is used, it is considered an attribute of the parent stream from that time onward. Thus, it shows up as a parameter on all subsequent transactions, even if it is unused.

Anonymous Attributes

ModelSim requires every transaction attribute to have a name. It is possible to neglect the name in the SCV and Verilog APIs for transaction recording, however. The simulator resolves the problem by inventing a name for the attribute.

SCV — an attribute is anonymous if the name is the empty string or the name is a NULL pointer. The simulator uses the data type to choose a new name as follows:

- If the type is a struct or class, the simulator constructs an attribute for each field or member, using the field or member name as the name of each attribute.
- If the type is anything other than a string or class, the simulator uses the type name (for example, "short", "float", etc.) as the name for the attribute.

Verilog — an attribute is anonymous if the name parameter is ignored or is an empty string. The simulator chooses a name as follows:

- If the value of the attribute is passed through a variable, the simulator uses the name of the variable as the name for the attribute.
- If the value of the attribute is passed as a literal or the return value from a function, the simulator uses the type name of the value as the name for the attribute.

In any language, if the simulator finds an attribute already exists with the same name and type as the one it is creating, it will re-use that attribute.

Relationships in Transactions

A relation is simply a name, a source transaction and a target transaction. It can be read as, "<source> has the <name> relation to <target>." ModelSim records the relationship — both from the source to the target and the target to the source — in the database so it is available for transaction debug and analysis. For instructions on recording relationships, see [“Freeing a Transaction Handle”](#) (SC) and [“Freeing a Transaction Handle”](#) (Verilog).

The Life-cycle of a Transaction

Any transaction has a life-cycle that can be summarized in four distinct phases:

- **Creation** — This is the moment in simulation when a design calls `$begin_transaction()` or an equivalent method.
- **Start time** — Usually, the start time is determined by the call to `$begin_transaction()`, except in the case of retroactive recording, when the start time is set earlier than the creation time.
- **End time** — Typically determined by a call to `$end_transaction()`, though it, too, can be adjusted.
- **End-of-life** — The moment in simulation when the design releases its handle to the transaction. No more additions or changes can be made to the transaction past this point.

This life-cycle is has several important implications:

- Attributes and relations can be added during the entire life-cycle, not just between the start and end times for the transaction, so long as you have a valid handle to the transaction. A valid handle is one whose returned value is non-zero. See “[Testing a Verilog Transaction Handle for Errors](#)” for information about how to detect errors.
- You can enable or disable logging of transactions anytime during the life-cycle, regardless of start and end times.
- A transaction stays in memory until its handle is released. Transaction handles should be freed as soon as possible, to minimize use of memory buffering and the retroactive WLF channels. Verilog designs must use the `$free_transaction()` task explicitly for every transaction.

Retroactive Recording / Start and End Times

The only time you must specify start and end times for a transaction is when you are recording a transaction retroactively. For all other transaction types, the simulator knows the start and end times. It is illegal to start or end a transaction in the future or before time 0. If either is specified, the simulator uses the current simulation time, and issues a non-fatal error message.

Start and End Times for Phase Transactions

The start and end times for phase transactions must be entirely within the timespan of the parent transaction. Start and end times of phases can match the start or end times of parent.

Transaction Handles and Memory Leaks

When a begin transaction call is made, the transaction handle is stored in memory and remains in memory until it is freed. In Verilog, you must free the transaction handle explicitly using `$free_transaction`. In SCV, the handle is freed for you when the handle goes out of scope. However, global or static transactions remain in memory for the entire simulation.

Though this memory loss may be more accurately described as “usage” rather than a “leak”, it is wasteful to use memory for transactions no longer in use. You should write your code in such a way as to free transaction handles once they are not needed.

Transaction Recording Procedures

The procedures for recording transactions in Verilog are much simpler than those for SystemC, so they are presented in that order to simplify your understanding of the recording process.

Recording Transactions in Verilog	510
Recording Transactions in SystemC	513

Transaction recording in Verilog is a much simpler task than it is in SystemC. For that reason, it is presented first.

Recording Transactions in Verilog

As there is not yet a standard for transaction recording in Verilog or SystemVerilog, the ModelSim tool includes a set of system tasks to perform transaction recording into a WLF file. See [CLI Debugging Command Reference](#) for specific tasks used to record the transactions. The API is the same for Verilog and SystemVerilog. As stated previously, the name "Verilog" refers both to Verilog and SystemVerilog unless otherwise noted.

The Verilog recording API is a bit simpler than the SCV API. Specifically, in Verilog:

- There is no database object as there is in SCV; the database is always WLF format (a .wlf file).
- There is no concept of begin and end attributes. All attributes are recorded with the system task `$add_attribute`.
- Your design code must free the transaction handle once the transaction is complete and all use of the handle for relations or attribute recording is complete. (In most cases, SystemC designs ignore this step since SCV frees the handle automatically.)

For a full example of recorded Verilog transactions with comments, see [Verilog API Code Example](#).

Prerequisites

- Understand the rules governing transaction recording. See the section entitled [Transaction Recording Guidelines](#).

Procedure

1. Defining a transaction stream

Use `$create_transaction_stream` to create one or more stream objects.

```
module top;
  integer hStream

  initial begin
    hStream = $create_transaction_stream("stream", "transaction");
    .
    .
  end
  .
  .
endmodule
```

This example code declares the stream *stream* in the current module. The stream is part of the WLF database and the stream will appear as an object in the GUI. The stream will be logged.

In some OVM or other class-based designs, you may want to specify stream a full path to the location where you wish to the stream to appear. See “[Full or Relative Pathnames](#)” for more information.

2. Starting a Transaction

Use [\\$begin_transaction](#), providing:

- a valid handle to a transaction stream
- a variable to hold the handle of the transaction itself

```
integer hTrans;
.
.
hTrans = $begin_transaction(hstream, "READ");
```

In this example, we begin a transaction named "READ" on the stream already created. The [\\$begin_transaction](#) system function accepts other parameters to specify: the start time for the transaction, and any relationship information, including its designation as a phase transaction (see “[Phase / Child Transactions](#)”). See [CLI Debugging Command Reference](#) for syntax details.

The return value is the handle for the transaction. It is needed to end the transaction or record attribute.

3. Recording an Attribute

Optional. Use the [\\$add_attribute](#) system task and provide:

- the type and handle of the transaction being recorded
- the name for the attribute
- a variable that holds the attribute value

Be aware that nothing prevents the design from setting the same attribute many times during the transaction. However, ModelSim records only the last value of the attribute

prior to the end of the transaction. Once the design uses an attribute, it becomes a permanent attribute of the parent stream from that time onward. Thus, it shows up as an element of all subsequent transactions, even if it is unused. Example:

```
integer address;  
.  
.  
$add_attribute(hTrans, address, "addr");
```

4. Ending a Transaction

Submit a call to [\\$send_transaction](#) and provide the handle of the transaction:

```
$send_transaction(hTrans);
```

This ends the specified transaction, though it does not invalidate the transaction handle. The handle is still valid for calls to record attributes and to define relations between transactions. As with `$begin_transaction()`, there are optional parameters for this system task. See [CLI Debugging Command Reference](#) for details.

5. Specifying Relationships

Provide:

- two valid transaction handles: one for the source, one for the target
- the <name> of the relation (that is, the relationship of the <source> to the <target>)
- Specify relation from an existing transaction to another existing transaction:

Submit a call to `$add_relation()`.

```
integer hSrc;  
integer hTgt;  
.  
.  
$add_relation(hSrc, hTgt, "successor");
```

6. Specifying Transaction Start and End Times

To specify a start and/or end time for any transaction, pass the start and end times as parameters to `$begin_transaction()` and `$end_transaction()`. The time must be the current simulation time or earlier. See [“Transaction Recording Guidelines”](#) for information on valid start and end times.

7. Freeing the Transaction Handle



To avoid memory leakage: You must explicitly free all transaction handles in your design. This is a requirement for Verilog (and SystemVerilog) recording. See [“Transaction Handles and Memory Leaks”](#).

- a. Ensure that the transaction is complete AND all use of the handle for recording attributes and relations has been completed.
- b. Submit a call to `$free_transaction`, providing the handle of the transaction being freed.

```
$free_transaction(hTrans);
```

where `hTrans` is the name of the transaction handle to be freed.

Example 12-2. Verilog API Code Example

This example is distributed with ModelSim and can be found in the `install_dir/examples/systemverilog/transactions/simple` directory.

```
module top;
  integer stream, tr;

  initial begin
    stream = $create_transaction_stream("Stream");
    #10;
    tr = $begin_transaction(stream, "Tran1");
    $add_attribute(tr, 10, "beg");
    $add_attribute(tr, 12, "special");
    $add_attribute(tr, 14, "end");
    #4;
    $end_transaction(tr);
    $free_transaction(tr);
  end
endmodule
```

Testing a Verilog Transaction Handle for Errors

You can use the `$create_transaction_stream()` and `$begin_transaction()` to test whether a handle is has errors. Handles returned by `$create_transaction_stream()` and `$begin_transaction()` are non-zero unless there is an error. Errors are reported to the transcript.

Recording Transactions in SystemC

SystemC users use the SCV library's transaction recording API routines to define transactions, to start them, to end them, to create relationships between them, and to attach additional information (attributes) to them. These routines are described in the "SystemC Verification Standard Specification, Version 1.0x": please refer to it for SCV specific details.

The SCV API is a bit more involved than the Verilog recording API. Specific differences in the SCV API are as follow:

- In SCV, you must create a database object that is tied to a .wlf (WLF formatted database) file.
- The concept of begin and end attributes is unique to SCV. In Verilog, all attributes are recorded with a single system task: \$add_attribute.
- Transaction handles are freed automatically in SCV.

For a full example of recorded SCV transactions with comments, see “[SCV API Code Example](#)”.

Prerequisites

- Understand the material in the section entitled “[Transaction Recording Guidelines](#)” to understand the basic rules and guidelines for recording transactions.
- Be aware of the limitations for recording transactions in SCV. See “[SCV Limitations](#)”.

Procedure

1. Initialize SCV and the MTI extensions for transaction recording and debug.
2. Create a database tied to WLF.
3. Provide SCV extensions, for user-defined types used with attributes.
4. Create transaction generators.
5. Write the transactions.

Initializing SCV and Creating WLF Database Object

Before transactions can be recorded, the design must initialize the SCV library once, as part of its own initialization.

1. Enter `scv_startup()` in the design code — this initializes the SCV library.
2. Enter `scv_tr_wlf_init()` in the design code — this creates the database tied to WLF, allowing transactions to then be written to specific database objects in the code.
3. Enter database object(s) — you can create many objects, or create one and specify it as the default object. All database objects are contained in a single .wlf file.

Example 12-3. SCV Initialization and WLF Database Creation

Here is an example of a one-time initialization routine that sets up SCV, ties all databases to WLF, and then creates one database as the default:

```
static scv_tr_db * init_recording() {
    scv_tr_db *txdb;

    /* Initialize SCV: */
    scv_startup();
}
```

```
/* Tie databases to WLF: */
scv_tr_wlf_init();

/* Create the new DB and make it the default: */
txdb = new scv_tr_db("txdb");

if (txdb != NULL)
    scv_tr_db::set_default_db(txdb);

return txdb;
}
```

ModelSim ignores the following:

- name argument to `scv_tr_db()` — All databases are tied to the WLF file once the user calls `scv_tr_wlf_init()`.
- `sc_time_unit` argument to `scv_tr_db()` when the database is a WLF database — The time unit of the database is specified by the overall simulation time unit.

Creating Transaction Generators

If your design uses standard C and SystemC types for attributes, no preparation is needed with SCV. C/C++ and SystemC types are supported as described in [Type Support](#). However, if your design uses user-defined types — such as classes, structures, or enumerations — you must provide SCV extensions so that SCV and the ModelSim tool can extract the necessary type and composition information to record the type.

For specific details on providing SCV extensions, refer to the SystemC Verification Standard Specification, Version 1.0e.

Writing SCV Transactions



Important: A space in any name (whether a database, stream, transaction, or attribute) requires the name be an escaped or extended identifier.

1. Defining a transaction stream

Before you can record a transaction, you must define the stream onto which the transaction will be written. In SCV, streams are tied to a specific database so that all transactions on them are written into that database only. Usually, the code declares the stream as a member of the module that will use it. Then, it must call the constructor, passing the stream's name and database as parameters. For example:

```
SC_MODULE(busModel)
{
    public:
        scv_tr_db *txdb;
        scv_tr_stream busStream;
```

```
SC_CTOR(busModel) :
    txdb(init_recording()),
    busStream( "busModel", "***TRANSACTION**" )
{
}
}
```

This example code declares the database and stream objects. In the module constructor, it initializes the database by calling the setup routine (defined in “[Initializing SCV and Creating WLF Database Object](#)”). It initializes the stream object with its display name and a string indicating the stream kind. The database is presumed to be the default, though the example could have been explicit and passed "txdb" as a third parameter.

The name of the stream must be passed as a parameter. ModelSim treats it as a path name. This defines where the stream will appear in the design during debug. Each stream lives in a design region: either the instance in which it was declared or an instance specified in the constructor parameters.

If the string is a simple name such as "busRead", ModelSim assumes the stream is to be created in the current scope, usually the instance of the module. If the string is a partial path such as "dut/bus/busRead", ModelSim will try to find parent region "dut/bus" as the home for the stream. If the string is a full path, such as "/top/dut/bus/busRead", ModelSim tries to find the exact region "/top/dut/bus".

If ModelSim can't find the region, it will create it. This lets the user place transactions into a region created solely for verification. If the user specifies a stream where one already exists, ModelSim treats these as the same stream even though the design will have two different stream objects.

For more specific details on writing a transaction, refer to the “SystemC Verification Standard Specification, Version 1.0e”.

2. Defining a transaction kind (This step is Optional.)

In SCV, each transaction is defined by a generator object, which is a template for a transaction. The generator:

- Specifies the name of the transaction. Anonymous transactions are not allowed.
- Specifies optional begin and end attributes. Begin and end attributes are part of the generator for that kind. They are treated as part of each instance of that transaction.

First, the code must declare each generator, usually in the module in which it will be used. Any begin and end attribute types must be provided as template parameters. Then, the generator must be constructed, usually in the constructor initialization list of the parent module:

```
SC_MODULE(busModel)
{
    public:
        scv_tr_db *txdb;
        scv_tr_stream busStream;
```

```
scv_tr_generator<busAddrAttr, busDataAttr> busRead;  
SC_CTOR(busModel) :  
    txdb(init_recording()),  
    busStream( "busModel", "***TRANSACTION**" ),  
    busRead( "busRead", busStream)  
    {  
    }  
}
```

The third and fourth arguments to `scv_tr_generator::scv_tr_generator()` are the names for the begin and end attributes, which SCV allows to be NULL by default. (Any attributes you create with an empty string or NULL pointer for the name are called *anonymous attributes*. For more information on how these are treated by ModelSim, see [“Anonymous Attributes”](#).)

The example above adds the declaration of the generator "busRead" and shows how the constructor is provided with a name (also "busRead") and the stream on which it will be used. The begin and end attributes are left anonymous.

Within ModelSim, a design can reuse an attribute name with a different type. However a warning is issued since this practice limits debug in the simulator. See [“Attribute Type”](#) for further details.

3. Starting a Transaction

- a. Prepare the value for the begin attribute.
- b. Call `scv_tr_generator::begin_transaction()` with the appropriate parameters as defined in the SCV API.
- c. Optional — You can apply additional parameters to specify relationships, or to specify a begin time other than the current simulation time. For more information, see [Recording Phase Transactions](#) and [Specifying Transaction Start and End Times](#).

Example:

```
scv_tr_handle txh;  
busAddrAttr busAddr;  
busAddr._addr = 0x00FC01;  
txh = busRead.begin_transaction(busAddr);
```

In this example, only the begin attribute "busAddr" is passed to `::begin_transaction()`. Other parameters may be used to specify relationships or specify a begin time other than the current simulation time. (See [“Relationships in Transactions”](#) and [“Retroactive Recording / Start and End Times”](#).)

4. Recording Special Attributes

Special attributes are not part of the original transaction generator: they are afterthoughts. Record special attributes by:

- a. Define the attribute type.

- b. Modify a specific transaction instance through the transaction handle using the `scv_tr_handle::record_attribute()` routine.

Example:

```
if (status != BUS_OK) {
    errorAttr err;
    err.code = status;
    txh.record_attribute(err);
}
```

Nothing prevents a design from setting the same special attribute many times during the transaction. However, the ModelSim simulator records only the last value of the attribute prior to the end of the transaction.

For greater detail on recording special attributes, refer to the SystemC Verification Standard Specification, Version 1.0e.

5. Recording Phase Transactions

Phase transactions are unique to ModelSim. If recorded, they appear as transactions within their parent transaction. The SCV specification does not describe this kind of transaction, but ModelSim can record it. Any transaction may have phases, including another phase transaction. To record phase transactions:

- a. Specify **mti_phase** as the relation name in a call to **::begin_transaction()**.

You can also specify your own relation name for phases by modifying the value of the variable `ScvPhaseRelationName` in the `modelsim.ini` from “`mti_phase`” to something else, such as “`child`”. This variable applies to recording only; once a phase is recorded in a WLF file, it is drawn as a phase, regardless of the setting of this variable.

- b. Provide an appropriate parent transaction handle in a call to **::begin_transaction()**.

6. Specifying Transaction Start and End Times

To specify a start and/or end time for any transaction, pass the start and end times as parameters to **::begin_transaction()** and **::end_transaction()**. The time must be the current simulation time or earlier. See “[Retroactive Recording / Start and End Times](#)” and “[Start and End Times for Phase Transactions](#)”.

7. Ending a Transaction

To end transactions in your SystemC code:

- a. Set the value for the end attribute.
- b. Call **scv_tr_generator::end_transaction()**, specifying any end attributes or other appropriate parameters as defined in the SCV API.
- c. Optional — You can specify an end time other than the current simulation time. For more information, see [Specifying Transaction Start and End Times](#).

8. Freeing a Transaction Handle

Transaction handles should be freed after `end_transaction()` is called to avoid a memory leak. Transaction handles are freed automatically in SCV when the transaction handle goes out of scope or when the transaction handle is reassigned. Global or static transactions remain in memory for the duration of the simulation. See “[Transaction Handles and Memory Leaks](#)” for details.

9. Specifying Relationships

Provide:

- two valid transaction handles: one for the source, one for the target
- the <name> of the relation (that is, the relationship of the <source> to the <target>)
- Specify relation within an existing transaction using `scv_tr_handle::add_relation()` methods. For example:

```
scv_tr_handle prev_txx;  
scv_tr_handle txx;  
busAddrAttr busAddr;  
busAddr._addr = 0x00FC01;  
txx = busRead.begin_transaction(busAddr);  
txx.add_relation("successor", prev_txx);
```

- Specify relation for a new transaction by creating a relationship to a target transaction when it begins the source transaction. For example:

```
scv_tr_handle prev_txx;  
scv_tr_handle txx;  
busAddrAttr busAddr;  
busAddr._addr = 0x00FC01;  
txx = busRead.begin_transaction(busAddr, "successor", prev_txx);
```

In both these examples, the design specifies that the current transaction is a “successor” to the previous transaction.

Example 12-4. SCV API Code Example

This example is distributed with ModelSim and can be found in the `install_dir/examples/systemc/transactions/simple` directory.

```
#include <systemc.h>  
#include <scv.h>  
  
typedef scv_tr_generator<int, int> generator;  
  
SC_MODULE(tx)  
{  
    public:  
    scv_tr_db      *txdb;          /* a handle to a transaction database */  
    scv_tr_stream *stream;        /* a handle to a transaction stream */  
};
```

```
generator      *gen;          /* a handle to a transaction generator */

SC_CTOR(tx)
{
    SC_THREAD(initialize);
    SC_THREAD(thread);
}

/* initialize transaction recording, create one new transaction */
/* database and one new transaction stream */
void initialize(void) {
    scv_startup();
    scv_tr_wlf_init();
    txdb = new scv_tr_db("txdb");
    stream = new scv_tr_stream("Stream", "*** TRANSACTOR ***", txdb);
}

/* create one new transaction */
void thread(void) {
    scv_tr_handle trh;

    gen = new generator("Generator", *stream, "begin", "end");

    wait(10, SC_NS);                /* Idle period          */
    trh = gen->begin_transaction(10); /* Start a transaction */
    wait(2, SC_NS);
    trh.record_attribute("special", 12); /* Add an attribute    */
    wait(2, SC_NS);
    gen->end_transaction(trh, 14);     /* End a transaction   */
    wait(2, SC_NS);                /* Idle period          */
}
};

SC_MODULE(top)
{
public:
    tx *a;
    SC_CTOR(top)
    {
        a = new tx("tx");
    }
};

SC_MODULE_EXPORT(top);
```

SCV Limitations

You can record transactions in only one WLF file at a time. The SCV API routines allow you to create and use multiple databases, however — if the chosen database is WLF — all databases are aliased to the same *.wlf* file. Once created, you may load multiple *.wlf* files that contain transactions into ModelSim for viewing and debugging.

Type Support

The following types are not supported for SystemC transactions:

- bit-field and T* (pointer) native C/C++ types
- SystemC fixed point types (`sc_fix`, `sc_fix_fast`, `sc_fixed`, `sc_fixed_fast`, `sc_ufix`, `sc_ufix_fast`, `sc_ufixed`, `sc_ufixed_fast`) are not supported.

CLI Debugging Command Reference

A list of CLI commands available for debugging your transactions are as follow:

add list	examine	search
add wave	find	show
context	left	up
dataset clear	log / nolog	write list
dataset save	precision	write wave
dataset snapshot	property list	
delete	property wave	
describe	radix	
down	right	

Verilog API System Task Reference

The ModelSim tool's available API system tasks used for recording transactions in Verilog (and SystemVerilog) are:

- [\\$create_transaction_stream](#) — creates the transaction stream
- [\\$begin_transaction](#) — starts a transaction
- [\\$add_attribute](#) — adds attributes to an existing transaction
- [\\$end_transaction](#) — ends the transaction
- [\\$add_relation](#) — records relations on an existing transaction
- [\\$free_transaction](#) — frees the transaction handle

[\\$add_attribute](#)

Add an attribute to a transaction.

Syntax

\$add_attribute(transaction, value, attribute_name)

Returns

Nothing

Arguments

Name	Type	Description
transaction	integer	Required. Handle for the transaction to which you are adding the attribute.
value	object	Required. Verilog object that is the value to be used for the attribute.
attribute_name	string	Optional. The name of the attribute to be added to the transaction. Default: The name of the variable used for the value parameter if it can be determined, “anonymous” otherwise.

Related Topics

[Recording Transactions in Verilog](#)

[Attribute Type](#)

[Multiple Uses of the Same Attribute](#)

[Anonymous Attributes](#)

\$add_relation

Add a relation from the source transaction to the target transaction.

Syntax

\$add_relation(source_transaction, target_transaction, relationship_name)

Returns

Nothing

Arguments

Name	Type	Description
source_transaction	integer	Required. Handle to the source transaction for which the relationship is to be established.
target_transaction	integer	Required. Handle to the target transactions for which the relationship is to be established.
relationship_name	string	Required. The name of the relationship.

Related Topics

[Recording Transactions in Verilog](#)

[Relationships in Transactions](#)

\$begin_transaction

Begin a transaction on the specified stream. The transaction handle must be saved for use in other transaction API calls. `$begin_transaction` is used to start all transactions. The optional fourth parameter allows you to specify a parent transaction, making the new transaction a phase transaction of the parent.

A handle returned by `$begin_transaction()` will be non-zero unless there is an error. The error is reported to the transcript.

Syntax

```
$begin_transaction(stream, transaction_name, begin_time, parent_transaction)
```

Returns

Name	Type	Description
transaction	integer	The handle to the newly started transaction.

Arguments

Name	Type	Description
stream	integer	Required. Handle to the previously created stream.
transaction_name	string	Required. Name of the transaction to begin.
begin_time	time	Optional. The absolute simulation time that the transaction will begin. Default: The current simulation time.
parent_transaction	integer	Optional. Handle to an existing transaction that is the parent to the new one. The new transaction will be a phase transaction of the parent. Default: NULL

Related Topics

[Recording Transactions in Verilog](#)

[Retroactive Recording / Start and End Times](#)

[The Life-cycle of a Transaction](#)

[Testing a Verilog Transaction Handle for Errors](#)

\$create_transaction_stream

Create a transaction stream that can be used to record transactions. The stream handle must be saved for use in other transaction API calls.

A handle returned by `$create_transaction_stream()` will be non-zero unless there is an error. The error is reported to the transcript.

Syntax

```
$create_transaction_stream(stream_name, stream_kind)
```

Returns

Name	Type	Description
stream	integer	Handle to the created stream.

Arguments

Name	Type	Description
stream_name	string	Required. The name of the stream to be created.
stream_kind	string	Optional. The kind of stream to be created. Default is "Stream". The "stream_kind" is an optional argument for both the SystemC and Verilog/SV APIs. At this time, the kind can be any string and it is not interpreted. It is stored in the WLF file.

Related Topics

[Recording Transactions in Verilog](#)

[About Transaction Streams](#)

[Names of Streams and Substreams](#)

[Stream Logging](#)

[Testing a Verilog Transaction Handle for Errors](#)

\$send_transaction

End the specified transaction. Ending the transaction simply sets the end-time for the transaction and may be done only once. However, if free is not specified, the transaction handle is still valid for use in recording relations and attributes until a call to \$free_transaction().

Syntax

```
$send_transaction(transaction, end_time, free)
```

Returns

Nothing

Arguments

Name	Type	Description
transaction	integer	Required. Handle to the name of the transaction being ended.
end_time	time	Optional. The absolute simulation time that the transaction will end. Default: The current simulation time.
free	integer	Optional. If this argument is non-zero, the memory allotted for this transaction will be freed. This is for convenience, and is equivalent to a call to <code>\$free_transaction</code> for this transaction. Use only when no more attributes will be recorded for this transaction and no relations will be made for this transaction. Default: zero - do not free memory.

Related Topics

[Recording Transactions in Verilog](#)

[Retroactive Recording / Start and End Times](#)

[The Life-cycle of a Transaction](#)

`$free_transaction`

Free a transaction. This call allows the memory allotted for this transaction to be freed. The handle will no longer be valid. Attributes can no longer be recorded for the transaction. Relations can no longer be made with the transaction.



Important: You must free all transaction handles in your design. This is a requirement specific to Verilog and SystemVerilog recording. If a handle is not freed, the result is a memory leak in the simulation.

Syntax

```
$free_transaction(transaction)
```

Returns

Nothing

Arguments

Name	Type	Description
transaction	integer	Handle to the transaction to be freed.

Related Topics

[The Life-cycle of a Transaction](#)

Chapter 13

Recording Simulation Results With Datasets

This chapter describes how to save the results of a ModelSim simulation and use them in your simulation flow. In general, any previously recorded simulation data that has been loaded into ModelSim is called a *dataset*.

One common example of a dataset is a wave log format (WLF) file that has been reopened for viewing. In particular, you can save any ModelSim simulation to a wave log format (WLF) file for future viewing or comparison to a current simulation.

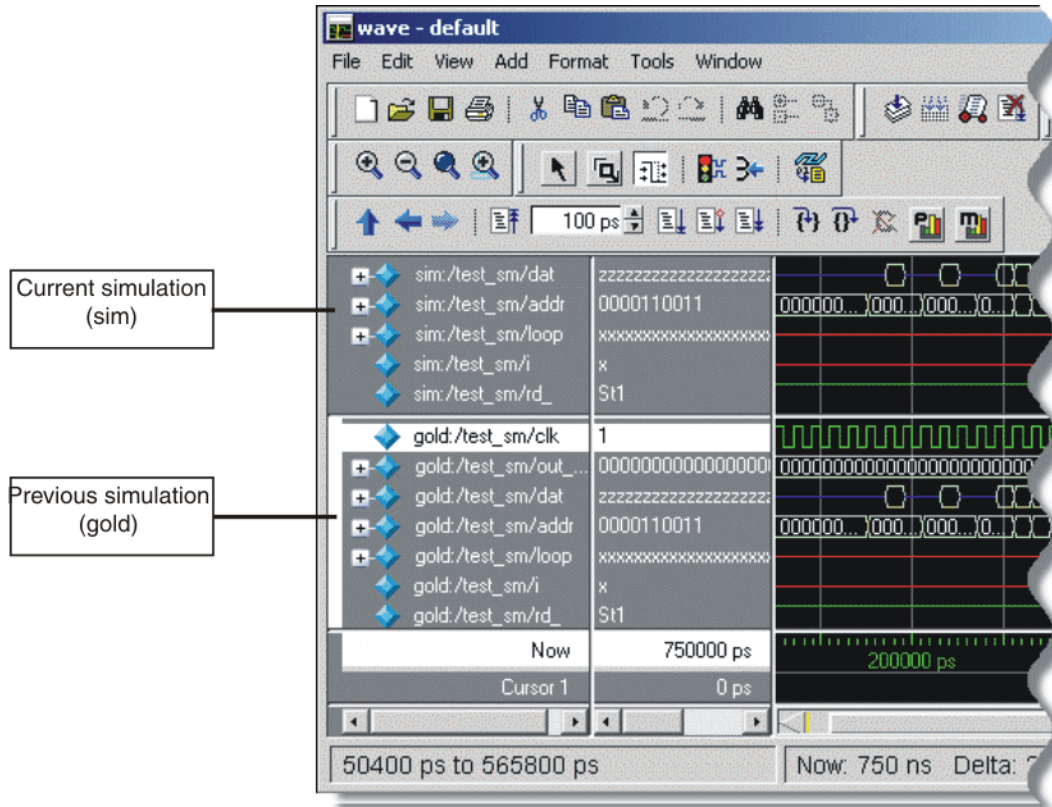
A WLF file is a recording of a simulation run that is written as an archive file in binary format and used to drive the debug windows at a later time. The files contain data from logged objects (such as signals and variables) and the design hierarchy in which the logged objects are found. You can record the entire design or choose specific objects.

A WLF file provides you with precise in-simulation and post-simulation debugging capability. You can reload any number of WLF files for viewing or comparing to the active simulation.

You can also create *virtual signals* that are simple logical combinations or functions of signals from different datasets. Each dataset has a logical name to indicate the dataset to which a command applies. This logical name is displayed as a prefix. The current, active simulation is prefixed by "sim:." WLF datasets are prefixed by the name of the WLF file by default.

Figure 13-1 shows two datasets in the Wave window. The current simulation is shown in the top pane along the left side and is indicated by the “sim” prefix. A dataset from a previous simulation is shown in the bottom pane and is indicated by the “gold” prefix.

Figure 13-1. Displaying Two Datasets in the Wave Window



The simulator resolution (see [Simulator Resolution Limit \(Verilog\)](#) or [Simulator Resolution Limit for VHDL](#)) must be the same for all datasets you are comparing, including the current simulation. If you have a WLF file that is in a different resolution, you can use the `wlfman` command to change it.

Saving a Simulation to a WLF File

If you add objects to the Dataflow, List, or Wave windows, or log objects with the `log` command, the results of each simulation run are automatically saved to a WLF file called `vsim.wlf` in the current directory. If you then run a new simulation in the same directory, the `vsim.wlf` file is overwritten with the new results.

If you want to save the WLF file and not have it be overwritten, select the Structure tab and then select **File > Save**. Or, you can use the `-wlf <filename>` argument to the `vsim` command or the `dataset save` command.

Note



If you do not use **dataset save** or **dataset snapshot**, you must end a simulation session with a **quit** or **quit -sim** command in order to produce a valid WLF file. If you do not end the simulation in this manner, the WLF file will not close properly, and ModelSim may issue the error message "bad magic number" when you try to open an incomplete dataset in subsequent sessions. If you end up with a damaged WLF file, you can try to repair it using the [wlfrecover](#) command.

WLF File Parameter Overview

There are a number of WLF file parameters that you can control via the *modelsim.ini* file or a simulator argument. This section summarizes the various parameters.

Table 13-1. WLF File Parameters

Feature	vsim argument	modelsim.ini	Default
WLF Filename	-wlf <filename>	WLFFilename=<filename>	<i>vsim.wlf</i>
WLF Size Limit	-wlfslim <n>	WLFSizeLimit = <n>	no limit
WLF Time Limit	-wlftlim <t>	WLFTimeLimit = <t>	no limit
WLF Compression	-wlfcompress -wlfnocompress	WLFCompress = 0 1	1 (-wlfcompress)
WLF Optimization ¹	-wlfopt -wlfnoopt	WLFOptimize = 0 1	1 (-wlfopt)
WLF Delete on Quit ^a	-wlfdeleteonquit -wlfnodeleteonquit	WLFDeleteOnQuit = 0 1	0
WLF Cache Size ^a	-wlf cachesize <n>	WLFCacheSize = <n>	0 (no reader cache)
WLF Sim Cache Size	-wlf simcachesize <n>	WLFSimCacheSize = <n>	0 (no reader cache)
WLF Collapse Mode	-wlf nocollapse -wlf collapsedelta -wlf collapse time	WLFCollapseModel = 0 1 2	1

1. These parameters can also be set using the [dataset config](#) command.

- **WLF Filename** — Specify the name of the WLF file.
- **WLF Size Limit** — Limit the size of a WLF file to <n> megabytes by truncating from the front of the file as necessary.
- **WLF Time Limit** — Limit the size of a WLF file to <t> time by truncating from the front of the file as necessary.

- **WLF Compression** — Compress the data in the WLF file.
- **WLF Optimization** — Write additional data to the WLF file to improve draw performance at large zoom ranges. Optimization results in approximately 15% larger WLF files. Disabling WLF optimization also prevents ModelSim from reading a previously generated WLF file that contains optimized data.
- **WLF Delete on Quit** — Delete the WLF file automatically when the simulation exits. Valid for current simulation dataset (*vsim.wlf*) only.
- **WLF Cache Size** — Specify the size in megabytes of the WLF reader cache. WLF reader cache size is zero by default. This feature caches blocks of the WLF file to reduce redundant file I/O. If the cache is made smaller or disabled, least recently used data will be freed to reduce the cache to the specified size.
- **WLFsimCacheSize** — Specify the size in megabytes of the WLF reader cache for the current simulation dataset only. This makes it easier to set different sizes for the WLF reader cache used during simulation and those used during post-simulation debug. If neither `-wlfsimcachesize` nor `WLFsimCacheSize` are specified, the `-wlfcachesize` or `WLFCacheSize` settings will be used.
- **WLF Collapse Mode** — WLF event collapsing has three settings: disabled, delta, time:
 - When disabled, all events and event order are preserved.
 - Delta mode records an object's value at the end of a simulation delta (iteration) only. Default.
 - Time mode records an object's value at the end of a simulation time step only.

Limiting the WLF File Size

The WLF file size can be limited with the `WLFSizeLimit` simulation control variable in the *modelsim.ini* file or with the `-wlfslim` switch for the `vsim` command. Either method specifies the number of megabytes for WLF file recording. A WLF file contains event, header, and symbol portions. The size restriction is placed on the event portion only. When ModelSim exits, the entire header and symbol portion of the WLF file is written. Consequently, the resulting file will be larger than the size specified with `-wlfslim`. If used in conjunction with `-wlftlim`, the more restrictive of the limits takes precedence.

The WLF file can be limited by time with the `WLFTimeLimit` simulation control variable in the *modelsim.ini* file or with the `-wlftlim` switch for the `vsim` command. Either method specifies the duration of simulation time for WLF file recording. The duration specified should be an integer of simulation time at the current resolution; however, you can specify a different resolution if you place curly braces around the specification. For example,

```
vsim -wlftlim {5000 ns}
```

sets the duration at 5000 nanoseconds regardless of the current simulator resolution.

The time range begins at the current simulation time and moves back in simulation time for the specified duration. In the example above, the last 5000ns of the current simulation is written to the WLF file.

If used in conjunction with `-wflslim`, the more restrictive of the limits will take effect.

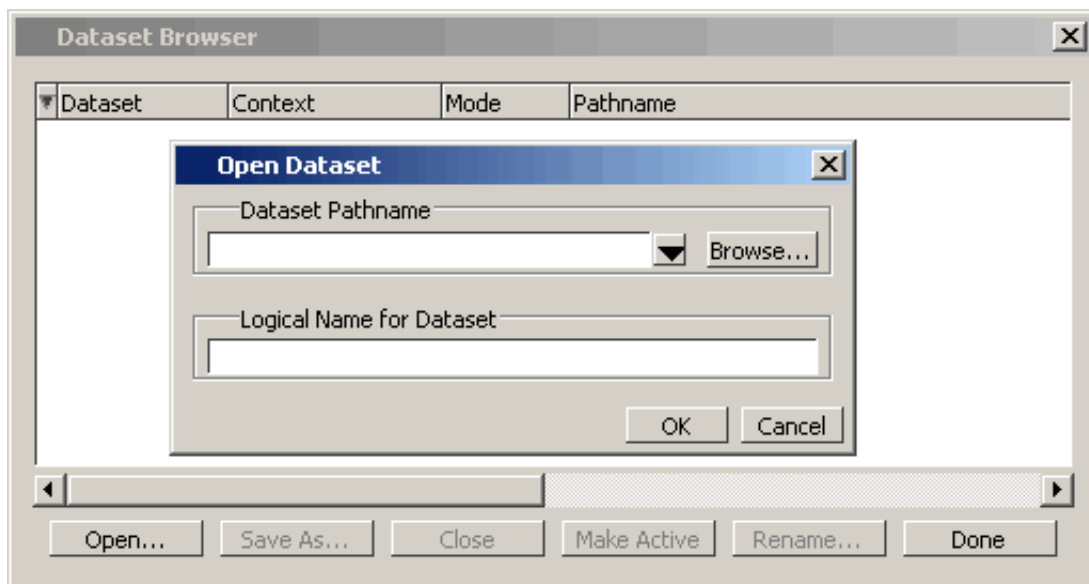
The `-wflslim` and `-wlftlim` switches were designed to help users limit WLF file sizes for long or heavily logged simulations. When small values are used for these switches, the values may be overridden by the internal granularity limits of the WLF file format. The WLF file saves data in a record-like format. The start of the record (checkpoint) contains the values and is followed by transition data. This continues until the next checkpoint is written. When the WLF file is limited with the `-wflslim` and `-wlftlim` switches, only whole records are truncated. So if, for example, you are logging only a couple of signals and the amount of data is so small there is only one record in the WLF file, the record cannot be truncated; and the data for the entire run is saved in the WLF file.

Opening Datasets

To open a dataset, do one of the following:

- Select **File > Open** to open the Open File dialog and set the “Files of type” field to Log Files (*.wlf). Then select the .wlf file you want and click the Open button.
- Select **File > Datasets** to open the Dataset Browser; then click the Open button to open the Open Dataset dialog (Figure 13-2).

Figure 13-2. Open Dataset Dialog Box



- Use the `dataset open` command.

The Open Dataset dialog includes the following options:

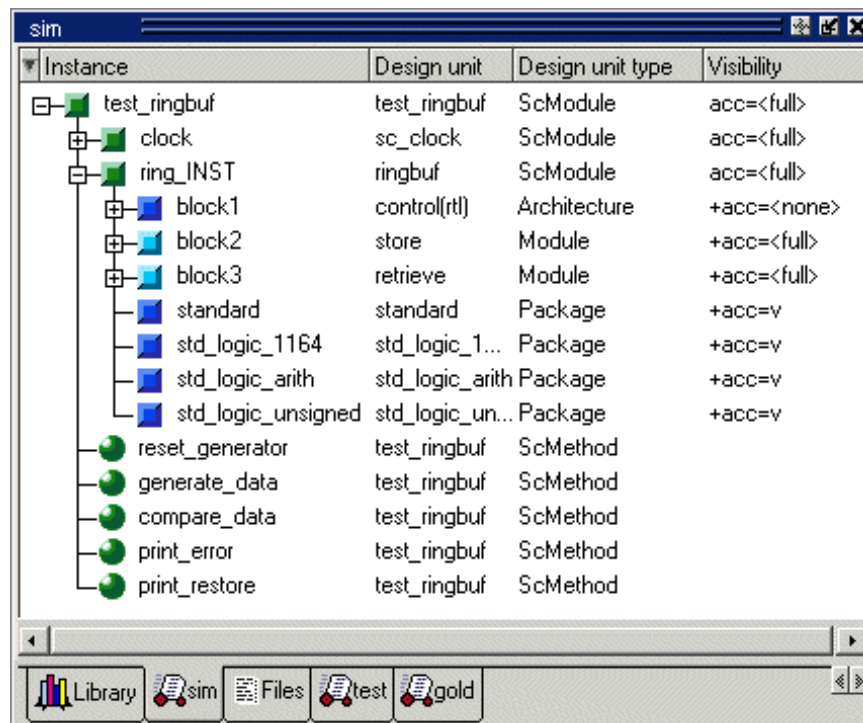
- **Dataset Pathname** — Identifies the path and filename of the WLF file you want to open.
- **Logical Name for Dataset** — This is the name by which the dataset will be referred. By default this is the name of the WLF file.

Viewing Dataset Structure

Each dataset you open creates a structure tab in the Main window. The tab is labeled with the name of the dataset and displays a hierarchy of the design units in that dataset.

The graphic below shows three structure tabs: one for the active simulation (*sim*) and one each for two datasets (*test* and *gold*).

Figure 13-3. Structure Tabs



If you have too many tabs to display in the available space, you can scroll the tabs left or right by clicking the arrow icons at the bottom right-hand corner of the window.

Structure Tab Columns

Each structure tab displays the following columns by default:

Table 13-2. Structure Tab Columns

Column name	Description
Instance	the name of the instance
Design unit	the name of the design unit
Design unit type	the type (for example, Module, Entity, and so forth) of the design unit
Visibility	the current visibility of the object as it relates to design optimization; see Design Object Visibility for Designs with PLI for more information

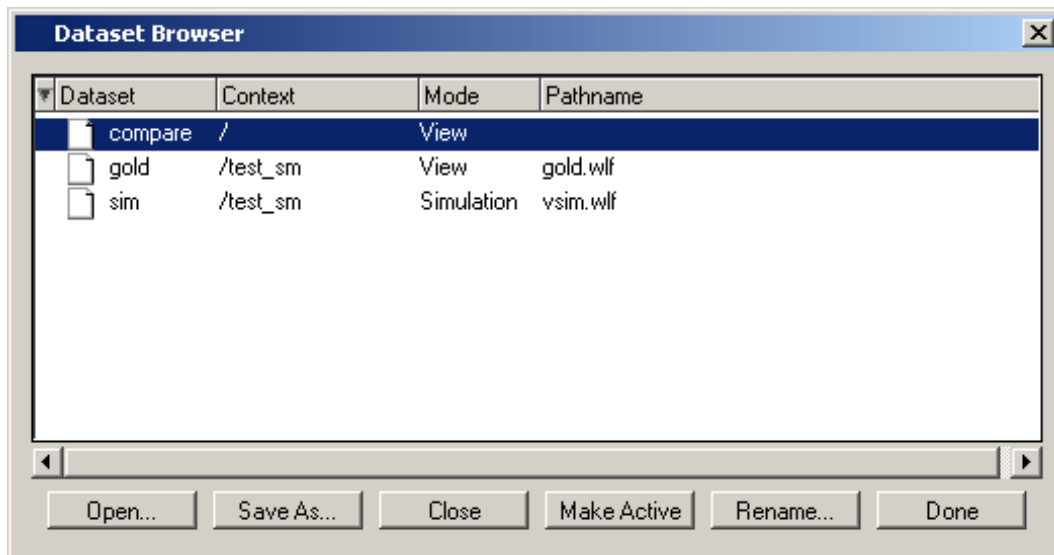
Aside from the columns listed above, there are numerous columns related to code coverage that can be displayed in structure tabs. You can hide or show columns by right-clicking a column name and selecting the name on the list.

Managing Multiple Datasets

GUI

When you have one or more datasets open, you can manage them using the **Dataset Browser**. To open the browser, select **File > Datasets**.

Figure 13-4. The Dataset Browser



Command Line

You can open multiple datasets when the simulator is invoked by specifying more than one **vsim -view <filename>** option. By default the dataset prefix will be the filename of the WLF file. You can specify a different dataset name as an optional qualifier to the **vsim -view** switch on the command line using the following syntax:

```
-view <dataset>=<filename>
```

For example:

```
vsim -view foo=vsim.wlf
```

ModelSim designates one of the datasets to be the active dataset, and refers all names without dataset prefixes to that dataset. The active dataset is displayed in the context path at the bottom of the Main window. When you select a design unit in a dataset's Structure window, that dataset becomes active automatically. Alternatively, you can use the Dataset Browser or the [environment](#) command to change the active dataset.

Design regions and signal names can be fully specified over multiple WLF files by using the dataset name as a prefix in the path. For example:

```
sim:/top/alu/out
```

```
view:/top/alu/out
```

```
golden:.top.alu.out
```

Dataset prefixes are not required unless more than one dataset is open, and you want to refer to something outside the active dataset. When more than one dataset is open, ModelSim will automatically prefix names in the Wave and List windows with the dataset name. You can change this default by selecting:

- List Window active: List > List Preferences; Window Properties tab > Dataset Prefix pane
- Wave Window active: Wave > Wave Preferences; Display tab > Dataset Prefix Display pane

ModelSim also remembers a "current context" within each open dataset. You can toggle between the current context of each dataset using the [environment](#) command, specifying the dataset without a path. For example:

```
env foo:
```

sets the active dataset to **foo** and the current context to the context last specified for **foo**. The context is then applied to any unlocked windows.

The current context of the current dataset (usually referred to as just "current context") is used for finding objects specified without a path.

You can lock the Objects window to a specific context of a dataset. Being locked to a dataset means that the pane updates only when the content of that dataset changes. If locked to both a dataset and a context (such as test: /top/foo), the pane will update only when that specific context changes. You specify the dataset to which the pane is locked by selecting **File > Environment**.

Restricting the Dataset Prefix Display

You can turn dataset prefix viewing on or off by setting the value of a preference variable called DisplayDatasetPrefix. Setting the variable value to 1 displays the prefix, setting it to 0 does not. It is set to 1 by default. To change the value of this variable, do the following:

1. Choose Tools > Edit Preferences... from the main menu.
2. In the Preferences dialog box, click the By Name tab.
3. Scroll to find the Preference Item labeled Main and click [+] to expand the listing of preference variables.
4. Select the DisplayDatasetPrefix variable then click the Change Value... button.
5. In the Change Preference Value dialog box, type a value of 0 or 1, where
 - o 0 = turns off prefix display
 - o 1 = turns on prefix display (default)
6. Click OK; click OK.

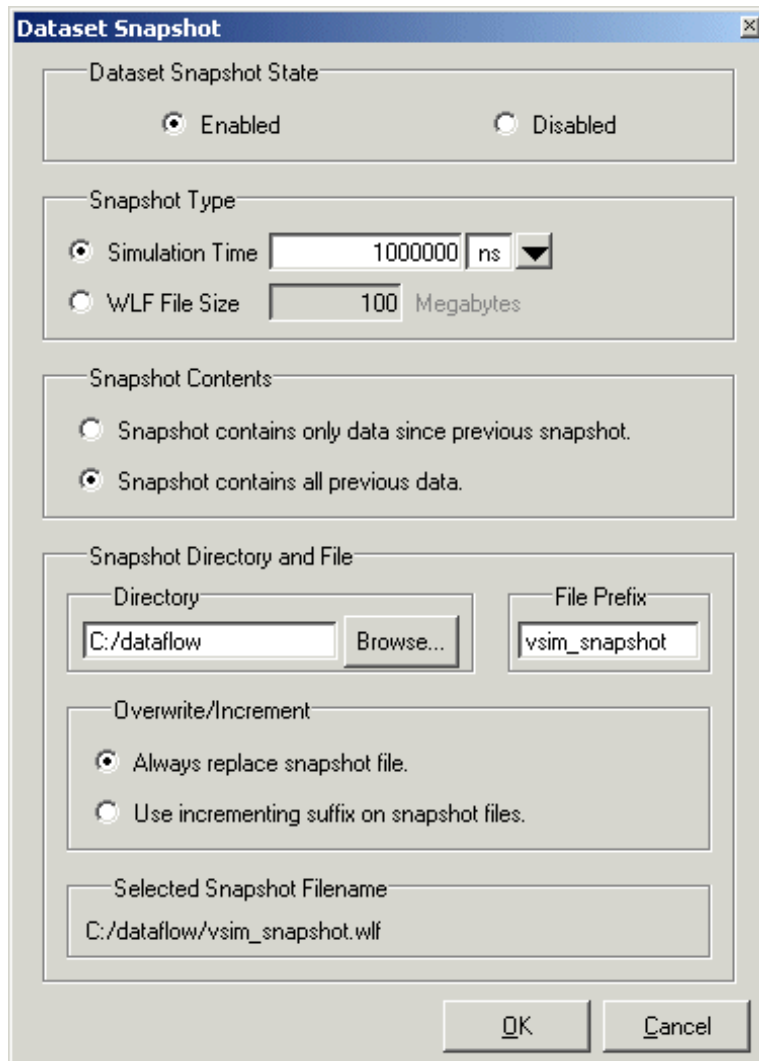
Additionally, you can prevent display of the dataset prefix by using the environment -nodataset command to view a dataset. To enable display of the prefix, use the [environment](#) -dataset command (note that you do not need to specify this command argument if the DisplayDatasetPrefix variable is set to 1). These arguments of the environment command override the value of the DisplayDatasetPrefix variable.

Saving at Intervals with Dataset Snapshot

Dataset Snapshot lets you periodically copy data from the current simulation WLF file to another file. This is useful for taking periodic "snapshots" of your simulation or for clearing the current simulation WLF file based on size or elapsed time.

Once you have logged the appropriate objects, select **Tools > Dataset Snapshot** (Wave window).

Figure 13-5. Dataset Snapshot Dialog



Collapsing Time and Delta Steps

By default ModelSim collapses delta steps. This means each logged signal that has events during a simulation delta has its final value recorded to the WLF file when the delta has expired. The event order in the WLF file matches the order of the first events of each signal.

You can configure how ModelSim collapses time and delta steps using arguments to the `vsim` command or by setting the `WLFCollapseMode` variable in the `modelsim.ini` file. The table below summarizes the arguments and how they affect event recording.

Table 13-3. vsim Arguments for Collapsing Time and Delta Steps

vsim argument	effect	modelsim.ini setting
-wfnocollapse	All events for each logged signal are recorded to the WLF file in the exact order they occur in the simulation.	WLFCollapseMode = 0
-wlfcollapsedelta	Each logged signal which has events during a simulation delta has its final value recorded to the WLF file when the delta has expired. Default.	WLFCollapseMode = 1
-wlfcollapsesttime	Same as delta collapsing but at the timestep granularity.	WLFCollapseMode = 2

When a run completes that includes single stepping or hitting a breakpoint, all events are flushed to the WLF file regardless of the time collapse mode. It's possible that single stepping through part of a simulation may yield a slightly different WLF file than just running over that piece of code. If particular detail is required in debugging, you should disable time collapsing.

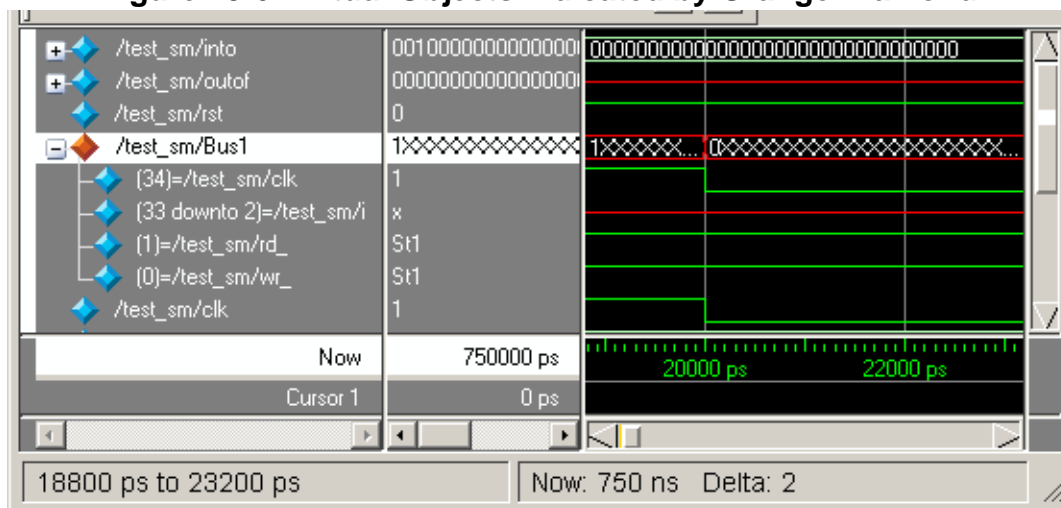
Virtual Objects

Virtual objects are signal-like or region-like objects created in the GUI that do not exist in the ModelSim simulation kernel. ModelSim supports the following kinds of virtual objects:

- [Virtual Signals](#)
- [Virtual Functions](#)
- [Virtual Regions](#)
- [Virtual Types](#)

Virtual objects are indicated by an orange diamond as illustrated by *bus* in [Figure 13-6](#):

Figure 13-6. Virtual Objects Indicated by Orange Diamond



Virtual Signals

Virtual signals are aliases for combinations or subelements of signals written to the WLF file by the simulation kernel. They can be displayed in the Objects, List, and Wave windows, accessed by the **examine** command, and set using the **force** command. You can create virtual signals using the **Wave or List > Combine Signals** menu selections or by using the [virtual signal](#) command. Once created, virtual signals can be dragged and dropped from the Objects pane to the Wave and List windows. In addition, you can create virtual signals for the Wave window using the Virtual Signal Builder (see [Creating a Virtual Signal](#)).

Virtual signals are automatically attached to the design region in the hierarchy that corresponds to the nearest common ancestor of all the elements of the virtual signal. The **virtual signal** command has an **-install <region>** option to specify where the virtual signal should be installed. This can be used to install the virtual signal in a user-defined region in order to reconstruct the original RTL hierarchy when simulating and driving a post-synthesis, gate-level implementation.

A virtual signal can be used to reconstruct RTL-level design buses that were broken down during synthesis. The [virtual hide](#) command can be used to hide the display of the broken-down bits if you don't want them cluttering up the Objects window.

If the virtual signal has elements from more than one WLF file, it will be automatically installed in the virtual region `virtuals:/Signals`.

Virtual signals are not hierarchical – if two virtual signals are concatenated to become a third virtual signal, the resulting virtual signal will be a concatenation of all the scalar elements of the first two virtual signals.

The definitions of virtuals can be saved to a macro file using the [virtual save](#) command. By default, when quitting, ModelSim will append any newly-created virtuals (that have not been saved) to the *virtuals.do* file in the local directory.

If you have virtual signals displayed in the Wave or List window when you save the Wave or List format, you will need to execute the *virtuals.do* file (or some other equivalent) to restore the virtual signal definitions before you re-load the Wave or List format during a later run. There is one exception: "implicit virtuals" are automatically saved with the Wave or List format.

Implicit and Explicit Virtuals

An implicit virtual is a virtual signal that was automatically created by ModelSim without your knowledge and without you providing a name for it. An example would be if you expand a bus in the Wave window, then drag one bit out of the bus to display it separately. That action creates a one-bit virtual signal whose definition is stored in a special location, and is not visible in the Objects pane or to the normal virtual commands.

All other virtual signals are considered "explicit virtuals".

Virtual Functions

Virtual functions behave in the GUI like signals but are not aliases of combinations or elements of signals logged by the kernel. They consist of logical operations on logged signals and can be dependent on simulation time. They can be displayed in the Objects, Wave, and List windows and accessed by the [examine](#) command, but cannot be set by the [force](#) command.

Examples of virtual functions include the following:

- a function defined as the inverse of a given signal
- a function defined as the exclusive-OR of two signals
- a function defined as a repetitive clock
- a function defined as "the rising edge of CLK delayed by 1.34 ns"

Virtual functions can also be used to convert signal types and map signal values.

The result type of a virtual function can be any of the types supported in the GUI expression syntax: integer, real, boolean, `std_logic`, `std_logic_vector`, and arrays and records of these types. Verilog types are converted to VHDL 9-state `std_logic` equivalents and Verilog net strengths are ignored.

Virtual functions can be created using the [virtual function](#) command.

Virtual functions are also implicitly created by ModelSim when referencing bit-selects or part-selects of Verilog registers in the GUI, or when expanding Verilog registers in the Objects,

Wave, or List window. This is necessary because referencing Verilog register elements requires an intermediate step of shifting and masking of the Verilog "vreg" data structure.

Virtual Regions

User-defined design hierarchy regions can be defined and attached to any existing design region or to the virtuals context tree. They can be used to reconstruct the RTL hierarchy in a gate-level design and to locate virtual signals. Thus, virtual signals and virtual regions can be used in a gate-level design to allow you to use the RTL test bench.

Virtual regions are created and attached using the [virtual region](#) command.

Virtual Types

User-defined enumerated types can be defined in order to display signal bit sequences as meaningful alphanumeric names. The virtual type is then used in a type conversion expression to convert a signal to values of the new type. When the converted signal is displayed in any of the windows, the value will be displayed as the enumeration string corresponding to the value of the original signal.

Virtual types are created using the [virtual type](#) command.

Chapter 14

Waveform Analysis

When your simulation finishes, you will often want to analyze waveforms to assess and debug your design. Designers typically use the Wave window for waveform analysis. However, you can also look at waveform data in a textual format in the List window.

To analyze waveforms in ModelSim, follow these steps:

1. Compile your files.
2. Load your design.
3. Add objects to the Wave or List window.

```
add wave <object_name>
add list <object_name>
```

4. Run the design.

Objects You Can View

The list below identifies the types of objects can be viewed in the Wave or List window. Refer to the section “[Using the WildcardFilter Preference Variable](#)” for information on controlling the information that is added to the Wave window when using wild cards.

- **VHDL objects** — (indicated by dark blue diamond in the Wave window)
signals, aliases, process variables, and shared variables
- **Verilog and SystemVerilog objects** — (indicated by light blue diamond in the Wave window)
nets, registers, variables, named events, and classes
- **SystemC objects** — (indicated by a green diamond in the Wave window)
primitive channels and ports
- **Virtual objects** — (indicated by an orange diamond in the Wave window)
virtual signals, buses, and functions, see; [Virtual Objects](#) for more information
- **Comparisons** — (indicated by a yellow triangle)
comparison regions and comparison signals; see [Waveform Compare](#) for more information

Wave Window Overview

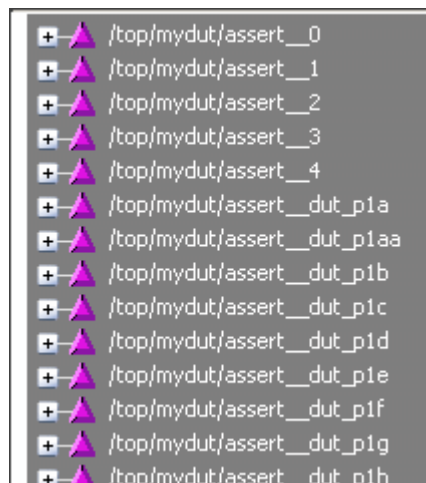
The Wave window opens in the Main window as shown [Figure 14-1](#). The window can be undocked from the main window by clicking the Undock button in the window header or by using the **view -undock wave** command. Setting the **PrefMain(ViewUndocked) wave** preference variable will change the default behavior so that the Wave window will open undocked each time you start ModelSim.

When the Wave window is docked in the Main window, all menus and icons that were in the undocked Wave window move into the Main window menu bar and toolbar.

Wave Window Panes

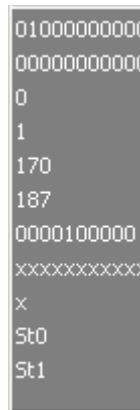
The Wave window is divided into a number of window panes. The Object Pathnames Pane displays object paths.

Figure 14-1. Wave Window Object Pathnames Pane



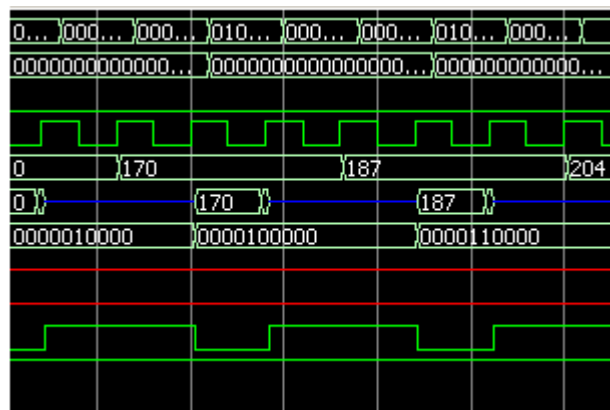
The Object Values Pane displays the value of each object in the pathnames pane at the time of the selected cursor.

Figure 14-2. Wave Window Object Values Pane



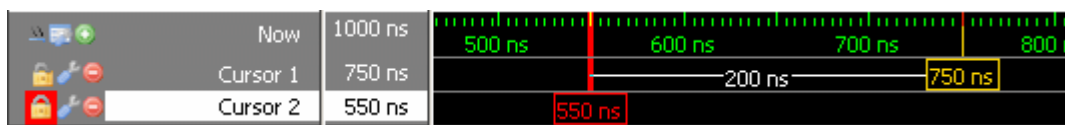
The Waveform Pane displays the object waveforms over the time of the simulation.

Figure 14-3. Wave Window Waveform Pane



The Cursor Pane displays cursor names, cursor values and the cursor locations on the timeline. This pane also includes a toolbox that gives you quick access to cursor and timeline features and configurations.

Figure 14-4. Wave Window Cursor Pane



All of these panes can be resized by clicking and dragging the bar between any two panes.

In addition to these panes, the Wave window also contains a Messages bar at the top of the window. The Messages bar contains indicators pointing to the times at which a message was output from the simulator.

Figure 14-5. Wave Window Messages Bar



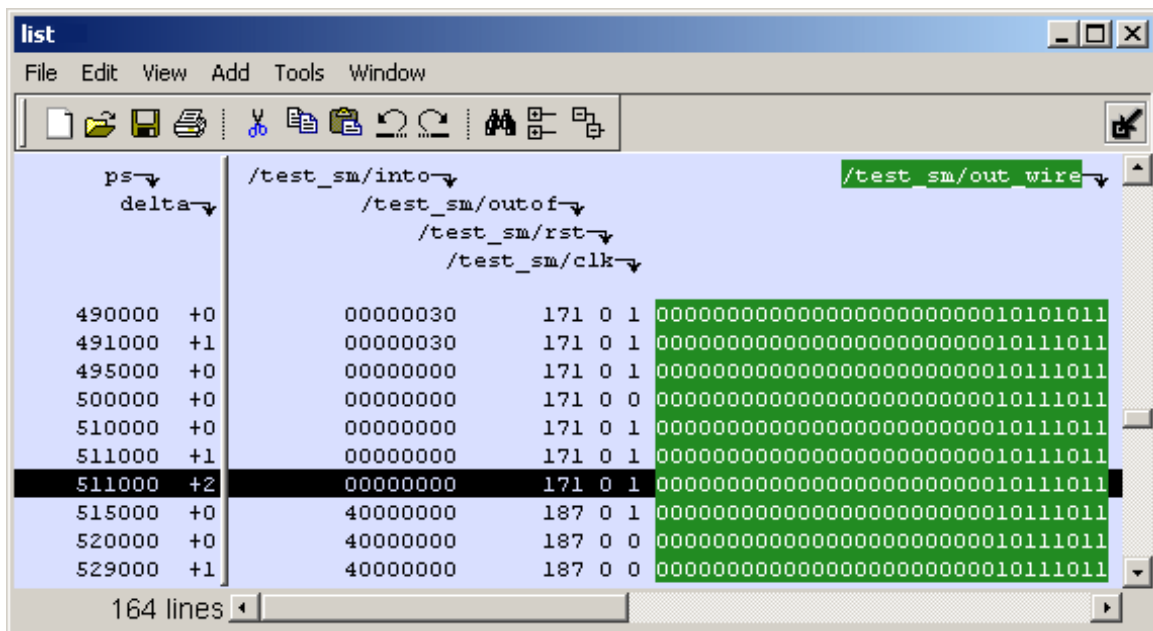
List Window Overview

The List window displays simulation results in tabular format. Common tasks that people use the window for include:

- Using gating expressions and trigger settings to focus in on particular signals or events. See [Configuring New Line Triggering in the List Window](#).
- Debugging delta delay issues. See [Delta Delays](#) for more information.

The window is divided into two adjustable panes, which allows you to scroll horizontally through the listing on the right, while keeping time and delta visible on the left.

Figure 14-6. Tabular Format of the List Window



Adding Objects to the Wave or List Window

You can add objects to the Wave or List window in several ways.

Adding Objects with Drag and Drop

You can drag and drop objects into the Wave or List window from the Structure, Processes, Memory, Objects, Source, or Locals windows. You can also drag objects from the Wave window to the List window and vice versa.

Select the objects in the first window, then drop them into the Wave window. Depending on what you select, all objects or any portion of the design can be added.

Adding Objects with Menu Selections

The **Add** menu in the Main window lets you add objects to the Wave window, List window, or Log file. You can also add objects using right-click popup menus. For example, if you want to add all signals in a design to the Wave window you can do one of the following:

- Right-click a design unit in a Structure (sim) window and select **Add > To Wave > All Items in Design** from the popup context menu.
- Right-click anywhere in the Objects window and select **Add > To Wave > Signals in Design** from the popup context menu.

Adding Objects with a Command

Use the [add list](#) or [add wave](#) commands to add objects from the command line. For example:

```
VSIM> add wave /proc/a
```

Adds signal */proc/a* to the Wave window.

```
VSIM> add list *
```

Adds all the objects in the current region to the List window.

```
VSIM> add wave -r /*
```

Adds all objects in the design to the Wave window.

Refer to the section [“Using the WildcardFilter Preference Variable”](#) for information on controlling the information that is added to the Wave window when using wild cards.

Adding Objects with a Window Format File

Select **File > Load** and specify a previously saved format file. See [Saving the Window Format](#) for details on how to create a format file.

Measuring Time with Cursors in the Wave Window

ModelSim uses cursors to measure time in the Wave window. Cursors extend a vertical line over the waveform display and identify a specific simulation time. Multiple cursors can be used to measure time intervals, as shown in the graphic below.

When the Wave window is first drawn it contains two cursors — the **Now** cursor, and **Cursor 1** (Figure 14-7).

Figure 14-7. Original Names of Wave Window Cursors



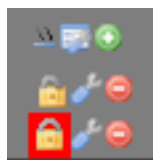
The **Now** cursor is always locked to the current simulation time and it is not manifested as a graphical object (vertical cursor bar) in the Wave window.

Cursor 1 is located at time zero. Clicking anywhere in the waveform display moves the **Cursor 1** vertical cursor bar to the mouse location and makes this cursor the selected cursor. The selected cursor is drawn as a bold solid line; all other cursors are drawn with thin lines.

Cursor and Timeline Toolbox

The Cursor and Timeline Toolbox on the left side of the cursor pane gives you quick access to cursor and timeline features.

Figure 14-8. Cursor and Timeline Toolbox



The action for each toolbox icon is shown in Table 14-1.

Table 14-1. Cursor and Timeline Toolbox Icons and Actions







Icon	Action
	Toggle short names <-> full names
	Edit grid and timeline properties
	Insert cursor

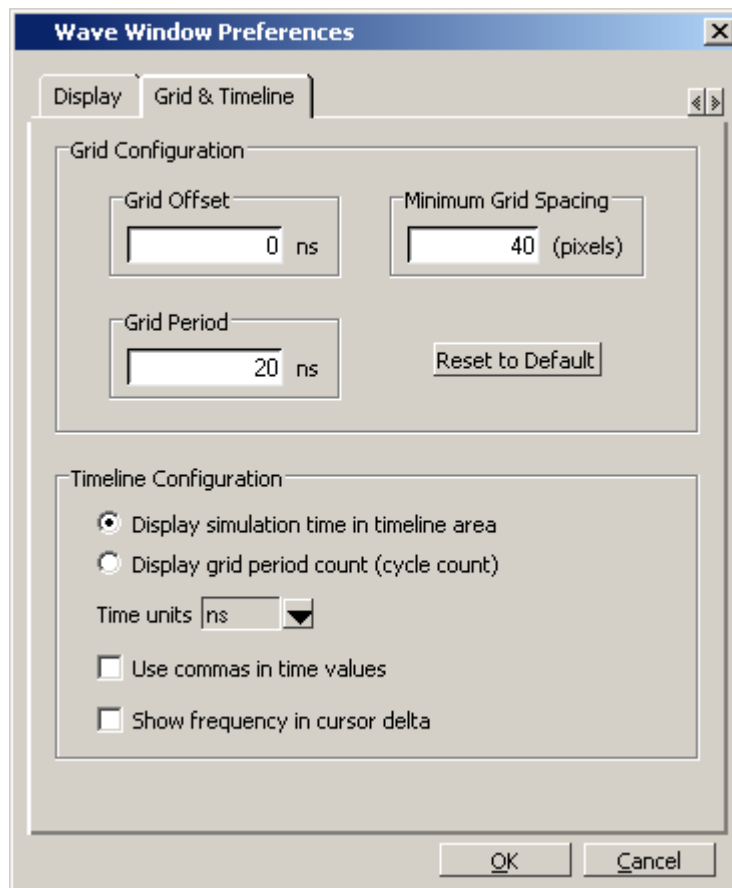
Table 14-1. Cursor and Timeline Toolbox Icons and Actions

Icon	Action
	Toggle lock on cursor to prevent it from moving
	Edit this cursor
	Remove this cursor

The **Toggle short names <-> full names** icon allows you to switch from displaying full pathnames (the default) in the Pathnames Pane to displaying short pathnames.

The **Edit grid and timeline properties** icon opens the Wave Window Properties dialog to the Grid & Timeline tab (Figure 14-9).

Figure 14-9. Grid and Timeline Properties



- The Grid Configuration selections allow you to set grid offset, minimum grid spacing, and grid period. You can also reset these grid configuration settings to their default values.

- The Timeline Configuration selections give you a user-definable time scale. You can display simulation time on a timeline or a clock cycle count. If you select Display simulation time in timeline area, use the Time Units dropdown list to select one of the following as the timeline unit:

fs, ps, ns, us, ms, sec, min, hr

Note

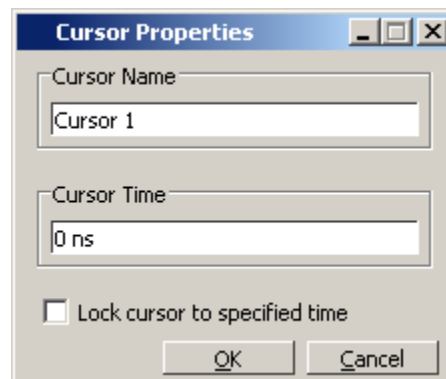

The time unit displayed in the Wave window does not affect the simulation time that is currently defined.

The current configuration is saved with the wave format file so you can restore it later.

- The **Show frequency in cursor delta** box causes the timeline to display the difference (delta) between adjacent cursors as frequency. By default, the timeline displays the delta between adjacent cursors as time.

To add cursors when the Wave window is active, click the Insert Cursor icon, or choose **Add > To Wave > Cursor** from the menu bar. Each added cursor is given a default cursor name (Cursor 2, Cursor 3, and so forth) which can be changed by simply right-clicking the cursor name, then typing in a new name, or by clicking the **Edit this cursor** icon. The Edit this cursor icon will open the Cursor Properties dialog (Figure 14-10), where you assign a cursor name and time. You can also lock the cursor to the specified time.

Figure 14-10. Cursor Properties Dialog Box






Working with Cursors

The table below summarizes common cursor actions.

Table 14-2. Actions for Cursors

Action	Menu command (Wave window docked)	Menu command (Wave window undocked)	Icon
Add cursor	Add > To Wave > Cursor	Add > Cursor	

Table 14-2. Actions for Cursors (cont.)

Action	Menu command (Wave window docked)	Menu command (Wave window undocked)	Icon
Edit cursor	Wave > Edit Cursor	Edit > Edit Cursor	
Delete cursor	Wave > Delete Cursor	Edit > Delete Cursor	
Zoom In on Active Cursor	Wave > Zoom > Zoom Cursor	View > Zoom > Zoom Cursor	NA
Lock cursor	Wave > Edit Cursor	Edit > Edit Cursor	
Select a cursor	Wave > Cursors	View > Cursors	NA

Shortcuts for Working with Cursors

There are a number of useful keyboard and mouse shortcuts related to the actions listed above:

- Select a cursor by clicking the cursor name.
- Jump to a hidden cursor (one that is out of view) by double-clicking the cursor name.
- Name a cursor by right-clicking the cursor name and entering a new value. Press <Enter> on your keyboard after you have typed the new name.
- Move a locked cursor by holding down the <shift> key and then clicking-and-dragging the cursor.
- Move a cursor to a particular time by right-clicking the cursor value and typing the value to which you want to scroll. Press <Enter> on your keyboard after you have typed the new value.

Understanding Cursor Behavior

The following list describes how cursors behave when you click in various panes of the Wave window:

- If you click in the waveform pane, the closest unlocked cursor to the mouse position is selected and then moved to the mouse position.
- Clicking in a horizontal track in the cursor pane selects that cursor and moves it to the mouse position.
- Cursors snap to the nearest waveform edge to the left if you click or drag a cursor along the selected waveform to within ten pixels of a waveform edge. You can set the snap distance in the Display tab of the Window Preferences dialog. Select **Tools > Options > Wave Preferences** when the Wave window is docked in the Main window MDI frame.

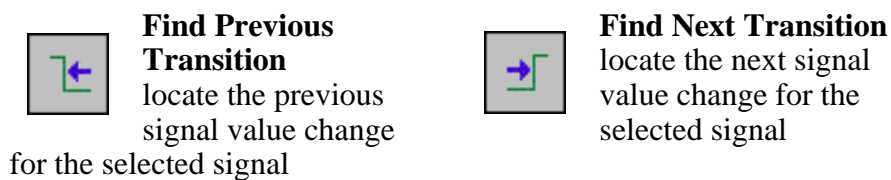
Select **Tools > Window Preferences** when the Wave window is a stand-alone, undocked window.

- You can position a cursor without snapping by dragging in the cursor pane below the waveforms.

Jumping to a Signal Transition

You can move the active (selected) cursor to the next or previous transition on the selected signal using these two toolbar icons shown in [Figure 14-11](#).

Figure 14-11. Find Previous and Next Transition Icons

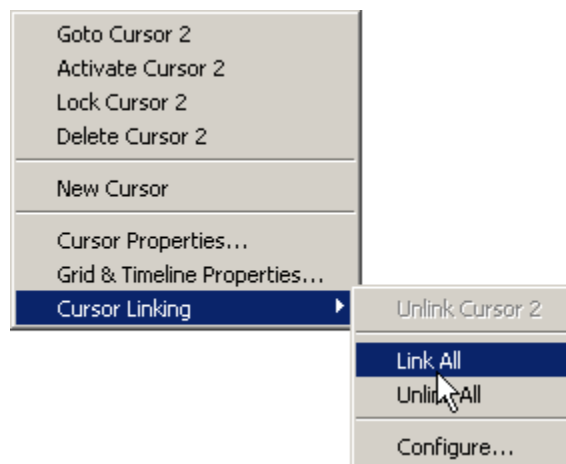


These actions will not work on locked cursors.

Linking Cursors

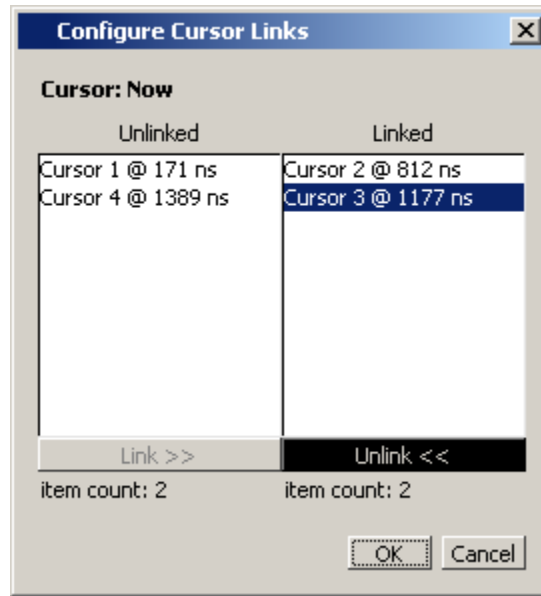
Cursors within the Wave window can be linked together, allowing you to move two or more cursors together across the simulation timeline. You simply click one of the linked cursors and drag it left or right on the timeline. The other linked cursors will move by the same amount of time. You can link all displayed cursors by right-clicking the time value of any cursor in the timeline, as shown in [Figure 14-12](#), and selecting **Cursor Linking > Link All**.

Figure 14-12. Cursor Linking Menu



You can link and unlink selected cursors by selecting **Cursor Linking > Configure** to open the **Configure Cursor Links** dialog ([Figure 14-13](#)).

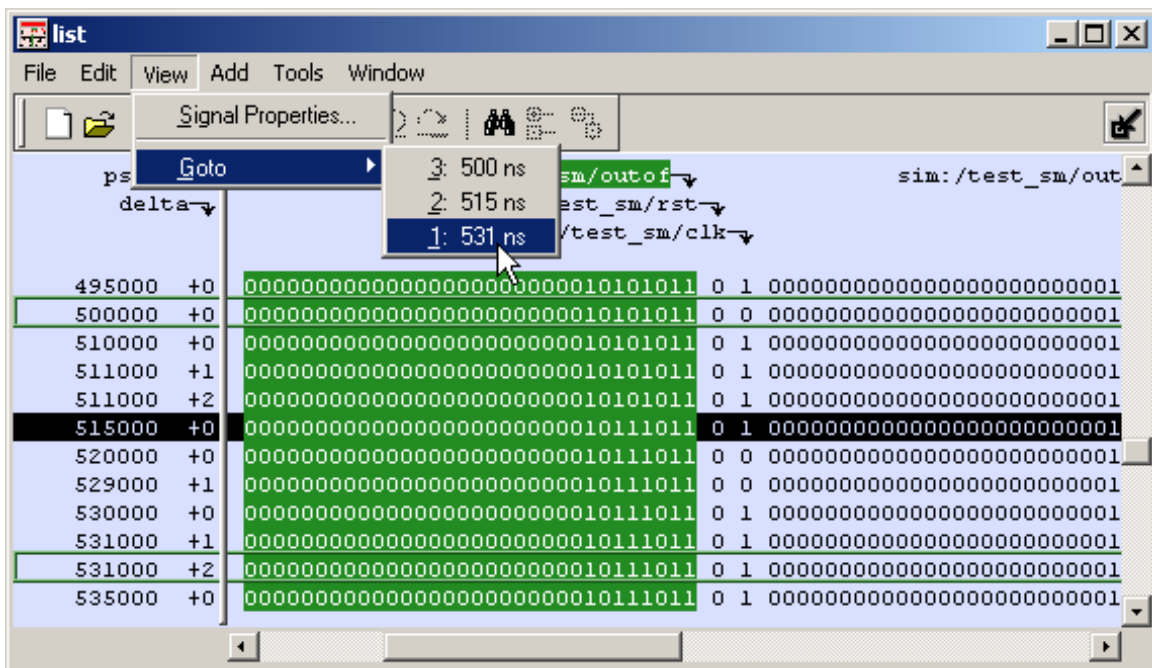
Figure 14-13. Configure Cursor Links Dialog



Setting Time Markers in the List Window

Time markers in the List window are similar to cursors in the Wave window. Time markers tag lines in the data table so you can quickly jump back to that time. Markers are indicated by a thin box surrounding the marked line.

Figure 14-14. Time Markers in the List Window



Working with Markers

The table below summarizes actions you can take with markers.

Table 14-3. Actions for Time Markers

Action	Method
Add marker	Select a line and then select List > Add Marker
Delete marker	Select a tagged line and then select List > Delete Marker
Goto marker	Select View > Goto > <time> (only available when undocked)

Expanded Time in the Wave and List Windows

When analyzing a design using ModelSim, you can see a value for each object at any time step in the simulation. If logged in the *.wlf* file, the values at any time step prior to and including the current simulation time are displayed in the Wave and List windows or by using the [examine](#) command.

Some objects can change values more than once in a given time step. These intermediate values are of interest when debugging glitches on clocked objects or race conditions. With a few exceptions (viewing delta time steps with the List window and [examine](#) command), the values prior to the final value in a given time step cannot be observed.

The expanded time function makes these intermediate values visible in the Wave window. Expanded time shows the actual order in which objects change values and shows all transitions of each object within a given time step.

Expanded Time Terminology

- **Simulation Time** — the basic time step of the simulation. The final value of each object at each simulation time is what is displayed by default in the Wave window.
- **Delta Time** — the time intervals or steps taken to evaluate the design without advancing simulation time. Object values at each delta time step are viewed in the List window or by using the `-delta` argument of the [examine](#) command. Refer to [Delta Delays](#) for more information.
- **Event Time** — the time intervals that show each object value change as a separate event and that shows the relative order in which these changes occur

During a simulation, events on different objects in a design occur in a particular order or sequence. Typically, this order is not important and only the final value of each object for each simulation time step is important. However, in situations like debugging glitches on clocked objects or race conditions, the order of events is important. Unlike simulation time steps and delta time steps, only one object can have a single value

change at any one event time. Object values and the exact order which they change can be saved in the *.wlf* file.

- **Expanded Time** — the Wave window feature that expands single simulation time steps to make them wider, allowing you to see object values at the end of each delta cycle or at each event time within the simulation time.
- **Expand** — causes the normal simulation time view in the Wave window to show additional detailed information about when events occurred during a simulation.
- **Collapse** — hides the additional detailed information in the Wave window about when events occurred during a simulation.

Recording Expanded Time Information

You can use the `vsim` command, or the `WLFCollapseMode` variable in the *modelsim.ini* file, to control recording of expanded time information in the *.wlf* file.

Table 14-4. Recording Delta and Event Time Information

vsim command argument	modelsim.ini setting	effect
<code>-wlfnocollapse</code>	<code>WLFCollapseMode = 0</code>	All events for each logged signal are recorded to the <i>.wlf</i> file in the exact order they occur in the simulation.
<code>-wlfcollapsedelta</code>	<code>WLFCollapseMode = 1</code> (Default)	Each logged signal that has events during a simulation delta has its final value recorded in the <i>.wlf</i> file when the delta has expired.
<code>-wlfcollapsestime</code>	<code>WLFCollapseMode = 2</code>	Similar to delta collapsing but at the simulation time step granularity.

Recording Delta Time

Delta time information is recorded in the *.wlf* file using the `-wlfcollapsedelta` argument of `vsim` or by setting the `WLFCollapseMode` *modelsim.ini* variable to 1. This is the default behavior.

Recording Event Time

To save multiple value changes of an object during a single time step or single delta cycle, use the `-wlfnocollapse` argument with `vsim`, or set `WLFCollapseMode` to 0. Unlike delta times (which are explicitly saved in the *.wlf* file), event time information exists implicitly in the *.wlf* file. That is, the order in which events occur in the simulation is the same order in which they are logged to the *.wlf* file, but explicit event time values are not logged.

Choosing Not to Record Delta or Event Time

You can choose not to record event time or delta time information to the *.wlf* file by using the **-wlfcollapse** argument with `vsim`, or by setting `WLFCollapseMode` to 2. This will prevent detailed debugging but may reduce the size of the *.wlf* file and speed up the simulation.

Viewing Expanded Time Information in the Wave Window

Expanded time information is displayed in the Wave window toolbar, the right portion of the Messages bar, the Waveform pane, the time axis portion of the Cursor pane, and the Waveform pane horizontal scroll bar as described below.

- **Expanded Time Toolbar** — The Expanded Time toolbar can (optionally) be displayed in the toolbar area of the undocked Wave window or the toolbar area of the Main window when the Wave window is docked. It contains three exclusive toggle buttons for selecting the Expanded Time mode (see [Toolbar Selections for Expanded Time Modes](#)) and four buttons for expanding and collapsing simulation time.
- **Messages Bar** — The right portion of the Messages Bar is scaled horizontally to align properly with the Waveform pane and the time axis portion of the Cursor pane.
- **Waveform Pane Horizontal Scroll Bar** — The position and size of the thumb in the Waveform pane horizontal scroll bar is adjusted to correctly reflect the current state of the Waveform pane and the time axis portion of the Cursor pane.
- **Waveform Pane and the Time Axis Portion of the Cursor Pane** — By default, the Expanded Time is off and simulation time is collapsed for the entire time range in the Waveform pane. When the Delta Time mode is selected (see [Recording Delta Time](#)), simulation time remains collapsed for the entire time range in the Waveform pane. A red dot is displayed in the middle of all waveforms at any simulation time where multiple value changes were logged for that object.

[Figure 14-15](#) illustrates the appearance of the Waveform pane when viewing collapsed event time or delta time. It shows a simulation with three signals, *s1*, *s2*, and *s3*. The red dots indicate multiple transitions for *s1* and *s2* at simulation time 3ns.

Figure 14-15. Waveform Pane with Collapsed Event and Delta Time

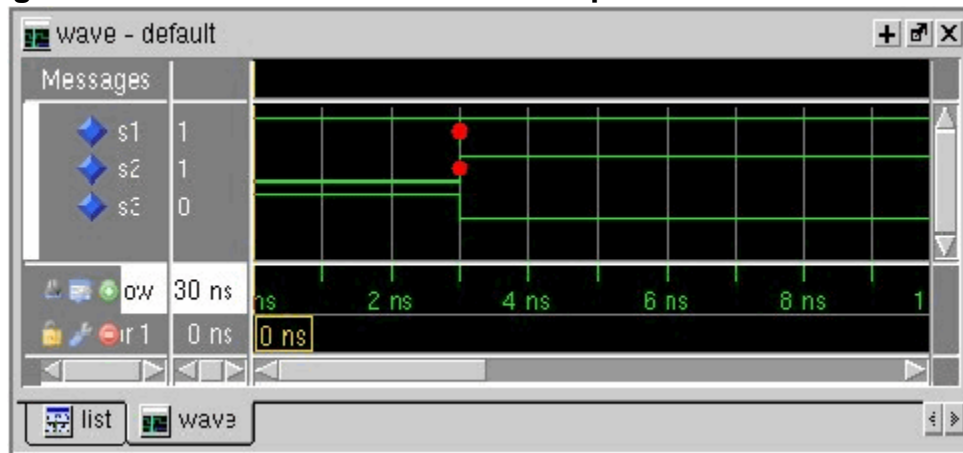
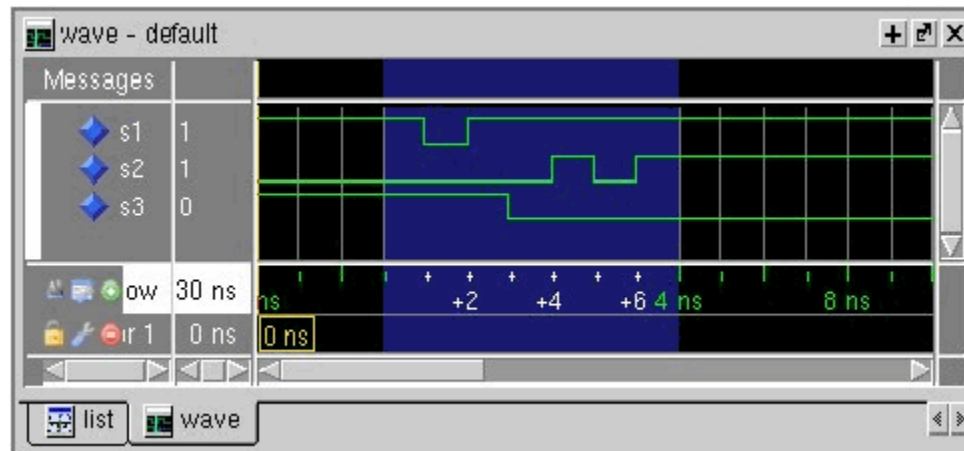


Figure 14-16 shows the Waveform pane and the timescale from the Cursors pane after expanding simulation time at time 3ns. The background color is blue for expanded sections in Delta Time mode and green for expanded sections in Event Time mode.

Figure 14-16. Waveform Pane with Expanded Time at a Specific Time



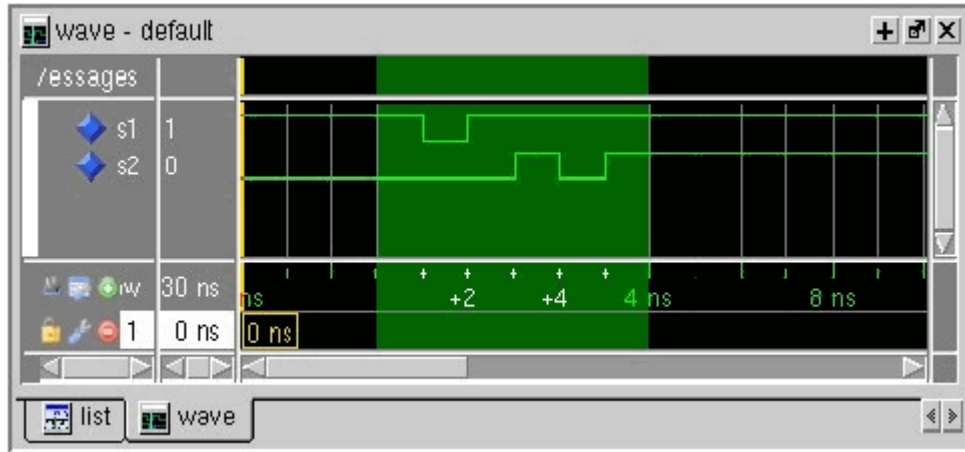
In Delta Time mode, more than one object may have an event at the same delta time step. The labels on the time axis in the expanded section indicate the delta time steps within the given simulation time.

In Event Time mode, only one object may have an event at a given event time. The exception to this is for objects that are treated atomically in the simulator and logged atomically. The individual bits of a SystemC vector, for example, could change at the same event time.

Labels on the time axis in the expanded section indicate the order of events from all of the objects added to the Waveform panes. If an object that had an event at a particular time but it is not in the viewable area of the Waveform panes, then there will appear to be no events at that time.

Depending on which objects have been added to the Wave window, a specific event may happen at a different event time. For example, if s3 shown in Figure 14-16, had not been added to the Wave window, the result would be as shown in Figure 14-17.

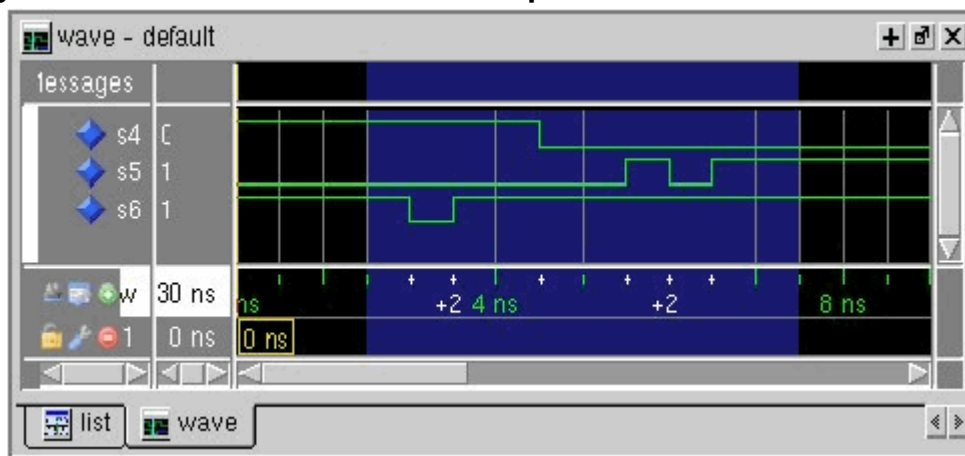
Figure 14-17. Waveform Pane with Event Not Logged



Now the first event on s2 occurs at event time $3\text{ns} + 2$ instead of event time $3\text{ns} + 3$. If s3 had been added to the Wave window (whether shown in the viewable part of the window or not) but was not visible, the event on s2 would still be at $3\text{ns} + 3$, with no event visible at $3\text{ns} + 2$.

Figure 14-18 shows an example of expanded time over the range from 3 ns to 5 ns. The expanded time range displays delta times as indicated by the blue background color. (If Event Time mode is selected, a green background is displayed.)

Figure 14-18. Waveform Pane with Expanded Time Over a Time Range



When scrolling horizontally, expanded sections remain expanded until you collapse them, even when scrolled out of the visible area. The left or right edges of the Waveform pane are viewed in either expanded or collapsed sections.

Expanded event order or delta time sections appears in all panes when multiple Waveform panes exist for a Wave window. When multiple Wave windows are used, sections of expanded event or delta time are specific to the Wave window where they were created.

For expanded event order time sections when multiple datasets are loaded, the event order time of an event will indicate the order of that event relative to all other events for objects added to that Wave window for that object's dataset only. That means, for example, that signal sim:s1 and gold:s2 could both have events at time 1ns+3.

Note

The order of events for a given design will differ for optimized versus unoptimized simulations, and between different versions of ModelSim. The order of events will be consistent between the Wave window and the List window for a given simulation of a particular design, but the event numbering may differ. See [Expanded Time Viewing in the List Window](#).

You may display any number of disjoint expanded times or expanded ranges of times.

Customizing the Expanded Time Wave Window Display

As noted above, the Wave window background color is blue instead of black for expanded sections in Delta Time mode and green for expanded sections in Event Time mode.

The background colors for sections of expanded event time are changed as follows:

1. Select **Tools > Edit Preferences** from the menus. This opens the Preferences dialog.
2. Select the By Name tab.
3. Scroll down to the Wave selection and click the plus sign (+) for Wave.
4. Change the values of the Wave Window variables waveDeltaBackground and waveEventBackground.

Selecting the Expanded Time Display Mode

There are three Wave window expanded time display modes: Event Time mode, Delta Time mode, and Expanded Time off. These display modes are initiated by menu selections, toolbar selections, or via the command line.

Menu Selections for Expanded Time Display Modes

Table 14-5 shows the menu selections for initiating expanded time display modes.

Table 14-5. Menu Selections for Expanded Time Display Modes

action	menu selection with Wave window docked or undocked
select Delta Time mode	docked: Wave > Expanded Time > Delta Time Mode undocked: View > Expanded Time > Delta Time Mode
select Event Time mode	docked: Wave > Expanded Time > Event Time Mode undocked: View > Expanded Time > Event Time Mode
disable Expanded Time	docked: Wave > Expanded Time > Expanded Time Off undocked: View > Expanded Time > Expanded Time Off

Select Delta Time Mode or Event Time Mode from the appropriate menu according to Table 14-5 to have expanded simulation time in the Wave window show delta time steps or event time steps respectively. Select Expanded Time Off for standard behavior (which is the default).

Toolbar Selections for Expanded Time Modes

There are three exclusive toggle buttons in the [Wave Expand Time Toolbar](#) for selecting the time mode used to display expanded simulation time in the Wave window.

- The "Expanded Time Deltas Mode" button displays delta time steps.
- The "Expanded Time Events Mode" button displays event time steps.
- The "Expanded Time Off" button turns off the expanded time display in the Wave window.

Clicking any one of these buttons on toggles the other buttons off. This serves as an immediate visual indication about which of the three modes is currently being used. Choosing one of these modes from the menu bar or command line also results in the appropriate resetting of these three buttons. The "Expanded Time Off" button is selected by default.

In addition, there are four buttons in the [Wave Expand Time Toolbar](#) for expanding and collapsing simulation time.

- The "Expand All Time" button expands simulation time over the entire simulation time range, from time 0 to the current simulation time.
- The "Expand Time At Active Cursor" button expands simulation time at the simulation time of the active cursor.
- The "Collapse All Time" button collapses simulation time over entire simulation time range.

- The “Collapse Time At Active Cursor” button collapses simulation time at the simulation time of the active cursor.

Command Selection of Expanded Time Mode

The command syntax for selecting the time mode used to display objects in the Wave window is:

wave expand mode [-window <win>] none | deltas | events

Use the wave expand mode command to select which mode is used to display expanded time in the wave window. This command also results in the appropriate resetting of the three toolbar buttons.

Switching Between Time Modes

If one or more simulation time steps have already been expanded to view event time or delta time, then toggling the Time mode by any means will cause all of those time steps to be redisplayed in the newly selected mode.

Expanding and Collapsing Simulation Time

Simulation time may be expanded to view delta time steps or event time steps at a single simulation time or over a range of simulation times. Simulation time may be collapsed to hide delta time steps or event time steps at a single simulation time or over a range of simulation times. You can expand or collapse the simulation time with menu selections, toolbar selections, via commands, or with the mouse cursor.

- Expanding/Collapsing Simulation Time with Menu Selections — Select **Wave > Expanded Time** when the Wave window is docked, and **View > Expanded Time** when the Wave window is undocked. You can expand/collapse over the full simulation time range, over a specified time range, or at the time of the active cursor,.
- Expanding/Collapsing Simulation Time with Toolbar Selections — There are four buttons in the toolbar for expanding and collapsing simulation time in the Wave window: Expand Full, Expand Cursor, Collapse Full, and Collapse Cursor.
- Expanding/Collapsing Simulation Time with Commands — There are six commands for expanding and collapsing simulation time in the Wave window.

wave expand all

wave expand range

wave expand cursor

wave collapse all

wave collapse range

wave collapse cursor

These commands have the same behavior as the corresponding menu and toolbar selections. If valid times are not specified, for [wave expand range](#) or [wave collapse range](#), no action is taken. These commands effect all Waveform panes in the Wave window to which the command applies.

Expanded Time Viewing in the List Window

Event time may be shown in the List window in the same manner as delta time by using the **-delta events** option with the [configure list](#) command.

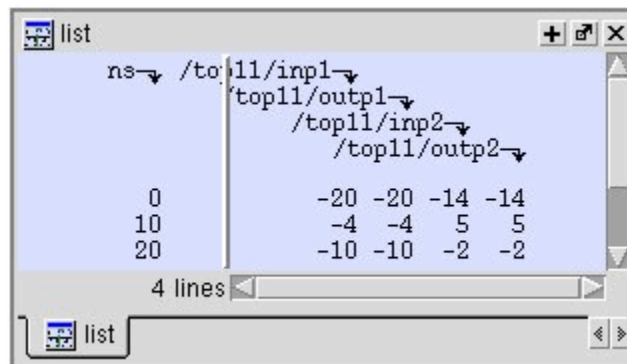
When the List window displays event times, the event time is relative to events on other signals also displayed in the List window. This may be misleading, as it may not correspond to event times displayed in the Wave window for the same events if different signals are added to the Wave and List windows.

The [write list](#) command (when used after the [configure list -delta events](#) command) writes a list file in tabular format with a line for every event. Please note that this is different from the [write list -events](#) command, which writes a non-tabular file using a print-on-change format.

The following examples illustrate the appearance of the List window and the corresponding text file written with the [write list](#) command after various options for the [configure list -delta](#) command are used.

[Figure 14-19](#) shows the appearance of the List window after the [configure list -delta none](#) command is used. It corresponds to the file resulting from the [write list](#) command. No column is shown for deltas or events.

Figure 14-19. List Window After write list -delta none Option is Used



[Figure 14-20](#) shows the appearance of the List window after the [configure list -delta collapse](#) command is used. It corresponds to the file resulting from the [write list](#) command. There is a column for delta time and only the final delta value and the final value for each signal for each simulation time step (at which any events have occurred) is shown.

Figure 14-20. List Window After write list -delta collapse Option is Used

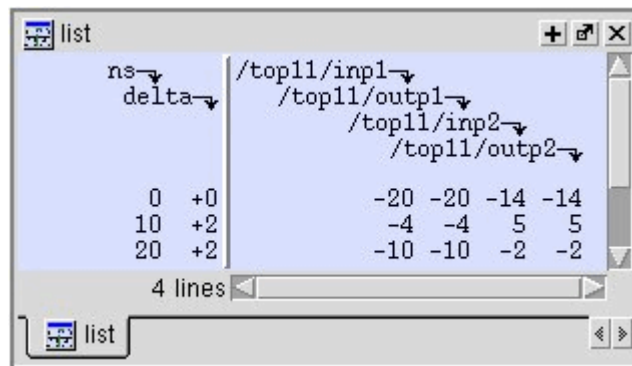


Figure 14-21 shows the appearance of the List window after the `configure list -delta all` option is used. It corresponds to the file resulting from the `write list` command. There is a column for delta time, and each delta time step value is shown on a separate line along with the final value for each signal for that delta time step.

Figure 14-21. List Window After write list -delta all Option is Used

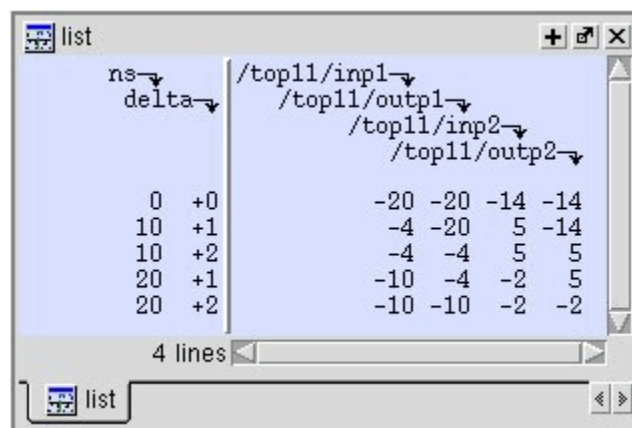
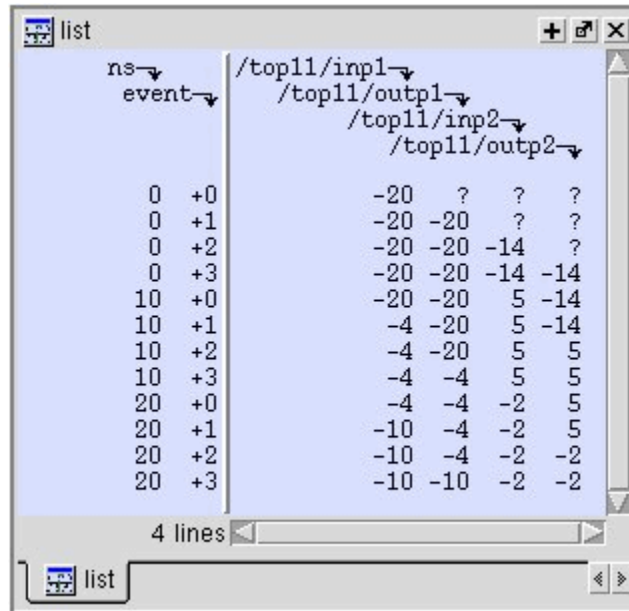


Figure 14-22 shows the appearance of the List window after the `configure list -delta events` command is used. It corresponds to the file resulting from the `write list` command. There is a column for event time, and each event time step value is shown on a separate line along with the final value for each signal for that event time step. Since each event corresponds to a new event time step, only one signal will change values between two consecutive lines.

Figure 14-22. List Window After write list -event Option is Used








Zooming the Wave Window Display

Zooming lets you change the simulation range in the waveform pane. You can zoom using the context menu, toolbar buttons, mouse, keyboard, or commands.

Zooming with the Menu, Toolbar and Mouse

You can access Zoom commands from the **View** menu in the Wave window when it is undocked, from the **Wave > Zoom** menu selections in the Main window when the Wave window is docked, or by clicking the right mouse button in the waveform pane of the Wave window.

These zoom buttons are available on the toolbar:

- | | |
|---|---|
|  <p>Zoom In 2x
zoom in by a factor of two from the current view</p> |  <p>Zoom Out 2x
zoom out by a factor of two from current view</p> |
|  <p>Zoom In on Active Cursor
centers the active cursor in the waveform display and zooms in</p> |  <p>Zoom Full
zoom out to view the full range of the simulation from time 0 to the current time</p> |
|  <p>Zoom Mode
change mouse pointer to zoom mode; see below</p> | |

To zoom with the mouse, first enter zoom mode by selecting **View > Zoom > Mouse Mode > Zoom Mode**. The left mouse button then offers 3 zoom options by clicking and dragging in different directions:

- Down-Right *or* Down-Left: Zoom Area (In)
- Up-Right: Zoom Out
- Up-Left: Zoom Fit

Also note the following about zooming with the mouse:

- The zoom amount is displayed at the mouse cursor. A zoom operation must be more than 10 pixels to activate.
- You can enter zoom mode temporarily by holding the <Ctrl> key down while in select mode.
- With the mouse in the Select Mode, the middle mouse button will perform the above zoom operations.

To zoom with your the scroll-wheel of your mouse, hold down the ctrl key at the same time to scroll in and out. The waveform pane will zoom in and out, centering on your mouse cursor

Saving Zoom Range and Scroll Position with Bookmarks

Bookmarks save a particular zoom range and scroll position. This lets you return easily to a specific view later. You save the bookmark with a name and then access the named bookmark from the Bookmark menu. Bookmarks are saved in the Wave format file (see [Adding Objects with a Window Format File](#)) and are restored when the format file is read.

Managing Bookmarks

The table below summarizes actions you can take with bookmarks.

Table 14-6. Actions for Bookmarks

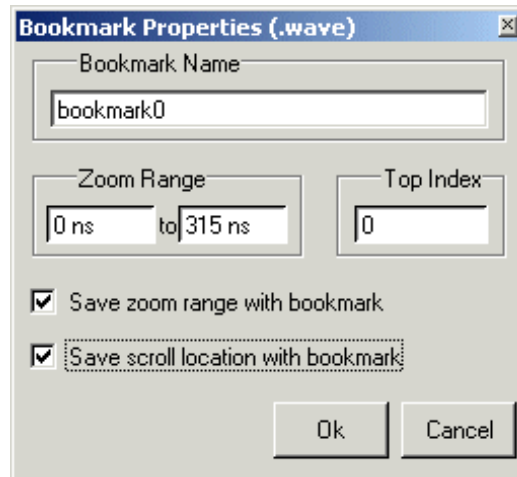
Action	Menu commands (Wave window docked)	Menu commands (Wave window undocked)	Command
Add bookmark	Add > To Wave > Bookmark	Add > Bookmark	bookmark add wave
View bookmark	Wave > Bookmarks > <bookmark_name>	View > Bookmarks > <bookmark_name>	bookmark goto wave
Delete bookmark	Wave > Bookmarks > Bookmarks > <select bookmark then Delete>	View > Bookmarks > Bookmarks > <select bookmark then Delete>	bookmark delete wave

Adding Bookmarks

To add a bookmark, follow these steps:

1. Zoom the Wave window as you see fit using one of the techniques discussed in [Zooming the Wave Window Display](#).
2. If the Wave window is docked, select **Add > Wave > Bookmark**. If the Wave window is undocked, select **Add > Bookmark**.

Figure 14-23. Bookmark Properties Dialog



3. Give the bookmark a name and click OK.

Editing Bookmarks

Once a bookmark exists, you can change its properties by selecting **Wave > Bookmarks > Bookmarks** if the Wave window is docked; or by selecting **Tools > Bookmarks** if the Wave window is undocked.

Searching in the Wave and List Windows

The Wave and List windows provide two methods for locating objects:

- Finding signal names – Select **Edit > Find**, click the Find toolbar button, or use the [find](#) command to search for the name of a signal.
- Search for values or transitions – Select **Edit > Signal Search**, click the Find toolbar button, or use the [search](#) command to locate transitions or signal values. The search feature is not available in all versions of ModelSim.

Wave window searches can be stopped by clicking the “Stop Wave Drawing” or “Break” toolbar buttons.

Finding Signal Names

The Find command is used to locate a signal name or value in the Wave or List window. When you select **Edit > Find**, the Find dialog appears.

Figure 14-24. Find Signals by Name or Value



One option of note is the **Exact** checkbox. Check **Exact** if you only want to find objects that match your search exactly. For example, searching for "clk" without **Exact** will find */top/clk* and *clk1*.

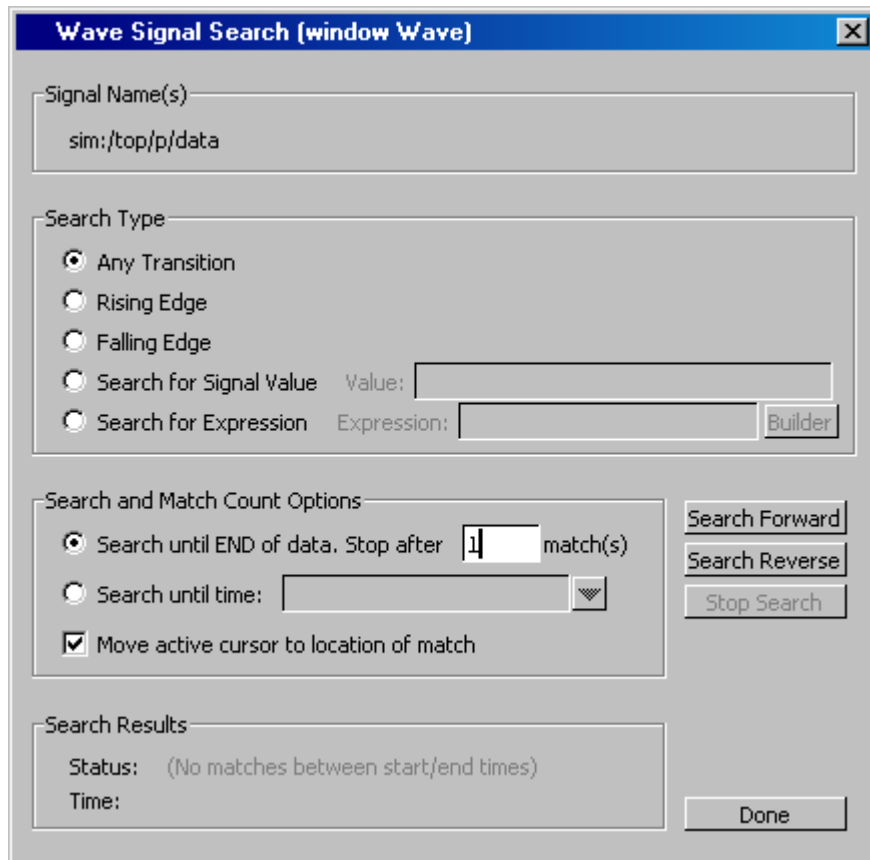
There are two differences between the Wave and List windows as it relates to the Find feature:

- In the Wave window you can specify a value to search for in the values pane.
- The find operation works only within the active pane in the Wave window.

Searching for Values or Transitions

The search command lets you search for transitions or values on selected signals. When you select **Edit > Signal Search**, the Signal Search dialog ([Figure 14-25](#)) appears.

Figure 14-25. Wave Signal Search Dialog



One option of note is **Search for Expression**. The expression can involve more than one signal but is limited to signals currently in the window. Expressions can include constants, variables, and DO files. See [Expression Syntax](#) for more information.

Note



If your signal values are displayed in binary radix, see [Searching for Binary Signal Values in the GUI](#) for details on how signal values are mapped between a binary radix and std_logic.

Using the Expression Builder for Expression Searches

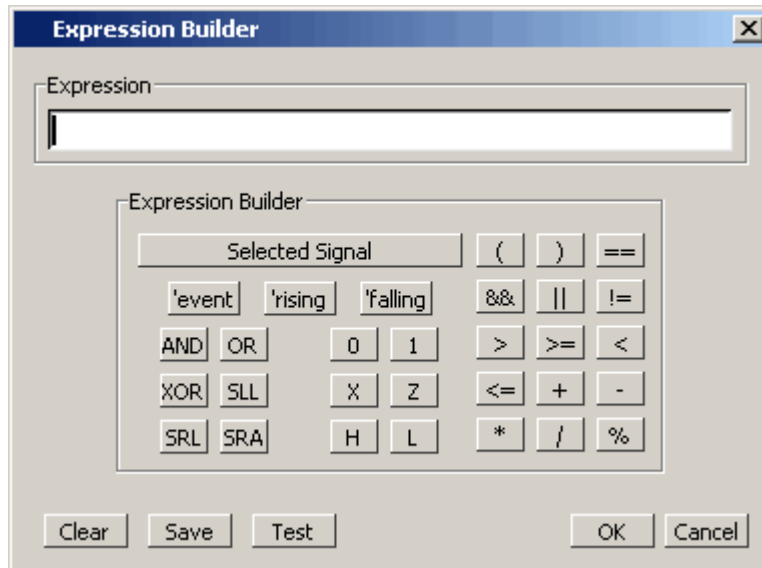
The Expression Builder is a feature of the Wave and List Signal Search dialog boxes and the List trigger properties dialog box. You can use it to create a search expression that follows the [GUI_expression_format](#).

To display the Expression Builder dialog box, do the following:

1. Choose **Edit > Signal Search...** from the main menu. This displays the Wave Signal Search dialog box.

2. Select **Search for Expression**.
3. Click the **Builder** button. This displays the Expression Builder dialog box shown in [Figure 14-26](#)

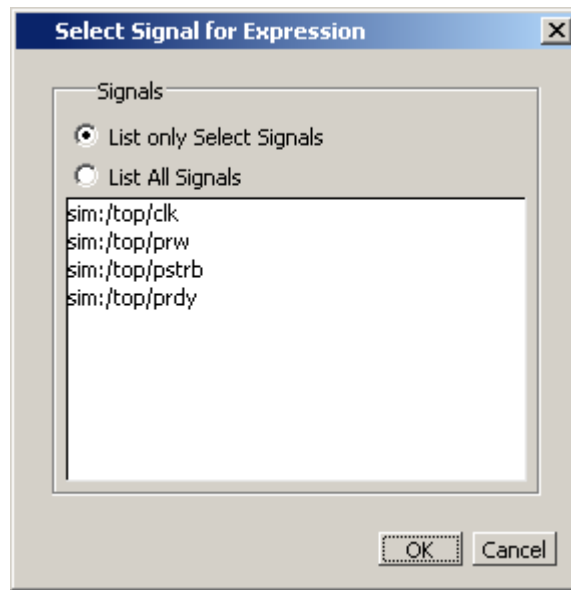
Figure 14-26. Expression Builder Dialog Box



You click the buttons in the Expression Builder dialog box to create a GUI expression. Each button generates a corresponding element of [Expression Syntax](#) and is displayed in the [Expression field](#). In addition, you can use the **Selected Signal** button to create an expression from signals you select from the associated Wave or List window.

For example, instead of typing in a signal name, you can select signals in a Wave or List window and then click **Selected Signal** in the Expression Builder. This displays the Select Signal for Expression dialog box shown in [Figure 14-27](#).

Figure 14-27. Selecting Signals for Expression Builder



Note that the buttons in this dialog box allow you to determine the display of signals you want to put into an expression:

- List only Select Signals — list only those signals that are currently selected in the parent window.
- List All Signals — list all signals currently available in the parent window.

Once you have selected the signals you want displayed in the Expression Builder, click OK.

Saving an Expression to a Tcl Variable

Clicking the **Save** button will save the expression to a Tcl variable. Once saved this variable can be used in place of the expression. For example, say you save an expression to the variable "foo." Here are some operations you could do with the saved variable:

- Read the value of *foo* with the set command:

```
set foo
```

- Put \$foo in the Expression: entry box for the Search for Expression selection.
- Issue a searchlog command using foo:

```
searchlog -expr $foo 0
```

Searching for when a Signal Reaches a Particular Value

Select the signal in the Wave window and click **Insert Selected Signal** and ==. Then, click the value buttons or type a value.

Evaluating Only on Clock Edges

Click the **&&** button to AND this condition with the rest of the expression. Then select the clock in the Wave window and click **Insert Selected Signal** and **'rising**. You can also select the falling edge or both edges.

Operators

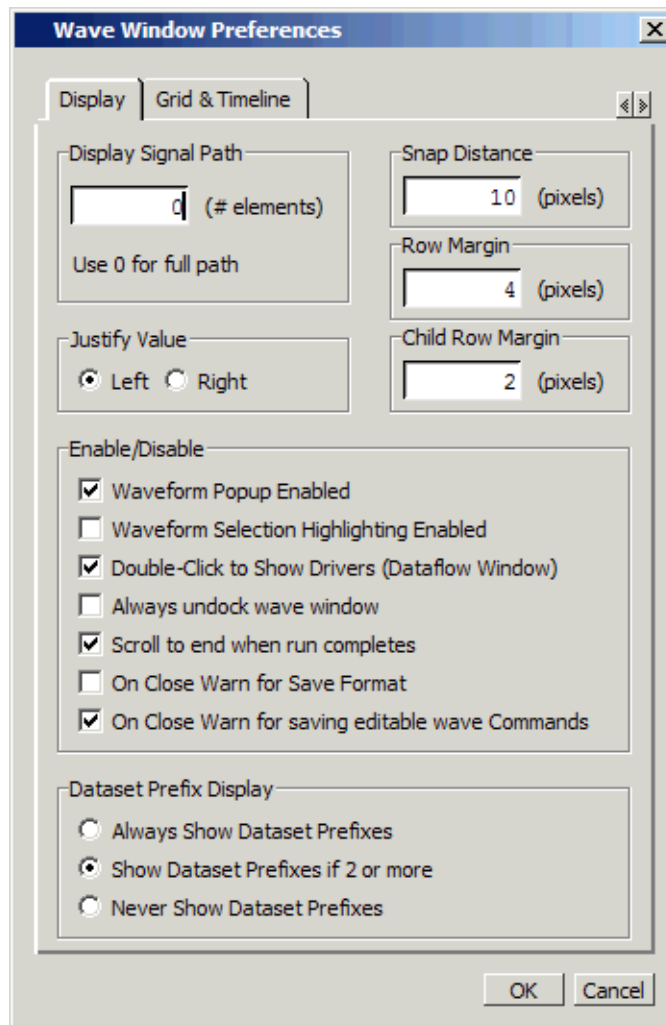
Other buttons will add operators of various kinds (see [Expression Syntax](#)), or you can type them in.

Formatting the Wave Window

Setting Wave Window Display Preferences

You can set Wave window display preferences by selecting **Wave > Wave Preferences** (when the window is docked) or **Tools > Window Preferences** (when the window is undocked). These commands open the Wave Window Preferences dialog ([Figure 14-28](#)).

Figure 14-28. Display Tab of the Wave Window Preferences Dialog Box



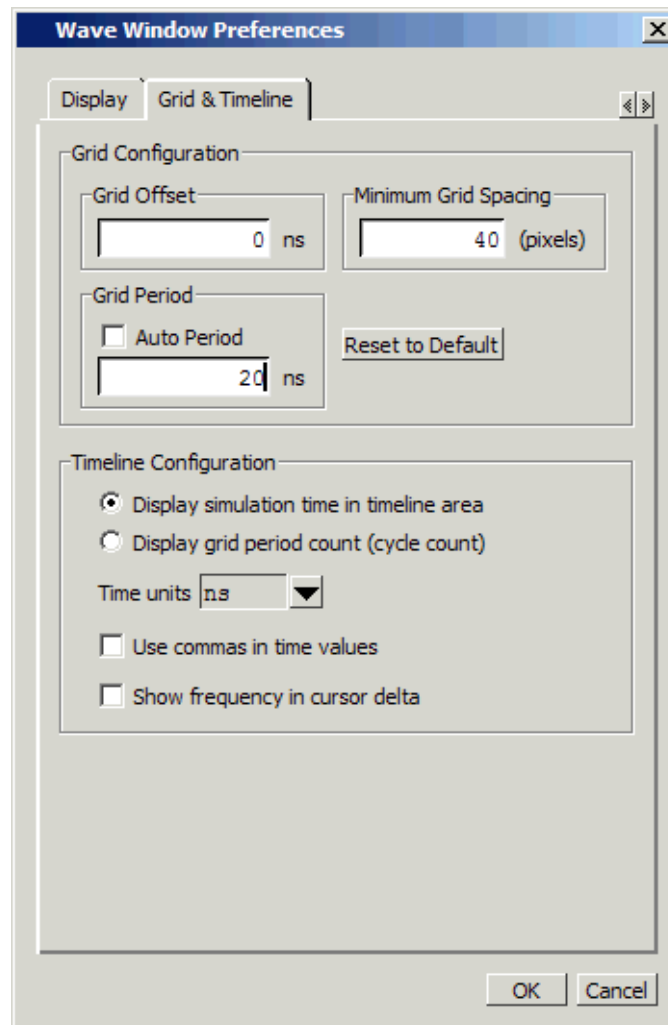
Hiding/Showing Path Hierarchy

You can set how many elements of the object path display by changing the Display Signal Path value in the Wave Window Preferences dialog (Figure 14-28). Zero indicates the full path while a non-zero number indicates the number of path elements to be displayed.

Setting the Timeline to Count Clock Cycles

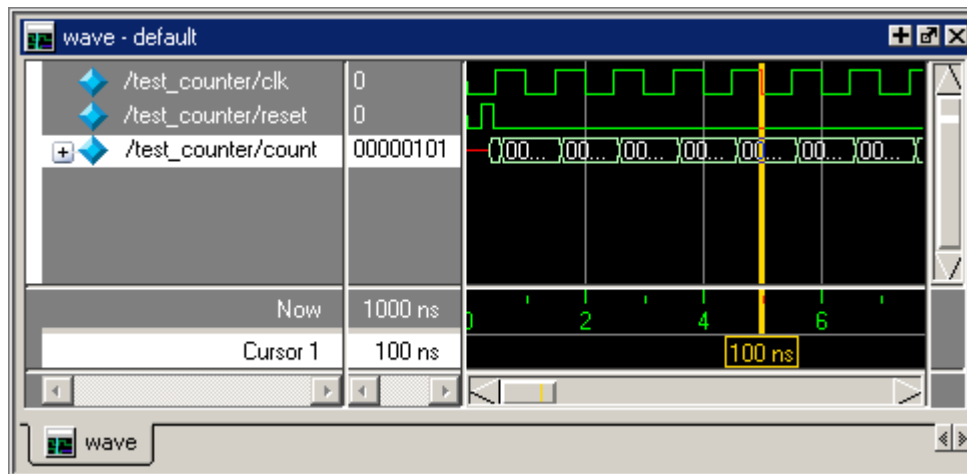
You can set the timeline of the Wave window to count clock cycles rather than elapsed time. If the Wave window is docked, open the Wave Window Preferences dialog by selecting **Wave > Wave Preferences** from the Main window menus. If the Wave window is undocked, select **Tools > Window Preferences** from the Wave window menus. This opens the Wave Window Preferences dialog. In the dialog, select the Grid & Timeline tab (Figure 14-29).

Figure 14-29. Grid & Timeline Tab of Wave Window Preferences Dialog Box



Enter the period of your clock in the Grid Period field and select “Display grid period count (cycle count).” The timeline will now show the number of clock cycles, as shown in [Figure 14-30](#).

Figure 14-30. Clock Cycles in Timeline of Wave Window



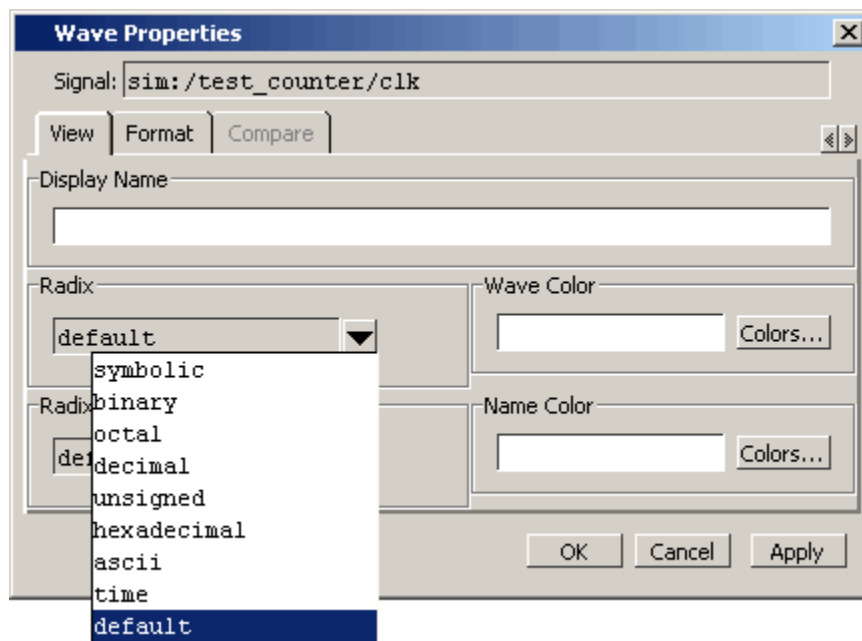
Formatting Objects in the Wave Window

You can adjust various object properties to create the view you find most useful. Select one or more objects and then select **Properties** or use the selections in the **Format** menu (when undocked).

Changing Radix (base) for the Wave Window

One common adjustment is changing the radix (base) of an object. When you select **Properties**, the Wave Signal Properties dialog appears.

Figure 14-31. Changing Signal Radix



The default radix is symbolic, which means that for an enumerated type, the value pane lists the actual values of the enumerated type of that object. For the other radices - binary, octal, decimal, unsigned, hexadecimal, or ASCII - the object value is converted to an appropriate representation in that radix.

Note

When the symbolic radix is chosen for SystemVerilog reg and integer types, the values are treated as binary. When the symbolic radix is chosen for SystemVerilog bit and int types, the values are considered to be decimal.

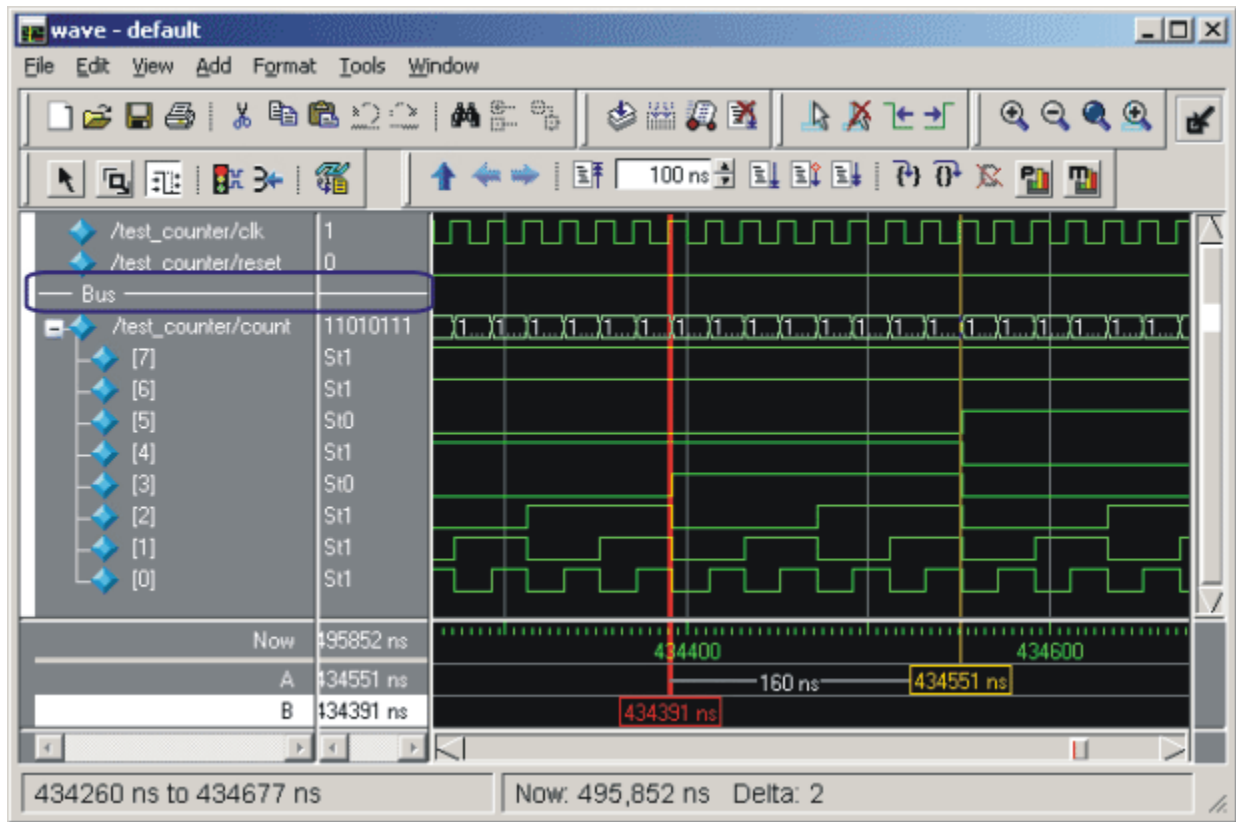
Aside from the Wave Signal Properties dialog, there are three other ways to change the radix:

- Change the default radix for the current simulation using **Simulate > Runtime Options** (Main window)
- Change the default radix for the current simulation using the [radix](#) command.
- Change the default radix permanently by editing the [DefaultRadix](#) variable in the *modelsim.ini* file.

Dividing the Wave Window

Dividers serve as a visual aid for debugging, allowing you to separate signals and waveforms for easier viewing. In the graphic below, a bus is separated from the two signals above it with a divider called "Bus."

Figure 14-32. Separate Signals with Wave Window Dividers



To insert a divider, follow these steps:

1. Select the signal above which you want to place the divider.
2. If the Wave pane is docked, select **Add > To Wave > Divider** from the Main window menu bar. If the Wave window stands alone, undocked from the Main window, select **Add > Divider** from the Wave window menu bar.
3. Specify the divider name in the Wave Divider Properties dialog. The default name is New Divider. Unnamed dividers are permitted. Simply delete "New Divider" in the Divider Name field to create an unnamed divider.
4. Specify the divider height (default height is 17 pixels) and then click OK.

You can also insert dividers with the **-divider** argument to the [add wave](#) command.

Working with Dividers

The table below summarizes several actions you can take with dividers:

Table 14-7. Actions for Dividers

Action	Method
Move a divider	Click-and-drag the divider to the desired location
Change a divider's name or size	Right-click the divider and select Divider Properties
Delete a divider	Right-click the divider and select Delete

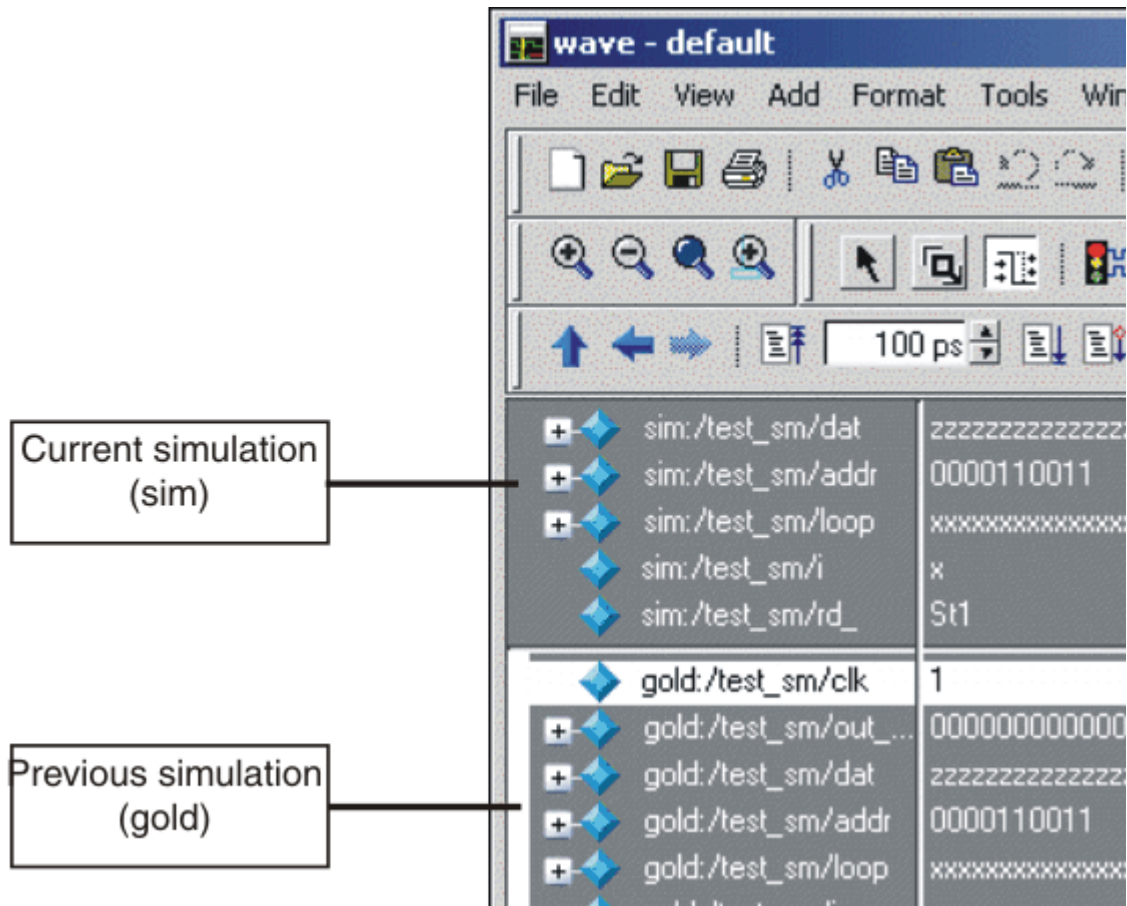
Splitting Wave Window Panes

The pathnames, values, and waveform panes of the Wave window display can be split to accommodate signals from one or more datasets. For more information on viewing multiple simulations, see [Recording Simulation Results With Datasets](#).

To split the window, select **Add > Window Pane**.

In the illustration below, the top split shows the current active simulation with the prefix "sim," and the bottom split shows a second dataset with the prefix "gold."

Figure 14-33. Splitting Wave Window Panes



The Active Split

The active split is denoted with a solid white bar to the left of the signal names. The active split becomes the target for objects added to the Wave window.

Wave Groups

You can create a wave group to collect arbitrary groups of items in the Wave window. Wave groups have the following characteristics:

- A wave group may contain 0, 1, or many items.
- You can add or remove items from groups either by using a command or by dragging and dropping.
- You can drag a group around the Wave window or to another Wave window.
- You can nest multiple wave groups, either from the command line or by dragging and dropping. Nested groups are saved or restored from a wave.do format file, restart and checkpoint/restore.

Creating a Wave Group

There are three ways to create a wave group:

- [Grouping Signals through Menu Selection](#)
- [Grouping Signals with the add wave Command](#)
- [Grouping Signals with a Keyboard Shortcut](#)

Grouping Signals through Menu Selection

If you've already added some signals to the Wave window, you can create a group of signals using the following procedure.

Procedure

1. Select a set of signals in the Wave window.
2. Select the **Wave > Group** menu item.

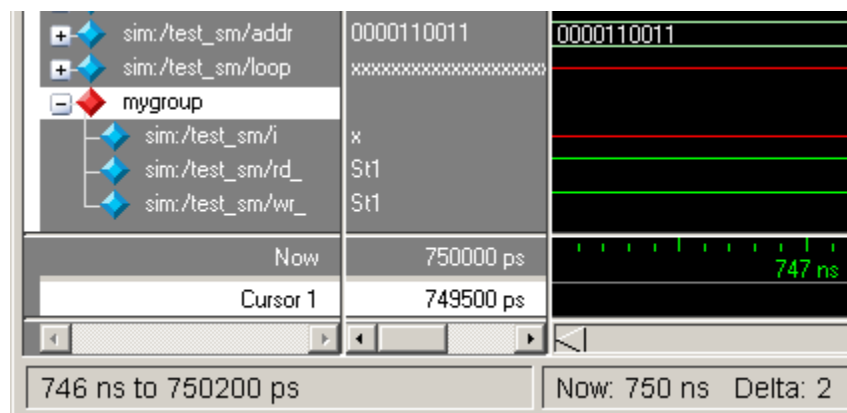
The Wave Group Create dialog appears.

3. Complete the Wave Group Create dialog box:
 - Group Name — specify a name for the group. This name is used in the wave window.
 - Group Height — specify an integer, in pixels, for the height of the space used for the group label.
4. Ok

Results

The selected signals become a group denoted by a red diamond in the Wave window pathnames pane, with the name specified in the dialog box.

Figure 14-34. Wave groups denoted by red diamond



Grouping Signals with the add wave Command

Add grouped signals to the Wave window from the command line use the following procedure.

Procedure

1. Determine the names of the signals you want to add and the name you want to assign to the group.
2. From the command line, use the `add wave` and the `-group` argument.

Examples

- Create a group named *mygroup* containing three items:

```
add wave -group mygroup sig1 sig2 sig3
```

- Create an empty group named *mygroup*:

```
add wave -group mygroup
```

Grouping Signals with a Keyboard Shortcut

If you've already added some signals to the Wave window, you can create a group of signals using the following procedure.

Procedure

1. Select the signals you want to group.
2. Ctrl-g

Results

The selected signals become a group with a name that references the dataset and common region, for example: `sim:/top/p`.

If you use Ctrl-g to group any other signals, they will be placed into any existing group for their region, rather than creating a new group of only those signals.

Deleting or Ungrouping a Wave Group

If a wave group is selected and cut or deleted the entire group and all its contents will be removed from the Wave window. Likewise, the `delete` wave command will remove the entire group if the group name is specified.

If a wave group is selected and the **Wave > Ungroup** menu item is selected the group will be removed and all of its contents will remain in the Wave window in existing order.

Adding Items to an Existing Wave Group

There are three ways to add items to an existing wave group.

1. Using the drag and drop capability to move items outside of the group or from other windows into the group. The insertion indicator will show the position the item will be dropped into the group. If the cursor is moved over the lower portion of the group item name a box will be drawn around the group name indicating the item will be dropped into the last position in the group.
2. The cut/copy/paste functions may be used to paste items into a group.
3. Use the **add wave -group** command.

The following example adds two more signals to an existing group called *mygroup*.

```
add wave -group mygroup sig4 sig5
```

Removing Items from an Existing Wave Group

You can use any of the following methods to remove an item from a wave group.

1. Use the drag and drop capability to move an item outside of the group.
2. Use menu or icon selections to cut or delete an item or items from the group.
3. Use the **delete** wave command to specify a signal to be removed from the group.

Note



The delete wave command removes all occurrences of a specified name from the Wave window, not just an occurrence within a group.

Miscellaneous Wave Group Features

Dragging a wave group from the Wave window to the List window will result in all of the items within the group being added to the List window.

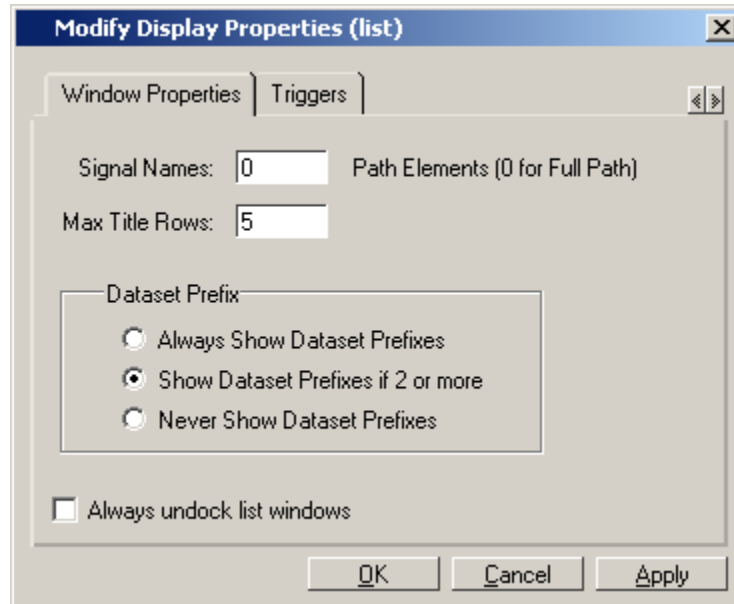
Dragging a group from the Wave window to the Transcript window will result in a list of all of the items within the group being added to the existing command line, if any.

Formatting the List Window

Setting List Window Display Properties

Before you add objects to the List window, you can set the window's display properties. To change when and how a signal is displayed in the List window, select **Tools > List Preferences** from the List window menu bar (when the window is undocked).

Figure 14-35. Modifying List Window Display Properties



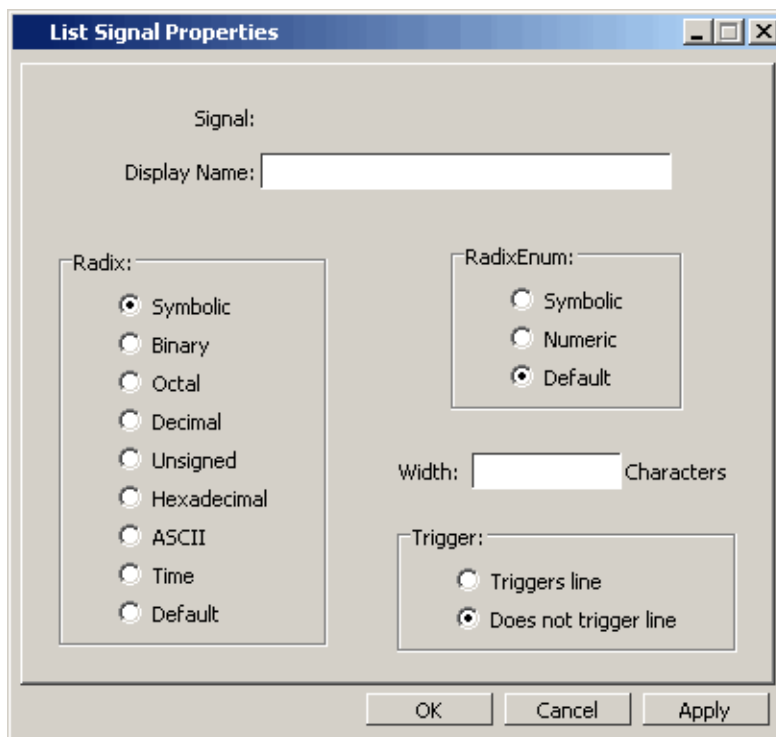
Formatting Objects in the List Window

You can adjust various properties of objects to create the view you find most useful. Select one or more objects and then select **View > Signal Properties** from the List window menu bar (when the window is undocked).

Changing Radix (base) for the List Window

One common adjustment you can make to the List window display is to change the radix (base) of an object. To do this, choose **View > Signal Properties** from the main menu, which displays the List Signal Properties dialog box. [Figure 14-36](#) shows the list of radix types you can select in this dialog box.

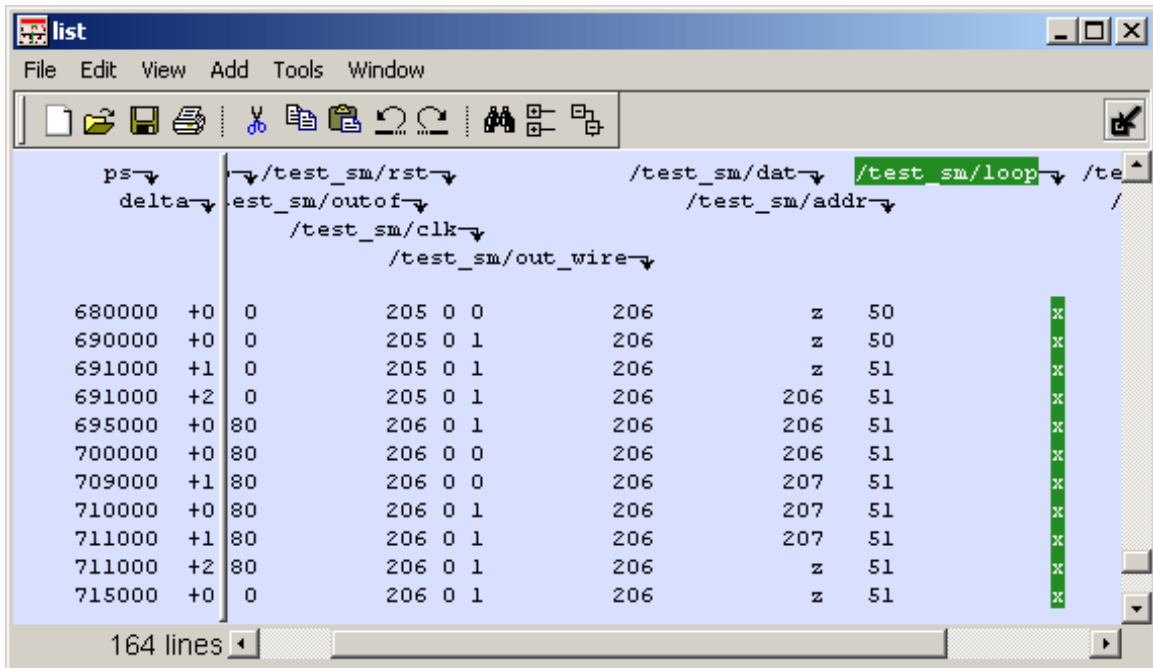
Figure 14-36. List Signal Properties Dialog



The default radix type is symbolic, which means that for an enumerated type, the window lists the actual values of the enumerated type of that object. For the other radix types (binary, octal, decimal, unsigned, hexadecimal, ASCII, time), the object value is converted to an appropriate representation in that radix.

Changing the radix can make it easier to view information in the List window. Compare the image below (with decimal values) with the image in the section [List Window Overview](#) (with symbolic values).

Figure 14-37. Changing the Radix in the List Window



In addition to the List Signal Properties dialog box, you can also change the radix:

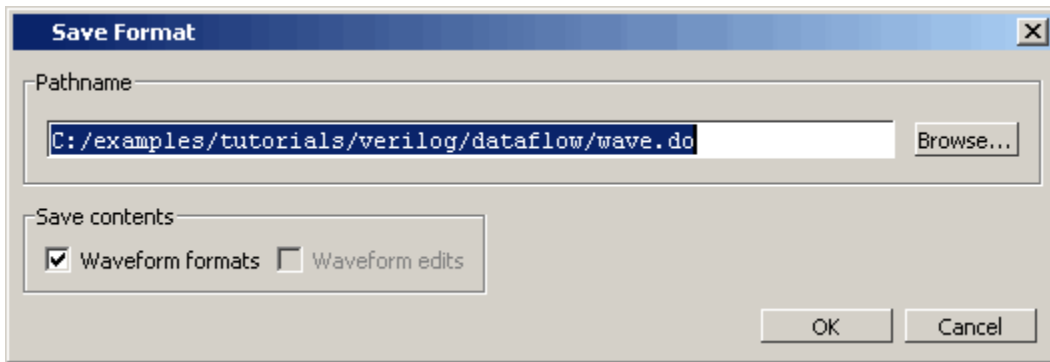
- Change the default radix for the current simulation using **Simulate > Runtime Options** (Main window)
- Change the default radix for the current simulation using the [radix](#) command.
- Change the default radix permanently by editing the [DefaultRadix](#) variable in the *modelsim.ini* file.

Saving the Window Format

By default all Wave and List window information is forgotten once you close the windows. If you want to restore the windows to a previously configured layout, you must save a window format file. Follow these steps:

1. Add the objects you want to the Wave or List window.
2. Edit and format the objects to create the view you want.
3. Save the format to a file by selecting **File > Save**. This opens the Save Format dialog, which allows you to save waveform formats in a *.do* file.

Figure 14-38. Save Format Dialog



To use the format file, start with a blank Wave or List window and run the DO file in one of two ways:

- Invoke the `do` command from the command line:

```
VSIM> do <my_format_file>
```
- Select **File > Load**.

Note



Window format files are design-specific. Use them only with the design you were simulating when they were created.

In addition, you can use the `write format` restart command to create a single `.do` file that will recreate all debug windows and breakpoints (see [Saving and Restoring Breakpoints](#)) when invoked with the `do` command in subsequent simulation runs. The syntax is:

```
write format restart <filename>
```

If the `ShutdownFile` `modelsim.ini` variable is set to this `.do` filename, it will call the `write format` restart command upon exit.

Printing and Saving Waveforms in the Wave window

You can print the waveform display or save it as an encapsulated postscript (EPS) file.

Saving a .eps Waveform File and Printing in UNIX

Select **File > Print Postscript** (Wave window) to print all or part of the waveform in the current Wave window in UNIX, or save the waveform as a `.eps` file on any platform (see also the `write wave` command).

Printing from the Wave Window on Windows Platforms

Select **File > Print** (Wave window) to print all or part of the waveform in the current Wave window, or save the waveform as a printer file (a Postscript file for Postscript printers).

Printer Page Setup

Select **File > Page setup** or click the Setup button in the Write Postscript or Print dialog box to define how the printed page will appear.

Saving List Window Data to a File

Select **File > Write List** in the List window to save the data in one of these formats:

- **Tabular** — writes a text file that looks like the window listing

```
ns    delta    /a    /b    /cin    /sum    /cout
0     +0       X     X     U       X       U
0     +1       0     1     0       X       U
2     +0       0     1     0       X       U
```

- **Events** — writes a text file containing transitions during simulation

```
@0 +0
/a X
/b X
/cin U
/sum X
/cout U
@0 +1
/a 0
/b 1
/cin 0
```

- **TSSI** — writes a file in standard TSSI format; see also, the [write tssi](#) command.

```
0 000000000000000010?????????
2 000000000000000010?????????1?
3 000000000000000010?????????010
4 0000000000000000100000000010
100 0000000100000000100000000010
```

You can also save List window output using the [write list](#) command.

Viewing SystemVerilog Class Objects

The suggested workflow for viewing SystemVerilog class objects in the Wave window is as follows.

1. Select a module in a Workspace structure view that contains the class variables you want to see. All class variables associated with that module are displayed in the Objects

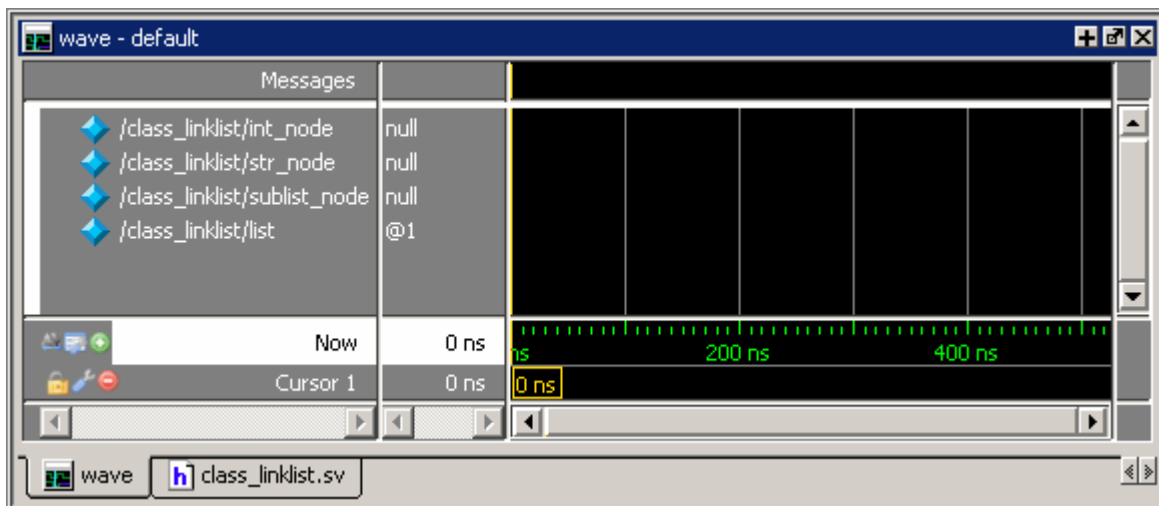
window. (Open the Objects window by selecting **View > Objects** from the menus or use the [view objects](#) command.)

2. You can place class objects in the Wave window by doing any one of the following:
 - Drag a class variable from the Objects window and drop it into the Wave window,
 - Right-click the class variable in the Objects window and select **Add > To Wave** from the popup context window.
 - Use the [add wave](#) command at the command prompt. For example:

```
add wave int_mode
```

SystemVerilog class objects are denoted in the Wave window by a light blue diamond, as shown in [Figure 14-39](#).

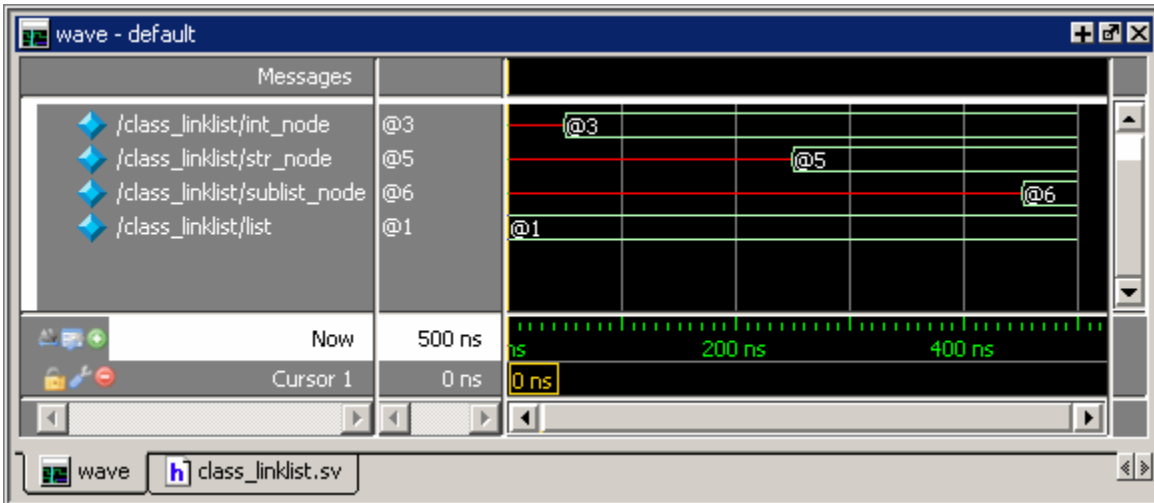
Figure 14-39. Class Objects in the Wave Window



- Items in the pathnames column are class variables.
- Items in the values columns are symbolic representations of class objects that refer to a class instance. These class references may have a “null” value - which means that they do not yet refer to any class instance - or they may be denoted with the “@” symbol, which does refer to a class instance. The “@” indicates that the value is a pointer (or a handle) to an object rather than the value of the object itself. The number that appears after the “@” is a unique reference number. This is needed because class objects are not named by the class variable that stores the handle to the object.

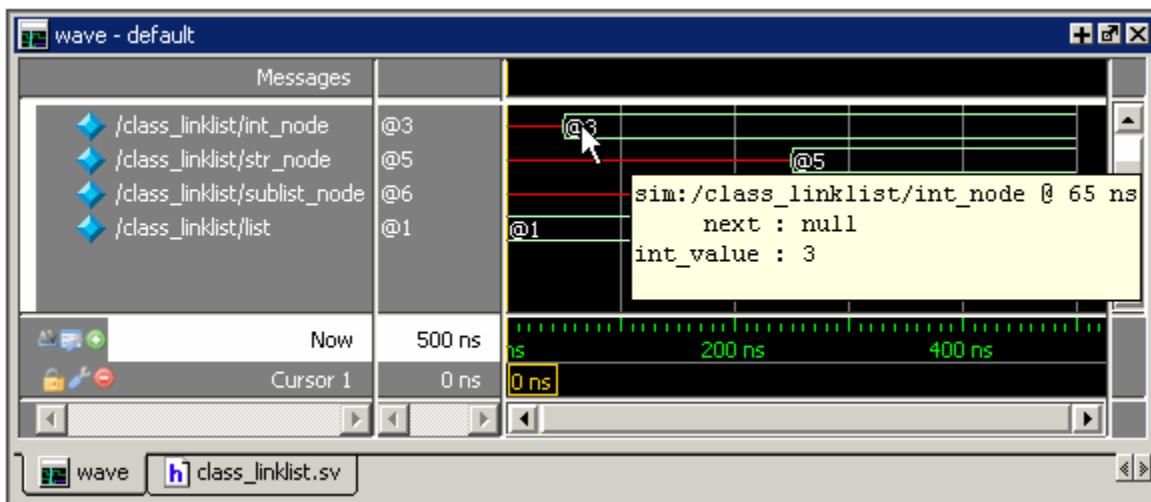
When the simulation is run, the “waveforms” for class objects appear as shown in [Figure 14-40](#).

Figure 14-40. Class Waveforms



You can hover the mouse over any class waveform to display information about the class variable (Figure 14-41).

Figure 14-41. Class Information Popup



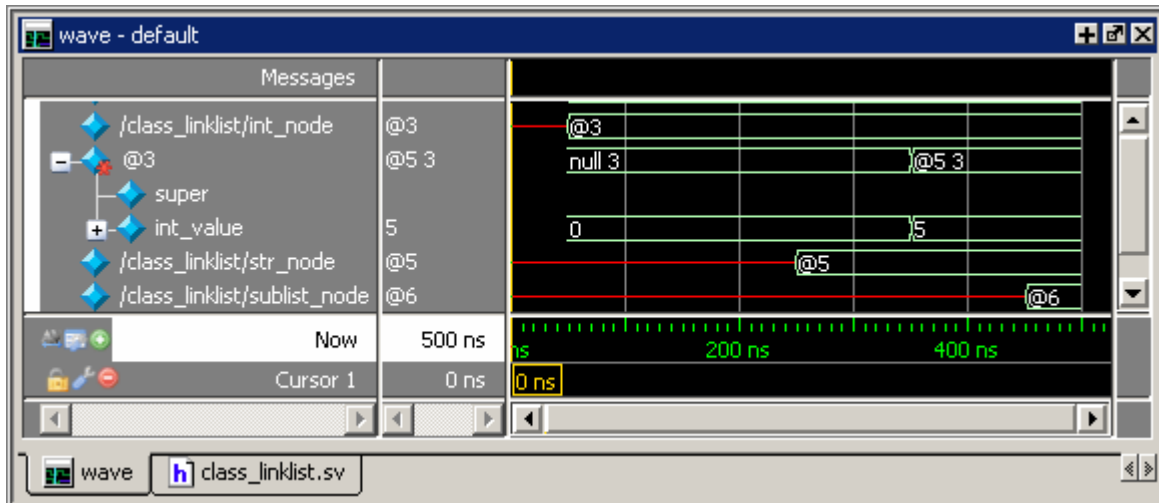
To display the waveforms for the actual class instances, do either of the following:

- Right-click the class “waveform” and select **Add to Wave** from the popup context menu.
- Use the add wave command with a class reference name.

add wave @3

The class instances are denoted by a light blue diamond with a red asterisk in the pathnames column. In Figure 14-42, the class object referred to by “@3” is expanded to show the integer values for the *int_value* instance.

Figure 14-42. Waveforms for Class Instances



Combining Objects into Buses

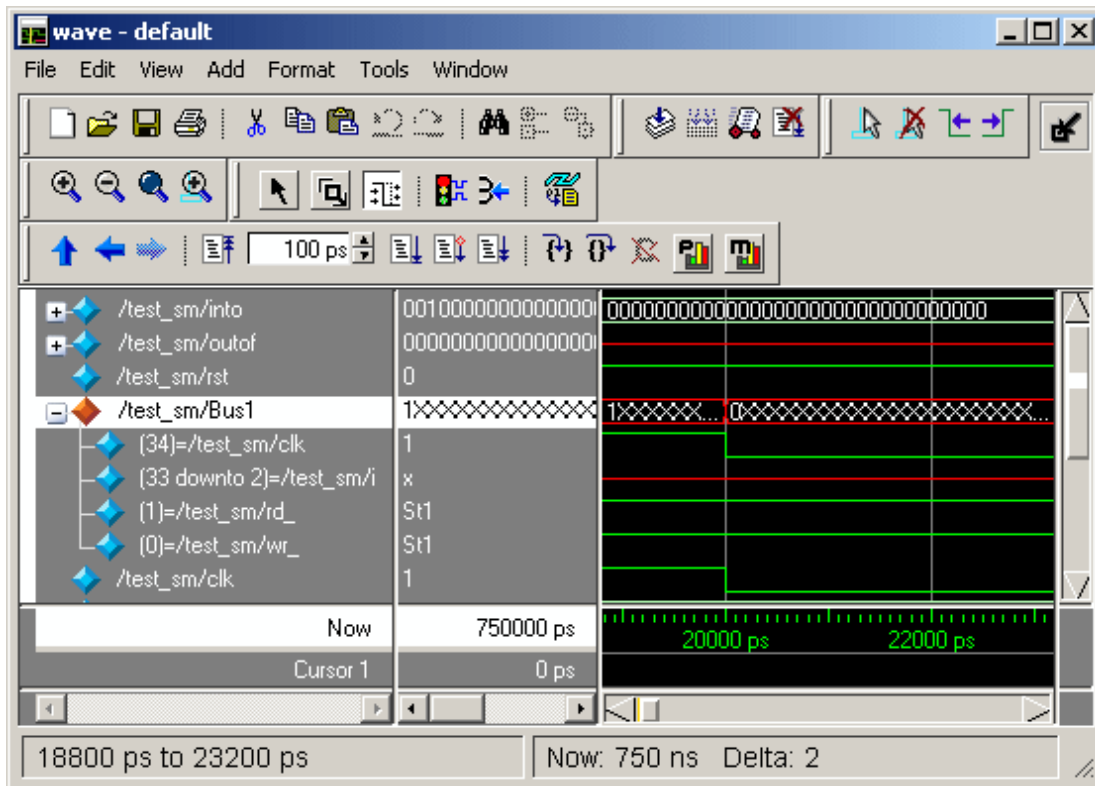
You can combine signals in the Wave or List window into buses. A bus is a collection of signals concatenated in a specific order to create a new virtual signal with a specific value. A virtual compare signal (the result of a comparison simulation) is not supported for combination with any other signal.

To combine signals into a bus, use one of the following methods:

- Select two or more signals in the Wave or List window and then choose **Tools > Combine Signals** from the menu bar. A virtual signal that is the result of a comparison simulation is not supported for combining with any other signal.
- Use the [virtual signal](#) command at the Main window command prompt.

In the illustration below, three signals have been combined to form a new bus called "Bus1." Note that the component signals are listed in the order in which they were selected in the Wave window. Also note that the value of the bus is made up of the values of its component signals, arranged in a specific order.

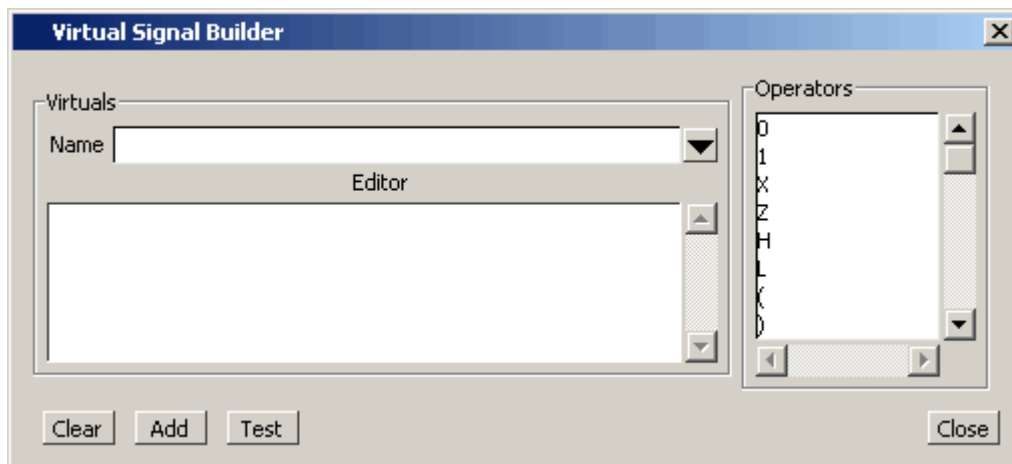
Figure 14-43. Signals Combined to Create Virtual Bus



Creating a Virtual Signal

The Wave window allows you to build Virtual Signals with the Virtual Signal Builder. The Virtual Signal Builder is accessed by selecting **Wave > Virtual Builder** when the Wave window is docked or selecting **Tools > Virtual Builder** when the Wave window is undocked.

Figure 14-44. Virtual Expression Builder



- The Name field allows you to enter the name of the new virtual signal.

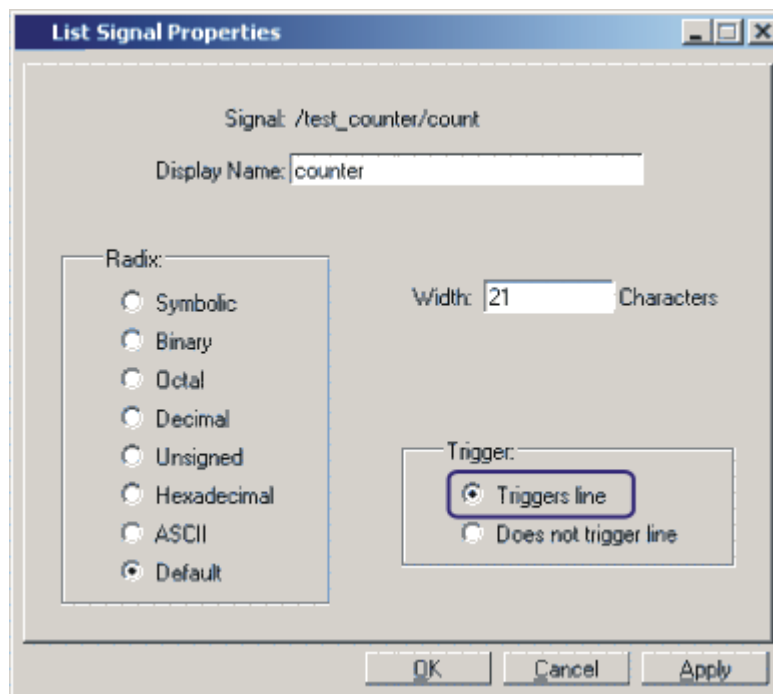
- The Editor field is simply a regular text box. You can write directly to it, copy and paste or drag a signal from the Objects window, Locals window or the Wave window and drop it in the Editor field.
- The Operators field allows you to select from a list of operators. Simply double-click an operator to add it to the Editor field.
- The Clear button will clear the Editor field.
- The Add button will add the virtual signal to the wave window
- The Test button will test your virtual signal for proper operation.

Configuring New Line Triggering in the List Window

New line triggering refers to what events cause a new line of data to be added to the List window. By default ModelSim adds a new line for any signal change including deltas within a single unit of time resolution.

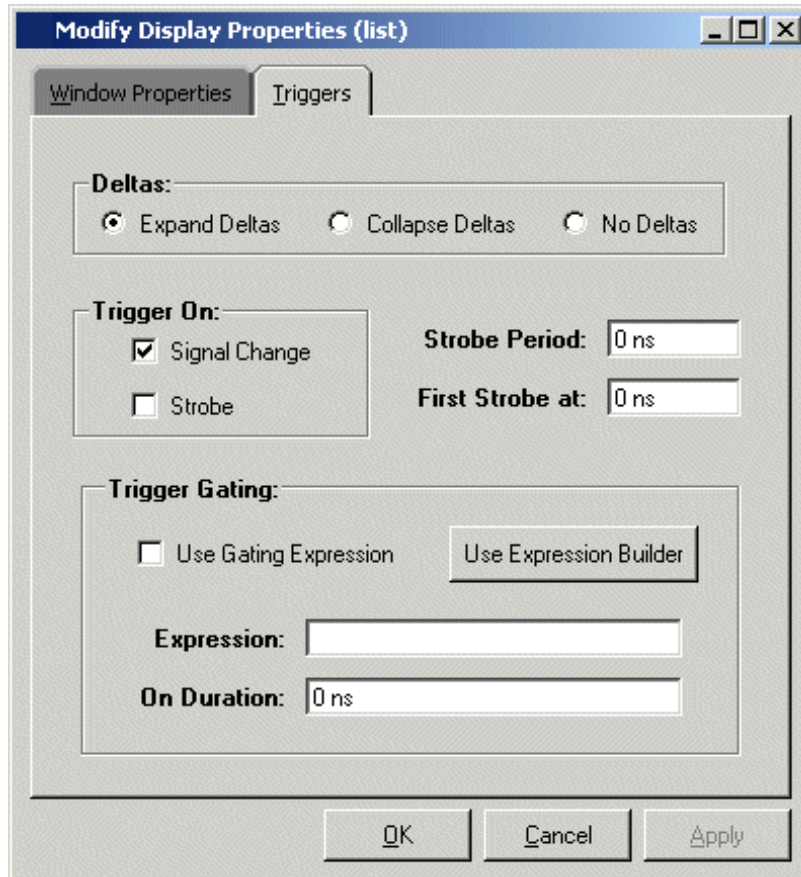
You can set new line triggering on a signal-by-signal basis or for the whole simulation. To set for a single signal, select **View > Signal Properties** from the List window menu bar (when the window is undocked) and select the **Triggers line** setting. Individual signal settings override global settings.

Figure 14-45. Line Triggering in the List Window



To modify new line triggering for the whole simulation, select **Tools > List Preferences** from the List window menu bar (when the window is undocked), or use the [configure](#) command. When you select **Tools > List Preferences**, the Modify Display Properties dialog appears:

Figure 14-46. Setting Trigger Properties



The following table summarizes the triggering options:

Table 14-8. Triggering Options

Option	Description
Deltas	Choose between displaying all deltas (Expand Deltas), displaying the value at the final delta (Collapse Delta). You can also hide the delta column all together (No Delta), however this will display the value at the final delta.
Strobe trigger	Specify an interval at which you want to trigger data display
Trigger gating	Use a gating expression to control triggering; see Using Gating Expressions to Control Triggering for more details

Using Gating Expressions to Control Triggering

Trigger gating controls the display of data based on an expression. Triggering is enabled once the gating expression evaluates to true. This setup behaves much like a hardware signal analyzer that starts recording data on a specified setup of address bits and clock edges.

Here are some points about gating expressions:

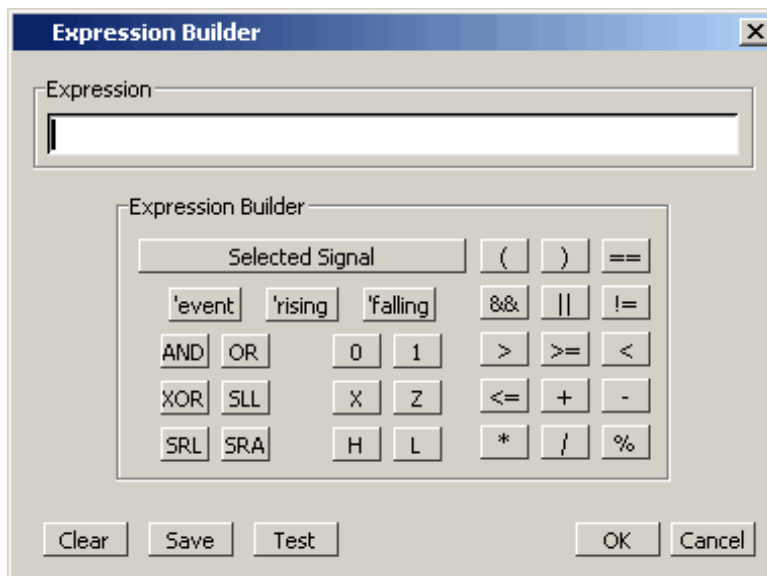
- Gating expressions affect the display of data but not acquisition of the data.
- The expression is evaluated when the List window would normally have displayed a row of data (given the other trigger settings).
- The duration determines for how long triggering stays enabled after the gating expression returns to false (0). The default of 0 duration will enable triggering only while the expression is true (1). The duration is expressed in x number of default timescale units.
- Gating is level-sensitive rather than edge-triggered.

Trigger Gating Example Using the Expression Builder

This example shows how to create a gating expression with the ModelSim Expression Builder. Here is the procedure:

1. Select **Tools > Window Preferences** from the List window menu bar (when the window is undocked) and select the Triggers tab.
2. Click the **Use Expression Builder** button.

Figure 14-47. Trigger Gating Using Expression Builder



3. Select the signal in the List window that you want to be the enable signal by clicking on its name in the header area of the List window.
4. Click **Insert Selected Signal** and then '**rising**' in the Expression Builder.
5. Click OK to close the Expression Builder.

You should see the name of the signal plus "rising" added to the Expression entry box of the Modify Display Properties dialog box.

6. Click **OK** to close the dialog.

If you already have simulation data in the List window, the display should immediately switch to showing only those cycles for which the gating signal is rising. If that isn't quite what you want, you can go back to the expression builder and play with it until you get it the way you want it.

If you want the enable signal to work like a "One-Shot" that would display all values for the next, say 10 ns, after the rising edge of enable, then set the **On Duration** value to **10 ns**.

Trigger Gating Example Using Commands

The following commands show the gating portion of a trigger configuration statement:

```
configure list -usegating 1
configure list -gateduration 100
configure list -gateexpr {/test_delta/iom_dd'rising}
```

See the [configure](#) command for more details.

Sampling Signals at a Clock Change

You easily can sample signals at a clock change using the [add list](#) command with the **-notrigger** argument. The **-notrigger** argument disables triggering the display on the specified signals. For example:

```
add list clk -notrigger a b c
```

When you run the simulation, List window entries for *clk*, *a*, *b*, and *c* appear only when *clk* changes.

If you want to display on rising edges only, you have two options:

1. Turn off the List window triggering on the clock signal, and then define a repeating strobe for the List window.
2. Define a "gating expression" for the List window that requires the clock to be in a specified state. See above.

Miscellaneous Tasks


Examining Waveform Values

You can use your mouse to display a dialog that shows the value of a waveform at a particular time. You can do this two ways:

- Rest your mouse pointer on a waveform. After a short delay, a dialog will pop-up that displays the value for the time at which your mouse pointer is positioned. If you'd prefer that this popup not display, it can be toggled off in the display properties. See [Setting Wave Window Display Preferences](#).
- Right-click a waveform and select **Examine**. A dialog displays the value for the time at which you clicked your mouse. This method works in the List window as well.

Displaying Drivers of the Selected Waveform

You can automatically display in the Dataflow window the drivers of a signal selected in the Wave window. You can do this three ways:

- Select a waveform and click the Show Drivers button on the toolbar. 
- Select a waveform and select Show Drivers from the shortcut menu
- Double-click a waveform edge (you can enable/disable this option in the display properties dialog; see [Setting Wave Window Display Preferences](#))

This operation opens the Dataflow window and displays the drivers of the signal selected in the Wave window. The Wave pane in the Dataflow window also opens to show the selected signal with a cursor at the selected time. The Dataflow window shows the signal(s) values at the current cursor position.

Sorting a Group of Objects in the Wave Window

Select **View > Sort** to sort the objects in the pathname and values panes.

Creating and Managing Breakpoints

ModelSim supports both signal (that is, when conditions) and file-line breakpoints. Breakpoints can be set from multiple locations in the GUI or from the command line.

Note



When running in full optimization mode, breakpoints may not be set. Run the design in non-optimized mode (or set +acc arguments) to enable you to set breakpoints in the design. See [Preserving Object Visibility for Debugging Purposes](#) and [Design Object Visibility for Designs with PLI](#).

Breakpoints within SystemC portions of the design can only be set using [File-Line Breakpoints](#).

Signal Breakpoints

Signal breakpoints (“when” conditions) instruct ModelSim to perform actions when the specified conditions are met. For example, you can break on a signal value or at a specific simulator time (see the [when](#) command for additional details). When a breakpoint is hit, a message in the Main window transcript identifies the signal that caused the breakpoint.

Setting Signal Breakpoints with the when Command

Use the [when](#) command to set a signal breakpoint from the VSIM> prompt. For example,

```
when {errorFlag = '1' OR $now = 2 ms} {stop}
```

adds 2 ms to the simulation time at which the “when” statement is first evaluated, then stops. The white space between the value and time unit is required for the time unit to be understood by the simulator. See the [when](#) command in the Command Reference for more examples.

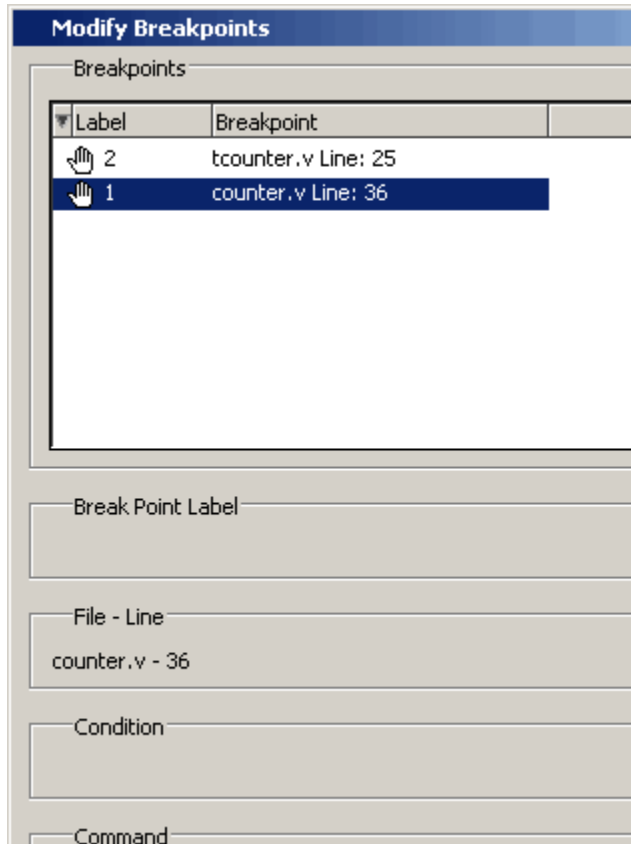
Setting Signal Breakpoints with the GUI

Signal breakpoints are most easily set in the [Objects Window](#) and the Wave window. Right-click a signal and select **Insert Breakpoint** from the context menu. A breakpoint is set on that signal and will be listed in the **Modify Breakpoints** dialog accessible by selecting **Tools > Breakpoints** from the Main menu bar.

Modifying Signal Breakpoints

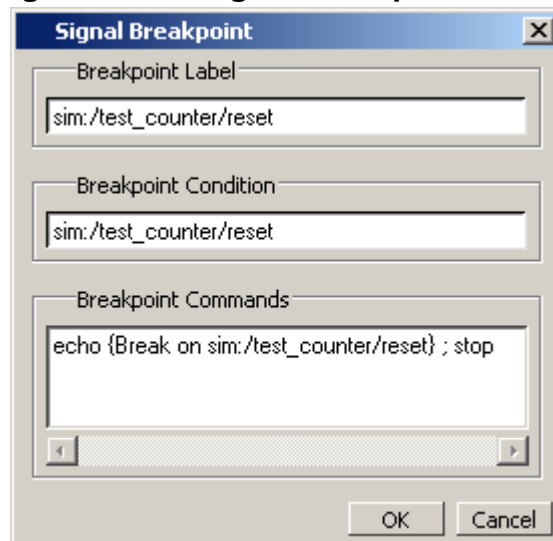
You can modify signal breakpoints by selecting **Tools > Breakpoints** from the Main menus. This will open the Modify Breakpoints dialog ([Figure 14-48](#)), which displays a list of all breakpoints in the design.

Figure 14-48. Modifying the Breakpoints Dialog



When you select a signal breakpoint from the list and click the Modify button, the Signal Breakpoint dialog (Figure 14-49) opens, allowing you to modify the breakpoint.

Figure 14-49. Signal Breakpoint Dialog



File-Line Breakpoints

File-line breakpoints are set on executable lines in your source files. When the line is hit, the simulator stops and the Source window opens to show the line with the breakpoint. You can change this behavior by editing the PrefSource(OpenOnBreak) variable. See [Simulator GUI Preferences](#) for details on setting preference variables.

Since C Debug is invoked when you set a breakpoint within a SystemC module, your C Debug settings must be in place prior to setting a breakpoint. See [Setting Up C Debug](#) for more information. Once invoked, C Debug can be exited using the C Debug menu.

Setting File-Line Breakpoints Using the bp Command

Use the `bp` command to set a file-line breakpoint from the `VSIM>` prompt. For example:

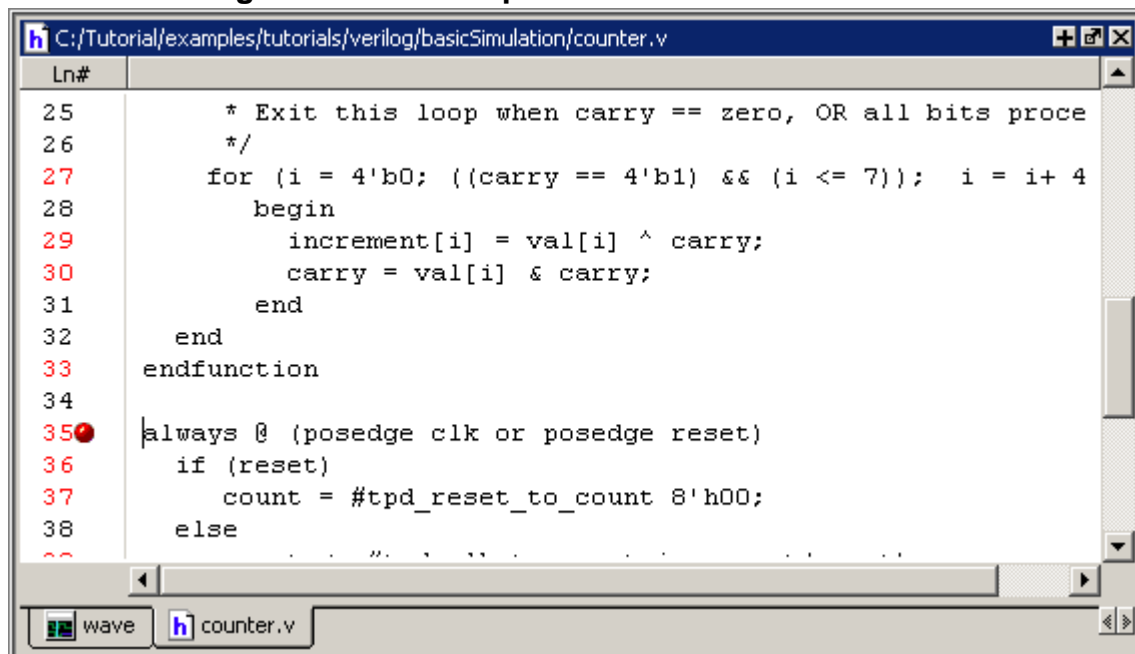
```
bp top.vhd 147
```

sets a breakpoint in the source file `top.vhd` at line 147.

Setting File-Line Breakpoints Using the GUI

File-line breakpoints are most easily set using your mouse in the [Source Window](#). Position your mouse cursor in the line number column next to a red line number (which indicates an executable line) and click the left mouse button. A red ball denoting a breakpoint will appear ([Figure 14-50](#)).

Figure 14-50. Breakpoints in the Source Window



The breakpoints are toggles. Click the left mouse button on the red breakpoint marker to disable the breakpoint. A disabled breakpoint will appear as a black ball. Click the marker again to enable it.

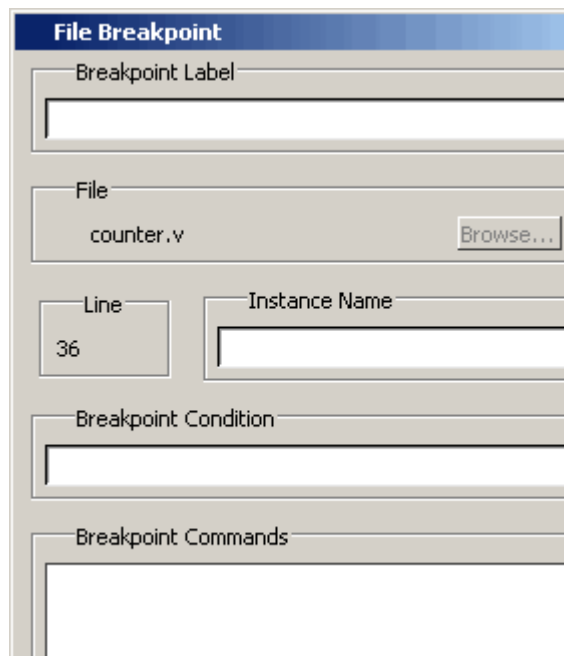
Right-click the breakpoint marker to open a context menu that allows you to **Enable/Disable**, **Remove**, or **Edit** the breakpoint. create the colored diamond; click again to disable or enable the breakpoint.

Modifying a File-Line Breakpoint

You can modify a file-line breakpoint by selecting **Tools > Breakpoints** from the Main menus. This will open the Modify Breakpoints dialog (Figure 14-48), which displays a list of all breakpoints in the design.

When you select a file-line breakpoint from the list and click the Modify button, the File Breakpoint dialog (Figure 14-51) opens, allowing you to modify the breakpoint.

Figure 14-51. File Breakpoint Dialog Box



The screenshot shows the 'File Breakpoint' dialog box with the following fields:

- Breakpoint Label:** An empty text input field.
- File:** A text input field containing 'counter.v' and a 'Browse...' button to its right.
- Line:** A text input field containing the number '36'.
- Instance Name:** An empty text input field.
- Breakpoint Condition:** An empty text input field.
- Breakpoint Commands:** An empty text input field.

Saving and Restoring Breakpoints

The **write format** restart command creates a single *.do* file that will recreate all debug windows, all file/line breakpoints, and all signal breakpoints created using the **when** command. The syntax is:

```
write format restart <filename>
```

If the **ShutdownFile** *modelsim.ini* variable is set to this *.do* filename, it will call the **write format** restart command upon exit.

The file created is primarily a list of [add list](#), [add wave](#), and [configure](#) commands, though a few other commands are included. This file may be invoked with the [do](#) command to recreate the window format on a subsequent simulation run.

Waveform Compare

The ModelSim Waveform Compare feature allows you to compare simulation runs. Differences encountered in the comparison are summarized and listed in the Main window transcript and are shown in the Wave and List windows. In addition, you can write a list of the differences to a file using the [compare info](#) command.

Note



The Waveform Compare feature is available as an add-on to the PE or LE versions.

The basic steps for running a comparison are as follows:

1. Run one simulation and save the dataset. For more information on saving datasets, see [Saving a Simulation to a WLF File](#).
2. Run a second simulation.
3. Setup and run a comparison.
4. Analyze the differences in the Wave or List window.

Mixed-Language Waveform Compare Support

Mixed-language compares are supported as listed in the following table:

Table 14-9. Mixed-Language Waveform Compares

Language	Compares
C/C++ types	bool, char, unsigned char short, unsigned short int, unsigned int long, unsigned long
SystemC types	sc_bit, sc_bv, sc_logic, sc_lv sc_int, sc_uint sc_bigint, sc_biguint sc_signed, sc_unsigned
Verilog types	net, reg

The number of elements must match for vectors; specific indexes are ignored.

Three Options for Setting up a Comparison

There are three options for setting up a comparison:

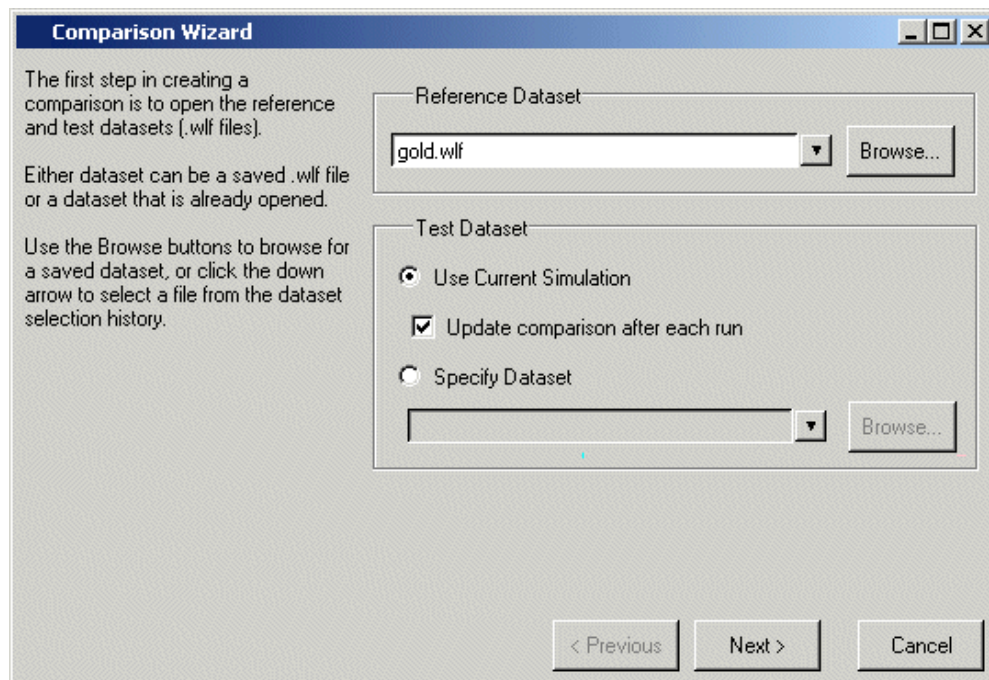
- Comparison Wizard – A series of dialogs that "walk" you through the process
- Comparison commands – Use a series of **compare** commands
- GUI – Use various dialogs to "manually" configure the comparison

Comparison Wizard

The simplest method for setting up a comparison is using the Wizard. The wizard is a series of dialogs that walks you through the process. To start the Wizard, select **Tools > Waveform Compare > Comparison Wizard** from either the Wave or Main window.

The graphic below shows the first dialog in the Wizard. As you can see from this example, the dialogs include instructions on the left-hand side.

Figure 14-52. Waveform Comparison Wizard



Comparison Graphic Interface

You can also set up a comparison via the GUI without using the Wizard. The steps of this process are described further in [Setting Up a Comparison with the GUI](#).

Comparison Commands

There are numerous commands that give you complete control over a comparison. These commands can be entered in the Transcript window or run via a DO file. The commands are detailed in the Reference Manual, but the following example shows the basic sequence:

```
compare start gold vsim  
compare add /*  
compare run
```

This example command sequence assumes that the *gold.wlf* reference dataset is loaded with the current simulation, the *vsim.wlf* dataset. The **compare start** command instructs ModelSim to compare the reference *gold.wlf* dataset against the current simulation. The **compare add /*** command instructs ModelSim to compare all signals in the *gold.wlf* reference dataset against all signals in the *vsim.wlf* dataset. The **compare run** command runs the comparison.

Comparing Signals with Different Names

You can use the **compare add** command to specify a comparison between two signals with different names.

Setting Up a Comparison with the GUI

To setup a comparison with the GUI, follow these steps:

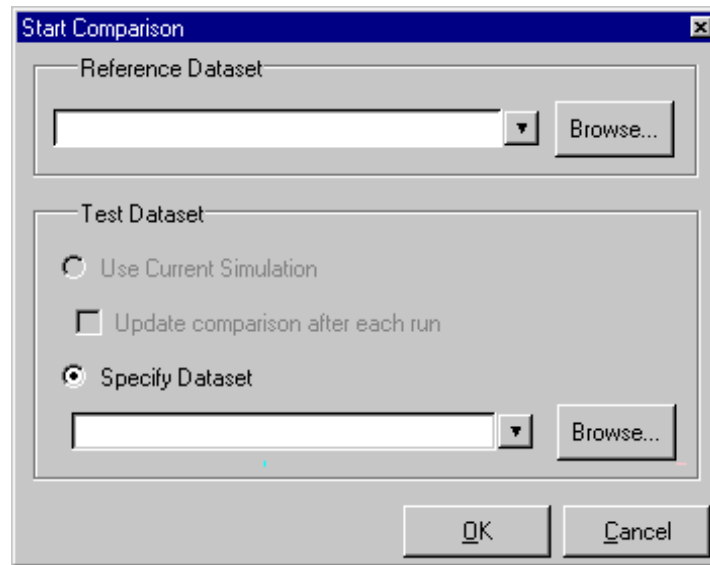
1. Initiate the comparison by specifying the reference and test datasets. See [Starting a Waveform Comparison](#) for details.
2. Add objects to the comparison. See [Adding Signals, Regions, and Clocks](#) for details.
3. Specify the comparison method. See [Specifying the Comparison Method](#) for details.
4. Configure comparison options. See [Setting Compare Options](#) for details.
5. Run the comparison by selecting **Tools > Waveform Compare > Run Comparison**.
6. View the results. See [Viewing Differences in the Wave Window](#), [Viewing Differences in the List Window](#), and [Viewing Differences in Textual Format](#) for details.

Waveform Compare is initiated from either the Main or Wave window by selecting **Tools > Waveform Compare > Start Comparison**.

Starting a Waveform Comparison

Select **Tools > Waveform Compare > Start Comparison** to initiate the comparison. The Start Comparison dialog box allows you define the Reference and Test datasets.

Figure 14-53. Start Comparison Dialog



Reference Dataset

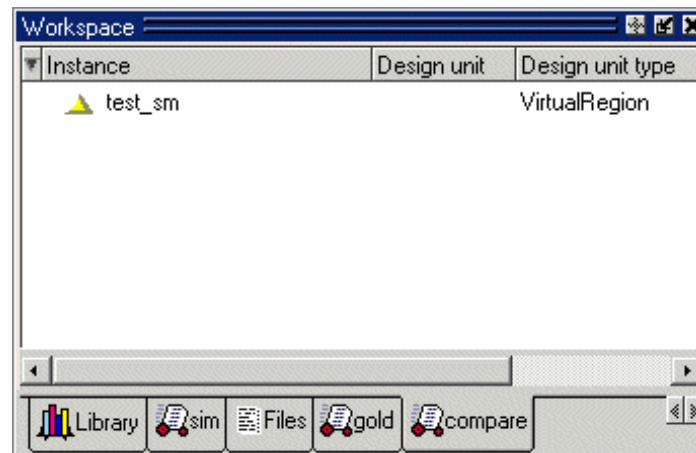
The Reference Dataset is the *.wlf* file to which the test dataset will be compared. It can be a saved dataset, the current simulation dataset, or any part of the current simulation dataset.

Test Dataset

The Test Dataset is the *.wlf* file that will be compared against the Reference Dataset. Like the Reference Dataset, it can be a saved dataset, the current simulation dataset, or any part of the current simulation dataset.

Once you click **OK** in the Start Comparison dialog box, ModelSim adds a Compare tab to the Main window.

Figure 14-54. Compare Tab in the Workspace Pane



After adding the signals, regions, and/or clocks you want to use in the comparison (see [Adding Signals, Regions, and Clocks](#)), you will be able to drag compare objects from this tab into the Wave and List windows.

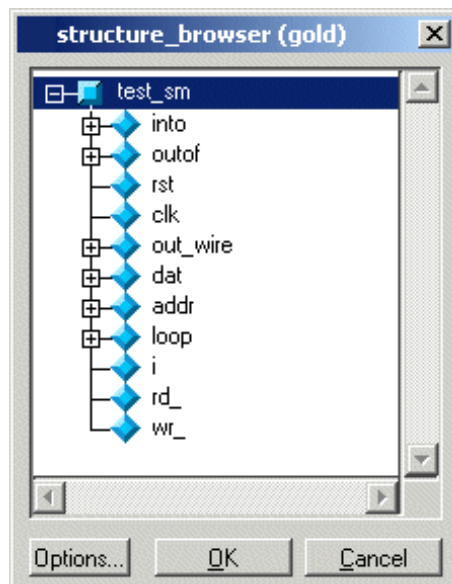
Adding Signals, Regions, and Clocks

To designate the signals, regions, or clocks to be used in the comparison, click **Tools > Waveform Compare > Add**.

Adding Signals

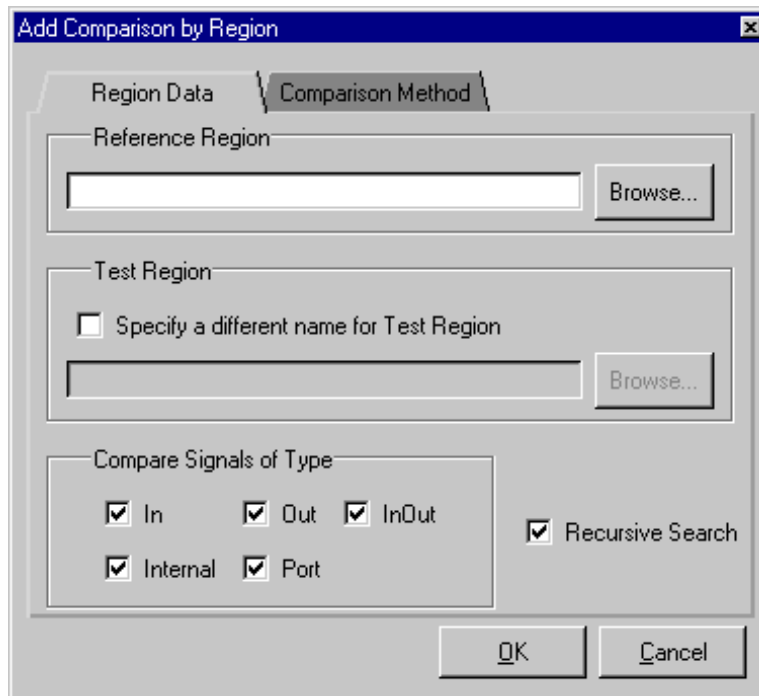
Clicking **Tools > Waveform Compare > Add > Compare by Signal** in the Wave window opens the structure_browser window, where you can specify signals to be used in the comparison.

Figure 14-55. Structure Browser



Adding Regions

Rather than comparing individual signals, you can also compare entire regions of your design. Select **Tools > Waveform Compare > Add > Compare by Region** to open the Add Comparison by Region dialog.

Figure 14-56. Add Comparison by Region Dialog

Adding Clocks

You add clocks when you want to perform a clocked comparison. See [Specifying the Comparison Method](#) for details.

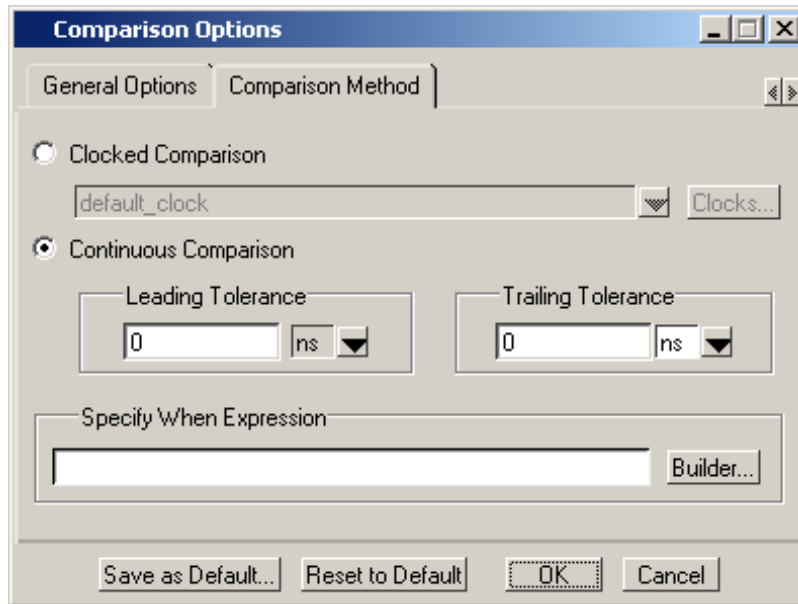
Specifying the Comparison Method

The Waveform Compare feature provides two comparison methods:

- Continuous comparison — Test signals are compared to reference signals at each transition of the reference. Timing differences between the test and reference signals are shown with rectangular red markers in the Wave window and yellow markers in the List window.
- Clocked comparisons — Signals are compared only at or just after an edge on some signal. In this mode, you define one or more clocks. The test signal is compared to a reference signal and both are sampled relative to the defined clock. The clock can be defined as the rising or falling edge (or either edge) of a particular signal plus a user-specified delay. The design need not have any events occurring at the specified clock time. Differences between test signals and the clock are highlighted with red diamonds in the Wave window.

To specify the comparison method, select **Tools > Waveform Compare > Options** and select the Comparison Method tab.

Figure 14-57. Comparison Methods Tab



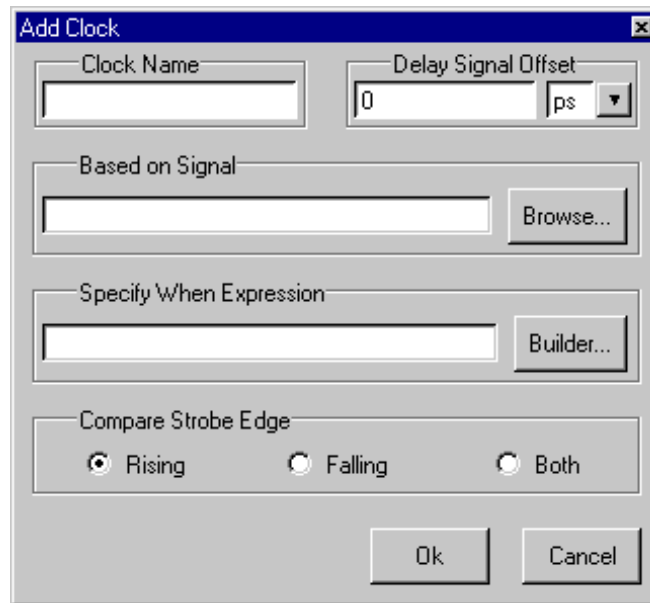
Continuous Comparison

Continuous comparisons are the default. You have the option of specifying leading and trailing tolerances and a when expression that must evaluate to "true" or 1 at the signal edge for the comparison to become effective.

Clocked Comparison

To specify a clocked comparison you must define a clock in the Add Clock dialog. You can access this dialog via the Clocks button in the Comparison Method tab or by selecting **Tools > Waveform Compare > Add > Clocks**.

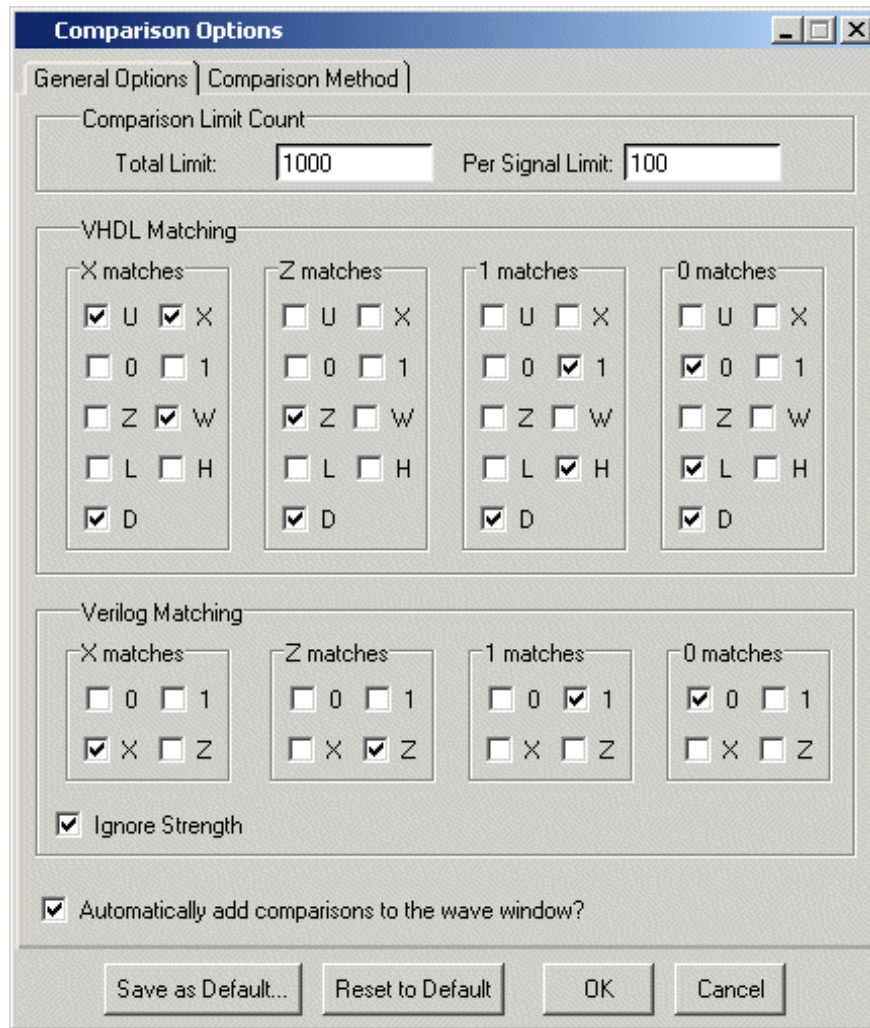
Figure 14-58. Adding a Clock for a Clocked Comparison



Setting Compare Options

There are a few "global" options that you can set for a comparison. Select **Tools > Waveform Compare > Options**.

Figure 14-59. Waveform Comparison Options

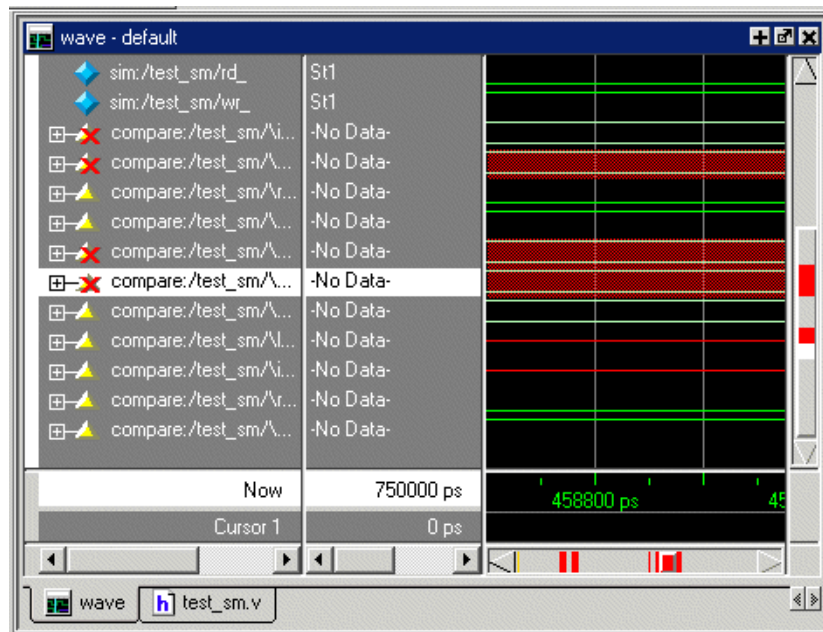


Options in this dialog include setting the maximum number of differences allowed before the comparison terminates, specifying signal value matching rules, and saving or resetting the defaults.

Viewing Differences in the Wave Window

The Wave window provides a graphic display of comparison results. Pathnames of all test signals included in the comparison are denoted by yellow triangles. Test signals that contain timing differences when compared with the reference signals are denoted by a red X over the yellow triangle.

Figure 14-60. Viewing Waveform Differences in the Wave Window



The names of the comparison objects take the form:

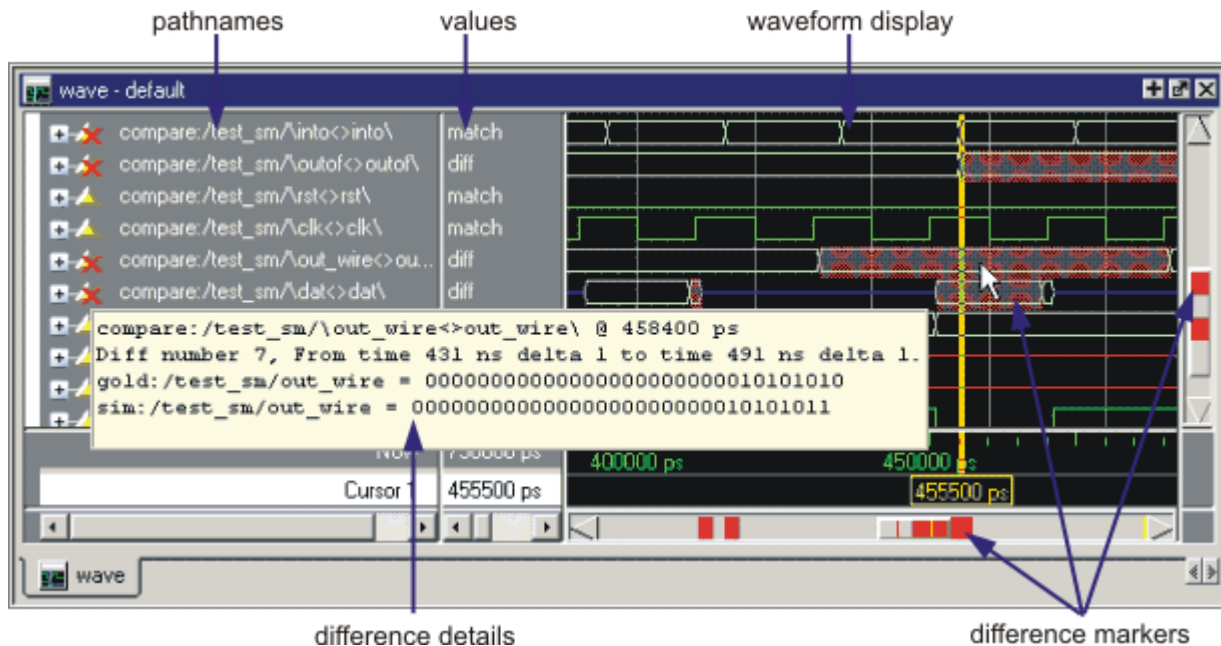
```
<path>/\refSignalName<>testSignalName\
```

If you compare two signals from different regions, the signal names include the uncommon part of the path.

In comparisons of signals with multiple bits, you can display them in "buswise" or "bitwise" format. Buswise format lists the busses under the compare object whereas bitwise format lists each individual bit under the compare object. To select one format or the other, click your right mouse button on the plus sign ('+') next to a compare object.

Timing differences are also indicated by red bars in the vertical and horizontal scroll bars of the waveform display, and by red difference markers on the waveforms themselves. Rectangular difference markers denote continuous differences. Diamond difference markers denote clocked differences. Placing your mouse cursor over any difference marker will initiate a popup display that provides timing details for that difference.

Figure 14-61. Waveform Difference Details and Markers



The values column of the Wave window displays the words "match" or "diff" for every test signal, depending on the location of the selected cursor. "Match" indicates that the value of the test signal matches the value of the reference signal at the time of the selected cursor. "Diff" indicates a difference between the test and reference signal values at the selected cursor.

Annotating Differences

You can tag differences with textual notes that are included in the difference details popup and comparison reports. Click a difference with the right mouse button, and select **Annotate Diff**. Or, use the [compare annotate](#) command.

Compare Icons

The Wave window includes six comparison icons that let you quickly jump between differences. From left to right, the icons do the following: find first difference, find previous annotated difference, find previous difference, find next difference, find next annotated difference, find last difference. Use these icons to move the selected cursor.



These buttons cycle through differences on all signals. To view differences for just the selected signal, press <tab> and <shift - tab> on your keyboard.

Note



If you have differences on individual bits of a bus, the compare icons will stop on those differences but <tab> and <shift - tab> will not.

The compare icons cycle through comparison objects in all open Wave windows. If you have two Wave windows displayed, each containing different comparison objects, the compare icons will cycle through the differences displayed in both windows.

Viewing Differences in the List Window

Compare objects can be displayed in the List window too. Differences are highlighted with a yellow background. Tabbing on selected columns moves the selection to the next difference (actually difference edge). Shift-tabbing moves the selection backwards.

Figure 14-62. Waveform Differences in the List Window

ns	delta	compare: /top/\clk<>clk	compare: /top/\paddr<>paddr	compare: /top/\prw<>prw	compare: /top/\pstrb<>pstrb	compare: /top/\prdy<>prdy
1980	+0	1 1 0 0 1 1 1 1	00001001 00001001	00000000000001001		
1985	+0	1 1 0 0 1 1 1 1	00001001 00001001	00000000000001001		
1990	+0	1 1 0 0 1 1 0 0	00001001 00001001	00000000000001001		
2000	+0	0 0 0 0 1 1 0 0	00001001 00001001	00000000000001001		
2020	+0	1 1 0 0 1 1 0 0	00001001 00001001	00000000000001001		
2025	+0	1 1 1 0 0 1 1 1	00000000 00001001	ZZZZZZZZZZZZZZZZ		
2035	+0	1 1 1 1 0 0 1 1	00000000 00000000	ZZZZZZZZZZZZZZZZ		
2040	+0	0 0 1 1 0 0 1 1	00000000 00000000	ZZZZZZZZZZZZZZZZ		
2060	+0	1 1 1 1 0 0 1 1	00000000 00000000	ZZZZZZZZZZZZZZZZ		
2065	+0	1 1 1 1 1 1 0 0	00000000 00000000	0000000000000000		
2080	+0	0 0 1 1 1 1 0 0	00000000 00000000	0000000000000000		
2100	+0	1 1 1 1 1 1 0 0	00000000 00000000	0000000000000000		
2105	+0	1 1 1 1 0 0 1 1	00000001 00000000	ZZZZZZZZZZZZZZZZ		
2120	+0	0 0 1 1 0 0 1 1	00000001 00000000	ZZZZZZZZZZZZZZZZ		
2140	+0	1 1 1 1 0 0 1 1	00000001 00000000	ZZZZZZZZZZZZZZZZ		
2145	+0	1 1 1 1 1 1 0 0	00000001 00000000	0000000000000001		
2160	+0	0 0 1 1 1 1 0 0	00000001 00000000	0000000000000001		
2180	+0	1 1 1 1 1 1 0 0	00000001 00000000	0000000000000001		

Right-clicking on a yellow-highlighted difference gives you three options: **Diff Info**, **Annotate Diff**, and **Ignore/Noignore** diff. With these options you can elect to display difference information, you can ignore selected differences or turn off ignore, and you can annotate individual differences.

Viewing Differences in Textual Format

You can also view text output of the differences either in the Transcript pane of the Main window or in a saved file. To view them in the transcript, select **Tools > Waveform Compare > Differences > Show**. To save them to a text file, select **Tools > Waveform Compare > Differences > Write Report**.

Saving and Reloading Comparison Results

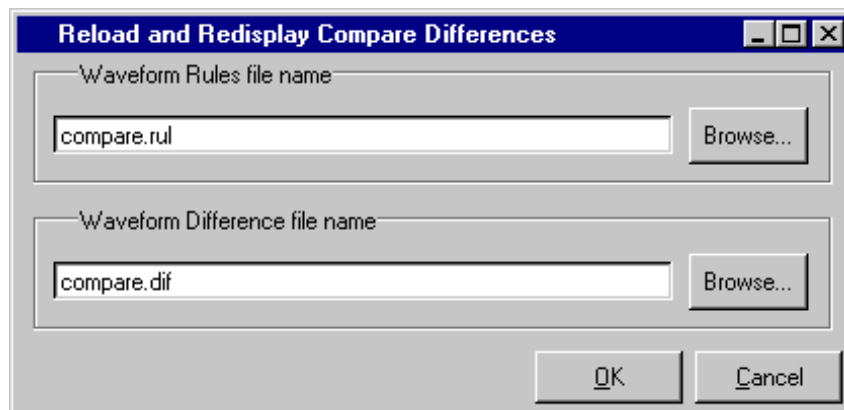
To save comparison results for future use, you must save both the comparison setup rules and the comparison differences.

To save the rules, select **Tools > Waveform Compare > Rules > Save**. This file will contain all rules for reproducing the comparison. The default file name is "*compare.rul*."

To save the differences, select **Tools > Waveform Compare > Differences > Save**. The default file name is "*compare.dif*."

To reload the comparison results at a later time, select **Tools > Waveform Compare > Reload** and specify the rules and difference files.

Figure 14-63. Reloading and Redisplaying Compare Differences



Comparing Hierarchical and Flattened Designs

If you are comparing a hierarchical RTL design simulation against a flattened synthesized design simulation, you may have different hierarchies, different signal names, and the buses may be broken down into one-bit signals in the gate-level design. All of these differences can be handled by ModelSim's Waveform Compare feature.

- If the test design is hierarchical but the hierarchy is different from the hierarchy of the reference design, you can use the `compare add` command to specify which region path in the test design corresponds to that in the reference design.
- If the test design is flattened and test signal names are different from reference signal names, the `compare add` command allows you to specify which signal in the test design will be compared to which signal in the reference design.
- If, in addition, buses have been dismantled, or "bit-blasted", you can use the `-rebuild` option of the `compare add` command to automatically rebuild the bus in the test design. This will allow you to look at the differences as one bus versus another.

If signals in the RTL test design are different in type from the synthesized signals in the reference design – registers versus nets, for example – the Waveform Compare feature will automatically do the type conversion for you. If the type differences are too extreme (say integer versus real), Waveform Compare will let you know.

Chapter 15

Debugging with the Dataflow Window

This chapter discusses how to use the Dataflow window for tracing signal values, browsing the physical connectivity of your design, and performing post-simulation debugging operations.

Dataflow Window Overview

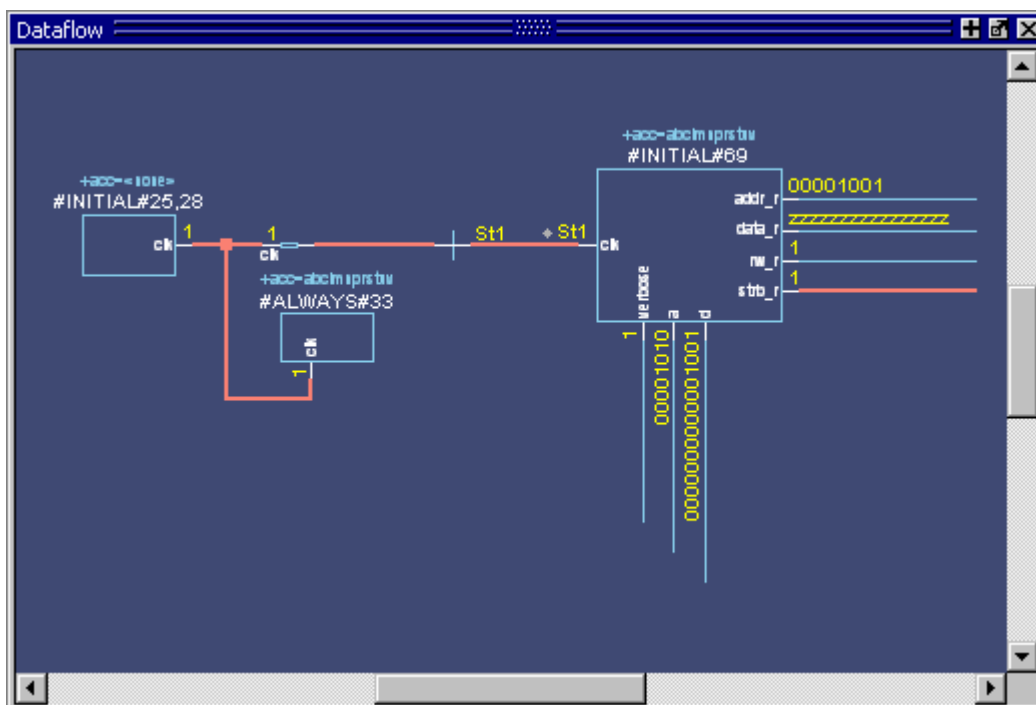
The Dataflow window allows you to explore the "physical" connectivity of your design; to trace events that propagate through the design; and to identify the cause of unexpected outputs.

Note



ModelSim versions operating without a dataflow license feature have limited Dataflow functionality. Without the license feature, the window displays the message "Extended mode disabled" and will show only one process and its attached signals or one signal and its attached processes.

Figure 15-1. The Dataflow Window

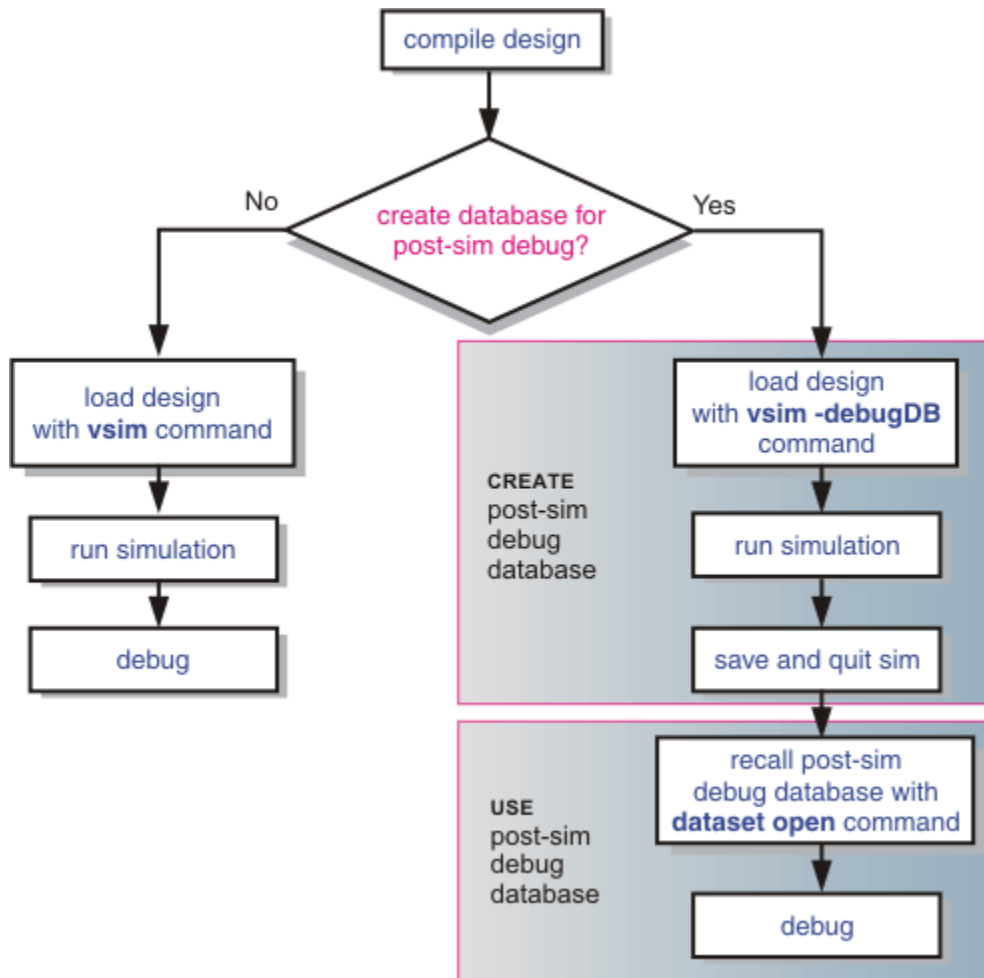


Dataflow Usage Flow

The Dataflow window can be used to debug the design currently being simulated, or to perform post-simulation debugging of a design. ModelSim is able to create a database for use with post-simulation debugging. The database is created at design load time, immediately after elaboration, and used later.

Figure 15-2 illustrates the current and post-sim usage flows for Dataflow debugging.

Figure 15-2. Dataflow Debugging Usage Flow



Post-Simulation Debug Flow Details

The post-sim debug flow for Dataflow analysis is most commonly used when performing simulations of large designs in simulation farms, where simulation results are gathered over extended periods and saved for analysis at a later date. In general, the process consists of two steps: creating the database and then using it. The details of each step are as follows:

Create the Post-Sim Debug Database

1. Compile the design using the `vlog` and/or `vcom` commands.
2. Load the design with the following commands:

```
vsim -debugDB=<db_pathname.dbg> -wlf <db_pathname.wlf> <design_name>  
add log -r /*
```

Specify the post-simulation database file name with the `-debugDB=<db_pathname>` argument to the `vsim` command. If a database pathname is not specified, ModelSim creates a database with the file name `vsim.dbg` in the current working directory. This database contains dataflow connectivity information.

Specify the dataset that will contain the database with `-wlf <db_pathname>`. If a dataset name is not specified, the default name will be `vsim.wlf`.

The debug database and the dataset that contains it should have the same base name (`db_pathname`).

The `add log -r /*` command instructs ModelSim to save all signal values generated when the simulation is run.

3. Run the simulation.
4. Quit the simulation.

The `-debugDB=<db_pathname>` argument to the `vsim` command only needs to be used once after any structural changes to a design. After that, you can reuse the `vsim.dbg` file along with updated waveform files (`vsim.wlf`) to perform post simulation debug.

A structural change is any change that adds or removes nets or instances in the design, or changes any port/net associations. This also includes processes and primitive instances. Changes to behavioral code are not considered structural changes. ModelSim does not automatically detect structural changes. This must be done by the user.

Use the Post-Simulation Debug Database

1. Start ModelSim by typing `vsim` at a UNIX shell prompt; or double-click a ModelSim icon in Windows.
2. Select **File > Change Directory** and change to the directory where the post-simulation debug database resides.
3. Recall the post-simulation debug database with the following:

```
dataset open <db_pathname.wlf>
```

ModelSim opens the `.wlf` dataset and its associated debug database (`.dbg` file with the same basename), if it can be found. If ModelSim cannot find `db_pathname.dbg`, it will attempt to open `vsim.dbg`.

Common Tasks for Dataflow Debugging

Common tasks for current and post-simulation Dataflow debugging include:

- [Adding Objects to the Dataflow Window](#)
- [Exploring the Connectivity of the Design](#)
- [Exploring Designs with the Embedded Wave Viewer](#)
- [Tracing Events \(Causality\)](#)
- [Tracing the Source of an Unknown State \(StX\)](#)
- [Finding Objects by Name in the Dataflow Window](#)

Adding Objects to the Dataflow Window

You can use any of the following methods to add objects to the Dataflow window:

- drag and drop objects from other windows
- use the **Add > To Dataflow** menu options
- use the [add dataflow](#) command
- double-click any waveform in the Wave window display

The **Add > To Dataflow** menu offers four commands that will add objects to the window:

- **View region** — clear the window and display all signals from the current region
- **Add region** — display all signals from the current region without first clearing the window
- **View all nets** — clear the window and display all signals from the entire design
- **Add ports** — add port symbols to the port signals in the current region

When you view regions or entire nets, the window initially displays only the drivers of the added objects. You can easily view readers as well by selecting an object selecting **Expand net to readers** from the right-click popup menu.

A small circle above an input signal on a block denotes a trigger signal that is on the process' sensitivity list.




Exploring the Connectivity of the Design

A primary use of the Dataflow window is exploring the "physical" connectivity of your design. One way of doing this is by expanding the view from process to process. This allows you to see the drivers/readers of a particular signal, net, or register.

You can expand the view of your design using menu commands or your mouse. To expand with the mouse, simply double click a signal, register, or process. Depending on the specific object you click, the view will expand to show the driving process and interconnect, the reading process and interconnect, or both.

Alternatively, you can select a signal, register, or net, and use one of the toolbar buttons or menu commands described in [Table 15-1](#).

Table 15-1. Icon and Menu Selections for Exploring Design Connectivity

	<p>Expand net to all drivers display driver(s) of the selected signal, net, or register</p>	<p>Add > To Dataflow > Expand net to drivers</p>
	<p>Expand net to all drivers and readers display driver(s) and reader(s) of the selected signal, net, or register</p>	<p>Add > To Dataflow > Expand net</p>
	<p>Expand net to all readers display reader(s) of the selected signal, net, or register</p>	<p>Add > To Dataflow > Expand net to readers</p>

As you expand the view, the layout of the design may adjust to show the connectivity more clearly. For example, the location of an input signal may shift from the bottom to the top of a process.

Limiting the Display of Readers

Some nets (such as a clock) in a design can have many readers. This can cause the display to draw numerous processes that you do not want to see when expanding the selected signal, net, or register. The dataflow display tests for the number of readers to be drawn and compares that number to a limit that you set in Dataflow Preferences (`outputquerylimit`). The default value of this limit is 100 (if you set `outputquerylimit` to 0, the test is not done). If this limit is exceeded, a dialog box asks whether you want all readers to be drawn. If you choose No, then no readers are displayed.

Note

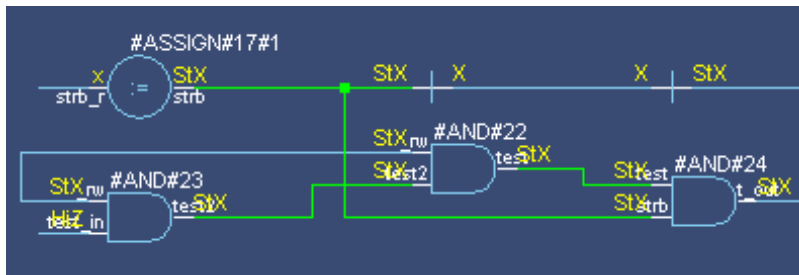


This limit does not affect the display of drivers.

Tracking Your Path Through the Design

You can quickly traverse through many components in your design. To help mark your path, the objects that you have expanded are highlighted in green.

Figure 15-3. Green Highlighting Shows Your Path Through the Design



You can clear this highlighting using the **Edit > Erase highlight** command or by clicking the **Erase highlight** icon in the toolbar.



Exploring Designs with the Embedded Wave Viewer

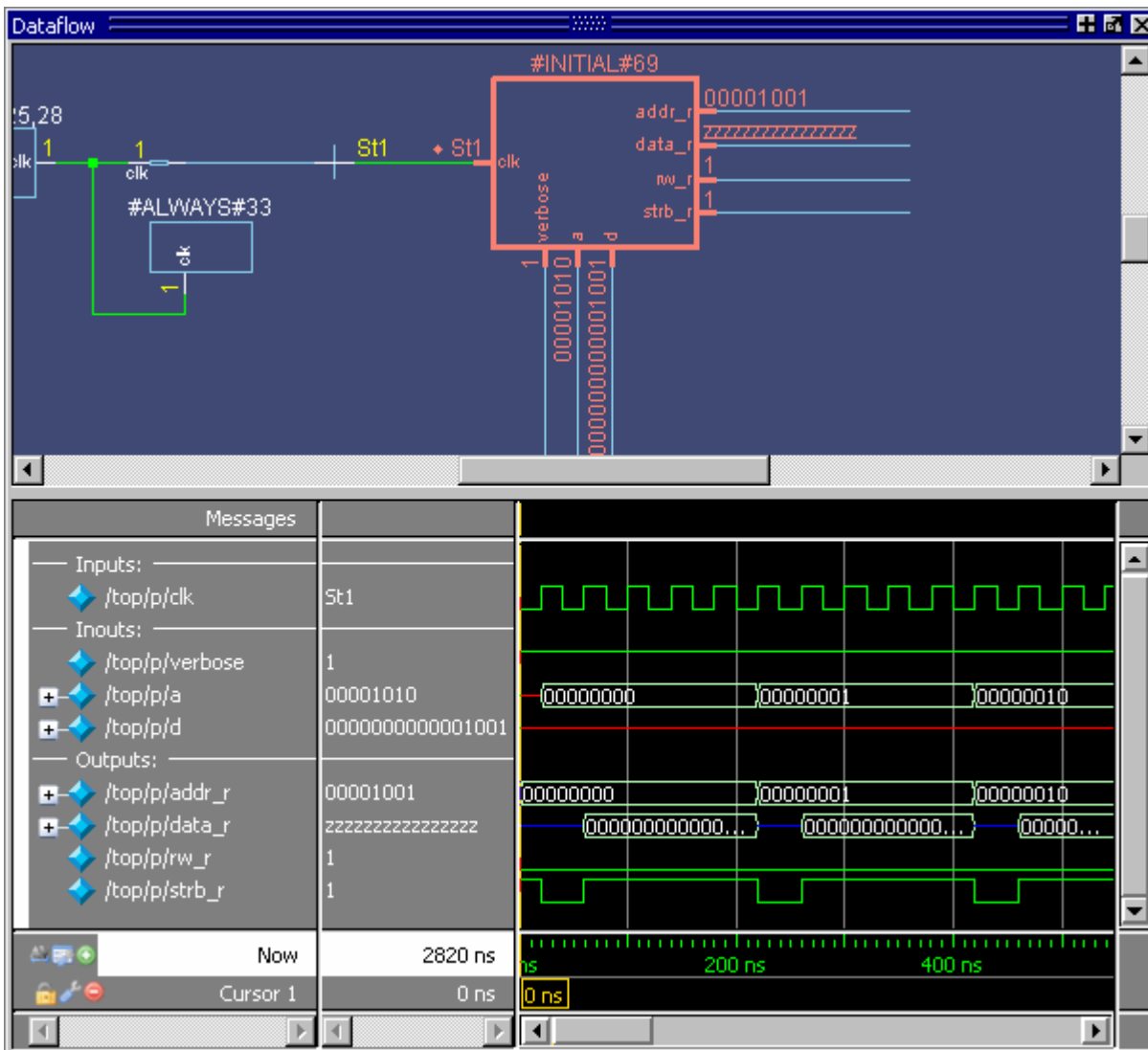
Another way of exploring your design is to use the Dataflow window's embedded wave viewer. This viewer closely resembles, in appearance and operation, the stand-alone Wave window (see [Waveform Analysis](#) for more information).

The wave viewer is opened using the **Dataflow > Show Wave** menu selection or by clicking the **Show Wave** icon.



One common scenario is to place signals in the wave viewer and the Dataflow panes, run the design for some amount of time, and then use time cursors to investigate value changes. In other words, as you place and move cursors in the wave viewer pane (see [Measuring Time with Cursors in the Wave Window](#) for details), the signal values update in the Dataflow window.

Figure 15-4. Wave Viewer Displays Inputs and Outputs of Selected Process



Another scenario is to select a process in the Dataflow pane, which automatically adds to the wave viewer pane all signals attached to the process.

See [Tracing Events \(Causality\)](#) for another example of using the embedded wave viewer.

Tracing Events (Causality)

You can use the Dataflow window to trace an event to the cause of an unexpected output. This feature uses the Dataflow window's embedded wave viewer (see [Exploring Designs with the Embedded Wave Viewer](#) for more details). First, you identify an output of interest in the dataflow pane, then use time cursors in the wave viewer pane to identify events that contribute to the output.

The process for tracing events is as follows:

1. Log all signals before starting the simulation (**add log -r /***).
2. After running a simulation for some period of time, open the Dataflow window and the wave viewer pane.
3. Add a process or signal of interest into the dataflow pane (if adding a signal, find its driving process). Select the process and all signals attached to the selected process will appear in the wave viewer pane.
4. Place a time cursor on an edge of interest; the edge should be on a signal that is an output of the process.

5. Right-click and select **Trace Next Event**. 

A second cursor is added at the most recent input event.

6. Keep selecting **Trace > Trace Next Event** until you've reached an input event of interest. Note that the signals with the events are selected in the wave viewer pane.

7. Right-click and select **Trace Event Set**. 

The Dataflow display "jumps" to the source of the selected input event(s). The operation follows all signals selected in the wave viewer pane. You can change which signals are followed by changing the selection.

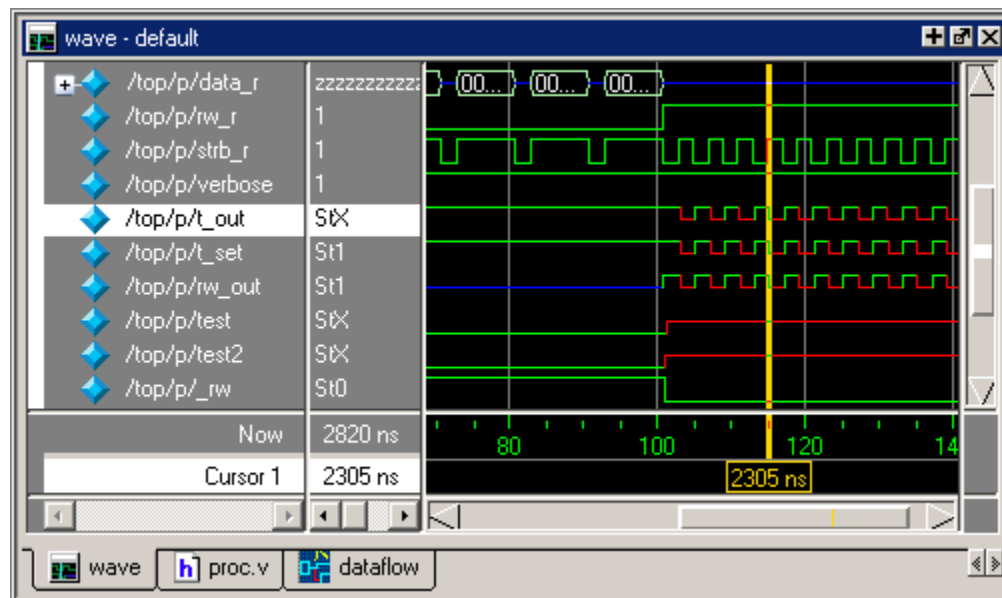
8. To continue tracing, go back to step 5 and repeat.

If you want to start over at the originally selected output, right-click and select **Trace Event Reset**.

Tracing the Source of an Unknown State (StX)

Another useful Dataflow window debugging tool is the ability to trace an unknown state (StX) back to its source. Unknown values are indicated by red lines in the Wave window ([Figure 15-5](#)) and in the wave viewer pane of the Dataflow window.

Figure 15-5. Unknown States Shown as Red Lines in Wave Window



The procedure for tracing to the source of an unknown state in the Dataflow window is as follows:

1. Load your design.
2. Log all signals in the design or any signals that may possibly contribute to the unknown value (**log -r /*** will log all signals in the design).
3. Add signals to the Wave window or wave viewer pane, and run your design the desired length of time.
4. Put a Wave window cursor on the time at which the signal value is unknown (StX). In [Figure 15-5](#), Cursor 1 at time 2305 shows an unknown state on signal *t_out*.
5. Add the signal of interest to the Dataflow window by doing one of the following:
 - o double-click on the signal's waveform in the Wave window,
 - o right-click the signal in the Objects window and select **Add > to Dataflow > Selected Signals** from the popup menu,
 - o select the signal in the Objects window and select **Add > to Dataflow > Selected Signals** from the menu bar.
6. In the Dataflow window, make sure the signal of interest is selected.
7. Trace to the source of the unknown by doing one of the following:
 - o If the Dataflow window is docked, make one of the following menu selections:
Tools > Trace > TraceX,
Tools > Trace > TraceX Delay,

Tools > Trace > ChaseX, or
Tools > Trace > ChaseX Delay.

- If the Dataflow window is undocked, make one of the following menu selections:
Trace > TraceX,
Trace > TraceX Delay,
Trace > ChaseX, or
Trace > ChaseX Delay.

These commands behave as follows:

- **TraceX / TraceX Delay**— **TraceX** steps back to the last driver of an X value. **TraceX Delay** works similarly but it steps back in time to the last driver of an X value. **TraceX** should be used for RTL designs; **TraceX Delay** should be used for gate-level netlists with back annotated delays.
- **ChaseX / ChaseX Delay** — **ChaseX** jumps through a design from output to input, following X values. **ChaseX Delay** acts the same as **ChaseX** but also moves backwards in time to the point where the output value transitions to X. **ChaseX** should be used for RTL designs; **ChaseX Delay** should be used for gate-level netlists with back annotated delays.

Finding Objects by Name in the Dataflow Window

Select **Edit > Find** from the menu bar, or click the Find icon in the toolbar, to search for signal, net, or register names or an instance of a component. This opens the search toolbar at the bottom of the Dataflow window.



With the search toolbar you can limit the search by type to instances or signals. You select **Exact** to find an item that exactly matches the entry you've typed in the **Find** field. The **Match case** selection will enforce case-sensitive matching of your entry. And the **Zoom to** selection will zoom in to the item in the **Find** field.

The **Find All** button allows you to find and highlight all occurrences of the item in the **Find** field. If **Zoom to** is checked, the view will change such that all selected items are viewable. If **Zoom to** is not selected, then no change is made to zoom or scroll state.

Automatically Tracing All Paths Between Two Nets

This behavior is referred to as point-to-point tracing. It allows you to visualize all paths connecting two different nets in your dataflow.

Prerequisites

- This feature is available during a live simulation, not when performing post-simulation debugging.

Procedure

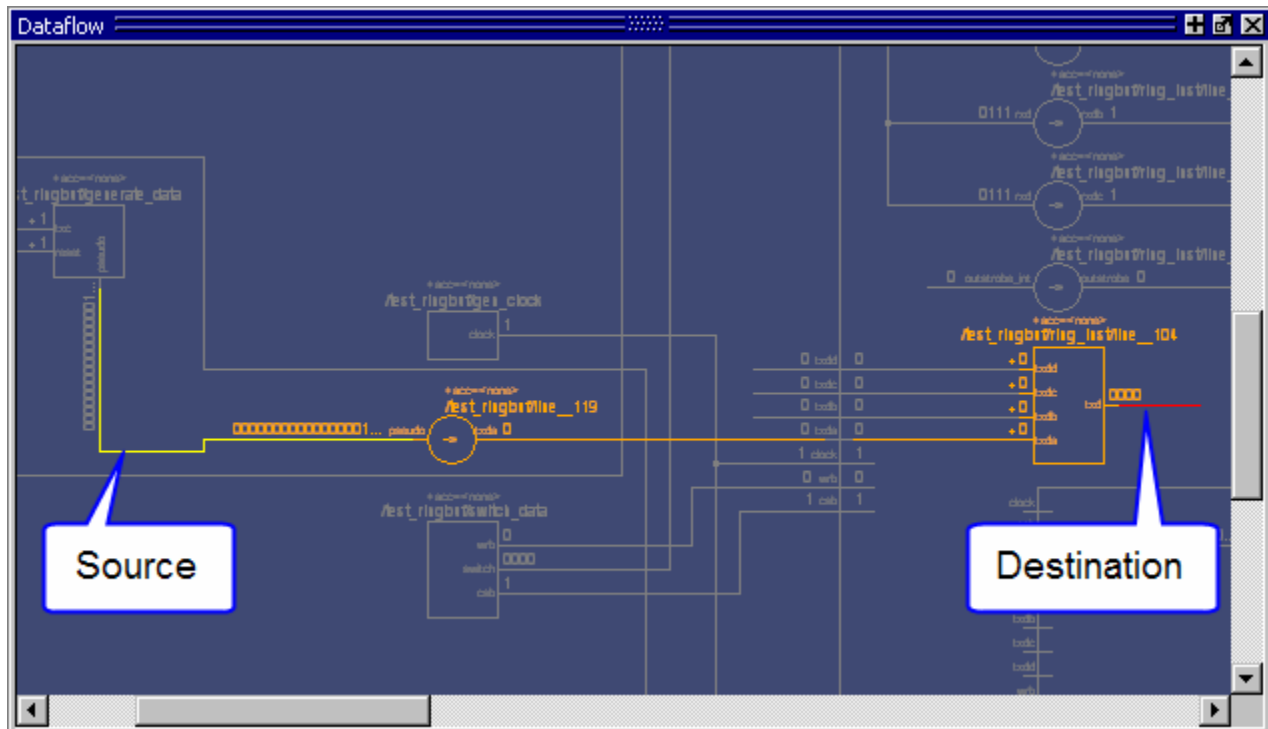
1. Select Source — Click on the net to be your source
2. Select Destination — Shift-click on the net to be your destination
3. Run point-to-point tracing — Right-click in the Dataflow window and select **Point to Point**.

Results

After beginning the point-to-point tracing, the Dataflow window highlights your design as shown in Figure 15-6:

1. All objects become gray
2. The source net becomes yellow
3. The destination net becomes red
4. All intermediate processes and nets become orange.

Figure 15-6. Dataflow: Point-to-Point Tracing



Related Tasks

- Change the limit of highlighted processes — There is a limit of 400 processes that will be highlighted.
 - a. **Tools > Edit Preferences**

- b. By Name tab
- c. **Dataflow > p2plimit** option
- Remove the point-to-point tracing
 - a. Right-click in the Dataflow window
 - b. Erase Highlights
- Perform point-to-point tracing from the command line
 - a. Determine the names of the nets
 - b. Use the `add dataflow` command with the `-connect` switch, for example:

```
add data -connect /test_ringbuf/pseudo /test_ringbuf/ring_inst/txd
```

where `/test_ringbuf/pseudo` is the source net and `/test_ringbuf/ring_inst/txd` is the destination net.

Dataflow Concepts

This section provides an introduction to the following important Dataflow concepts:

- [Symbol Mapping](#)
- [Current vs. Post-Simulation Command Output](#)

Symbol Mapping

The Dataflow window has built-in mappings for all Verilog primitive gates (for example, AND, OR, and so forth). For components other than Verilog primitives, you can define a mapping between processes and built-in symbols. This is done through a file containing name pairs, one per line, where the first name is the concatenation of the design unit and process names, (DUnit.Processname), and the second name is the name of a built-in symbol. For example:

```
xorg(only).pl XOR
org(only).pl OR
andg(only).pl AND
```

Entities and modules are mapped the same way:

```
AND1 AND
AND2 AND # A 2-input and gate
AND3 AND
AND4 AND
AND5 AND
AND6 AND
xnor(test) XNOR
```

Note that for primitive gate symbols, pin mapping is automatic.

The Dataflow window looks in the current working directory and inside each library referenced by the design for the file *dataflow.bsm* (.bsm stands for "Built-in Symbol Map"). It will read all files found.

User-Defined Symbols

You can also define your own symbols using an ASCII symbol library file format for defining symbol shapes. This capability is delivered via Concept Engineering's Nlview™ widget Symlib format.

For more specific details on this widget, see

www.model.com/support/documentation/BOOK/nlviewSymlib.pdf.

The Dataflow window will search the current working directory, and inside each library referenced by the design, for the file *dataflow.sym*. Any and all files found will be given to the Nlview widget to use for symbol lookups. Again, as with the built-in symbols, the DU name and optional process name is used for the symbol lookup. Here's an example of a symbol for a full adder:

```
symbol adder(structural) * DEF \  
  port a in -loc -12 -15 0 -15 \  
  pinattrdsp @name -cl 2 -15 8 \  
  port b in -loc -12 15 0 15 \  
  pinattrdsp @name -cl 2 15 8 \  
  port cin in -loc 20 -40 20 -28 \  
  pinattrdsp @name -uc 19 -26 8 \  
  port cout out -loc 20 40 20 28 \  
  pinattrdsp @name -lc 19 26 8 \  
  port sum out -loc 63 0 51 0 \  
  pinattrdsp @name -cr 49 0 8 \  
  path 10 0 0 7 \  
  path 0 7 0 35 \  
  path 0 35 51 17 \  
  path 51 17 51 -17 \  
  path 51 -17 0 -35 \  
  path 0 -35 0 -7 \  
  path 0 -7 10 0
```

Port mapping is done by name for these symbols, so the port names in the symbol definition must match the port names of the Entity|Module|Process (in the case of the process, it's the signal names that the process reads/writes).

Note



When you create or modify a symlib file, you must generate a file index. This index is how the Nlview widget finds and extracts symbols from the file. To generate the index, select **Tools > Create symlib index** (Dataflow window) and specify the symlib file. The file will be rewritten with a correct, up-to-date index.

Current vs. Post-Simulation Command Output

ModelSim includes [drivers](#) and [readers](#) commands that can be invoked from the command line to provide information about signals displayed in the Dataflow window. In live simulation mode, the [drivers](#) and [readers](#) commands will provide both topological information and signal values. In post-simulation mode, however, these commands will provide only topological information. Driver and reader values are not saved in the post-simulation debug database.

Dataflow Window Graphic Interface Reference

This section answers several common questions about using the Dataflow window's graphic user interface:

- [What Can I View in the Dataflow Window?](#)
- [How is the Dataflow Window Linked to Other Windows?](#)
- [How Can I Print and Save the Display?](#)
- [How Do I Configure Window Options?](#)
- [How Do I Zoom and Pan the Display?](#)

What Can I View in the Dataflow Window?

The Dataflow window displays:

- processes
- signals, nets, and registers
- interconnects

The window has built-in mappings for all Verilog primitive gates (for example, AND, OR, and so forth). For components other than Verilog primitives, you can define a mapping between processes and built-in symbols. See [Symbol Mapping](#) for details.

You cannot view SystemC objects in the Dataflow window; however, you can view HDL regions from mixed designs that include SystemC.

How is the Dataflow Window Linked to Other Windows?

The Dataflow window is dynamically linked to other debugging windows and panes as described in [Table 15-2](#).

Table 15-2. Dataflow Window Links to Other Windows and Panes

Window	Link
Main Window	select a signal or process in the Dataflow window, and the structure tab updates if that object is in a different design unit
Processes Window	select a process in either window, and that process is highlighted in the other
Objects Window	select a design object in either window, and that object is highlighted in the other
Wave Window	trace through the design in the Dataflow window, and the associated signals are added to the Wave window
	move a cursor in the Wave window, and the values update in the Dataflow window
Source Window	select an object in the Dataflow window, and the Source window updates if that object is in a different source file

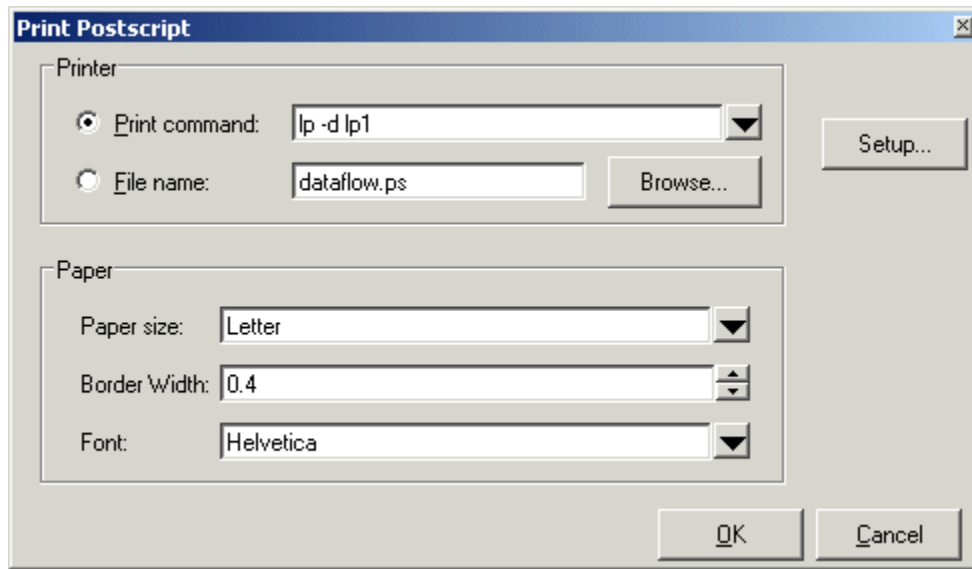
How Can I Print and Save the Display?

You can print the Dataflow window display from a saved *.eps* file in UNIX, or by simple menu selections in Windows. The Dataflow Page Setup dialog allows you to configure the display for printing.

Saving a *.eps* File and Printing the Dataflow Display from UNIX

With the Dataflow window active, select **File > Print Postscript** to setup and print the Dataflow display in UNIX, or save the waveform as a *.eps* file on any platform ([Figure 15-7](#)).

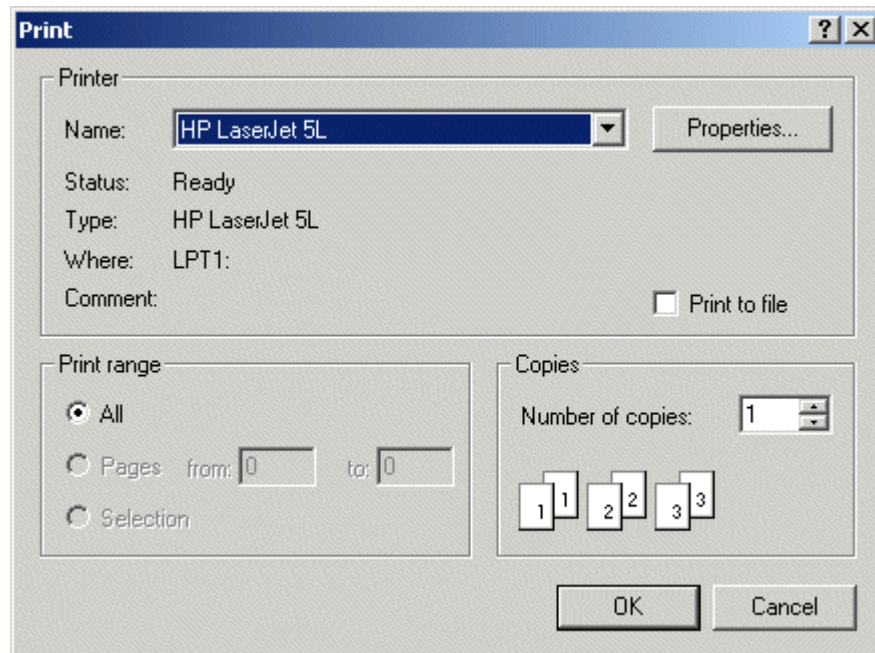
Figure 15-7. The Print Postscript Dialog



Printing from the Dataflow Display on Windows Platforms

With the Dataflow window active, select **File > Print** to print the Dataflow display or to save the display to a file (Figure 15-8).

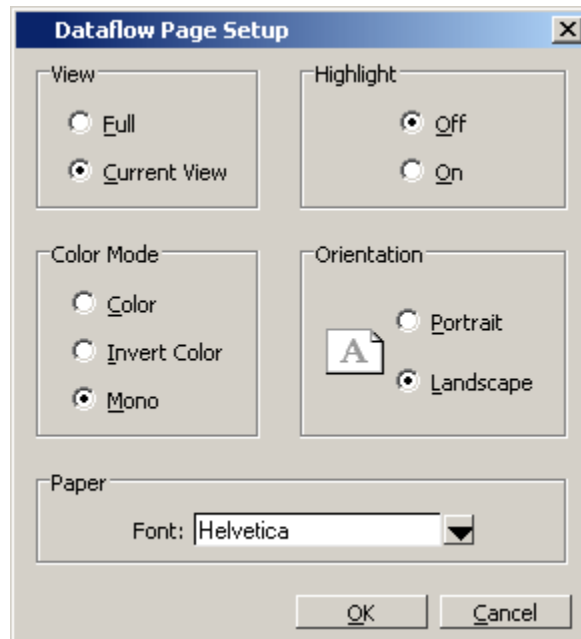
Figure 15-8. The Print Dialog



Configure Page Setup

With the Dataflow window active, select **File > Page setup** to open the Dataflow Page Setup dialog (Figure 15-9). You can also open this dialog by clicking the Setup button in the Print Postscript dialog (Figure 15-7). This dialog allows you to configure page view, highlight, color mode, orientation, and paper options.

Figure 15-9. The Dataflow Page Setup Dialog

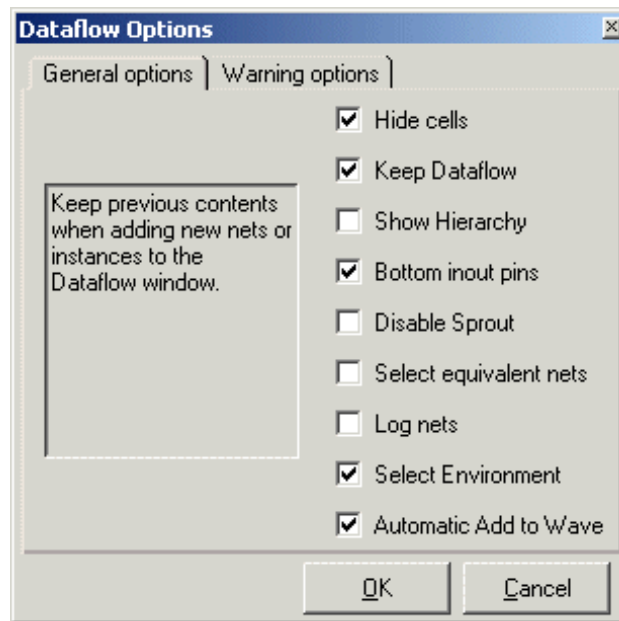


How Do I Configure Window Options?

You can configure several options that determine how the Dataflow window behaves. The settings affect only the current session.

Select **DataFlow > Dataflow Preferences > Options** to open the Dataflow Options dialog box.

Figure 15-10. Configuring Dataflow Options



How Do I Zoom and Pan the Display?

The Dataflow window offers tools for zooming and panning the display.

These zoom buttons are available from the Zoom toolbar:



Zoom In
zoom in by a factor
of two from the
current view



Zoom Out
zoom out by a
factor of two from
current view



Zoom Full
zoom out to view
the entire schematic

To zoom with the mouse, you can either use the middle mouse button or enter Zoom Mode by selecting **Dataflow > Zoom** and then use the left mouse button.

Four zoom options are possible by clicking and dragging in different directions:

- Down-Right: Zoom Area (In)
- Up-Right: Zoom Out (zoom amount is displayed at the mouse cursor)
- Down-Left: Zoom Selected
- Up-Left: Zoom Full

Panning with the Mouse

You can pan with the mouse in two ways:

- enter Pan Mode by selecting **Dataflow > Zoom > Pan** and then drag with the left mouse button to move the design
- hold down the <Ctrl> key and drag with the middle mouse button to move the design.

Panning with the Keyboard

- Arrow Keys — pans the window in the specified direction.
 - Unmodified — pans by a small amount.
 - Ctrl+<arrow key> — pans by a larger amount
 - Shift+<arrow key> — pans the view to the edge of the display

Chapter 16

Code Coverage

Code coverage is the only verification metric generated automatically from design source in RTL or gates. While a high level of code coverage is required by most verification plans, it does not necessarily indicate correctness of your design. It only measures how often certain aspects of the source are exercised while running a suite of tests.

Missing code coverage is usually an indication of one of two things: either unused code, or holes in the tests. Because it is automatically generated, code coverage is a metric achieved with relative ease, obtained early in the verification cycle. 100% code coverage can be achieved even for designs containing impossible to achieve coverage (because of sections containing unused code) by using a sophisticated exclusions mechanism (see “[Coverage Exclusions](#)”). Code coverage statistics are collected and can be saved into the Unified Coverage DataBase for later analysis.

This chapter includes the following topics related to code coverage.

Overview of Code Coverage Types	636
Language and Datatype Support	636
Usage Flow for Code Coverage Collection	636
Specifying Coverage Types for Collection	637
Enabling Simulation for Code Coverage Collection	638
Saving Code Coverage in the UCDB	639
Code Coverage in the UCDB	641
Code Coverage in the Graphic Interface	641
Code Coverage Types	644
Statement Coverage	644
Branch Coverage	644
Condition and Expression Coverage	645
Toggle Coverage	651
Finite State Machine Coverage	656
Coverage Exclusions	656
Coverage Reports	669
Notes on Coverage and Optimization	674

Note



The functionality described in this chapter requires a coverage license feature in your ModelSim license file. Please contact your Mentor Graphics sales representative if you currently do not have such a feature.

Overview of Code Coverage Types

ModelSim code coverage provides graphical and report file feedback on the following:

- **Statement coverage** — counts the execution of each statement on a line individually, even if there are multiple statements in a line.
- **Branch coverage** — counts the execution of each conditional “if/then/else” and “case” statement and indicates when a true or false condition has not executed.
- **Condition coverage** — analyzes the decision made in “if” and ternary statements and can be considered as an extension to branch coverage.
- **Expression coverage** — analyzes the expressions on the right hand side of assignment statements, and is similar to condition coverage.
- **Toggle coverage** — counts each time a logic node transitions from one state to another.
- **FSM coverage** — counts the states, transitions, and paths within a finite state machine.

For details related to each of these types of coverage, see “[Code Coverage Types](#)”.

Language and Datatype Support

ModelSim code coverage supports VHDL and Verilog/SystemVerilog language constructs. Code coverage does not work on SystemC design units.

Statement and Branch coverage have no limitations on support, however, sometimes optimizations can make it appear that statements or branches are uncovered. See “[Notes on Coverage and Optimization](#)” for more details.

For condition and expression coverage datatype support, see “[Condition and Expression Coverage](#)”.

For FSM coverage datatype support, see “[Finite State Machine Coverage](#)”.

For toggle coverage datatype support, see “[Toggle Coverage](#)”.

Usage Flow for Code Coverage Collection

To collect coverage data for a design, you must actively select the type of code coverage you want to collect, and then enable the coverage collection mechanism for the simulation run. You

can view coverage results during the current simulation run or save the coverage data to a UCDB for post-process viewing and analysis. The data can be saved either on demand, or at the end of simulation (see “[Saving Code Coverage Data On Demand](#)” and “[Saving Code Coverage at End of Simulation](#)”).



Tip: Design units compiled with **-nodebug** are ignored by coverage: they are treated as if they were excluded.

The basic flow for collecting code coverage in a ModelSim simulation is as follows:

1. Compile the design and specify the types of coverage to collect:

```
vlog top.v proc.v
```

```
vopt top -o opttop +cover
```

The vlog (or vcom, if design is VHDL) command compiles the specified files. The -o specifies the output name for the optimized version of the design. The +cover argument to the vopt command designates all coverage types for collection.

You may wish to apply coverage arguments differently, depending on whether you want to collect coverage for a specific source file, or just a module/sub-module, or the entire design. See “[Specifying Coverage Types for Collection](#)” for coverage application options.

2. Enable coverage collection during simulation:

```
vsim -coverage opttop
```

Coverage is enabled for the entire design using the optimized design *opttop*. See “[Enabling Simulation for Code Coverage Collection](#)” for further details.

3. Optionally, you can save the collected information for post-process viewing and analysis:

```
coverage save -onexit top.ucdb
```

This command saves the coverage data at the end of simulation, in the current directory in *top.ucdb*. See “[Saving Code Coverage in the UCDB](#)” for a list of all methods for saving data to a UCDB.

Specifying Coverage Types for Collection

When specifying the coverage types for collection, you are essentially instructing the code to collect coverage statistics when coverage collection is enabled at run time. Since extra instructions reduce simulation performance, you should only enable code for which you intend to collect coverage statistics.

You can apply coverage to:

- specific **source files** in the design — by supplying the +cover arguments to [vcom](#) or [vlog](#) during compile:

```
vlog top.v proc.v cache.v +cover=bcesfx -coveropt 1
```

- specific **modules or instance** of design —by supplying the +cover arguments to [vopt](#), using the +<selection> modifier to designate the desired design units or instances:

```
vlog top.v proc.v cache.v
```

```
vopt -o top_opt +cover=bcesxf+moduleA +cover=st+/top/proc/cache
```

```
vsim -coverage top_opt
```

- **entire design**, globally — by supplying the +cover arguments to [vopt](#):

```
vlog top.v proc.v cache.v
```

```
vopt -o top_opt +cover=bcesxf
```

```
vsim -coverage top_opt
```

or by supplying the +cover arguments using vsim -voptargs (when not specifically using vopt):

```
vlog top.v proc.v cache.v
```

```
vsim -coverage top -voptargs="+cover=bcesfx"
```

For information on the use of +cover= arguments and how the union of coverage arguments apply, see “[Union of Coverage Types](#)”.

Union of Coverage Types

For all coverage type arguments specified with “+cover=”, the arguments applied are a union of all arguments for a given module or design unit. For example, if module A was compiled with the argument +cover=xf (extended toggle and FSM) and the entire design (containing modules A, B and C) was optimized with +cover=bce, the coverage results would be:

```
Module A - bcefx
```

```
Module B - bce
```

```
Module C - bce
```

This union of arguments does not apply to the optimization number specified with -coveropt <1-4>. In this case, any optimization level applied to a design unit or module takes precedence over the globally specified -coveropt level.

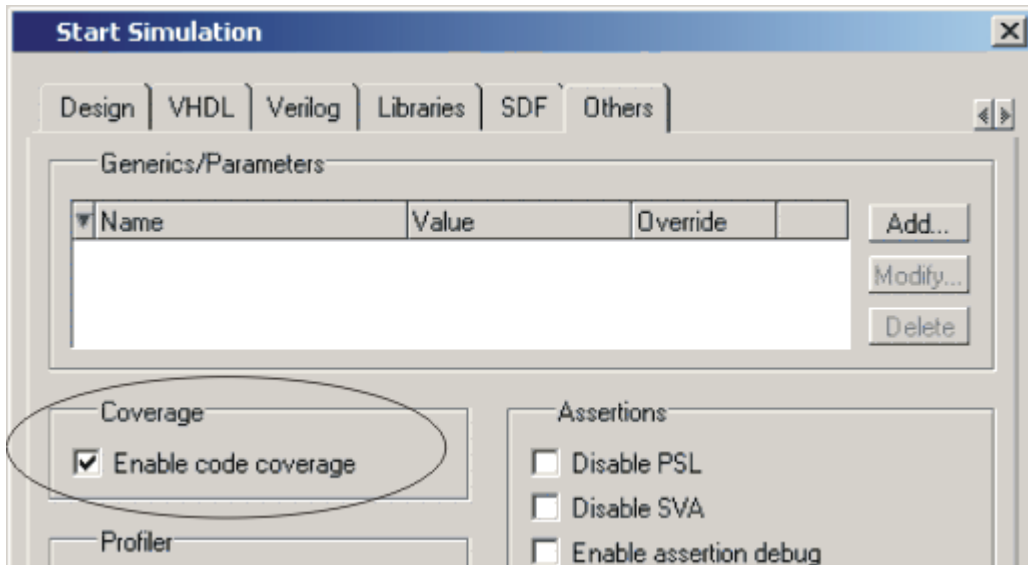
Enabling Simulation for Code Coverage Collection

Once the coverage types have been specified for coverage (“[Specifying Coverage Types for Collection](#)”), enable the simulation to collect the code coverage statistics using one of the following methods:

- CLI command: Use the **-coverage** argument to **vsim**. For example,

```
vsim -coverage work.top
```
- GUI: **Simulate > Start Simulation > Others > Enable Code Coverage** checkbox, as shown in [Figure 16-1](#).

Figure 16-1. Enabling Code Coverage in the Start Simulation Dialog



Saving Code Coverage in the UCDB

When you run a design with coverage enabled you can save the code coverage that was collected for later use, either on demand or at the end of simulation. By default, even if coverage is enabled, the tool will not save the data unless you explicitly specify that the data should be saved.

Often, users simulate designs multiple times, with the intention of capturing different coverage data from each test for post-process viewing and analysis. When this is the case, the naming of the tests becomes important. By default, the name ModelSim assigns to a test is the same as the UCDB file base name. If you fail to name the test you run explicitly, you can unintentionally overwrite your data.

To explicitly name a test **before** saving the UCDB, use a command such as:

```
coverage attribute -test mytestname
```

Saving Code Coverage Data On Demand

Options for saving coverage data dynamically (during simulation) or in coverage view mode are:

- GUI: **Tools > Coverage Save**

This brings up the Coverage Save dialog box, where you can specify coverage types to save, select the hierarchy, and output UCDB filename.

- CLI command: coverage save

During simulation, the [coverage save](#) command saves data from the current simulation into a UCDB file called *myfile1.ucdb*:

```
coverage save myfile1.ucdb
```

While viewing results in Coverage View mode, you can make changes to the data (using the [coverage attribute](#) command, for example). You can then save the changed data to a new file using the following command:

```
coverage save myfile2.ucdb
```

To save coverage results only for a specific design unit or instance in the design, use a command such as:

```
coverage save -instance <path> ... <dbname>
```

The resulting UCDB, *<dbname>.ucdb*, contains only coverage results for that instance, and by default, all of its children. For full command syntax, see [coverage save](#).

- Verilog System Task:
\$coverage_save (code coverage only)

This non-standard SystemVerilog system task saves code coverage data only, whereas the other methods capture all coverage types. For that reason, it is not recommended. For more information, see “[System Tasks and Functions Specific to the Tool](#).”

Saving Code Coverage at End of Simulation

By default, coverage data is not automatically saved at the end of simulation. To enable the auto-save of coverage data, set a legal filename for the data using any of the following methods:

- Set the *modelsim.ini* file variable: **UCDBFilename**="*<filename>*"

By default, *<filename>* is an empty string ("").

- Specify at the *Vsim>* prompt: **coverage save -onexit** command

The **coverage save** command preserves instance-specific information. For example:

```
coverage save -onexit myoutput.ucdb
```

- Execute the SystemVerilog command: **\$set_coverage_db_name(<filename>)**

If more than one method is used for a given simulation, the last command encountered takes precedence. For example, if you issue the command **coverage save -onexit vsim.ucdb**, but your SystemVerilog code also contains a **\$set_coverage_db_name()** task, with no name specified, coverage data is not saved for the simulation.

Code Coverage in the UCDB

ModelSim stores saved coverage statistics in a Unified Coverage DataBase (UCDB) file, a single persistent database that is the repository for all coverage data — both code coverage and functional coverage.

Once the UCDB coverage data is saved, you can:

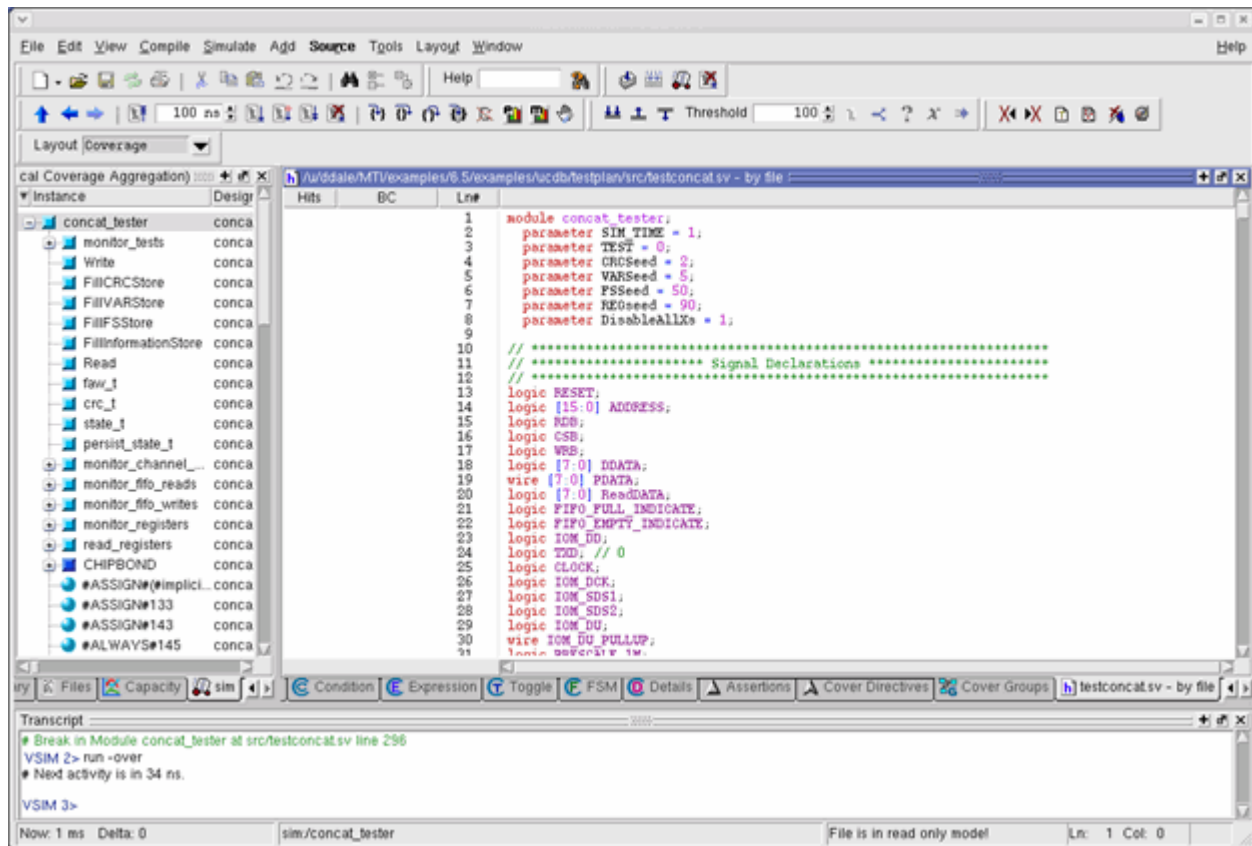
- Analyze coverage statistics in the GUI, either interactively with an active simulator, or in a post-processing mode with `vsim -viewcov` (see “[Usage Flow for Code Coverage Collection](#)”)
- Run and view reports on the collected code coverage data (see “[Coverage Reports](#)”)
- Exclude certain data from the coverage statistics (see “[Excluding Objects from Coverage](#)”)
- View, merge, and rank sets of code coverage data without elaboration of the design or a simulation license. You can also merge test data with a verification plan. See the “[Verification Management](#)” chapter.

For information on working with both functional coverage and code coverage in the verification of your design, see the “[Verification Management](#)” chapter.

Code Coverage in the Graphic Interface

When you simulate a design with code coverage enabled, coverage data is displayed in several window tabs ([Figure 16-2](#)). You can also write coverage statistics in different text and HTML reports (see “[Coverage Reports](#)”). You can save raw coverage data to a UCDB (see “[Code Coverage in the UCDB](#)”) and recall, or merge it with coverage data from previous simulations.

Figure 16-2. Coverage Data is Shown in Window Tabs



The table below summarizes the coverage windows. For further details on what exactly is in these windows, see “[Windows Containing Code Coverage Data](#)”.

Table 16-1. Coverage Windows


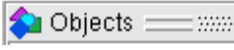


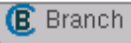




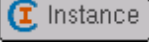

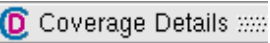
Coverage window	Description
 Structure (sim)	Use this window as a design navigation aid. Displays coverage data and graphs for each design object or file, including coverage from child instances compiled with coverage arguments. By default, the information is displayed for only the local instance, non-recursively. You can select to view coverage recursively by selecting Code Coverage > Enable Recursive Coverage Sums . Columns are available for all types of code coverage. See “ Code Coverage in Structure Window ”.
 Objects	Use as your center for Toggle Coverage analysis. Displays details of toggle coverage. Various columns show the toggle numbers collected for each variable and signal shown in the window. Details window will populate for each selected object. See “ Toggle Coverage in the Objects Window ”.

Table 16-1. Coverage Windows

Coverage window	Description
Source  testconcat.sv - by file	Most useful for statement and branch coverage analysis. Displays source code for covered items. See “ Coverage Data in the Source Window ”.
Missed <Coverage_Type>      	Use this window to perform in-depth analysis of incomplete coverage numbers. Windows: Missed Coverage, Missed Branch, Missed Condition, Missed Expression, Missed Toggle, Missed FSM. Displays missed coverage (anything with less than 100% coverage) for the selected design object or file. Click on each line to display details of object in Details window. See “ Missed Coverage Windows ”.
Instance Coverage 	Use this window as the primary navigation tool when exploring code coverage numbers. Displays coverage statistics for each instance. It recursively shows all child instances under the currently selected region in the Structure window. Use this window for analysis based on sorting by coverage numbers. See “ Instance Coverage Window ”.
Current Exclusions 	Displays all currently active exclusions, whether they originate from source-based pragma exclusions, from the “coverage exclude” command, or from various GUI exclusion actions. See “ Current Exclusions Window ”.
Details 	Displays details of missed statement, branch, condition, expression, and toggle coverage. When you select items in Missing <Coverage type>, Objects, or Source windows, the details populate in this window. Used to perform in-depth analysis of incomplete coverage numbers. See “ Coverage Details Window ”.

Understanding Unexpected Coverage Results

When you encounter unexpected coverage results, it may be helpful to keep in mind the following special circumstances related to collecting coverage statistics:

- Optimizations affect coverage results. See “[Notes on Coverage and Optimization](#)”.

- Poorly planned or executed merges can produce unexpected results. One example: if you improperly apply the `-strip` and `-install` options of “`vcover merge`”).
- Package bodies, whether VHDL or SystemVerilog, are not instance-specific: ModelSim sums the counts for all invocations no matter who the caller is.
- All standard and accelerated VHDL packages are ignored for coverage statistics calculation.
- You may find that design units or instances excluded from code coverage will appear in toggle coverage statistics reports. This happens when ports of the design unit or instance are connected to nets that have toggle coverage turned on elsewhere in the design.

Code Coverage Types

Code coverage types are:

- [Statement Coverage](#)
- [Branch Coverage](#)
- [Condition and Expression Coverage](#)
- [Toggle Coverage](#)
- [Finite State Machine Coverage](#)

Statement Coverage

Statement coverage is the most basic form of coverage supported by ModelSim. The metric for statement coverage is the count of how many times a given statement is executed during simulation. Multiple statements may be present on a single line of HDL source code. Each such statement is processed independently of other statements on the same line. Statement coverage counts are prominently displayed in the Source Window. They are present in most of the other coverage windows as well.

Branch Coverage

Branch coverage is related to statement coverage. It is related to branching constructs such as “if” and “case” statements. Both true and false branches are measured. In order to achieve 100% branch coverage, each branching statement in the source code must have taken both the true and false paths.

For “if” statements without a corresponding “else”, an implicit branch known as the “allfalse” (or “all false”) branch is measured. If the “if” condition is executed and found to be false, the allfalse branch is considered to be hit. In the following VHDL example,

```
if (fsel = "10") then
```

```
        z <= a;
    elsif (fsel = "11") then
        z <= b;
    end if;
```

the allfalse branch is hit when “fsel” is not equal to 2 or 3. In the following Verilog example:

```
if (fsel == INDF_ADDRESS) begin
    fileaddr <= fsr[6:0];
end
```

the allfalse branch is hit when “fsel” is not equal to INDF_ADDRESS.

You can exclude an allfalse branch from participation in branch coverage using the **-allfalse** argument to a pragma exclusion or the [coverage exclude](#) command.

For “case” statements, the case expression itself is not considered a branch. Rather, each case item is considered a separate and independent branch. To achieve 100% branch coverage in a “case” statement, each case item must have been executed and found to contain both true and false values during simulation.

In order to gain more coverage detail on the HDL expressions used in branching statements, the Condition and Expression Coverage features may be used (see “[Condition and Expression Coverage](#)”).

Condition and Expression Coverage

A variety of condition and expression coverage metrics can be calculated and presented using ModelSim. Use them accordingly, to suit your purposes:

- User Defined Primitive (UDP) — The term is borrowed from the Verilog language, which uses the same basic table format to model user-defined primitives.

UDP truth tables are composed of columns that correspond to each input of the targeted condition or expression. The right-most column corresponds to the expression’s output value. The table rows correspond to combinations of input and output values. Values can be ‘0’, ‘1’, or ‘-’ (don’t-care). ‘Z’ values are automatically excluded. When the simulator evaluates an expression, each UDP row is examined. If the current values match the given row, the row is said to be hit, and its hit count increments. If all rows have non-0 hit counts, the expression or condition has reached 100% coverage. See “[UDP Coverage Details and Examples](#)” for further details on UDP analysis.

- Focused Expression Coverage (FEC) — a different style of measurement than UDP, also based on truth table evaluation.

FEC checks that every input has taken both true and false values under conditions that allow it to control the output. See “[FEC Coverage Details and Examples](#)” for further details on report output and analysis.

- Sum-of-Products — based on UDP data
Sum-of-Products checks that each set of inputs that satisfies the expression (results in a “1”) must be exercised at least once, but not necessarily independently.
- Basic Sub-Condition — based on UDP data
Basic sub-condition checks that each subexpression has been both true and false.

Effect of Short-circuiting on Expression and Condition Coverage

By default, the simulator follows LRM rules for short-circuit evaluation for Verilog and VHDL expressions. In brief, for Verilog, the &&, ||, and ternary operators short-circuit. And for VHDL, expressions are short-circuited when their operands are of boolean or bit types, and the expression is purely composed of logical operators.

For example, in the following expression, if A has a value of '0', the term B || C will never be evaluated:

```
Z <= A && (B || C);
```

Short-circuit evaluation remains in effect per LRM rules when coverage is enabled.

However, you may want to analyze the coverage results when short-circuit evaluation is turned off, and all terms in an expression are considered in an evaluation. To achieve this effect, use the **-nocovershort** argument to `vlog/vcom/vopt`. Generally, expression and condition coverage percentages are lower when short-circuit evaluation is active, since, on average, less inputs are considered when evaluating expressions and conditions.

A brief short-circuit status is given in the Details window and the text coverage report for each condition and expression.

Reporting Condition and Expression Coverage

UDP / FEC:

- By default, when coverage is enabled with the “+cover=ec” argument (where “=ec” enables expression and condition coverage) to `vcom/vlog` or `vopt`, both the UDP and FEC style of coverage statistics are collected and reported.
- Turn off FEC statistics collection using the **-nocoverfec** argument to `vcom/vlog`, or `vopt`.
- You can print condition and expression coverage truth tables in coverage reports by:
 - GUI: Select **Coverage Reports > Condition Coverage** or **Expression Coverage** (see [Coverage Reports](#))

- Command Line: with `coverage report -details`, when one or more of the rows has a zero hit count. To force the table to be printed even when it is 100% covered, apply the `-dump` argument to the coverage report command.
- The default maximum limit for the number of rows allowed in a UDP table is 192. The number of input patterns allowed for FEC is also 192. You can customize this limit using either the `vlog` or `vcom -maxfecrows/-maxudprows` arguments, or the `CoverMaxFECRows/CoverMaxUDPRows` *modelsim.ini* file variables.
- FEC detailed analysis metrics are reported in detail using a command such as:

```
coverage report -details -fecanalysis
```

or

```
vcover report -details -fecanalysis
```

Sum-of-Products / Basic Sub-Condition:

- The Sum-of-Products and Basic Sub-Condition calculations are based on the UDP data and can be reported in detail using a command such as:

```
coverage report -details -metricanalysis
```

or

```
vcover report -details -metricanalysis
```

FEC Coverage Details and Examples

Focused Expression Coverage (FEC) is a code coverage metric for condition and expression coverage. FEC checks that every input has taken both true and false values under conditions that allow it to control the output. FEC is an important part of Modified Condition and Decision Coverage (MCDC) methodologies. An excellent reference on MCDC is NASA's article entitled "A Practical Tutorial on Modified Condition / Decision Coverage", available on the web.

Example 16-1. FEC-based Expression Coverage Example

An example FEC report table is as follows:

```
# Focused expression coverage for file <filename> --
#
# -----Focused Expression-----
# Line      36 Stmt      1      assign a = a | b;
# Expression totals: 2 out of 4 rows covered = 50.0%
#   Row      Hits FEC Target      Matching input patterns
#     1:         6      a_0      {00}
#     2:  ***0***      a_1      {10}
#     3:         6      b_0      {00}
#     4:  ***0***      b_1      {01}
#
```

FEC ensures that each input (ab[1] and ab[2]) has been shown to independently affect the expression output. FEC is measured by verifying that the targeted input holds its critical output activation state (0 or 1) while all other inputs are in a quiescent condition.

In effect, this calculation can help to determine if there is a functional bug in the logic that is feeding the targeted input (FEC Target). This ensures that the effects of such a bug are not masked by other terms in the expression's logic. (i.e. the expression's other input terms do not dominate the expression output). However, FEC does not guarantee that downstream logic (not in the expression itself) will not mask the value of the expression's output.

One method of raising FEC coverage numbers is to modify test stimulus such that appropriate patterns appear at the expression's inputs, matching input for FEC rows currently not covered.

You can report matching input patterns using the **-fecanalysis** argument to the [vcover report](#) or [coverage report](#) commands.

UDP Coverage Details and Examples

Condition coverage analyzes the decision made in "if" and ternary statements and can be considered an extension to branch coverage. Expression coverage analyzes the activity of expressions on the right-hand side of assignment statements, and is similar to condition coverage. See [Example 16-2](#).

Expression coverage analyzes the expressions on the right hand side of assignment statements and counts when these expressions are executed. For expressions that involve logical operators, a truth table is constructed and counts are tabulated for conditions matching rows in the truth table. See [Example 16-4](#).

A truth table is constructed for the condition or expression, and counts are kept for each row of the truth table that occurs.

Example 16-2. UDP Condition Truth Table

For example, consider the following IF statement:

```
Line 180: IF (a or b) THEN x := 0; else x := 1; endif;
```

It reflects a truth table as shown in [Table 16-2](#):

Table 16-2. Condition UDP Truth Table for Line 180

Truth table for line 180				
	counts	a	b	(a or b)
Row 1	5	1	-	1
Row 2	0	-	1	1
Row 3	8	0	0	0

Table 16-2. Condition UDP Truth Table for Line 180

Truth table for line 180				
	counts	a	b	(a or b)
unknown	0			

Row 1 indicates that $(a \text{ or } b)$ is true if a is true, no matter what b is. The "counts" column indicates that this combination has executed 5 times. The '-' character means "don't care." Likewise, row 2 indicates that the result is true if b is true no matter what a is, and this combination has executed zero times. Finally, row 3 indicates that the result is always zero when a is zero and b is zero, and that this combination has executed 8 times. The unknown row indicates how many times the line was executed when one of the variables had an unknown state.

If more than one row matches the input, each matching row is counted. If you would prefer no counts to be incremented on multiple matches, set "[CoverCountAll](#)" to 0 in your *modelsim.ini* file to reverse the default behavior. Alternatively, you can use the **-covercountnone** argument to [vsim](#) to disable the count for a specific invocation.

Example 16-3. Vectors in UDP Condition Truth Table

Values that are vectors are treated as subexpressions external to the table until they resolve to a boolean result. For example, take the IF statement:

Line 38:IF ((e = '1') AND (bus = "0111")) ...

A UDP truth table will be generated in which $\text{bus} = "0111"$ is evaluated as a subexpression and the result, which is boolean, becomes an input to the truth table. The truth table looks as follows:

Table 16-3. Condition UDP Truth Table for Line 38

Truth table for line 38				
	counts	e	(bus="0111")	(e='1') AND (bus = "0111")
Row 1	0	0	-	0
Row 2	10	-	0	0
Row 3	1	1	1	1
unknown	0			

Index expressions also serve as inputs to the table. Conditions containing function calls cannot be handled and will be ignored for condition coverage.

If a line contains a condition that is uncovered — that is, some part of its truth table was not encountered — that line will appear in the **Missed Conditions** window > **Conditions** tab. When

that line is selected, the condition truth table will appear in the Details window and the line will be highlighted in the Source window.

Example 16-4. Expression UDP Truth Table

For the statement:

```
Line 236: x <= a xor (not b(0));
```

The following truth table results, with the associated counts.

Table 16-4. Expression UDP Truth Table for line 236

Truth table for line 236				
	counts	a	b(0)	(a xor (not b(0)))
Row 1	1	0	0	1
Row 2	0	0	1	0
Row 3	2	1	0	0
Row 4	0	1	1	1
unknown	0			

If a line contains an expression that is uncovered (some part of its truth table was not encountered) that line appears in the Missed <Coverage_type> window under the Expressions tab. When that line is selected, the expression truth table appears in the Details window and the line will be highlighted in the Source window.

VHDL Condition and Expression Type Support

Condition and expression coverage supports bit, boolean and std_logic types. Arbitrary types are supported when they involve a relational operator with a boolean result. These types of subexpressions are treated as an external expression that is first evaluated and then used as a boolean input to the full condition. The subexpression can look like:

(var <relop> const)

or:

(var1 <relop> var2)

where var, var1 and var2 may be of any type; <relop> is a relational operator (e.g., ==, <, >, >=); and const is a constant of the appropriate type.

Expressions containing only one input variable are ignored, as are expressions containing vectors. Logical operators (e.g., and, or, xor) are supported for std_logic/std_ulogic, bit, and boolean variable types.

When condition or expression coverage is enabled, all VHDL expression inputs are converted to one of 4 states: 0, 1, X, or Z. In particular, a common scenario is for U to be converted to X, which can sometimes visibly affect simulation results.

Verilog/SV Condition and Expression Type Support

For Verilog/SV condition and expression coverage, as in VHDL, arbitrary types are supported when they involve a relational operator with a boolean result. Expressions containing only one input variable are ignored, as are expressions resulting in vector values. Logical operators (&& || ^, for example) are supported for one-bit net, logic, and reg types.

Toggle Coverage

Toggle coverage is the ability to count and collect changes of state on specified nodes, including:

- Verilog and SystemVerilog signal types: net, register, bit, enum and integer (which includes shortint, int, longint, byte, real, integer, fixed-size multi-dimensional arrays, structures, and time). SystemVerilog integer types are treated as 32-bit registers and counts are kept for each bit.
- VHDL signal types: boolean, bit, bit_vector, enum, integer, std_logic/std_ulogic, and std_logic_vector/std_ulogic_vector.

There are two modes of toggle coverage operation - standard (or 2-state) and extended (or 3-state). Extended coverage allows a more detailed view of test bench effectiveness and is especially useful for examining coverage of tri-state signals. (It helps to ensure, for example, that a bus has toggled from high 'Z' to a '1' or '0', and a '1' or '0' back to a high 'Z'.)

When compiling or simulating, specify standard (2-state) toggle using the “t” code, and extended (3-state) toggle using the “x” code. See “[Specifying Toggle Coverage Statistics Collection](#)” for more information on this topic.

Toggle coverage can be excluded from statistics collection, though proper management of exclusions is important. See “[Toggle Exclusion Management](#)” for information on this topic.

Toggle Coverage and Performance Considerations

Toggle coverage can be expensive in terms of performance since it applies so many object in simulations. The following [vcom](#), [vlog](#), and [vsim](#) options help control performance and capacity when toggle coverage is in effect: -togglecountlimit, -togglewidthlimit, -togglevlogint, -togglemaxintvalues, -togglevlogreal, -togglemaxrealvalues, -togglefixedsizearray, and -togglemaxfixedsizearray.

VHDL Toggle Coverage Type Support

Supported types for toggle coverage are: boolean, bit, enum, integer, std_logic/std_ulogic, and arrays of these types. Counts are recorded for each enumeration value and a signal is considered “toggled” if all the enumerations have non-zero counts.

For VHDL integers, a record is kept of each value the integer assumes and an associated count. The maximum number of values recorded is determined by a limit variable that can be changed on a per-signal basis. The default is 100 values. The limit variable can be turned off completely with the **-notoggleints** option for the `vsim` command or setting `ToggleNoIntegers` in the `modelsim.ini` file. The limit variable can be increased by setting the `vsim` command line option **-togglemaxintvalues**, setting `ToggleFixedSizeArray` in the `modelsim.ini` file, or setting the Tcl variable `ToggleMaxIntValues`.

For VHDL arrays, toggles are counted when the array has less than `ToggleWidthLimit` elements (see “[Limiting Toggle Coverage](#)”).

Multi-dimensional arrays, arrays-of-arrays, records, and access types are not supported for VHDL toggle coverage.

Verilog/SV Toggle Coverage Type Support

Supported types for toggle coverage are net, register, bit, logic, fixed-size multi-dimensional array (both packed and unpacked), real, enum, integer atoms (i.e. integer, time, byte, shortint, int, and longint), packed unions, and structures (both packed and unpacked) with fields of types supported for toggle coverage. For objects of non-scalar type, toggle counts are kept for each bit of the object. Dynamic arrays, associative arrays, queues, unpacked unions, classes, class-like objects such as mailbox and semaphore, and events do not participate in toggle statistics gathering.

SystemVerilog integer types are treated as toggle nodes unless the **-notogglevlogints** argument is applied to the `vsim` command line, or the `ToggleVlogIntegers` variable is turned off in `modelsim.ini`. The simulator breaks up integers into individual bits and counts them as toggle nodes.

SystemVerilog real types (real, shortreal) are not treated as toggle nodes by default. To treat them as toggle nodes, use the `vsim` command's **-togglevlogreal** argument or turn on the `ToggleVlogIntegers` variable in `modelsim.ini`. When toggle collection is in effect for SV real types, a record is kept of each value the real assumes and an associated count. The maximum number of values recorded is determined by a limit variable. The default is 100 values. The limit variable can be increased by setting the `vsim` command line option **-togglemaxrealvalues**, or setting “`ToggleMaxRealValues`” in the `modelsim.ini` file.

SystemVerilog packed types include sophisticated data structures such as packed struct, packed union, tagged packed union, multi-dimensional packed arrays, enumerated types, and compositions of these types. By default, toggle coverage is reported for each dimension or

member of such types. However, you can control this by making use of the **-togglepackedasvec** argument to the `vsim` command. This option causes coverage to be reported as if the object was an equivalent one-dimensional packed array with the same overall number of bits. The “**TogglePackedAsVec**” `modelsim.ini` variable provides a default value for **-togglepackedasvec**.

Objects of enumerated types are considered to be covered if all of the enumeration values occur during simulation. However, the **-togglevlogenumbits** argument to the `vsim` command can be used to cause the object to be treated as an equivalent packed array of bit or logic type. The “**ToggleVlogEnumBits**” `modelsim.ini` variable provides a default value for **-togglevlogenumbits**.

SystemVerilog unpacked array support is limited to fixed-size arrays. See the **-togglefixedsizearray** and **-togglemaxfixedsizearray** arguments to the `vsim` command. Other kinds of unpacked arrays (dynamic arrays, associative arrays, and queues) are not supported for toggle coverage. The **-togglepackedasvec** option only applies to the packed dimensions of multi-dimensional SystemVerilog arrays.

SystemVerilog unpacked structs are supported as long as all struct elements consist of supported data types. Unpacked structs are broken into their fields and toggle coverage for each field is calculated individually.

Understanding Toggle Counts

This section defines what is considered as a “toggle” during a simulation.

All toggle coverage ignores zero-delay glitches: they do not count. Also, initialization values are not counted.

Standard and Extended Toggle coverage (for bits)

Standard (2-state) toggle coverage only counts Low or 0 <--> High or 1 transitions. Extended (3-state) toggle coverage counts these transitions plus the following:

```
Z <--> 1 or H
Z <--> 0 or L
```

For extended toggle coverage, a signal is considered toggled if and only if:

- it has 0->1 and 1->0 transitions and NO Z transitions, or
- if there are ANY Z transitions, it must have ALL four of the Z transitions.

Moreover — whether in standard or extended mode — all reg, logic, and bit *variables* are considered as toggled when both (0L->1H, 1H->0L) columns have nonzero values.

Specifying Toggle Coverage Statistics Collection

You can specify that toggle coverage statistics be collected for a design, either standard toggle or extended, using any of the following methods:

- Compile (vcom/vlog) using the argument `+cover=` with either 't' or 'x'. See “[Specifying Coverage Types for Collection](#)” for more information.
- Entering the `toggle add` command at the command line.
- Select **Tools > Toggle Coverage > Add** or **Tools > Toggle Coverage > Extended** in the Main window menu.

Using the Toggle Add Command

The `toggle add` command allows you to initiate toggle coverage at any time from the command line. Upon the next running of the simulation, toggle coverage data will be collected according to the arguments employed (i.e., the **-full** argument enables collection of extended toggle coverage statistics).

Note



If you use a toggle add command on a group of signals to get standard toggle coverage, then try to convert to extended toggle coverage with the “`toggle add -full`” command on the same signals, nothing will change. The only way to change the internal toggle triggers from standard to extended toggle coverage is to restart vsim and use the correct command.

Using the Main Window Menu Selections

You can enable toggle coverage by selecting **Tools > Toggle Coverage > Add** or **Tools > Toggle Coverage > Extended** from the Main window menu. These selections allow you to enable toggle coverage for Selected Signals, Signals in Region, or Signals in Design.

After making a selection, toggle coverage statistics will be captured the next time you run the simulation.

Limiting Toggle Coverage

The `ToggleCountLimit` *modelsim.ini* variable limits the toggle coverage count for a toggle node. After the limit is reached, further activity on the node will be ignored for toggle coverage. All possible transition edges must reach this count for the limit to take effect. For example, if you are collecting toggle data on 0->1 and 1->0 transitions, both transition counts must reach the limit. If you are collecting "full" data on 6 edge transitions, all 6 must reach the limit. The default setting for this variable is 1. If the limit is set to zero, then it is treated as unlimited.

If you want different toggle count limits on different design units, use the **-togglecountlimit** argument for **vcom** or **vlog**. The **-countlimit** argument for the **toggle add** command will set a count limit on a specific node.

If you want to override the **ToggleCountLimit** variable everywhere, like for a batch run, use the **-togglecountlimit** argument for **vsim**.

The **ToggleWidthLimit** *modelsim.ini* variable limits the maximum width of signals that are automatically added to toggle coverage with the **+cover=t** argument to **vcom** or **vlog**. The default limit is 128. A value of 0 is taken as "unlimited." This limit is designed to filter out memories from toggle coverage. The limit applies to Verilog registers and VHDL arrays. If the register or array is larger than the limit, it is not added to toggle coverage.

You can change the default toggle width limit on a design unit basis with the **-togglewidthlimit** argument for **vcom**, **vlog**, or **vsim**.

The **-widthlimit** argument for the **toggle add** command will set the width limit for signals on a specific node.

Viewing Toggle Coverage Data in the Objects Window

To view toggle coverage data in the Objects window right-click in the window to open a context popup menu the **Toggle Coverage** selection. When highlighted, this selection allows you to display toggle coverage data for the **Selected Signals**, the **Signals in Region**, or the **Signals in Design**.

Toggle coverage data is displayed in the Objects window in multiple columns, as shown below. There is a column for each of the six transition types. Right click any column name to toggle that column on or off. See [Toggle Coverage in the Objects Window](#) for more details on each column.

Figure 16-3. Toggle Coverage Data in the Objects Window

Name	Value	Kind	Mode	1H->0L	0L->1H	0L->Z	Z->0L	1H->Z	Z->1H	#Nodes	#Toggled	% Toggled	% 01	% Full	% Z
into	0100000000...	Reg	Internal	119628	119629	0	0	0	0	32	11	34.38%	34.38%	11.46%	0%
outof	0000000000...	Reg	Internal	20800	20804	0	0	0	0	32	6	18.75%	21.88%	7.292%	0%
rst	0	Reg	Internal	2	1	0	0	0	0	1	1	100%	100%	33.33%	0%
clk	1	Reg	Internal	83222	83223	0	0	0	0	1	1	100%	100%	33.33%	0%
out_wire	0000000000...	Net	Internal	20800	20804	0	0	0	0	32	6	18.75%	21.88%	7.292%	0%
dat	0000000000...	Net	Internal	23401	28607629308634542	119620	114418			32	6	18.75%	21.88%	47.92%	60.94%
addr	0000100000	Net	Internal	26006	26007	0	0	0	0	10	4	40%	40%	13.33%	0%
loop	xxxxxxxxxxxx...	Reg	Internal	0	0	0	0	0	0	32	0	0%	0%	0%	0%
i	x	Variable	Internal												
rd_	St0	Net	Internal	15602	15601	0	0	0	0	1	1	100%	100%	33.33%	0%
wr_	St1	Net	Internal	7803	7803	0	0	0	0	1	1	100%	100%	33.33%	0%

Finite State Machine Coverage

Because of the complexity of state machines, FSM designs can contain a higher than average level of defects. It is important, therefore, to analyze the coverage of FSMs in RTL before going to the next stages of synthesis in the design cycle.

Refer to the chapter “[Finite State Machines](#)” for additional information.

Coverage Exclusions

Exclusions are stored in the UCDB. This allows report generation based on the most recent snapshot of coverage state.

What Objects can be Excluded?

You can exclude the following from coverage statistics collection:

- Any number of lines or files containing various constructs such as states, branches, expressions and conditions.
- Condition and expression truth table rows (see “[Exclude Rows from UDP and FEC Truth Tables](#)”).
- FSM transitions and states (see [FSM Coverage Exclusions](#)).
- Toggles (see [Toggle Exclusion Management](#)).

Exclusions can be instance or file specific. You can also exclude nodes from toggle statistics collection using “[coverage exclude -code t](#)” or “[toggle disable](#)”.

Auto Exclusions

The compiler (vcom/vlog/vopt) in automatically applies exclusions to certain code constructs. One good example is assertion code, which is normally not considered part of the “design”, and is not normally desired to count for or against code coverage.

Another case is in FSMs state exclusions. By default, when a state is excluded, all transitions to and from that state are excluded. This behavior is called "auto exclusion." To explicitly control auto exclusion, set the [vsim](#) argument -autoexclusionsdisable. For example, you can use the following command to turn off the auto exclusion feature for FSMs:

```
vsim <your vsim args> -autoexclusionsdisable=fsm
```

To change the default behavior of the tool, set the variable [AutoExclusionsDisable](#) to in the *modelsim.ini* file.

Excluding Objects from Coverage

ModelSim includes the following mechanisms for excluding coverage from the UCDB.

- Using the GUI:
 - Right-click a file in Files window and select **Code Coverage > Exclude Selected File** from the popup menu.
 - Right-click an entry in one of the Missed <Coverage Type> windows and select **Exclude Selection** or **Exclude Selection For Instance <inst_name>** from the popup menu.
 - Right-click a line in the Hits column of the Source window and select **Exclude Coverage Line xxx**, **Exclude Coverage Line xxx For Instance <inst_name>**, or **Exclude Entire File**.
- Using source code pragmas to exclude individual code coverage (bces) metrics. See [“Exclude Individual Metrics with Pragmas”](#).
- Using the CLI:
 - The [coverage exclude](#) command excludes code coverage items. Examples:

```
coverage exclude -du <du_name> //excludes particular design unit
coverage exclude -du *          //excludes entire design
```

Specific CLI commands are available to:

- Manage toggle coverage and exclusions (see [“Toggle Exclusion Management”](#))
- [Exclude Rows from UDP and FEC Truth Tables](#)
- [Exclude Any/All Coverage Data in a Single File](#)

Exclude Individual Metrics with Pragmas

ModelSim also supports the use of source code pragmas to selectively turn coverage off and on for individual code coverage metrics. Pragmas allow you to turn statement, branch, condition, expression, toggle and FSM coverage on and off independently. See [“Exclude Nodes from Toggle Coverage”](#) for toggle pragma, and [“FSM Coverage Exclusions”](#) for FSM coverage pragma.

The pragmas supported are as follows.

```
coverage on           See "coverage on and coverage off Pragma Syntax"
coverage off
coverage never
coverage fsm_off
coverage toggle_ignore
```

```
pragma synthesis_off
pragma synthesis_on
pragma translate_off
pragma translate_on
vcs coverage on
vcs coverage off
vnavigatoroff
vnavigatoron
```

Usage

- Each pragma is preceded in the code line by either a “//” (Verilog) or “--” (VHDL). For example:

```
// coverage never      (Verilog)
-- coverage never      (VHDL)
```

- Bracket the line(s) you want to exclude with these pragmas. For example:

```
-- coverage on b
...
...
-- coverage off b
```

- The “pragma” keyword can also be replaced with either “synopsys”, “mentor”, or “synthesis”.
- Pragmas are enforced at the design unit level only, and must be placed inside a design unit scope.

For example, if you place “-- coverage off” inside an architecture body, all the following statements in that architecture are excluded from coverage; however, statements in all subsequent design units are included in statement coverage (until the next “-- coverage off”). If you place a pragma outside a design unit scope, it has no effect.

- The “coverage on|off” pragma only applies to branches, conditions, expressions, and statements.
- For information on toggle exclusions, see “[Toggle Exclusion Management](#)”.
- The “fsm_off” pragma selectively turns coverage off and on for FSM states and transitions:

```
// coverage fsm_off <fsm_name> (Verilog)
-- coverage fsm_off <fsm_name> (VHDL)
```

For more detailed information, see “[Exclude FSM with Pragma](#)”.

- The “coverage never” pragma turns off coverage completely. It takes effect at compile time, and thus can never provide coverage statistics for specified areas of the design unless the “coverage never” pragma is removed and the design recompiled. In contrast, “coverage off” and “coverage on” pragmas are simply report-time options, and thus the

coverage statistics for the specified items can be toggled on and off via the GUI or the [coverage exclude](#) command.

- The “coverage off” and “coverage on” pragmas turn on and off coverage for specified items. If no coverage items are specified, all items are affected.

coverage on and coverage off Pragma Syntax

Two forms of the coverage on/off pragma are available. The first form is used to make general exclusions of specific coverage types, or for all types if none are specified. The second form, called fine-grained exclusion, is used to exercise very precise control over exclusions in complex code constructs.

Syntax for general exclusions:

```
coverage {on | off} [sbec]
```

Syntax for fine-grained exclusions:

```
coverage {on | off}
  [-item {b c e s} {[<int> | <int>-<int>]+}]
  [-allfalse]
  [-condrow [<int>|<int>-<int>]+]
  [-exprrow [<int>|<int>-<int>]+]
  [-feccondrow [<int>|<int>-<int>]+]
  [-fecexprrow [<int>|<int>-<int>]+]
```

where:

[sbec]

selectively turns on/off statement coverage (“s”), branch (“b”), expression (“e”), or condition (“c”). If no coverage type is specified, all are affected.

-item

selectively turns on/off branch (“b”), condition (“c”), expression (“e”) or statement coverage (“s”) only for the line of code immediately following the pragma. Requires both a specification for type of coverage and an integer specifying the item numbers (<int>) for the line immediately following pragma. Item number can be specified as an integer or a series of integers (item 1 or items 2-4). Multiple items may be specified separated by whitespace.

-allfalse

affects only the “all false” branch from the branch coverage of a specified “if” statement. This argument is only valid for use with “coverage on -item b <item#>”.

The term “allfalse” is being used as a name for an implicit branch at the end of an “if” or “if-else” decision tree. The allfalse branch is considered to be hit when none of the conditions in the decision tree are true. An allfalse branch doesn’t exist for any decision tree which ends with a bare “else”. For further details on “all false” and how it applies to the code, see [“Branch Coverage”](#).

- condrow
affects only the specified rows from the UDP table of the specified condition. Only valid for use with “coverage on -item c <item#>”.
- fecondrow
affects only the specified rows from the FEC table of the specified condition. Only valid for use with “coverage on -item c <item#>”.
- exprrow
affects only the specified rows from the UDP table of the specified expression. Only valid for use with “coverage on -item e <item#>”.
- fecexprrow
affects only the specified rows from the FEC table of the specified expression. Only valid for use with “coverage on -item e <item#>”.

Usage

- The effect of the “coverage on/off” pragma exclusion is limited to the next valid line of source code after excluding all blank lines and comments.
- The -item argument to “coverage on/off” selectively turns on/off coverage for statements, branches, conditions and expressions for the next line of code.
- You can combine two or more coverage items in one coverage pragma if the item numbers are the same. For example,

```
(// coverage off -item bs 2)
```

turns off coverage for statement #2 and branch #2 of the next line.

- To exclude/include different item numbers for different coverage items, use two different pragmas.

```
// coverage on -item b 2  
// coverage on -item c 3-5
```

turns on coverage for branch #2 and condition #3,4,5 of the next line.

- You can use multiple line numbers and ranges in one pragma.

```
// coverage on -item s 1 3-5 7-9 11
```

- For Branches, enabling/disabling coverage for the (case) branch automatically enables/disables coverage for all its branches even if they are not on the same line of the (case) branch. You can override the coverage of a certain branch by an additional pragma that changes coverage of this branch.
- For Conditions, you can selectively turn coverage on/off for certain UDP condition rows and FEC condition rows using the -condrow and -fecondrow arguments. For example,

```
// coverage off -item c 1 -condrow 1 3-5
```

excludes UDP condition rows (1, 3, 4, 5) of the first condition item from coverage.

- For Expressions, the same functionality can be achieved using `-exprrow` and `-fecexprrow` options.

```
// coverage off -item e 1 -fecexprrow 1-4 6
```

excludes FEC expression rows (1, 2, 3, 4, 6) of the first expression item from coverage.

Examples

- Exclude all the following conditions, and expressions, statement, branches, until a “`// coverage on`” pragma is reached, or the end of the design unit is reached.

```
// coverage off
```

- Exclude 1st row from the UDP table of the first condition on the next line

```
-- coverage off -item c 1 -condrow 1
```

- Exclude the 2nd branch and 2nd statement from the next line

```
-- coverage off -item bs 2
```

- Exclude 3rd, 5th and 6th statements from statement coverage

```
// coverage off -item s 3 5-6
```

- Include coverage for 2nd and 3rd branches, and condition #4 of the next line

```
// coverage on -item b 2-3  
// coverage on -item c 4
```

- Exclude only the allfalse branch from the 4th branch on the next line

```
-- coverage off -item b 4 -allfalse
```

- Exclude both of these rows from the following line of code:

- 1st row in UDP table and 2nd row in FEC table of 2nd expression, and the
- 3rd row in UDP table and 4th row in FEC table of 2nd condition

```
-- coverage off -item ce 2 -condrow 3 -feccondrow 4
```

Exclude Rows from UDP and FEC Truth Tables

You can exclude lines and rows from condition and expression UDP truth tables using the **coverage exclude** command or the “`coverage off`” pragma. For more details, see the [coverage exclude](#) command and “[coverage on and coverage off Pragma Syntax](#)”.

Exclude Any/All Coverage Data in a Single File

In cases where you would like to exclude all types of coverage data in a given source file, use the [coverage exclude](#) command. It can be used to exclude any / all of the following types of coverage:

- Lines within a source file

- Rows within a condition or expression truth table
- Instances or design units
- Transitions or states within a Finite State Machine

A *.do* file is created when the user does a **File > Save** with the Current Exclusions window active. The default name of the *.do* file is *exclude.do*.

Example 16-5. Creating Coverage Exclusions with a *.do* File

Suppose you are doing a simulation of a design and you want to exclude selected lines from each file in the design and all mode INOUT toggle nodes. You can put all exclusions in a *.do* file and name it, say, *exclusions.do*. The contents of the *exclusions.do* file might look like this:

```
coverage exclude -srcfile xyz.vhd -linerange 12 55 67-90
coverage exclude -srcfile abc.vhd -linerange 3-6 9-14 77
coverage exclude -srcfile pqr.vhd
coverage exclude -du * -togglenode * -inout
```

This excludes lines 12, 55, and 67 to 90 (inclusive) of file *xyz.vhd*; lines 3 to 6, 9 to 14, and 77 of *abc.vhd*; all lines from *pqr.vhd*, and all INOUT toggle nodes in the design.

After compiling (using **vcom +cover**), you can load and run the simulation with the following commands:

```
vsim -coverage <design_name> -do exclusions.do
run -all
```

Default Exclusion Filter File

The Tcl preference variable `PrefCoverage(pref_InitFilterFrom)` specifies a default exclusion filter file to read when a design is loaded with the **-coverage** switch. By default this variable is not set. See “[Simulator GUI Preferences](#)” for details on changing this variable. You can use this setting to automatically load an *exclusions.do* file at startup, thus avoiding the command “-do exclusions.do” in the example above.

Toggle Exclusion Management

Toggle coverage as it relates to exclusions are more complex to configure than other coverage types because of the historical fact that the “toggle” command existed before code coverage was introduced in ModelSim. Thus, there are multiple ways of achieving the same effects.

Two Methods for Excluding Toggles

ModelSim offers two independent flows for excluding toggle coverage:

- **Manual flow** —
Using this flow, you manually add/enable/disable toggles with the following commands:
 - **toggle add** — tells the simulator to cover a set of toggles. This automatically enables the added toggles. It requires that nets and/or variables be visible to the simulator (in other words, it will not work in a completely optimized simulation.)
 - **toggle disable** — disables previously added or enabled toggles.
 - **toggle enable** — enables previously disabled toggles.
- **Compiler/Simulator flow** —
Using this flow, you set up ModelSim to recognize toggles in the design during compilation, and enable the collection/exclusion of toggle data during simulation using the following commands:
 - **vcom/vlog +cover=t** — prepares to add all toggles found in the compiled design units, except pragma-excluded toggles. See “[Exclude Nodes from Toggle Coverage](#)”.



Important: Since pragma-excluded toggles are parsed in the source compilation, they are only relevant to the compiler/simulator flow with `+cover=t` and `-coverage`. The pragma exclusion has no effect on toggle add, disable, or enable.

- **vsim -coverage** — required in order to add all the toggles previously found by the compiler.
- **vcover report -excluded** — prints an exclusions report detailing all toggles specific toggles that were recognized in the design during compilation. The generated report is actually an executable `.do` file that you can run at a later time.
- **coverage exclude [disable|enable] -pragma** — dynamically enables or disables reporting on toggle nodes that were previously excluded by the compiler.

In this method, both “`vcom/vlog +cover=t`” and “`vsim -coverage`” are required in order to add toggles for coverage.

These two flows of managing toggle coverage and exclusions are quite distinct. You can apply toggle exclusions by executing an exclusions report as a `.do` file (TCL format), as mentioned above. However, this `.do` file only consistently reproduces the same set of enabled toggles in the compiler/simulator flow. This is because the exclude commands in the exclusions report depend on having a given set of toggles currently enabled. In other words, if you introduce any toggle add/enable/disable commands before applying a set of toggle exclusions from a saved `.do` file, the resulting set of toggle exclusions will not be identical to your original set. The toggle exclusions can only be applied with respect to currently enabled toggles, i.e., not to a pristine, “toggle-free” environment.

This is important, because nothing in ModelSim prevents you from mixing commands from the manual and compiler/simulator flows, however you should only do so with a solid understanding of how they interact.

Exclude Nodes from Toggle Coverage

The toggle disable command is intended to be used as follows:

1. Enable toggle statistics collection for all signals using the **+cover=t** or **+cover=x** argument to **vcom** or **vlog**, or use the **toggle add** command at run time.
2. Exclude certain signals by disabling them with the “toggle disable” command.

You can re-enable toggle statistics collection on nodes whose toggle coverage has previously been disabled via the toggle disable command using the **toggle enable** command.

Toggle Pragma Exclusion

You can also exclude toggle nodes by pragma using the “coverage toggle_ignore”, including specific bus bits.

In Verilog, the command is:

```
// coverage toggle_ignore <simple_signal_name> [<list>]
```

or, in VHDL:

```
-- coverage toggle_ignore <simple_signal_name> [<list>]
```

The following rules apply to the use of these pragmas:

- <list> is a space-separated list of bit indices or ranges, where a range is two integers separated by ':' or '-'.
- If <list> is not specified, the entire signal is excluded.
- If using a range, the range must be in the same ascending or descending order as the signal declaration.
- The pragma must be placed within the declarative region of the module or architecture in which <simple_signal_name> is declared.

Exclude Bus Bits from Toggle Coverage

You can use the “<list>” specifier in the “coverage toggle_ignore” pragma to exclude bus bits. You can also use the “**toggle add -exclude <list>**” command.

Re-enable Toggles Excluded with Pragmas

Toggles that have been previously excluded using pragmas can be re-enabled (in the compiler/simulator flow) using either the "coverage exclude -code t -pragma -clear" or "coverage exclude -pragma -clear -togglenode" commands. If the compiled database includes a set of pragma-excluded toggle nodes, these CLI commands override any pragma exclusions and include the specified toggles in coverage statistics.

Exclude enum Signals from Toggle Coverage

You can exclude individual VHDL enums or ranges of enums from toggle coverage and reporting by specifying enum exclusions in source code pragmas or by using the **-exclude** argument to the [toggle add](#) command. See [Toggle Exclusion Management](#) for important information specific to toggle exclusions.

FSM Coverage Exclusions

In ModelSim, any transition or state of an FSM can be excluded from the coverage reports using the [coverage exclude](#) command at the command line or by pragma. See the [coverage exclude](#) command for syntax details.

Exclude FSM with coverage exclude Command

The [coverage exclude](#) command is used to exclude the specified transitions from coverage reports. Consider the following coverage report:

```
# FSM Coverage for du fsm_top--
#
# FSM_ID: state
#   Current State Object : state
#   -----
#   State Value MapInfo :
#   -----
#           State Name           Value
#   -----
#           idle                 0
#           rd_wd_1              8
#           wt_blk_1             3
#           wt_wd_1              1
#           ctrl                 10
#           wt_wd_2              2
#           wt_blk_2             4
#           wt_blk_3             5
#   Covered Transitions :
#   -----
#           Trans_ID            Transition           Hit_count
#   -----
#           0                   idle -> idle           9
#           2                   idle -> wt_wd_1          4
#           3                   idle -> wt_blk_1          2
#           4                   idle -> rd_wd_1          6
```

#	5	rd_wd_1 -> rd_wd_2	6
#	7	wt_blk_1 -> wt_blk_2	2
#	9	wt_wd_1 -> wt_wd_2	4

The following are some examples of commands used to exclude data from the coverage report:

coverage exclude -du fsm_top -fstate <state> S1

excludes FSM state S1 from coverage in the design unit *fsm_top*. *<state>* is the current state variable. By default, when a state is excluded, all transitions to and from that state are excluded (see “[Auto Exclusions](#)”).

coverage exclude -du fsm_top -ftrans state

excludes all transitions from the FSM whose FSM_ID is *state* in the design unit *fsm_top*.

coverage exclude -du fsm_top -ftrans state {idle -> wt_wd_1} {idle -> rd_wd_1}

excludes specified transitions (2 and 3) from the FSM whose FSM_ID is *state*, in the design unit *fsm_top*. If whitespace is present in the transition, it should be surrounded by curly braces.

coverage exclude -scope /fsm_top/a1 -ftrans state

excludes all the transitions from the */fsm_top/a1* instance, in the FSM whose FSM_ID is *state*, in instance */fsm_top/a1*.

coverage exclude -scope /fsm_top/a1 -ftrans state {idle -> rd_wd_1} {idle -> rd_wd_1}

excludes specified transitions (numbers 3 and 4) from the FSM whose FSM_ID is *state*, in instance */fsm_top/a1*.

Using -clear with coverage exclude

When the **-clear** option is used with [coverage exclude](#), it re-enables the reporting of those transitions which have been excluded. The transitions are specified in the same manner as that for the coverage exclude command. For example:

coverage exclude -clear -du fsm_test -ftrans <state_var> {idle -> rd_wd_1} {idle -> rd_wd_1}

re-enables the reporting of the specified transitions.

Exclude FSM with Pragma

You can use coverage pragmas to selectively turn coverage off and on for FSM states and transitions.

In Verilog, the pragma is:

```
// coverage fsm_off <fsm_name>
```

In VHDL, the pragma is:

```
-- coverage fsm_off <fsm_name>
```

The FSM(s) with current state variable <fsm_name> are excluded from coverage. The pragma should come after the object declaration; otherwise, it will have no effect. The FSM state or transition specified by “fsm_object_name” is excluded from code coverage.

Warnings are printed only if code coverage is turned on with the +cover=f argument during compile (with [vcom](#) or [vlog](#)). If an FSM coverage pragma is specified and coverage is turned on, the Warning may look like the following:

```
** Warning: [13] fsm_safel.vhd(18): Turning off FSM coverage for "state".
```

If an FSM coverage pragma is specified before the object declaration, the Warning may appear as follows:

```
** Warning: [13] fsm_safel.vhd(17): Can't find decl "state" for turning  
off FSM coverage.
```

For more information on general coverage exclusions, see “[Coverage Exclusions](#)”.

Saving and Recalling Exclusions

You may specify files and line numbers or condition and expression UDP truth table rows (see below for details) that you wish to exclude from coverage statistics. These exclusions appear in the Current Exclusions window. You can then create a *.do* file that contains these exclusions in one of two ways:

- Make the Current Exclusions window active and choose **File > Save** from the menus.
- With “coverage report -excluded -file <filename>.do” command.

To load this *.do* file during a future analysis, select the Current Exclusions window and select **File > Open**.

For example, the contents of the *exclusions.do* file might look like the following:

```
coverage exclude -srcfile xyz.vhd -linerange 12 55 67-90  
coverage exclude -srcfile abc.vhd -linerange 3-6 9-14 77  
coverage exclude -srcfile pqr.vhd
```

This excludes lines 12, 55, and 67 to 90 (inclusive) of file *xyz.vhd*; lines 3 to 6, 9 to 14, and 77 of *abc.vhd*; and all lines from *pqr.vhd*.

This *exclude.do* file can then be used as follows:

1. Compile your design with the +cover=<argument> to:
 - **vopt**, if using 3-step vopt flow

- **vcom** or **vlog**, if not explicitly running vopt (2-step vopt flow)
2. Load and run your design with:

```
vsim -coverage <design_name> -do exclude.do run -all
```

To avoid running the “-do exclude.do” explicitly, you can set the default exclusion filter to run the *exclusion.do* file automatically upon invocation. See the “[Default Exclusion Filter File](#)” for details.

Example 16-6. Excluding, Merging and Reporting on Several Runs

Suppose you are doing a number of simulations, *i*, numbered from 1 to *n*.

1. Use **vlib** to create a working library.
2. Use **vcom** and/or **vlog** to compile.
3. Use **vsim** to load and run the design:

```
vsim -c <design_i> -do "log -r /*;  
coverage save -onexit <results_i>;  
run -all; do <exclude_file_i.do>; quit -f"
```

Note, you can have different exclude files *<exclude_file_i>* for each run *i*, numbered from 1 to *n*.

4. Use **vcover merge** to merge the coverage data:

```
vcover merge <merged_results_file> <results_1> <results_2> ...  
<results_n>
```

5. Use **vcover report** to generate your report:

```
vcover report [switches_you_want] -output <report_file>  
<merged_results_file>
```

Exclusions are invoked during **vsim**, in step 3.

All the various results files *<results_i>* contain the exclusion information inserted at step 3.

The exclusion information for the merged results file is derived by ORing the exclusion flags from each **vsim** run. So, for example, if runs 1 and 2 exclude *xyz.vhd* line 12, but the other runs don't exclude that line, the exclusion flag for *xyz.vhd* line 12 is set in the merged results since at least one of the runs excluded that line. Then the final **vcover report** will not show coverage results for file *xyz.vhd* line 12.

Let's suppose your *<exclude_file_i>* are all the same, and called *exclude.do*.

The contents of *exclude.do* file could be:

```
coverage exclude -srcfile xyz.vhd -linerange 12 55 67-90  
coverage exclude -srcfile abc.vhd -linerange 3-6 9-14 77
```

```
coverage exclude -srcfile pqr.vhd -linerange all
```

This will exclude lines 12, 55, and 67 to 90 (inclusive) of file *xyz.vhd*; lines 3 to 6, 9 to 14, and 77 of *abc.vhd*; and all lines from *pqr.vhd*.

Coverage Reports

You may create coverage reports from the command line or with the GUI, using:

- the **Coverage Report** dialog
- the [coverage report](#) command — use when a simulation is loaded; creates an organized list of report data, including toggle data
- the [toggle report](#) command — produces an unordered list of unique toggles
- the [vcover report](#) command — produces textual output of coverage data from UCDB generated by a previous code or functional coverage run

HTML reports are also available through the **Coverage Report** dialog, or by applying the **-html** argument to the [coverage report](#) and [vcover report](#) commands. See “[Generating HTML Coverage Reports](#)” for more information.

Using the coverage report Command

The [coverage report](#) command produces textual output of coverage statistics or exclusions of the current simulation.

Example 16-7. Reporting Coverage Data from the Command Line

Here is a sample command sequence that outputs a code coverage report and saves the coverage data:

```
vlog ../rtl/host/top.v
vlog ../rtl/host/a.v
vlog ../rtl/host/b.v
vlog ../rtl/host/c.v

vopt +cover=bcefsx top
vsim -c -coverage top
run 1 ms
coverage report -file d:\\sample\\coverage_rep.txt
coverage save d:\\sample\\coverage.ucdb
```

The [vlog](#) command compiles Verilog and SystemVerilog design units. The **+cover=bcefs[t|x]** argument applied to either **vopt** (for [Three-Step Flow](#)) or **vlog** (for [Two-Step Flow](#)) prepares the design and specifies the types of coverage statistics to collect:

b = branch coverage

c = condition coverage
e = expression coverage
f = finite state machine coverage
t = toggle coverage (two-state)
s = statement coverage
x= toggle coverage (four-state)

The **-coverage** option for the **vsim** command enables code coverage statistics collection during simulation.

The **-file** option for the **coverage report** command specifies a filename for the coverage report: *coverage_rep.txt*. And the **coverage save** command saves the coverage data to *d:\sample\coverage.ucdb*.

Using the toggle report Command

The **toggle report** command displays a list of all nodes that have not transitioned to both 0 and 1 at least once, and the counts for how many times each node toggled for each state transition type. Also displayed is a summary of the number of nodes checked, the number that toggled, the number that didn't toggle, and a percentage that toggled.

The **toggle report** command is intended to be used as follows:

1. Enable statistics collection with the **+cover=t** argument to either **vlog/vcom** (if not explicitly running **vopt**), or to **vopt** for the three-step **vopt** flow.
2. Run the simulation with the **run** command.
3. Produce the report with the **toggle report** command.

By default, the report only shows togglenodes that did not toggle. In order to show all toggle nodes, including those that have already toggled, use “toggle report -all”.

Figure 16-4. Sample Toggle Report

Toggle Report	Node	1H->0L	0L->1H	0L->Z	Z->0L	1H->Z	Z->1H
/test_sm/dat(7)		0	1	0	1	23404	23404
/test_sm/dat(6)		2600	2600	10403	10404	13001	13001
/test_sm/dat(5)		2600	2601	13001	13002	10403	10403
/test_sm/dat(4)		2600	2600	18203	18204	5201	5201
/test_sm/dat(3)		0	1	0	1	23404	23404
/test_sm/dat(2)		2600	2600	10403	10404	13001	13001
/test_sm/dat(1)		2600	5202	5200	7802	18204	15603
/test_sm/dat(0)		10401	13002	10402	13004	13002	10401

Total Node Count	=	587
Toggled Node Count	=	131
Untoggled Node Count	=	456
Toggle Coverage	=	22.32 %

You can produce this same information using the [coverage report](#) command.

Port Collapsing and Toggle Coverage

The simulator collapses certain ports that are connected to the same signal in order to improve performance. Collapsed signals will not appear in the toggle coverage report. If you want to ensure that you are reporting all signals in the design, use the **-nocollapse** argument to **vsim** when you load your design. The **-nocollapse** argument degrades simulator performance, so it should be used only when it is absolutely necessary to see all signals in a toggle report.

Ordering of Toggle Nodes

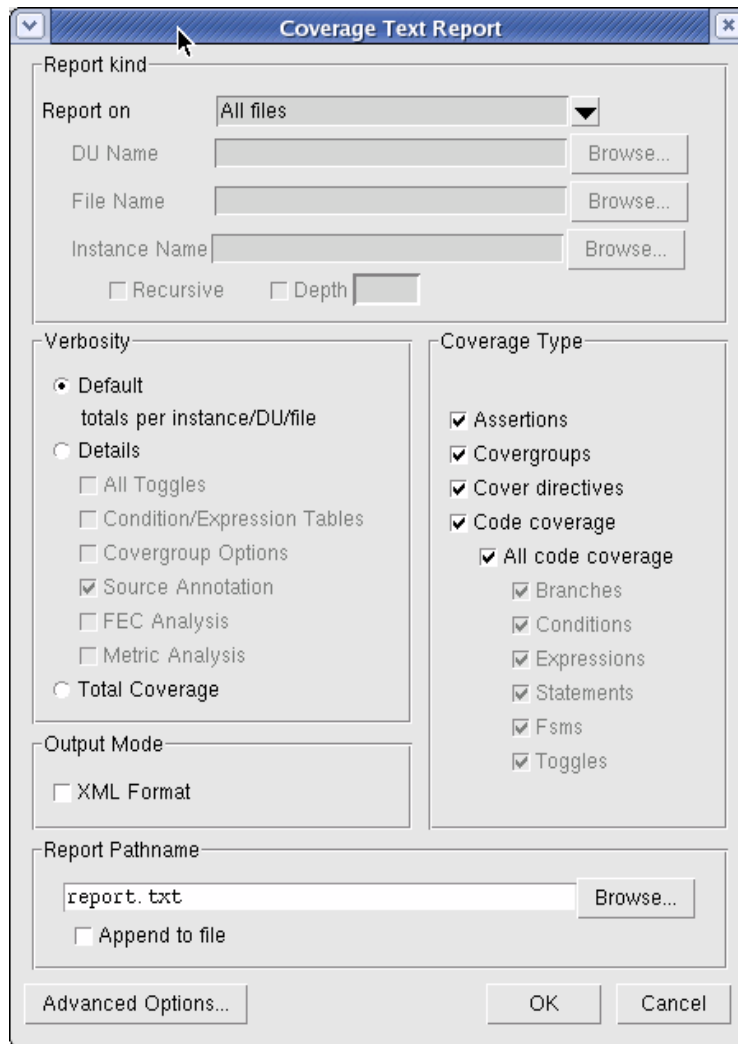
The ordering of nodes in the report may vary depending on how you specify the signal list. If you use a wildcard in the signal argument (e.g., `toggle report -all -r /*`), the nodes are listed in the order signals are found when searching down the context tree using the wildcard. Multiple elements of the same net will be listed multiple times. If you do not use a wildcard (e.g., `toggle report -all -r /*`), the nodes are listed in the order in which they were originally added to toggle coverage, and elements are not duplicated.

Using the Coverage Report Dialog

To create a coverage report using the ModelSim GUI, access the Coverage Report dialogs by right-clicking any object in the Files or Structure (sim) Windows and selecting **Code Coverage**

> **Code Coverage Reports**; or, select **Tools > Coverage Report > Text** or **HTML** or **Exclusions**.

Figure 16-5. Coverage Report Text Dialog



Setting a Default Coverage Reporting Mode

You can specify a default coverage mode that persists from one ModelSim session to the next through the preference variable `PrefCoverage(DefaultCoverageMode)`. The modes available allow you to specify that lists and data given in each report are listed by: file, design unit, or instance. By default, the report is listed by file. See [Simulator GUI Preferences](#) for details on changing this variable.

You may also specify a default coverage mode for the current invocation of ModelSim by using the `-setdefault [byfile | byinstance | bydu]` argument for either the [coverage report](#) or the [vcover report](#) command.

XML Output

You can output coverage reports in XML format by checking **Write XML Format** in the Coverage Report dialog or by using the **-xml** argument to the [coverage report](#) command.

The following example is an abbreviated "By Instance" report that includes line details:

```
<?xml version="1.0" ?>
- <coverage_report>
- <code_coverage_report lines="1" byInstance="1">
- <instanceData path="/concat_tester/CHIPBOND/control_inst" du="micro"
  sec="rtl">
- <sourceTable files="1">
  <fileMap fn="0" path="src/Micro.vhd" />
</sourceTable>
  <statements active="65" hits="64" percent="98.5" />
  <stmt fn="0" ln="83" st="1" hits="2430" />
  <stmt fn="0" ln="84" st="1" hits="30" />
  <stmt fn="0" ln="85" st="1" hits="15" />
  <stmt fn="0" ln="86" st="1" hits="14" />
  <stmt fn="0" ln="87" st="1" hits="15" />
  ...
  ...
```

"fn" stands for filename, "ln" stands for line number, and "st" stands for statement.

There is also an XSL stylesheet named *covreport.xsl* located in
<install_dir>/examples/tutorials/vhdl/coverage, or
<install_dir>/examples/tutorials/verilog/coverage.

Use it as a foundation for building your own customized report translators.

HTML Output

You can output coverage reports in HTML format by checking **Write HTML Format** in the Coverage Report dialog or by using the **-html** argument to the [coverage report](#) command.

For more information on HTML output reports, see “[Generating HTML Coverage Reports](#)”.

Coverage Reporting on a Specific Test

You can output coverage reports for specific tests in all formats, except XML, by using the **-testextract** argument to either [vcover](#) report or the [coverage report](#) command, or to the **-html** argument for either of those commands.

For more information on HTML output reports, see “[Generating HTML Coverage Reports](#)”.

Notes on Coverage and Optimization

The optimization process removes constructs in your design that are not functionally essential, such as code in a procedure that is never called. These constructs can include statements, expressions, conditions, branches, and toggles. This results in a trade-off between aggressive optimization levels and the ease with which the coverage results can be understood. While aggressive levels of optimization make the simulation run fast, your results may at times give you the mistaken impression that your design is not fully covered. This is due to the fact that native code is not generated for all HDL source code in your design. Those fragments of HDL code that *do not* result in native code generation are never instrumented for coverage, either. And thus, those fragments of code do not participate in coverage gathering, measurement, or reporting activities.

When observing the Source window, you can tell which statements do not participate in coverage activities by looking at the Statement and Branch Count columns on the left of the window. If those columns are completely blank (no numbers or 'X' symbols at all), then the associated statements have been optimized out of the simulation database, and they will not participate in coverage activities.

Customizing Optimization Level for Coverage Runs

It is conceivable that you will achieve 100% coverage in an optimized design, even if certain statements or constructs have been optimized away. This is due to the fact that at the lowest level, all coverage calculations are of the form “Total Hits / Total Possible Hits = % Coverage”. Constructs that have been optimized out of the design do not count as Possible Hits. Also, because the statements never execute, they never contribute to Total Hits. Thus, statements that are optimized out of the design do not participate in coverage results in any way. (This is similar to how statements that you explicitly exclude from coverage don't contribute to coverage results.)

By default, ModelSim enables a reasonable level of optimizations while still maintaining the logic necessary for the collection of coverage statistics (for details, see [CoverOpt modelsim.ini](#) file variable). If you achieve 100% coverage with the default optimization level, the results are as viable as achieving 100% coverage with no optimizations enabled at all.

You can customize the default optimization levels used when coverage is enabled for the simulation as follows:

- To change optimizations applied to all runs —
Change the value (1 - 4) of CoverOpt *modelsim.ini* variable from the default level. See [CoverOpt](#) for a description of the available optimization levels.
- To change optimizations applied to a specific run —
Set the `-coveropt` argument to `vlog`, `vcom`, or `vopt`. For example:

```
vcom +cover=cbesxf -coveropt 2
```

See [CoverOpt](#) for a description of the available optimization levels.

For more information about the tradeoffs of optimization, refer to “[Optimizing Designs with vopt](#)”.

Interaction of Optimization and Coverage Arguments

In ModelSim, the default level of optimization in vopt is -O5. When -novopt is used with vsim at the command line, the default is -O4.

The [CoverOpt](#) *modelsim.ini* variable corresponds to the number options of the vlog/vcom -coveropt command line option. The valid settings are 1, 2, 3, and 4. The lower the number, the less optimizations are enabled. Less optimizations translate into greater design visibility, yet slower performance.

CoverOpt works as follows: After all other optimization-control options have been processed, the specified level of CoverOpt optimizations is applied. All CoverOpt can do is turn OFF certain optimizations known to be harmful or confusing to coverage. CoverOpt never turns on an optimization that was not enabled already. Some optimizations are always turned off when code coverage is in effect, and some +acc flags are always turned on when code coverage is in effect (such as when line numbering is correctly preserved).

The CoverOpt setting gives you a level of control over how much optimization is applied to your design when specifying coverage types for collection.

Chapter 17

Finite State Machines

A Finite State Machine (FSM) reflects the changes a state-based design has gone through from the start of simulation to the present. Transitions indicate state changes and are described by the conditions required to enable them. Because of the complexity of FSMs, designs containing them can contain a high number of defects. It is important, therefore, to analyze the FSMs in RTL before going to the next stages of synthesis in the design cycle.

FSM Recognition	677
FSM Coverage	681
FSM Multi-State Transitions	681
Collecting FSM Coverage Metrics	682
Reporting Coverage Metrics for FSMs	684
Viewing FSM Information in the GUI	685
FSM Coverage Metrics Available in the GUI	686
Advanced Command Arguments for FSMs	688
Recognized FSM Note	688
FSM Recognition Info Note	689
FSM Coverage Text Report	691

FSM Recognition

ModelSim recognizes VHDL and Verilog FSMs during compilation or optimization when you are [Collecting FSM Coverage Metrics](#) or [Viewing FSM Information in the GUI](#) and when they fit the following criteria:

- There should be a finite number of states which the state variable can hold.
- The next state assignments to the state variable must be made under a clock.
- The next state value must depend on the current state value of the state variable.

State assignments that do not depend on the current state value are considered reset assignments.

ModelSim recognizes the following VHDL and Verilog FSM design styles:

- FSMs using a current state variable.
- FSMs using current state and next state variables.

- FSMs using multiple next-state variables, where all are used as a buffer assignment.
- FSMs using parameters/generics (only supported when using vopt)
- FSMs using a single or multiple Case statements.
- FSMs using a single or multiple If-Else statements.
- FSMs using mixed If-Else and Case statements.
- FSMs using a VHDL wait/select statement.
- FSMs using a VHDL when/else statement.
- FSMs defined using a one-hot or one-cold style (supported for Verilog only).
- FSMs using a current- or next-state variable as a VHDL record or SystemVerilog struct field. Nested structures are not supported.
- FSMs using a current- or next-state variable as a VHDL or Verilog index expression.
- FSMs using any integral SystemVerilog types like logic, int, bit_vector, enum, packed struct. Typedefs of these types are also supported.
- Verilog FSMs having state variable assignment to a 'x (unknown) value. X-assignment is enabled by default.

Unsupported FSM Design Styles

ModelSim does not recognize the following design styles:

- Using Verilog part-select expressions as a current-state variable.
- Using VHDL slice expressions as a current-state variable.
- Defining a single FSM in multiple modules.
- Using an FSM that is spanned over procedures.

FSM Design Style Examples

The following examples illustrate several supported FSM design styles.

Example 17-1. Verilog Single-State Variable FSM

```
module fsm_lproc (output reg out, input [7:0] inp, input clk, en, rst);  
  
    typedef enum {s0, s1, s2, s3, s4, s5, s6, s7} state_t;  
    state_t state;  
  
    always_ff @(posedge clk, posedge rst)  
        if (rst)  
            state <= s0;
```

```

else
  casex (state)
    s0: begin out <= inp[0]; if (en) state <= s1; end
    s1: begin out <= inp[1]; if (en) state <= s2; end
    s2: begin out <= inp[2]; if (en) state <= s3; end
    s3: begin out <= inp[3]; if (en) state <= s4; end
    s4: begin out <= inp[4]; if (en) state <= s5; end
    s5: begin out <= inp[4]; if (en) state <= s6; end
    s6: begin out <= inp[6]; if (en) state <= s7; end
    s7: begin out <= inp[7]; if (en) state <= s0; end
    default: begin out <= inp[5]; state <= s1; end
  endcase

endmodule

```

Example 17-2. VHDL Single-State Variable FSM

```

library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
entity fsm is port( in1 : in signed(1 downto 0);
                   in2 : in signed(1 downto 0);
                   en  : in std_logic_vector(1 downto 0);
                   clk: in std_logic;
                   reset : in std_logic_vector( 3 downto 0);
                   out1 : out signed(1 downto 0));
end fsm;

architecture arch of fsm is
  type my_enum is (s0 , s1, s2, s3,s4,s5);
  type mytype is array (3 downto 0) of std_logic;
  signal test : mytype;
  signal cst : my_enum;

begin
  process(clk,reset)
  begin
    if(reset(1 downto 0) = "11") then
      cst <= s0;
    elsif(clk'event and clk = '1') then
      case cst is
        when s0 =>  cst <= s1;
        when s1 =>  cst <= s2;
        when s2 =>  cst <= s3;
        when others =>  cst <= s0;
      end case;
    end if;
  end process;
end arch;

```

Example 17-3. Verilog Current-State Variable with a Single Next-State Variable FSM

```

module fsm_2proc (output reg out, input [7:0] inp, input clk, en, rst);

  typedef enum {s0, s1, s2, s3, s4, s5, s6, s7} state_t;

```

```
state_t c_state, n_state;

always_ff @(posedge clk, posedge rst)
  if (rst)
    c_state <= s0;
  else
    if (en) c_state <= n_state;

always_comb
  casex (c_state)
    s0: begin out = inp[0]; n_state = s1; end
    s1: begin out = inp[1]; n_state = s2; end
    s2: begin out = inp[2]; n_state = s3; end
    s3: begin out = inp[3]; n_state = s4; end
    s4: begin out = inp[4]; n_state = s5; end
    s5: begin out = inp[4]; n_state = s6; end
    s6: begin out = inp[6]; n_state = s7; end
    s7: begin out = inp[7]; n_state = s0; end
    default: begin out = inp[5]; n_state = s1; end
  endcase

endmodule
```

Example 17-4. VHDL Current-State Variable and Single Next-State Variable FSM

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use work.pack.all;
entity fsm is port( in1 : in signed(1 downto 0);
                   in2 : in signed(1 downto 0);
                   en  : in std_logic_vector(1 downto 0);
                   clk: in std_logic;
                   reset : in std_logic_vector( 3 downto 0);
                   out1 : out signed(1 downto 0));
end fsm;

architecture arch of fsm is
  type my_enum is (s0 , s1, s2, s3,s4,s5);
  type mytype is array (3 downto 0) of std_logic;
  signal test : mytype;
  signal cst, nst : my_enum;

  begin
    process(clk,reset)
    begin
      if(reset(1 downto 0) = "11") then
        cst <= s0;
      elsif(clk'event and clk = '1') then
        cst <= nst;
      end if;
    end process;

    process(cst)
    begin
      case cst is
        when s0 =>  nst <= s1;
      end case;
    end process;
  end arch;
```



```
        when s1 =>    nst <= s2;  
        when s2 =>    nst <= s3;  
        when others => nst <= s0;  
    end case;  
end process;  
end arch;
```

FSM Coverage

ModelSim recognizes FSMs in your design during the compilation stages prior to simulation. The simulation stage collects coverage metrics about which states and transitions were used while simulating the test bench with the DUT.

The following metrics are collected for FSMs:

- **State Coverage Metric** — determines how many FSM states have been reached during simulation.
- **Transition Coverage Metric** — determines how many transitions have been exercised in the simulation of the state machine.
- **Multi-state transition coverage** — tracks the various possible sequences of transitions that have been exercised in the simulation of the state machine. This is also referred to as Sequence coverage.

Related Topics

[Collecting FSM Coverage Metrics](#)
[FSM Coverage Metrics Available in the GUI](#)
[Code Coverage](#)

FSM Multi-State Transitions

A multi-state transition is also known as a state sequence. In the coverage domain, using the switch `-fsmmultitrans` with `vcom` or `vlog` or `vopt` yields a metric sometimes known as sequence coverage, since it measures the progress of an FSM through a sequence of states. The FSM recognition messages shows multi-state transitions as:

```
#      S0 => S1 => S0
```

When you specify `-fsmmultitrans` you will be able to view this information in the:

- [FSM Recognition Info Note](#) in the transcript, specifically the multi-state transition table.
- [FSM Coverage Text Report](#), specifically the covered transition and uncovered transition tables.
- Details window

- Missed FSMs window

Collecting FSM Coverage Metrics

You can enable the recognition and collection of coverage metrics for FSMs in your design through the use of command arguments in your simulation flow.

Prerequisites

- Evaluate the commands and switches in [Table 17-1](#) to determine which are required for your flow.

Table 17-1. Commands Used for FSM Coverage Collection

Task	Command/Switch	Required
Enable the collection of FSM coverage metrics for individual design units.	<code>vcom</code> or <code>vlog</code> with <code>+cover=f</code> ¹	Yes ²
Enable the collection of FSM coverage metrics for the complete design.	<code>vopt</code> with <code>+cover=f</code> ¹	Yes ²
Produce a detailed report in the transcript for each recognized FSM.	<code>vcom</code> or <code>vlog</code> or <code>vopt</code> with <code>-fsmverbose</code>	No
Enable the reporting and collection of coverage metrics for FSM Multi-State Transitions	<code>vcom</code> or <code>vlog</code> or <code>vopt</code> with <code>-fsmmultitrans</code>	No
Collect coverage metrics for the design under simulation.	<code>vsim</code> with <code>-coverage</code>	Yes

1. You can also use `+cover` with no arguments, which enables collection of all coverage metrics.
2. You must specify `+cover=f` at some point in the procedure with `vcom` or `vlog` or `vopt`.

Procedure

1. Compile your design units with `vcom` or `vlog`.
 Include any switches from [Table 17-1](#) in addition to any other command arguments required for your design and environment.
2. Optimize your design with `vopt`.
 Include any switches from [Table 17-1](#) in addition to any other command arguments required for your design and environment.
3. Load your simulation using the `-coverage` switch with the `vsim` command. The `-coverage` switch is required.
4. Run your simulation with the `run` command.

Examples

- Enable FSM coverage on the complete design.

```
vcom a.vhdl b.vhdl
vcom top.vhdl
vopt +cover=f top -o opt_top
vsim -coverage opt_top
run -all
```

- Enable coverage for all types on the complete design.

```
vlog *.v
vopt +cover top -o opt_top
vsim -coverage opt_top
run -all
```

- Enable FSM coverage, including multi-state transitions, on the complete design with verbose reporting.

```
vcom top.vhdl
vcom a.vhdl b.vhdl
vopt +cover=f -fsmverbose -fsmmultitrans top -o opt_top
vsim -coverage opt_top
run -all
```

- Enable FSM coverage only on selected design units.

```
vlog +cover=f a.v b.v
vlog top.v
vopt top -o opt_top
vsim -coverage opt_top
run -all
```

Results

- The vcom and vlog and vopt commands produce messages related to any recognized FSMs. Refer to the sections [“Recognized FSM Note”](#) and [“FSM Recognition Info Note”](#) for more information.
- The vsim command loads the simulation and changes the GUI layout to Coverage mode.
- Several of the GUI windows will contain coverage metrics, refer to the section [“FSM Coverage Metrics Available in the GUI”](#).

Related Topics

[FSM Recognition](#)
[FSM Coverage](#)
[Code Coverage](#)
[Code Coverage in the Graphic Interface](#)
[FSM Coverage Exclusions](#)

Reporting Coverage Metrics for FSMs

You can use the GUI or [coverage report](#) command to create a text report of coverage metrics for FSMs in your design.

Prerequisites

- Run a simulation to collect coverage metrics for FSMs.
- (Optional) Exclude transitions or states from coverage collection. This will allow you to reach 100% FSM coverage. Refer to the section “[FSM Coverage Exclusions](#)” for more information.

Procedure

1. Select **Tools > Coverage Report > Text**.
Displays the Coverage Text Report dialog box.
2. From the Report on dropdown, select one of the following:
 - All files — reports data for FSMs for all design units defined in each file. (-byfile switch with coverage report)
 - All instances — reports data for all FSMs in each instance, merged together. (-byinst with coverage report)
 - All design unit — reports data for all FSMs in all instances of each design unit, merged together. (-bydu with coverage report)
3. In the Coverage Type pane, ensure that **Fsms** is selected. (-code f with coverage report)
4. Alter any of the other options as needed.
5. Click **OK**

Results

- Writes the report (*report.txt*) to the current working directory.
- Opens a notepad window containing the *report.txt* file.

Related Topics

[FSM Coverage](#)
[FSM Coverage Metrics Available in the GUI](#)
[Code Coverage](#)
[Using the Coverage Report Dialog](#)
[Coverage Reports](#)

Viewing FSM Information in the GUI

You can enable the creation of debug information for FSMs in your design through the use of command arguments in your simulation flow.

Prerequisites

- Invoke ModelSim in GUI mode.
- Evaluate the commands and switches in [Table 17-2](#) to determine which are required for your flow.

Table 17-2. Commands Used to Capture FSM Debug Information

Task	Command/Switch	Required
Retain visibility of and capture debugging information about FSMs for individual design units.	<code>vcom</code> or <code>vlog</code> with <code>+acc=f</code> ¹	Yes ²
Retain visibility of and capture debugging information about FSMs for the complete design.	<code>vopt</code> with <code>+acc=f</code> ¹	Yes ²

1. You can also specify `+acc` with no arguments, which retains visibility for most design elements.
2. You must specify `+acc=f` at some point in the procedure with `vcom` or `vlog` or `vopt`.

Procedure

1. Compile your design units with `vcom` or `vlog`.
Include any switches from [Table 17-2](#) in addition to other switches required for your design and environment.
2. Optimize your design with `vopt`.
Include any switches from [Table 17-2](#) in addition to other switches required for your design and environment.
3. Load your simulation with `vsim`.

ModelSim does not generate any FSM debug information if you specify `-novopt`.

4. Select **View > FSM List**

Displays the [FSM List Window](#), which lists all recognized finite state machines.

5. Double-click on an FSM in the FSM List window.

Displays the FSM in an [FSM Viewer Window](#).

6. Add an FSM to the Wave window:

a. Right-click on an FSM from the FSM List Window

b. Select **Add to Wave > Selected FSM**

The FSM is automatically displayed in the Wave window as a group of signals with the label: **FSM (<current_state>)**. You can change the name of the group through the FSM Display Options dialog (**FSM View > Options**)

The FSM Viewer and the Wave window are dynamically linked, allowing you to analyze states and their transitions, based on your cursor position.

7. Run your simulation with the `run` command.

8. Rearrange the GUI so can see both the FSM Viewer and Wave windows simultaneously.

9. Link the FSM Viewer window to the cursor of the Wave window:

a. Select **FSM View > Track Wave Cursor**

b. Move the cursor in the wave window to see how the states change.

Green indicates current state and yellow the previous state for the cursor location.

10. Unselect **FSM View > Show Transitions to “Reset”**

Removes transitions to the reset state from the FSM Viewer window.

Related Topics

[FSM Recognition](#)


FSM Coverage Metrics Available in the GUI

The GUI presents coverage metrics in several windows within the GUI. This section provides an overview of where you can find this information.

- **Missed FSMs Window** — lists states and transitions that have not been fully covered during simulation.

Transitions are listed under states, and source line numbers for each transition are listed under their respective transitions.

You must select a design unit from the Structure window that contains a state machine before anything will appear in this window

The icon that appears next to the *state* variable name is also a button , which opens the FSM in the [FSM Viewer Window](#).

The Missed FSMs window is linked to several windows:

- When you double-click on a state or transition, the FSM will open in an FSM Viewer window.
- When you select a state or transition, it will be highlighted in the Coverage Details window.
- When you select the source line number for the transition, a Source window will open and display the line number you have selected.
- Coverage Details Window — provides detailed coverage information about any FSM item selected in the Missed FSMs window.
- Columned Windows — provide FSM coverage metrics in the Structure, Files, Objects and Instance Coverage windows, as indicated in [Table 17-3](#).

Table 17-3. FSM Coverage Columns

Column	Structure Window	Files Window	Objects Window	Instance Coverage Window	Information
State %	X	X	X		state hits divided by states
State Graph	X	X		X	displays a green bar when 90% or greater, otherwise the bar is red
States Hit	X	X	X	X	
States Missed	X	X		X	
States	X		X	X	
Transition %	X	X		X	transition hits divided by transitions
Transition Graph	X	X		X	displays a green bar when 90% or greater, otherwise the bar is red
Transitions Hit	X	X		X	
Transitions Missed	X	X		X	
Transitions	X			X	

Related Topics

[FSM Coverage](#)
[Code Coverage](#)
[Code Coverage in the Graphic Interface](#)

Advanced Command Arguments for FSMs

Table 17-4 lists more ModelSim command arguments you can use for FSM recognition.

Table 17-4. Additional FSM-Related Arguments

Command	Argument	Description
vcom vlog vopt	-fsmimplicittrans -nofsmimplicittrans	Controls recognition of implied same-state transitions.
	-fsmresettrans -nofsmresettrans	Controls recognition of implicit asynchronous reset transitions.
	-fsmsingle -nofsmsingle	Controls recognition of FSMs having a single-bit current-state variable.
	-fsmxassign -nofsmxassign	Controls recognition of FSMs containing an X assignment.

Related Topics

[Collecting FSM Coverage Metrics](#)
[Viewing FSM Information in the GUI](#)

Recognized FSM Note

Output from: [vlog](#), [vcom](#), [vopt](#)

Note ID: [vlog-143](#), [vcom-143](#), [vopt-143](#)

The [vcom](#) or [vlog](#) or [vopt](#) commands write a note to the transcript whenever they recognize an FSM. The note is of the format:

```
** Note: (<command>-143) Recognized '<n>' FSM/s in design unit '<du>'.
```


Parameters

Table 17-5 defines the replaceable values from the Recognized FSM note.

Table 17-5. Recognized FSM Note Parameters

Keyword	Description
<command>	Specifies the command (vlog, vcom, vopt) that issued the Note.
<n>	Specifies the number of FSMs recognized in the design unit.
<du>	Specifies the name of the design unit.

Example

```
# ** Note: (vlog-143) Recognized '1' FSM/s in design unit 'preproc'.
# ** Note: (vlog-143) Recognized '1' FSM/s in design unit 'psi_coder'.
```

Related Topics

[FSM Recognition](#)

FSM Recognition Info Note

Output from: [vlog](#), [vcom](#), [vopt](#) with the -fsmverbose switch

Note ID: vlog-1947, vcom-1947, vopt-1947

The vcom or vlog or vopt commands write a note to the transcript for every recognized FSM when you use the -fsmverbose switch.

Parameters

Table 17-6 defines the information in the FSM Recognition Info note.

Table 17-6. FSM Recognition Info Note Parameters

Keyword	Description
FSM recognized in	Specifies the file containing the FSM.
Current State Variable	Specifies the name, file, and line number of the current state variable.
Next State Variable	Specifies the name, file, and line number of the next state variable.
Clock	Specifies the name of the clock controlling the FSM
Reset States	Specifies the reset states of the FSM

Table 17-6. FSM Recognition Info Note Parameters (cont.)

Keyword	Description
State Set	Specifies the complete list of state names in the FSM.
Transition table	Lists all possible state transitions and any related line numbers.
Multi-state Transition table ¹	Lists all possible multi-state transitions.
INFO	Provides additional information about the FSM, such as: <ul style="list-style-type: none"> • identifying unreachable states. • identifying which states have no transitions, other than to a reset state. • identifying RTL code that will never be executed.

1. This section appears only when you specify -fsmmultitrans

Example

```
# ** Note: (vlog-1947)   FSM RECOGNITION INFO
# Fsm recognized in : ./rice_src/sysv/decode_top.sv
# Current State Variable : present_state : ./rice_src/sysv/decode_top.sv(19)
# Next State Variable : next_state : ./rice_src/sysv/decode_top.sv(19)
# Clock : pins.clk
# Reset States are: { S0 , XXX }
# State Set is : { S0 , S1 , XXX }
# Transition table is
# -----
# S0  =>  S1      Line : (32 => 34)
# S0  =>  S0      Line : (24 => 24)
# S0  =>  XXX     Line : (30 => 30)
# S1  =>  S0      Line : (36 => 38) (24 => 24)
# S1  =>  XXX     Line : (30 => 30)
# XXX =>  S0      Line : (24 => 24) (42 => 42)
# XXX =>  XXX     Line : (30 => 30)
# -----
# Multi-state transition table is
# -----
# S0 => S1 => S0                (Loop)
# S0 => S1 => XXX              (Loop)
# S0 => S1 => XXX => S0        (Loop)
# S0 => XXX => S0              (Loop)
# S1 => S0 => S1              (Loop)
# S1 => S0 => XXX              (Loop)
# S1 => XXX => S0              (Loop)
# S1 => XXX => S0 => S1        (Loop)
# XXX => S0 => S1              (Loop)
# XXX => S0 => S1 => XXX      (Loop)
# XXX => S0 => XXX            (Loop)
# -----
```

Related Topics

[FSM Recognition](#)
[FSM Multi-State Transitions](#)

FSM Coverage Text Report

Generated by:

- [coverage report](#) -code f -details
- **Tools > Coverage Report > Text**

This report contains available coverage metrics for the FSMs in your design.

Parameters

The FSM Coverage Report contains the following sections:

- Header — specifies whether the report was generated by file (-byfile), instance (-byinstance), or design unit (-bydu).
- FSM Coverage — coverage metrics for States and Transitions
- FSM_ID — the name of the current state variable.
- State Value MapInfo — a mapping of the state names to internal values.
- Covered States — coverage metrics for each state
- Covered Transitions — coverage metrics for each transition, including multi-state transitions if you use the -fsmmultitrans switch.
- Uncovered Transitions — a list of all transitions that have no coverage metrics.
- Summary — the same information as the FSM Coverage table at the top of the report.

Example

This examples shows an FSM coverage report, where the metrics are reported by file.

```
# Coverage Report by file with details
#
# File: test.vhdl
# FSM Coverage:
#   Enabled Coverage      Active      Hits % Covered
#   -----
#   States                3         3    100.0
#   Transitions           13        10    76.9
#
# =====FSM Details=====
#
# FSM Coverage for file test.vhdl --
#
# FSM_ID: cst
```

Finite State Machines
FSM Coverage Text Report

```

# Current State Object : cst
# -----
# State Value MapInfo :
# -----
#           State Name           Value
#           -----           -----
#                s0                0
#                s1                1
#                s2                2
# Covered States :
# -----
#           State           Hit_count
#           -----           -----
#                s0                20
#                s1                16
#                s2                16
# Covered Transitions :
# -----
#           Trans_ID           Transition           Hit_count
#           -----           -----           -----
#                0           s0 -> s1           16
#                1           s0 -> s0           2
#                2           s1 -> s2           16
#                4           s2 -> s0           16
#                5           s0->s1->s2           16
#                7           s1->s2->s0           16
#                9           s2->s0->s1           14
#                10          s0->s1->s2->s0           16
#                11          s1->s2->s0->s1           14
#                12          s2->s0->s1->s2           14
# Uncovered Transitions :
# -----
#           Trans_ID           Transition
#           -----           -----
#                3           s1 -> s0
#                6           s0->s1->s0
#                8           s1->s0->s1
#
# Summary           Active           Hits % Covered
# -----           -----           -----
# States           3           3           100.0
# Transitions     13          10           76.9

```

Related Topics

- [FSM Coverage](#)
- [FSM Coverage Metrics Available in the GUI](#)
- [Code Coverage](#)
- [Code Coverage in the Graphic Interface](#)
- [Coverage Reports](#)

Chapter 18

Verification Management

Note



The functionality described in this chapter requires a coverage license feature in your ModelSim license file. Please contact your Mentor Graphics sales representative if you currently do not have such a feature.

This chapter contains the following information regarding Verification Management with ModelSim.

Verification Management Overview	693
What is the Unified Coverage Database?	695
Coverage and Simulator Use Modes	695
Coverage View Mode and the UCDB	696
Running Tests and Collecting Data	696
Collecting and Saving Coverage Data	696
Rerunning Tests and Executing Commands	698
Merging Coverage Test Data	701
Ranking Coverage Test Data	704
About the Merge Algorithm	705
Merge Usage Scenarios	707
Viewing and Analyzing Verification Data	708
Understanding the Test Data in the UCDB	709
Storing User Attributes in UCDB	711
Viewing Test Data in the GUI	711
Generating HTML Coverage Reports	714
Storing User Attributes in UCDB	711
Retrieving Test Attribute Record Content	716

Verification Management Overview

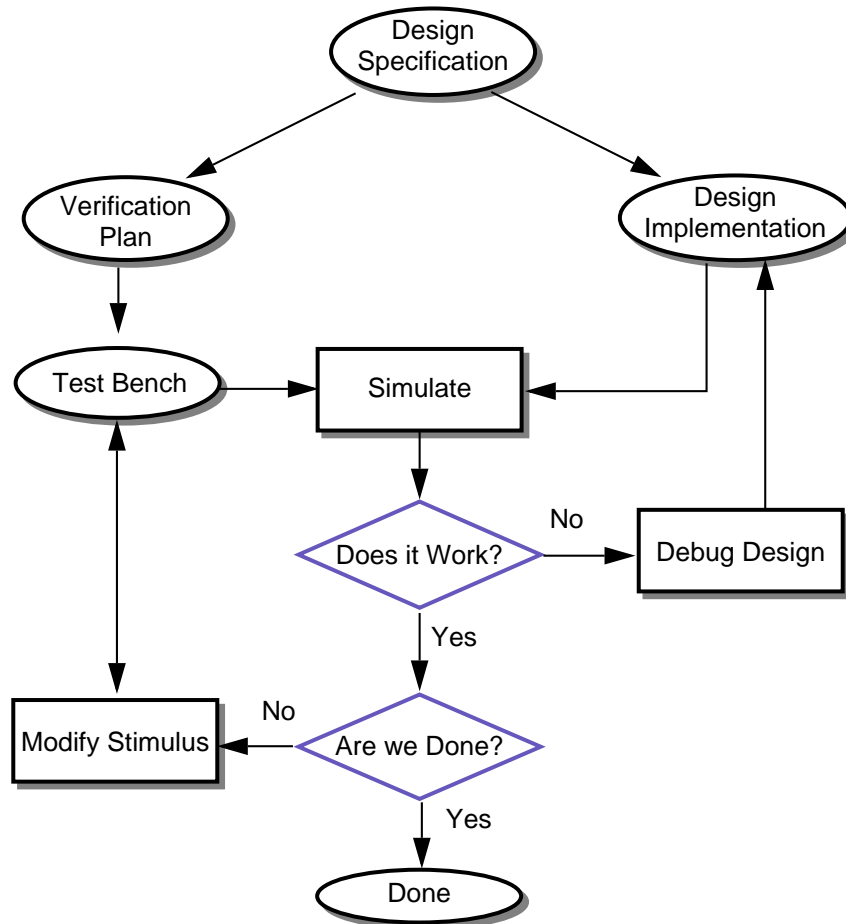
Verification Management within ModelSim is a set of functionality which allows you to manage your test environment. The management features included in this chapter are:

- the merging and aggregation of coverage data
- ranking of tests
- analysis of coverage in light of late-stage ECO's
- test and command re-runs

- various analyses of coverage data

The flow described in [Figure 18-1](#) represents a typical design verification process as it can be applied in the ModelSim environment.

Figure 18-1. Verification of a Design



Every project starts with a design specification. The specification contains elaborate details on the design construction and its intent.

A verification team uses the design specification to create a verification plan. The verification plan contains a list of all questions that need to be answered by the verification process (the golden reference). The verification plan also serves as a functional spec for the test bench.

Once the test bench is built and the designers succeed in implementing the design, you simulate the design to answer the question: “Does it work?”. If the answer is no, the verification engineer gives the design back to designers to debug the design. If yes, it is time to ask the next question: “Are we done yet?”. Answering this question involves investigating how much of the design has been exercised by looking at the coverage data and comparing it against the verification plan.

What is the Unified Coverage Database?

The Unified Coverage DataBase (UCDB) is a single persistent form for various kinds of verification data, notably: coverage data of all kinds, and some other information useful for analyzing verification results. The types of coverage data collected in the database include:

- Code coverage: branch, condition, expression, statement, and toggle
- Finite State Machine (FSM) coverage
- SystemVerilog covergroup coverage
- SVA and PSL directive coverage
- User-defined data
- Test data

The UCDB is used natively by ModelSim for all coverage data, deprecating previous separate file formats for code coverage and functional coverage.

When created from ModelSim, the UCDB is a single "snapshot" of data in the kernel. Thus, it represents all coverage and assertion objects in the design and test bench, along with enough hierarchical environment to indicate where these objects reside. This data is sufficient to generate complete coverage reports and can also be combined with data acquired outside ModelSim – for example, 0-In coverage and user-defined data.

Coverage and Simulator Use Modes

Most commands related to coverage are used in one of three simulation use modes that correspond to the type of coverage analysis required.

Table 18-1. Coverage Modes

Mode	Type of Coverage Analysis	Commands to Use
Simulation Mode	Interactive simulation	coverage , toggle , and vcov commands (such as clear , merge , report , save , tag , unlinked...)
Coverage View Mode	Post-process	coverage open <file>.ucdb or vsim -viewcov <file>.ucdb brings up separate GUI All coverage related commands are available
Batch Mode	Batch simulation	vcov commands (such as merge , report , stats , testnames...)

Each of these modes of analysis act upon a single, universal database that stores your coverage data, the Unified Coverage Database.

Coverage View Mode and the UCDB

Raw UCDB coverage data can be saved, merged with coverage statistics from the current simulation or from previously saved coverage data, and viewed at a later date using Coverage View mode.

Coverage View mode allows all ModelSim coverage data saved in the UCDB format – code coverage, covergroup coverage, directive coverage, and assertion data – to be called up and displayed in the same coverage GUIs used for simulation. The coverage view invocation of the tool is separate from that of the simulation. You can view coverage data in the Coverage View mode using the [coverage open](#) command or `vsim -viewcov`.

Running Tests and Collecting Data

Collecting and Saving Coverage Data	696
Rerunning Tests and Executing Commands	698
Merging Coverage Test Data	701
Ranking Coverage Test Data	704
About the Merge Algorithm	705
Merge Usage Scenarios.	707

Collecting and Saving Coverage Data

When you run tests, the coverage data which you instruct the simulator to save is placed in the Unified Coverage DataBase (UCDB). The UCDB is a single persistent form for various kinds of verification data, notably: coverage data of all kinds, and some other information useful for analyzing verification results. For more information on the UCDB, see “[What is the Unified Coverage Database?](#)”.

Prerequisites

Before coverage data can be saved, you must first:

1. Select the type of code coverage to be collected (`vlog +cover`). See “[Specifying Coverage Types for Collection](#)”.
2. Enable the coverage collection mechanism for the simulation run. See “[Enabling Simulation for Code Coverage Collection](#)”.
3. Run the simulation.

Naming the Test UCDB Files

By default, the test name given to a test is the same as the UCDB file base name, however you can name the test before saving the UCDB using a command such as:

```
coverage attribute -test mytestname
```



Tip — If you are saving test data for later test-associated merging and ranking, it is important that the test name for each test be unique. Otherwise, you will not be able to distinguish between tests when they are reported in per-test analysis.

Saving Coverage Data

Optionally, you can save the coverage data to a UCDB for post-process viewing and analysis.

Methods

The coverage data you have collected can be saved either on demand, or at the end of simulation.

Saving Data On Demand

Options for saving coverage data dynamically (during simulation) or in coverage view mode are:

- GUI: **Tools > Coverage Save**

This brings up the Coverage Save dialog box, where you can specify coverage types to save, select the hierarchy, and output UCDB filename.

- [coverage save](#) CLI command

During simulation, the following command saves data from the current simulation into a UCDB file called *myfile1.ucdb*:

```
coverage save myfile1.ucdb
```

While viewing results in coverage view mode, you can make changes to the data (using the [coverage attribute](#) command, for example). You can then save the changed data to a new file using the following command:

```
coverage save myfile2.ucdb
```

- `$coverage_save` system task (not recommended)

This non-standard SystemVerilog system task saves code coverage data only. It is not recommended for that reason. For more information, see “[System Tasks and Functions Specific to the Tool](#).”

Saving Data at End of Simulation

By default, coverage data is not automatically saved at the end of simulation. To enable the auto-save of coverage data, set a legal filename for the data using any of the following methods:

- **GUI: Tools > Coverage Save.** Enable the “Save on exit” radio button.
This brings up the Coverage Save dialog box, where you can also specify coverage types to save, select the hierarchy, and the output UCDB filename.
- **UCDBFilename**—“<filename>”, set in *modelsim.ini*
By default, <filename> is an empty string (“”).
- **coverage save -onexit** command, specified at Vsim> prompt
The **coverage save** command preserves instance-specific information. For example:

```
coverage save -onexit myoutput.ucdb
```
- **\$set_coverage_db_name(<filename>)**, executed in SystemVerilog code

If more than one method is used for a given simulation, the last command encountered takes precedence. For example, if you issue the command **coverage save -onexit vsim.ucdb** before simulation, but your SystemVerilog code also contains a **\$set_coverage_db_name()** task, with no name specified, coverage data is not saved for the simulation.

Related Topics

[Running Tests and Collecting Data](#)

[Merging Coverage Test Data](#)

[Ranking Coverage Test Data](#)

Rerunning Tests and Executing Commands

You can rerun tests and execute commands from the **Verification Browser > Command Execution** functionality.

Requirements

The following requirement applies only if:

- you are running multiple simulations using the same UCDB filename and you have used the same UCDB name in different directories (fred/cov.ucdb, george/cov.ucdb, and so forth)

OR


- you are loading multiple UCDBs from the same basic test (that is, fred.ucdb is the basic test and you want to create multiple runs of that test)

If either of these cases is true, your **initial** simulation run (the one you intend to re-run) must include a command to set the TESTNAME attribute. Failure to set the TESTNAME attribute in these cases may result in otherwise unique tests being identified as duplicates (and therefore not executed) by the re-run algorithm and in the merge/rank output files. See the Concept note below for further information.

To explicitly set the TESTNAME attribute in simulation, include a command such as:

coverage attribute -test <testname>

See “[coverage attribute](#)” for command syntax.

 When you rerun a test, the simulator uses an attribute called TESTNAME, saved in each test record, to build a list of unique files selected for re-run of that test. By default, the TESTNAME is the pathless basename of the UCDB file into which the coverage results of a given test were stored from the initial run.

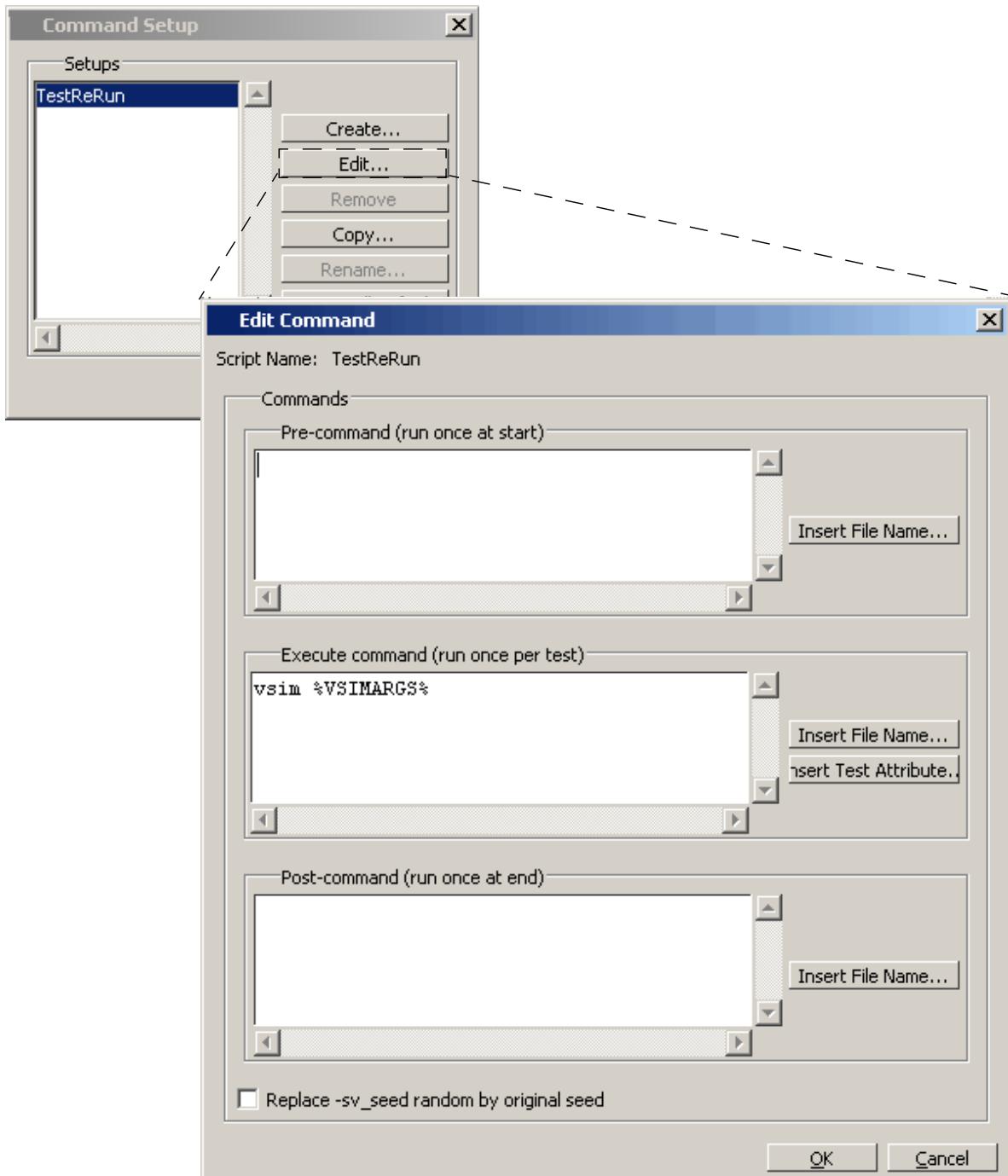
Procedure

To rerun a test or execute a command from the Browser:

1. Enter the re-run setup:
 - a. Select one or more UCDB files.
 - b. Right-click and select **Command Execution > Setup**.

This displays the Command Setup dialog box, shown in [Figure 18-2](#).

Figure 18-2. Command Setup Dialog Box



The Command Execution Setup dialog box allows you to select and view user-defined command setups, save new setups, and remove run setups previously saved. You can either select an existing test to re-run, or enter the following commands to run individually:

- Pre-command — a script you may need to run once at startup, prior to the run

- **Execute Command** — commands to execute: This field is pre-populated with the command(s) necessary to rerun the test(s) selected when you opened the dialog.
- **Post-command** — a script you may need to run at the end (for example, a cleanup script)

You can also select a radio button to apply the original seed (defined by the last run wherein the `vsim -sv_seed random` argument was used) to the current execution.

c. Select OK to apply the setup as edited.

2. Rerun the test: Right-click in the Browser, and select:

- **Command Execution > Execute on All** to re run all tests listed in browser, or
- **Command Execution > Execute on Selected** to run only those tests associated with the currently selected UCDB files.

Related Topics

[Running Tests and Collecting Data](#)

[Rerunning Tests and Executing Commands](#)

[Ranking Coverage Test Data](#)

[Merging Coverage Test Data](#)

Merging Coverage Test Data

When you have multiple sets of coverage data, from multiple tests of the same design, you can combine the results into a single UCDB by merging the UCDB files. The merge utility supports:

- instance-specific toggles
- summing the instances of each design unit
- source code annotation
- printing of condition and expression truth tables
- cumulative / concurrent merges

The coverage data contained in the merged UCDB is a union of the items in the UCDBs being merged. For more information, see [“About the Merge Algorithm”](#).

A file locking feature of the merge allows for cumulative merging on a farm -- `vcover merge out out in --` such that the "out" file is not corrupted with multiple concurrent merges. It recovers from crashing merges, crashing hosts, and allows time-out of merges, as well as backups of the previous output.

Methods

The tool allows you to merge test data using the:

- GUI: Verification Browser window
- Command Line: See the [vcover merge](#) command for syntax

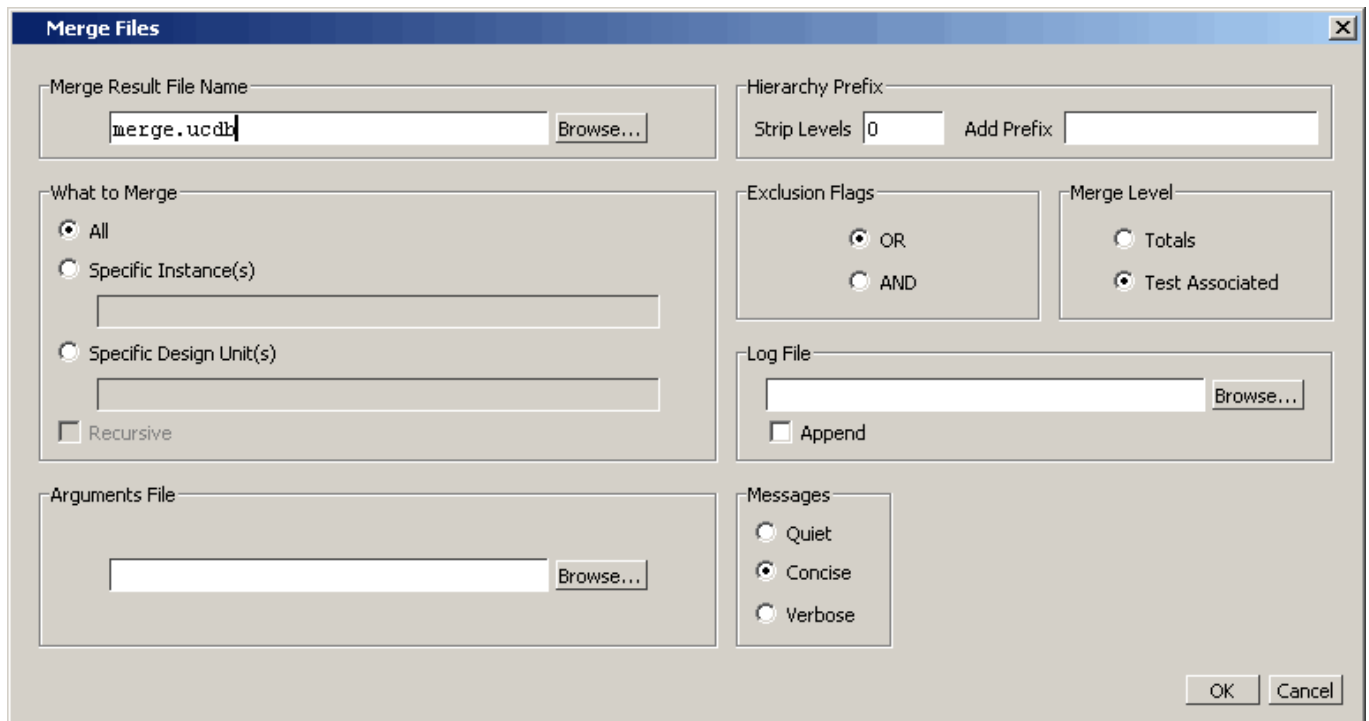
Merging within Verification Browser Window

You can merge multiple .ucdb files (including a verification plan) from the Verification Browser window as follows:

1. Select the .ucdb file(s) to merge.
2. Right-click over the file names and select Merge.

This displays the Merge Files Dialog Box, as shown in [Figure 18-3](#). The various options within the dialog box correspond to the arguments available with the [vcover merge](#) command.

Figure 18-3. File Merge Dialog



3. Fill in fields in the Merge Files dialog box, as required. A few of the more important, less intuitive fields are highlighted here. For full details related to these fields, see “[vcover merge](#)”.
 - Set the Hierarchy Prefix: Strip Level / Add Prefix to add or remove levels of hierarchy from the specified instance or design unit.
 - For Exclusion Flags, select AND when you want to exclude statements in the output file *only* if they are excluded in all input files. When OR is selected (default) a

statement is excluded in the output merge file if the statement is excluded in any of the input files.

- o Test Associated merge is the default Merge Level. Before selecting Totals as the Merge Level, be sure you understand the difference between them. If not refer to “[Test-Associated Merge versus Totals Merge Algorithm](#)”.

4. Select OK

This creates the merged file and loads the merged file into the Verification Browser window.

Validation

If the merge was successful, a transcript message such as the following appears:

```
# Merge in Process.....
#
# Merging file C:/QuestaSim_6.4/examples/ucdb/testplan/DataTest.ucdb
# Merging file C:/QuestaSim_6.4/examples/ucdb/testplan/FifoTest.ucdb
# Merging file C:/QuestaSim_6.4/examples/ucdb/testplan/IntialTest.ucdb
# Merging file C:/QuestaSim_6.4/examples/ucdb/testplan/ModeTwoTest.ucdb
# Writing merged result to merge.ucdb
```

Merging with the vcover merge Command

The merge command, [vcover merge](#), allows you to merge multiple coverage data files offline, without first loading a design. The merge utility is a standard ModelSim utility that can be invoked from the command line. For example,

```
vcover merge output inputA.ucdb inputB.ucdb
```

merges coverage statistics in UCDB files inputA.ucdb and inputB.ucdb and writes them to a new UCDB file called output. See “[vcover merge](#)” for a complete list and description of available arguments.

Merging and Source Code Mismatches

By default ModelSim performs checks on source code stability when performing operations like merging statement coverage, or other source-based data.

If one UCDB is generated with version X of file *t.v*, and then another UCDB is generated with version Y of file *t.v*, it doesn't make sense to merge the source-based coverage metrics in those two UCDBs. This kind of checking is known as design unit signature checking. When a merge such this is attempted, Warning #6820 is issued stating that the merge of the instance in which those lines occur is being skipped.

One cause of legitimate difference between the design source in two different UCDBs is the use of ``ifdef` to conditionally define code. However, this difference may not be substantive. In cases

such as this, you might want to work around this check. To bypass the ModelSim DU signature check, use the `-ignoredusig` argument to the `vcover merge` command.

Caution



You should not use `-ignoredusig` lightly, without validating that the differences in source code are OK. Misuse of `-ignoredusig` can lead to very confusing coverage results, because code coverage results are merged based on line numbers, and merged results can be significantly wrong if line numbers have changed between versions of the source.

Related Topics

[About the Merge Algorithm](#)

[About the Merge Algorithm](#)

[Merge Usage Scenarios](#)

[Ranking Coverage Test Data](#)

[Rerunning Tests and Executing Commands](#)

Ranking Coverage Test Data

You can rank your tests by any number of criteria using either the **Verification Browser** > **Rank** menu selection, or the `vcover ranktest` command with various parameters and UCDB files as input. The ranking result files are based on the selected `.ucdb` files.

Procedure

1. Select one or more `.ucdb` files.
2. Right-click and select **Rank**.

This displays the Rank Files Dialog Box. The various options within the dialog box correspond to arguments available with the `-du` and `-path` arguments to `vcover ranktest` command.

3. Fill in What to Rank, Rank By, and Stop Ranking When, as desired.
4. Select Advanced Options to open the dialog box to set your coverage metrics, arguments file, and ranked results file names.
5. OK

This creates the `.rank` file, loads it into the Test Browser, and also outputs ranking data to the transcript. For example:

```
#
#           Metric           Bins   Covered%   Inc%
#
# Cover Groups/Points      5/18     0.0000    0.0000
#   CoverDirectives         10     0.0000    0.0000
#       Statements      2605    47.0633    47.0633  *****
#           Branches     1978    29.6764    29.6764  *****
#       Expressions        711    18.2841    18.2841   ***
#           Conditions    1315    15.9696    15.9696   ***
```


#	ToggleNodes	2214	1.1743	1.1743	
#	States	17	17.6471	17.6471	***
#	Transitions	45	6.6667	6.6667	*
#	AssertPasses	12	0.0000	0.0000	

Test-Associated vs. Iterative Ranking

Test-associated ranking performs a merge and proceeds to rank based upon a test-associated merged result held in memory, whereas iterative ranking ranks each individual test by performing an iteration of merges on the file system.

The test-associated ranking method is superior to the iterative method in two ways:

- better performance
- ranking is performed with respect to the entire coverage space:

If the coverage space differs between files — perhaps because of differently parameterized covergroups or differently elaborated versions of the design — that is a problem for ranking. To handle the case where new tests expose new holes that disturb the ranking, the ranking algorithm and its metrics must be more complex and are more difficult to explain.

However, there are some cases where the test-associated ranking does not always work intuitively: Because it only records what test covered a particular bin, the test-associated algorithm may underestimate coverage for test subsets where "at_least" values are greater than 1.

The iterative ranking option is available to work around cases of covergroups and cover directives where `at_least > 1`, however it is considerably less efficient (slower).

Related Topics

[About the Merge Algorithm](#)

[Test-Associated Merge versus Totals Merge Algorithm](#)

[Merge Usage Scenarios](#)

About the Merge Algorithm

- When you perform a merge on multiple UCDBs, all test data records with unique testnames are concatenated into the merged UCDB file. If you merge two tests that have identical names but different data contents, a warning is issued.
- A merged file contains one test data record for each of the different tests that were merged into the file. For example, if you merged three UCDBs saved from simulation (vsim), you get three test attribute records. If you merge that file with another one saved from vsim, you get $3 + 1 = 4$ test data records, and so on. See “[Understanding the Test Data in the UCDB](#)” for more information on the content of test data records.

- The merge algorithm that ModelSim uses is a union merge. Line numbers from the files are merged together, so that if different UCDBs have different sets of coverage source lines, the resulting merged database contains a union of the set of source lines in the inputs.
- Toggles and FSMs, which have no source information, are merged as follows:
 - Toggles are merged with a union operation: objects with the same name are always merged together, regardless of how many are present in each UCDB input file.
 - FSMs are merged together by the order in which they appear in a given module instance or design unit.

Test-Associated Merge versus Totals Merge Algorithm

You can choose one of two levels of information that is preserved in the merged database by using either the `-testassociated` (default), or the `-totals` argument to the `vcover merge` command. The merge options are:

- **-totals** merge — Creates a basic merge: sums the coverage.

Merges together the coverage scopes, design scopes, and test plan scopes. The counts are incremented together (ORed together in the case of vector bin counts). The final merge is a union of objects from the input files. Information about which test contributed what coverage into the merge is lost. Information about tests themselves are not lost — test data records are added together from all merge inputs. While the list of tests can be known, it cannot be known what tests might have incremented particular bins.
- **-testassociated** merge — This is the default merge. Includes all data in totals merge and additionally marks covered bins with the test that covered them.

Includes the basic information obtained with `-totals` as well as the associated tests and bins. When tests and bins are associated, each coverage count is marked with the test that caused it to be covered.

 - For functional coverage, this means that the bin count should be greater than or equal to the `at_least` parameter.
 - For code coverage and assertion data, any non-zero count for a test causes the bin to be marked with the test.

While the test-associate merge can not tell you which test incremented a bin by exactly how much, it can tell you which test caused a bin to be covered.

Related Topics

[Ranking Coverage Test Data](#)

[Merge Usage Scenarios](#)

Merge Usage Scenarios

The decision on how to merge a set of UCDB files depends upon where and how the data being merged is stored in the databases. As a way of understanding your options, consider three basic merge scenarios, as follows:

Scenario 1: Two UCDBs, same scope

You have data from two or more UCDB files, at the same level of hierarchy (scope) in the design. Example commands:

```
vclover merge output.ucdb file1.ucdb file2.ucdb
```

Scenario 2: Two UCDBs, different scopes

You have data from two or more UCDB files, at different levels of hierarchy. For example: */top/des* instance in *filea.ucdb*, and *top/i/des* instance in *fileb.ucdb*.

- Option 1: Strip top levels of hierarchy from both and then merge the stripped files. Example commands:

```
vclover merge -strip 1 filea_stripped.ucdb filea.ucdb  

vclover merge -strip 2 fileb_stripped.ucdb fileb.ucdb  

vclover merge output.ucdb filea_stripped.ucdb fileb_stripped.ucdb
```

- Option 2: Strip levels off instance in one UCDB file, and install to match the hierarchy in the other. In this example, strip */top/* off the */top/des* and then add the */top/i* hierarchy to it. Example commands:

```
vclover merge -strip 1 filea_stripped.ucdb filea.ucdb  

vclover merge -install /top/i filea_installed.ucdb filea_stripped.ucdb  

vclover merge output.ucdb filea_installed.ucdb fileb.ucdb
```

Scenario 3: Single UCDB, two sets of data

You have two sets of data from a *single* UCDB file, at different levels of hierarchy. Because they are instantiated at different levels within the same file, the tool cannot merge both of them into the same database. In this scenario, it is best to merge by design unit type using the [vclover merge -du](#) command.

For example, */top/designinst1* and */top/other/designinst2* are two separate instantiations of the same design unit within a single UCDB file. An example command for merging all instances in *file3.ucdb* would be:

- for Verilog with a module name of *design*
`vcover merge -du design output.ucdb file3.ucdb`
- for VHDL with an entity name of *design* and an architecture name of *arch1* would be
`vcover merge -du design(arch1) output.ucdb file3.ucdb`

Scenario 4: Concurrent merge jobs

You can have concurrent merge jobs running on different machines which are simultaneously writing to the same target merge file. A lock file is created which prevents any conflicts. The utility can recover from crashing merges and crashing hosts. It also allows a configurable time-out of merges, as well as backups of the previous output. See the [vcover merge](#) command for syntax details.

Use the vcover merge command as follows:

```
vcover merge out.ucdb out.ucdb in.ucdb
```

Note



If this is the very first merge, the input file “out.ucdb” will not exist yet, so the simulator issues a warning. In this case, specify the appropriate <input>.ucdb file.

This command takes the output UCDB and merges it with a second input UCDB.

```
vcover merge out.ucdb out.ucdb in2.ucdb -timeout 10 -backup
```

Then, another machine can take the output of the first merge command and third input UCDB, and so on.

Related Topics

[Merging Coverage Test Data](#)

[About the Merge Algorithm](#)

Viewing and Analyzing Verification Data

Understanding the Test Data in the UCDB.	709
Storing User Attributes in UCDB.	711
Viewing Test Data in the GUI	711
Generating HTML Coverage Reports.	714
Retrieving Test Attribute Record Content	716

Understanding the Test Data in the UCDB

When you save a set of coverage data into the UCDB, that data is written into individual test records, one for each test that is run. Each test record contains test record attributes (fields) which, in turn, contain two sub-sets of attributes. Specifically, these are:

- specific predefined attributes which contain information about the test, such as the testname or username. These predefined attributes define the columns that appear by default in the Browser window. See [Table 18-2](#) for a list of predefined attributes which appear as columns.
- user-defined attributes (as name/value pairs). The values of these attributes define the columns that can be selected to appear in the Browser window. See “[Storing User Attributes in UCDB](#)” for instructions on creating user-defined attributes.

When you perform a merge on multiple UCDBs, all test data records with unique testnames are concatenated into the merged UCDB file. If you merge two tests that have identical names but different data contents, a warning is issued. A merged file contains one test data record for each of the different tests that were merged into the file. For example, if you merged three UCDBs saved from simulation (vsim), you get three test attribute records. If you merge that file with another one saved from vsim, you get $3 + 1 = 4$ test data records, and so on.

Test Attribute Records in UCDB

Test attribute records are stored in the UCDB when you save your coverage information. One test attribute record exists for each simulation (test). Each test attribute record contains name-value pairs — which are attributes themselves — representing information about that particular test. Many of these attributes within the test attribute record are predefined, however, you can also create your own using the [coverage attribute](#) command.

Predefined Attribute Data

Each field has a default value based on your simulation. You can override some values with the coverage attribute command, while in simulation mode, and before saving the UCDB file with the coverage save command.

[Table 18-2](#) lists fields in the test attribute record (in the UCDB) that are predefined.

Table 18-2. Predefined Fields in UCDB Test Attribute Record

Field / Attribute Name	Override with coverage attribute command	Description
TESTNAME	-name TESTNAME -value <string>	Name of the coverage test. This is also the name of the test record.

Table 18-2. Predefined Fields in UCDB Test Attribute Record

Field / Attribute Name	Override with coverage attribute command	Description
SIMTIME		Simulation time at completion of the test. (In ModelSim, the \$Now TCL variable contains the current simulation time in a string of the form: <i>simtime simtime_units</i> .)
TIMEUNIT		Units for simulation time: "fs", "ps", "ns", "us", "ms", "sec", "min", "hr".
CPUTIME		CPU time for completion of the test. (In QuestaSim, the <i>simstats</i> command returns the CPU time.)
DATE		Timestamp is at the start of simulation. If created by ModelSim, this is a string of the format: yyymmddhhmmss for example: 20060105160030 which represents 4:00:30 PM January 5, 2006
VSIMARGS	-name VSIMARGS -value <string>	Simulator command line arguments.
USERNAME	-name USERNAME -value <string>	User ID of user who ran the test.
TESTSTATUS	-name TESTSTATUS -value <int>	Status of the test, where the values are either an integer (transcript) or an enumerated value (GUI): 0 (OK) - this is the default setting 1 (WARNING) 2 (ERROR) 3 (FATAL) 4 (MISSING) 5 (MERGE_ERROR)
ORIGFILENAME		name of the test file.
SEED	-seed <int>	Randomization seed for the test. (Same as the seed value provided by the "-sv_seed" vsim option.)
COMPULSORY	-compulsory <int>	Whether (1) or not (0) this test should be considered compulsory (that is, a "must-run" test).
RUNCWD		Current working directory for the test.

Table 18-2. Predefined Fields in UCDB Test Attribute Record

Field / Attribute Name	Override with coverage attribute command	Description
HOSTNAME		Computer identification
HOSTOS		Operating System
WLFNAME		Associated WLF file for the test.
LOGNAME		Associated transcript or log file for the test.
TESTCOMMENT	-comment	String (description) saved by the user associated with the test. This field will only appear when explicitly specified.
TESTCMD	-command	Test script arguments. Used to capture "knob settings" for parameterizable tests, as well as the name of the test script. This field will only appear when explicitly specified.

Related Topics

[Storing User Attributes in UCDB](#)

Storing User Attributes in UCDB

You can add your own attributes to a specified test record using the coverage attribute command. with a command such as:

```
coverage attribute -test testname -name Responsible -value Joe
```

This command adds the “Responsible” attribute to the list of attributes and values displayed when you create a coverage report on *testname.UCDB*.

Viewing Test Data in the GUI

Data related to the management of your verification data can be viewed in the Verification Browser window (**Layout > VMgmt** or **View > Verification Management > Browser**).

Viewing Test Data in the Browser Window

You can view both UCDB (.ucdb) and rank result (.rank) files in the Verification Browser window.

Prerequisites

- You must be located in a directory containing .ucdb or .rank files.

Procedure

1. Open the Verification Management window:
View > Verification Management > Browser
2. Add files to the Browser using one of the following three methods:
 - Right-click in the window and select **Add File**. Select desired .ucdb files from the list that appears in the **Add File(s)** dialog box.
 - When the window is active, select **Verification Browser > Add File** from the menu bar of the Main window. Select desired .ucdb files from the list that appears in the **Add File(s)** dialog box.
 - At the vsim command prompt, execute the **add testbrowser** command, which accepts UCDB and rank result files as arguments. For example,
add testbrowser test.ucdb

The Verification Browser window appears, similar to [Figure 18-4](#).

Figure 18-4. Test Data in Verification Browser Window

FileName	TestName	Statements	Branches	Expressions	Conditions	ToggleNode
DataTest.ucdb	DataTest	68.62	58.21	59.91	30.85	37.0
FifoTest.ucdb	FifoTest	72.21	64.52	67.79	34.14	45.0
IntialTest.ucdb	IntialTest	70.92	63.97	64.83	34.00	42.0
merge.ucdb	-	95.23	91.88	76.93	64.82	74.0
ModeTwoTest.ucdb	ModeTwoTe...	71.41	64.42	66.24	34.78	41.0
testplan.ucdb	-	0.00	0.00	0.00	0.00	0.0
TxDataTest.ucdb	TxDataTest	71.41	64.42	66.52	34.78	42.0
VariableTest.ucdb	VariableTest	70.92	63.97	64.97	34.00	43.0

Deleting UCDB Files from the Browser Window

To remove UCDB files from Browser, highlight the test(s) you want to delete from view and select or <Ctrl-Del> (while the Verification Browser window is active). A popup appears for you to confirm if you want to delete the selected test(s) from the Verification Browser window.

Invoking Coverage View Mode

UCDB files from previously saved simulations are only viewable in Coverage View mode (post-processing). You can invoke Coverage View Mode on any of your .ucdb files in the Test Browser or at the command line. This allows you to view saved and/or merged coverage results from earlier simulations.

Procedure

- GUI:
 - a. Right-click to select .ucdb file. This functionality does not work on .rank files.
 - b. Select **Invoke CoverageView Mode**.

The tool then opens the selected .ucdb file and reformats the Main window into the coverage layout. A new dataset is created.

- Command Line:

Enter `vsim` with the `-viewcov <ucdb_filename>` argument. Multiple `-viewcov` arguments are allowed. For example, the Coverage View mode is invoked with:

```
vsim -viewcov myresult.ucdb
```

where *myresult.ucdb* is the coverage data saved in the UCDB format. The design hierarchy and coverage data is imported from a UCDB.

Related Topics

[Coverage View Mode and the UCDB](#)

Customizing the Column Views

You can customize the display of columns in the Verification Browser window, and then save these views for later use.

Procedure

1. Select [**Create/Edit/Remove ColumnLayout...**] from the pull down list.

This displays the Create/Edit/Remove Column Layout dialog box.
2. Enter a new name in the Layout Name text entry box.
3. OK

You can also add or modify pre-defined column arrangement from the Create/Edit/Remove Column Layout dialog box by adding columns to or removing them from the Visible Columns box as desired.

After applying your selections, the rearranged columns and custom layouts are saved and appear when you next open that column view in the Verification Browser or Tracker windows.

Related Topics

[Test Attribute Records in UCDB](#)



Generating HTML Coverage Reports

You can create on-screen, static coverage reports in HTML that are easy to use and understand.

Requirements and Recommendations

- For best results, the report should be viewed with a browser that supports the following:
 - JavaScript — Without this support, your browser will work, but the report is not as aesthetically pleasing.
 - cookies — For convenience of viewing coverage items in the HTML pages, you should enable cookies.
 - frames and Cascading Stylesheets (CSS) — Though support is recommended for frames, reports can still be displayed on browsers without this support. The report writer uses CSS to control the presentation, and will be best viewed with browsers that support frames and CSS.

Procedure

To generate an HTML report from the GUI:

1. Select a single UCDB file from the Browser
2. From the main menu, select **Browser > HTML Report** or in the Browser, select **Right click > HTML Report**

This brings up the dialog box that allows the user to control the generation and subsequent viewing of the report.

You can also use the `-html` switch with the [coverage report](#) or [vcover report](#) command at the command line.

An example HTML coverage report is shown in [Figure 18-5](#).

HTML Generation for Large Designs

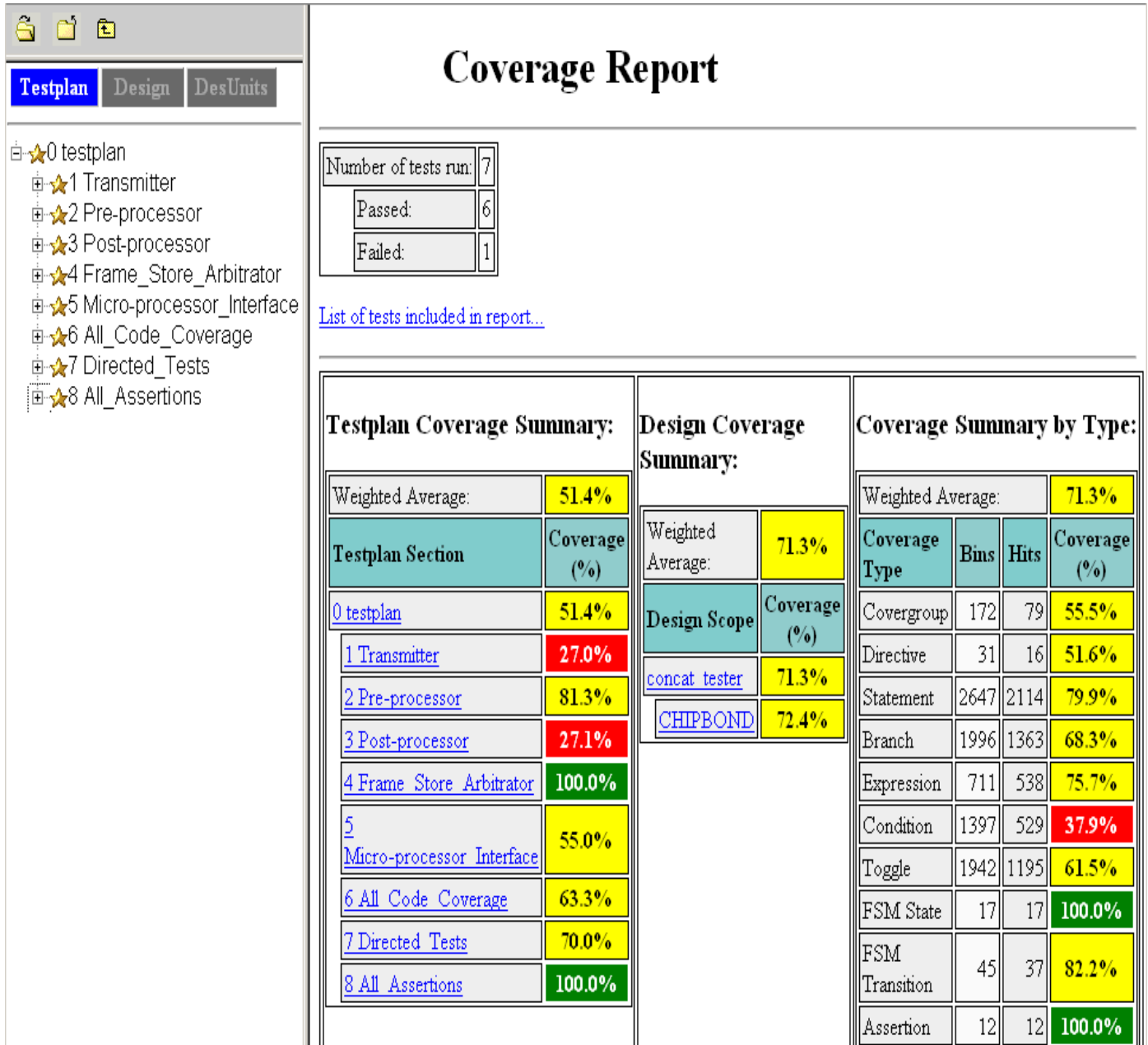
The `"-noframes"` option disables generation of JavaScript-based tree which has known performance problems for designs with a large number of design scopes. With this option, the report comes up as a single frame containing the top-level summary page and an HTML-only design scope index page is available as a link from the top-level page.

The `"-nodetails"` option omits coverage detail pages. This can save report generation time and disk space for very large designs.

Output

The output of this utility is an index.html file viewable with any reasonably modern web browser (See Figure 18-5). The web browser allows you to explore the hierarchy of the design, much like you might browse a file system. Colorized copies of the design source code are generated and linked into the report at the appropriate places.

Figure 18-5. HTML Coverage Report



Retrieving Test Attribute Record Content

Two commands can be used to retrieve the content of test attributes: [coverage attribute](#) and [vcover attribute](#), depending on which of the simulation modes you are in.

To retrieve test attribute record contents from:

- the simulation database during simulation (vsim), use [coverage attribute](#). For example:
coverage attribute
- a UCDB file during simulation, use [vcover attribute](#). For example:
vcover attribute <file>.ucdb
- a UCDB file loaded with -viewcov, use [coverage attribute](#). For example:
coverage attribute -test <testname>

The Verification Browser window displays columns which correspond to the individual test data record contents, including name/value pairs created by the user. The pre-defined attributes that appear as columns are listed in [Table 18-2](#).

See “[Customizing the Column Views](#)” for more information on customizing the column view.

C Debug allows you to interactively debug FLI/PLI/VPI/DPI/SystemC/C/C++ source code with the open-source gdb debugger. Even though C Debug does not provide access to all gdb features, you may wish to read gdb documentation for additional information. For debugging memory errors in C source files, please refer to the application note titled *Using the valgrind Tool with ModelSim*.

Note



To use C Debug, you must have a cdebug license feature in your ModelSim license file. If you currently do not have such a feature, please contact your Mentor Graphics sales representative.



Tip: Before you use C Debug, please note the following qualifications and requirements:

- C Debug is an interface to the open-source gdb debugger. ModelSim contains no customized gdb source code, and C Debug does not remove any limitations or problems of gdb.
- You should have some experience and competence with C or C++ coding, and C debugging in general.
- Recommended usage is that you invoke C Debug once for a given simulation and then quit both C Debug and ModelSim. Starting and stopping C Debug more than once during a single simulation session may cause problems for gdb.
- Generally, you should not have an existing *.gdbinit* file. If you do, make certain you haven't done any of the following within it: defined your own commands or renamed existing commands; used 'set annotate...', 'set height...', 'set width...', or 'set print...'; set breakpoints or watchpoints.
- To use C Debug on Windows platforms, you must compile your source code with gcc/g++. Refer to [Running C Debug on Windows Platforms](#), below.

Supported Platforms and gdb Versions

ModelSim ships with the gdb 6.0 debugger. Testing has shown this version to be the most reliable for SystemC applications. However, for FLI/PLI/VPI applications, you can also use a current installation of gdb if you prefer.

For gcc versions 4.0 and above, gdb version 6.1 (or later) is required.

C Debug has been tested on these platforms with these versions of gdb:

Table 19-1. Supported Platforms and gdb Versions

Platform	Required gdb version
32-bit Solaris 8, 9, 10 ¹	<code>gdb-5.0-sol-2.6</code>
32-bit Redhat Linux 7.2 or later ¹	<code>/usr/bin/gdb 5.2</code> or later
32-bit Windows 2000 and XP	<code>gdb 6.0</code> from MinGW-32
Opteron / SuSE Linux 9.0 or Redhat EWS 3.0 (32-bit mode only) ¹	<code>gdb 6.0</code> or later
x86 / Redhat Linux 6.0 to 7.1 ¹	<code>/usr/bin/gdb 5.2</code> or later
Opteron & Athlon 64 / Redhat EWS 3.0	<code>gdb 5.3.92</code> or <code>6.1.1</code>

1. ModelSim ships gdb 6.3 for Solaris 8, 9, 10 and Linux platforms.

To invoke C Debug, you must have the following:

- A *cdebug* license feature.
- The correct gdb debugger version for your platform.

Running C Debug on Windows Platforms

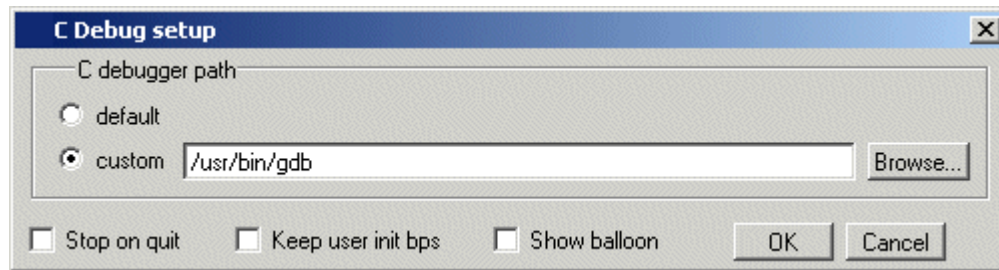
To use C Debug on Windows, you must compile your C/C++ source code using the gcc/g++ compiler installed separately from ModelSim. Source compiled with Microsoft Visual C++ is not debuggable using C Debug.

You should install the g++ compiler at the same directory level as your product install

Setting Up C Debug

Before viewing your SystemC/C/C++ source code, you must set up the C Debug path and options. To set up C Debug, follow these steps:

1. Compile and link your C code with the **-g** switch (to create debug symbols) and without **-O** (or any other optimization switches you normally use). See [SystemC Simulation](#) for information on compiling and linking SystemC code. Refer to the chapter [Verilog Interfaces to C](#) for information on compiling and linking C code.
2. Specify the path to the gdb debugger by selecting **Tools > C Debug > C Debug Setup**

Figure 19-1. Specifying Path in C Debug setup Dialog

Select "default" to point at the supplied version of gdb or "custom" to point at a separate installation.

3. Start the debugger by selecting **Tools > C Debug > Start C Debug**. ModelSim will start the debugger automatically if you set a breakpoint in a SystemC file.
4. If you are not using **gcc**, or otherwise haven't specified a source directory, specify a source directory for your C code with the following command:

```
ModelSim> gdb dir <srcdirpath1>[:<srcdirpath2>[...]]
```

Running C Debug from a DO File

You can run C Debug from a DO file but there is a configuration issue of which you should be aware. It takes C Debug a few moments to start-up. If you try to execute a run command before C Debug is fully loaded, you may see an error like the following:

```
# ** Error: Stopped in C debugger, unable to real_run mti_run 10us
# Error in macro ./do_file line 8
# Stopped in C debugger, unable to real_run mti_run 10us
#   while executing
# "run 10us
```

In your DO file, add the command **cdbg_wait_for_starting** to alleviate this problem. For example:

```
cdbg enable_auto_step on
cdbg set_debugger /modelsim/5.8c_32/common/linux
cdbg debug_on
cdbg_wait_for_starting
run 10us
```

Setting Breakpoints

Breakpoints in C Debug work much like normal HDL breakpoints. You can create and edit them with ModelSim commands ([bp](#), [bd](#), [enablebp](#), [disablebp](#)) or via a Source window in the GUI (see [File-Line Breakpoints](#)). Some differences do exist:

- The Modify Breakpoints dialog, accessed by selecting **Tools > Breakpoints**, in the ModelSim GUI does not list C breakpoints.

- C breakpoint id numbers require a "c." prefix when referenced in a command.
- When using the `bp` command to set a breakpoint in a C file, you must use the `-c` argument.
- You can set a SystemC breakpoint so it applies only to the specified instance using the `-inst` argument to the `bp` command.
- If you set a breakpoint inside an export function call that was initiated from an `SC_METHOD`, you must use the `-scdpidebug` argument to the `vsim` command. This will enable you to single-step through the code across the SystemC/SystemVerilog boundary.

Here are some example commands:

```
bp -c *0x400188d4
```

Sets a C breakpoint at the hex address 400188d4. Note the '*' prefix for the hex address.

```
bp -c or_checktf
```

Sets a C breakpoint at the entry to function **or_checktf**.

```
bp -c or.c 91
```

Sets a C breakpoint at line 91 of *or.c*.

```
bp -c -cond "x < 5" foo.c 10
```

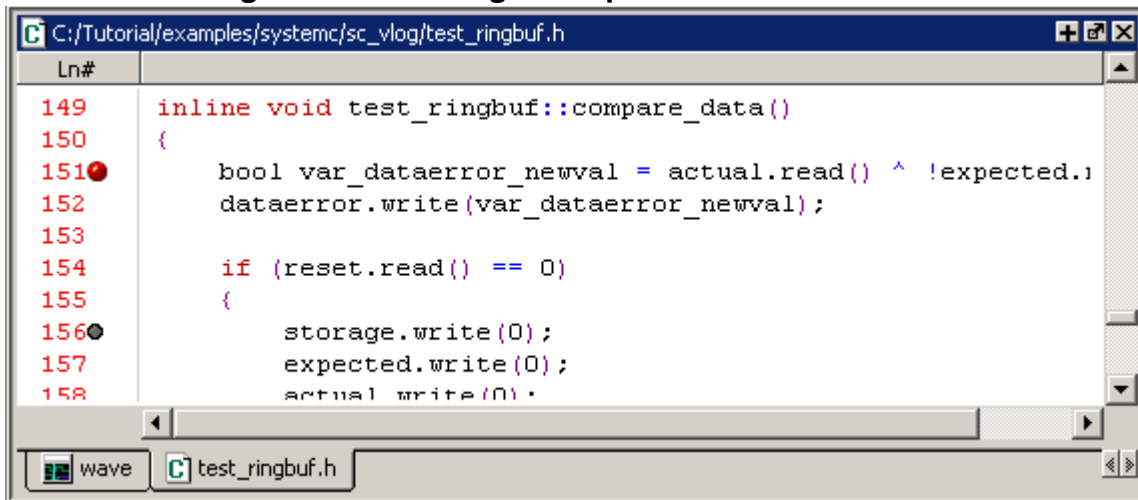
Sets a C breakpoint at line 10 of source file *foo.c* for the condition expression "x < 5".

```
enablebp c.1
```

Enables C breakpoint number 1.

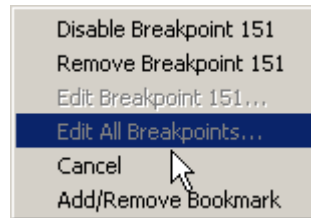
The graphic below shows a C file with one enabled breakpoint (indicated by a red ball on line 151) and one disabled breakpoint (indicated by a gray ball on line 154).

Figure 19-2. Setting Breakpoints in Source Code



Clicking the red ball with your right (third) mouse button pops up a menu with commands for removing or enabling/disabling the breakpoints.

Figure 19-3. Right Click Pop-up Menu on Breakpoint



Note



The gdb debugger has a known bug that makes it impossible to set breakpoints reliably in constructors or destructors. Do not set breakpoints in constructors of SystemC objects; it may crash the debugger.




Stepping in C Debug

Stepping in C Debug works much like you would expect. You use the same buttons and commands that you use when working with an HDL-only design.

Table 19-2. Simulation Stepping Options in C Debug

Button	Menu equivalent	Other equivalents
--------	-----------------	-------------------

Table 19-2. Simulation Stepping Options in C Debug

 <p>Step steps the current simulation to the next statement; if the next statement is a call to a C function that was compiled with debug info, ModelSim will step into the function</p>	<p>Tools > C Debug > Run > Step</p>	<p>use the step command at the CDBG> prompt see: step command</p>
 <p>Step Over statements are executed but treated as simple statements instead of entered and traced line-by-line; C functions are not stepped into unless you have an enabled breakpoint in the C file</p>	<p>Tools > C Debug > Run > Step -Over</p>	<p>use the step -over command at the CDBG> prompt see: step command</p>
 <p>Continue Run continue the current simulation run until the end of the specified run length or until it hits a breakpoint or specified break event</p>	<p>Tools > C Debug > Run > Continue</p>	<p>use the run -continue command at the CDBG> prompt see: run command</p>

Debugging Active or Suspended Threads

You can use C Debug to debug either an active or a suspended thread and then view its contents (such as call stack, local variables, and source code).

You can debug a suspended thread in either of the following situations:

- While the simulation is running
- When the simulation is stopped at a breakpoint in an active SystemC/HDL thread

Known Problems With Stepping in C Debug

The following are known limitations which relate to problems with gdb:

- With some platform and compiler versions, **step** may actually behave like **run -continue** when in a C file. This is a gdb limitation that results from not having any debugging information when in an internal function to VSIM (that is, any FLI or VPI function). In these situations, use **step -over** to move line-by-line.
- Single-stepping into DPI-SC import function occasionally does not work if the SystemC source files are compiled with gcc-3.2.3 on linux platform. This is due to a gcc/gdb interaction issue. It is recommended that you use gcc-4.0.2 (the default gcc compiler for linux platform in current release) to compile the SystemC source code.

Quitting C Debug

To end a debugging session, you can do one of the following.

- From the GUI:
Select **Tools > C Debug > Quit C Debug**.
- From the command line, enter the following in the Transcript window:

```
cgdb quit
```

Note



Recommended usage is that you invoke C Debug once for a given simulation and then quit both C Debug and ModelSim. Starting and stopping C Debug more than once during a single simulation session may cause problems for gdb.

Finding Function Entry Points with Auto Find bp

ModelSim can automatically locate and set breakpoints at all currently known function entry points (that is, PLI/VPI/DPI system tasks and functions and callbacks; and FLI subprograms and callbacks and processes created with **mti_CreateProcess**). Select **Tools > C Debug > Auto find bp** to invoke this feature.

The **Auto find bp** command provides a "snapshot" of your design when you invoke the command. If additional callbacks get registered later in the simulation, ModelSim will not identify these new function entry points *unless* you re-execute the **Auto find bp** command. If you want functions to be identified regardless of when they are registered, use [Identifying All Registered Function Calls](#) instead.

The **Auto find bp** command sets breakpoints in an enabled state and does not toggle that state to account for **step -over** or **run -continue** commands. This may result in unexpected behavior. For example, say you have invoked the **Auto find bp** command and you are currently stopped on a line of code that calls a C function. If you execute a **step -over** or **run -continue** command, ModelSim will stop on the breakpoint set in the called C file.

Identifying All Registered Function Calls

Auto step mode automatically identifies and sets breakpoints at registered function calls (that is, PLI/VPI system tasks and functions and callbacks; and FLI subprograms and callbacks and processes created with **mti_CreateProcess**). Auto step mode is helpful when you are not entirely familiar with a design and its associated C routines. As you step through the design, ModelSim steps into and displays the associated C file when you hit a C function call in your HDL code. If you execute a **step -over** or **run -continue** command, ModelSim does not step into the C code.

When you first enable Auto step mode, ModelSim scans your design and sets enabled breakpoints at all currently known function entry points. As you step through the simulation, Auto step continues looking for newly registered callbacks and sets enabled breakpoints at any new entry points it identifies. Once you execute a **step -over** or **run -continue** command, Auto step disables the breakpoints it set, and the simulation continues running. The next time you execute a step command, the automatic breakpoints are re-enabled and Auto step sets breakpoints on any new entry points it identifies.

Note that Auto step does not disable user-set breakpoints.

Enabling Auto Step Mode

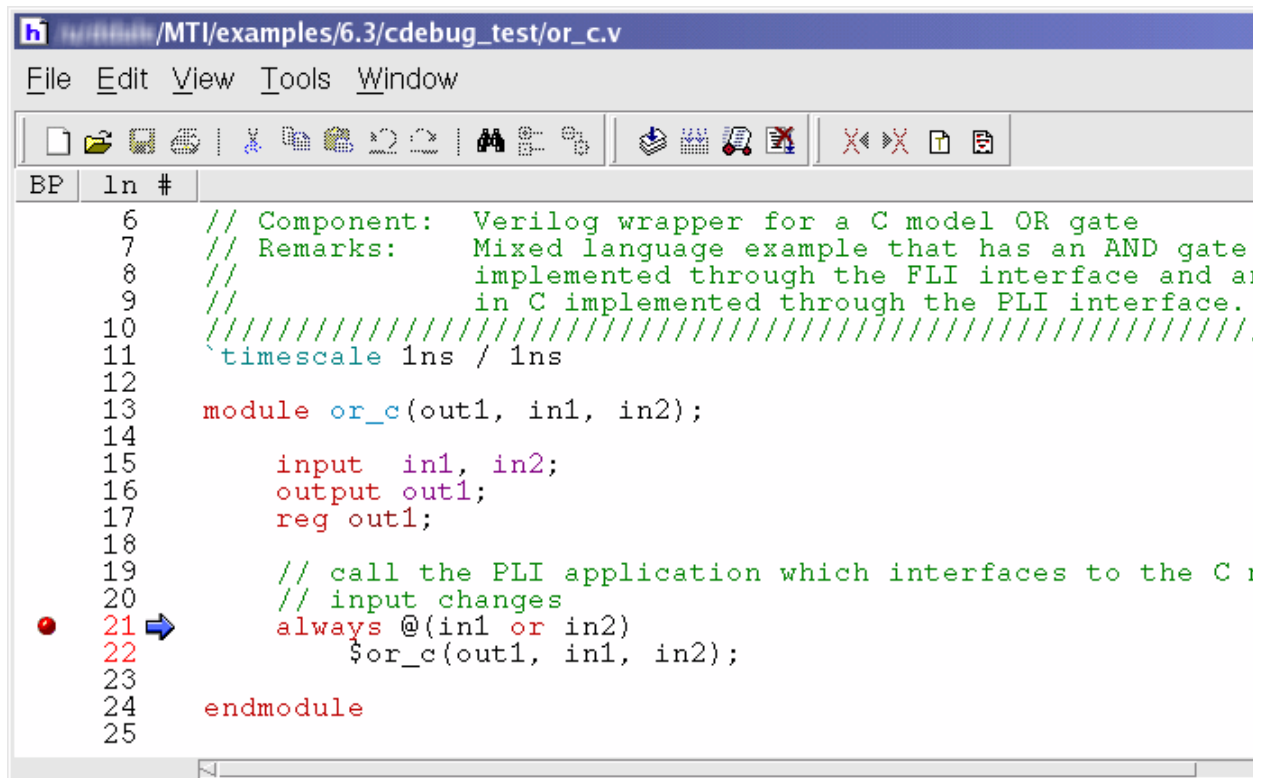
To enable Auto step mode, follow these steps:

1. Configure C Debug as described in [Setting Up C Debug](#).
2. Select **Tools > C Debug > Enable auto step**.
3. Load and run your design.

Example

The graphic below shows a simulation that has stopped at a user-set breakpoint on a PLI system task.

Figure 19-4. Simulation Stopped at Breakpoint on PLI Task



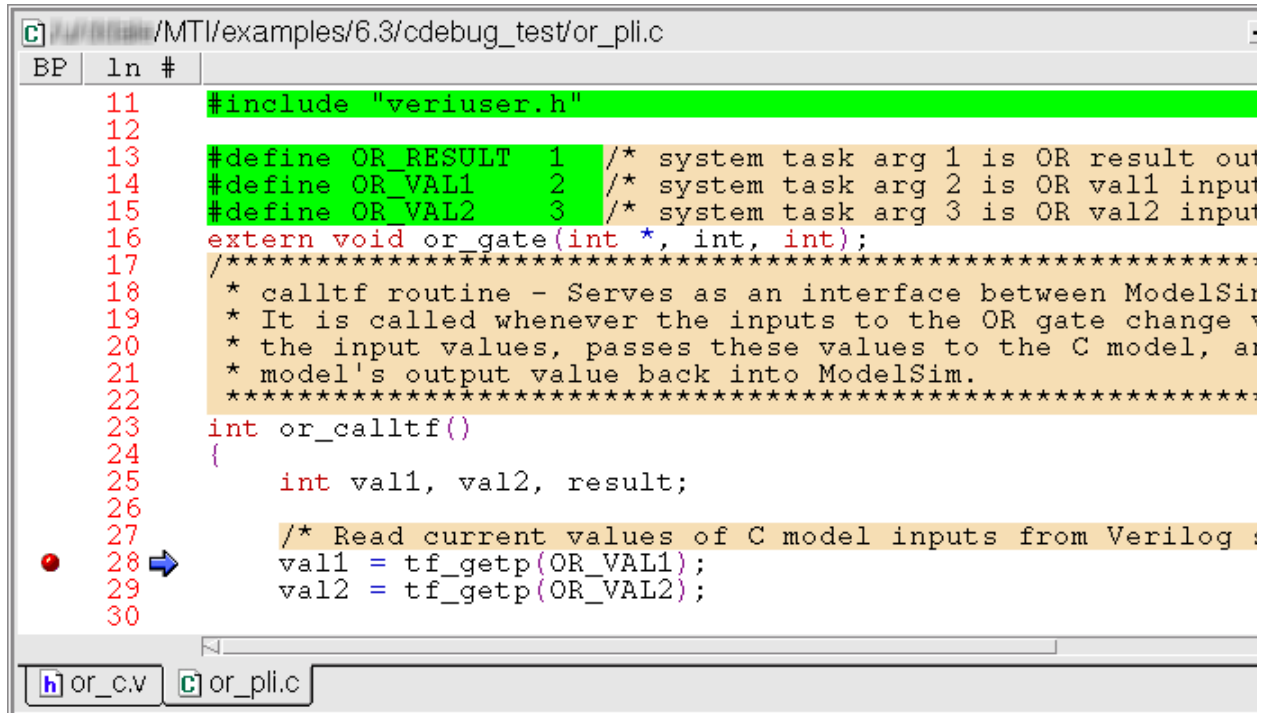
```

BP | ln # |
---|---|
6  | // Component: Verilog wrapper for a C model OR gate
7  | // Remarks:   Mixed language example that has an AND gate
8  | //           implemented through the FLI interface and a
9  | //           in C implemented through the PLI interface.
10 | ///////////////////////////////////////////////////////////////////
11 | `timescale 1ns / 1ns
12 |
13 | module or_c(out1, in1, in2);
14 |
15 |     input  in1, in2;
16 |     output out1;
17 |     reg out1;
18 |
19 |     // call the PLI application which interfaces to the C
20 |     // input changes
21 |     always @(in1 or in2)
22 |         $or_c(out1, in1, in2);
23 |
24 | endmodule
25 |

```

Because Auto step mode is enabled, ModelSim automatically sets a breakpoint in the underlying *xor_gate.c* file. If you click the step button at this point, ModelSim will step into that file.

Figure 19-5. Stepping into Next File



Auto Find bp Versus Auto Step Mode

As noted in [Finding Function Entry Points with Auto Find bp](#), the **Auto find bp** command also locates and sets breakpoints at function entry points. Note the following differences between Auto find bp and Auto step mode:

- Auto find bp provides a "snapshot" of currently known function entry points at the time you invoke the command. Auto step mode continues to locate and set automatic breakpoints in newly registered function calls as the simulation continues. In other words, Auto find bp is static while Auto step mode is dynamic.
- Auto find bp sets automatic breakpoints in an enabled state and does not change that state to account for step-over or run-continue commands. Auto step mode enables and disables automatic breakpoints depending on how you step through the design. In cases where you invoke both features, Auto step mode takes precedence over Auto find bp. In other words, even if Auto find bp has set enabled breakpoints, if you then invoke Auto step mode, it will toggle those breakpoints to account for step-over and run-continue commands.

Debugging Functions During Elaboration

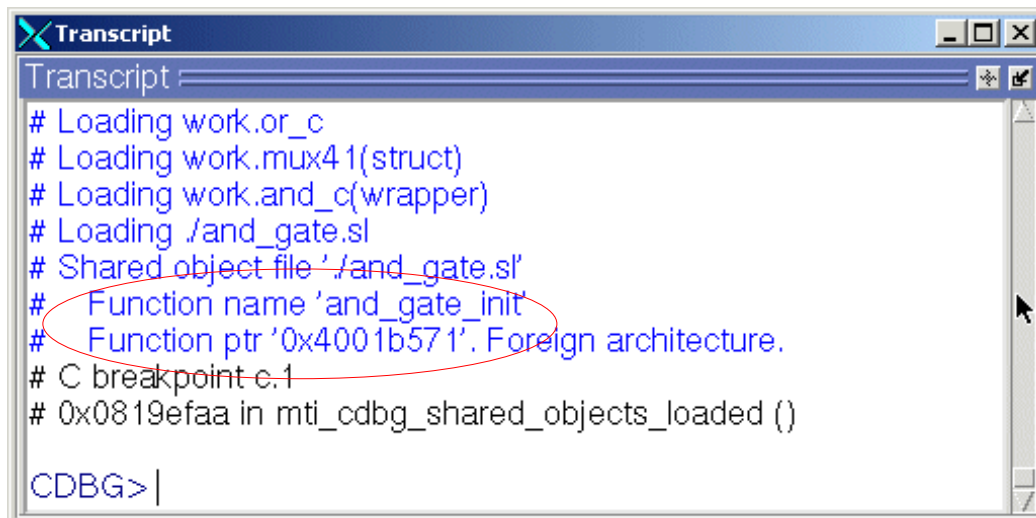
Initialization mode allows you to examine and debug functions that are called during elaboration (that is, while your design is in the process of loading). When you select this mode, ModelSim sets special breakpoints for foreign architectures and PLI/VPI modules that allow you to set breakpoints in the initialization functions. When the design finishes loading, the special breakpoints are automatically deleted, and any breakpoints that you set are disabled (unless you specify **Keep user init bps** in the C debug setup dialog).

To run C Debug in initialization mode, follow these steps:

1. Start C Debug by selecting **Tools > C Debug > Start C Debug** *before* loading your design.
2. Select **Tools > C Debug > Init mode**.
3. Load your design.

As the design loads, ModelSim prints to the Transcript the names and/or hex addresses of called functions. For example the Transcript below shows a function pointer to a foreign architecture:

Figure 19-6. Function Pointer to Foreign Architecture



To set a breakpoint on that function, you would type:

```
bp -c *0x4001b571
```

or

```
bp -c and_gate_init
```

ModelSim in turn reports that it has set a breakpoint at line 37 of the *and_gate.c* file. As you continue through the design load using **run -continue**, ModelSim hits that breakpoint and displays the file and associated line in a Source window.

Figure 19-7. Highlighted Line in Associated File

```
and_gate.c
ln #
35     mtiInterfaceListT *generics;
36     mtiInterfaceListT *ports;
37     {
38         inst_rec *ip;
39         mtiSignalIdT outp;
40         mtiProcessIdT proc;
41         /* extern free(); */
42
43     ip = (inst_rec *)mti_Malloc(sizeof(inst_rec));
44     mti_AddRestartCB((mtiVoidFuncPtrT) mti_Free, ip);
45     ip->in1 = mti_FindPort(ports, "in1");
46     ip->in2 = mti_FindPort(ports, "in2");
47     outp = mti_FindPort(ports, "out1");
48     ip->out1 = mti_CreateDriver(outp);
49
50     proc = mti_CreateProcess("p1", (mtiVoidFuncPtrT) do_and, i
51     mti_Sensitize(proc, ip->in1, MTI_EVENT);
```

FLI Functions in Initialization Mode

There are two kinds of FLI functions that you may encounter in initialization mode. The first is a foreign architecture which was shown above. The second is a foreign function. ModelSim produces a Transcript message like the following when it encounters a foreign function during initialization:

```
# Shared object file './all.sl'
#   Function name 'in_params'
#   Function ptr '0x4001a950'. Foreign function.
# C breakpoint c.1
# 0x0814fc96 in mti_cdbg_shared_objects_loaded ()
```

You can set a breakpoint on the function using either the function name (for example, `bp -c in_params`) or the function pointer (for example, `bp -c *0x4001a950`). Note, however, that foreign functions aren't called during initialization. You would hit the breakpoint only during runtime and then only if you enabled the breakpoint after initialization was complete or had specified **Keep user init bps** in the C debug setup dialog.

PLI Functions in Initialization Mode

There are two methods for registering callback functions in the PLI: 1) using a `veriusertfs` array to define all `usertf` entries; and 2) adding an `init_usertfs` function to explicitly register each `usertfs` entry (see [Registering PLI Applications](#) for more details). The messages ModelSim produces in initialization mode vary depending on which method you use.

ModelSim produces a Transcript message like the following when it encounters a `veriusertfs` array during initialization:

```
# vsim -pli ./veriuser.sl mux_tb
# Loading ./veriuser.sl
# Shared object file './veriuser.sl'
#   veriusertfs array - registering calltf
#   Function ptr '0x40019518'. $or_c.
# C breakpoint c.1
# 0x0814fc96 in mti_cdbg_shared_objects_loaded ()
cont
# Shared object file './veriuser.sl'
#   veriusertfs array - registering checktf
#   Function ptr '0x40019570'. $or_c.
# C breakpoint c.1
# 0x0814fc96 in mti_cdbg_shared_objects_loaded ()
cont
# Shared object file './veriuser.sl'
#   veriusertfs array - registering sizetf
#   Function ptr '0x0'. $or_c.
# C breakpoint c.1
# 0x0814fc96 in mti_cdbg_shared_objects_loaded ()
cont
# Shared object file './veriuser.sl'
#   veriusertfs array - registering misctf
#   Function ptr '0x0'. $or_c.
# C breakpoint c.1
# 0x0814fc96 in mti_cdbg_shared_objects_loaded ()
```

You can set breakpoints on non-null callbacks using the function pointer (for example, `bp -c *0x40019570`). You cannot set breakpoints on null functions. The `sizetf` and `misctf` entries in the example above are null (the function pointer is `'0x0'`).

ModelSim reports the entries in multiples of four with at least one entry each for `calltf`, `checktf`, `sizetf`, and `misctf`. `checktf` and `sizetf` functions are called during initialization but `calltf` and `misctf` are not called until runtime.

The second registration method uses `init_usertfs` functions for each `usertfs` entry. ModelSim produces a Transcript message like the following when it encounters an `init_usertfs` function during initialization:

```
# Shared object file './veriuser.sl'
#   Function name 'init_usertfs'
#   Function ptr '0x40019bec'. Before first call of init_usertfs.
# C breakpoint c.1
# 0x0814fc96 in mti_cdbg_shared_objects_loaded ()
```

You can set a breakpoint on the function using either the function name (for example, `bp -c init_usertfs`) or the function pointer (for example, `bp -c *0x40019bec`). ModelSim will hit this breakpoint as you continue through initialization.

VPI Functions in Initialization Mode

VPI functions are registered via routines placed in a table named `vlog_startup_routines` (see [Registering PLI Applications](#) for more details). ModelSim produces a Transcript message like the following when it encounters a `vlog_startup_routines` table during initialization:

```
# Shared object file './vpi_test.sl'  
#   vlog_startup_routines array  
#   Function ptr '0x4001d310'. Before first call using function pointer.  
# C breakpoint c.1  
# 0x0814fc96 in mti_cdbg_shared_objects_loaded ()
```

You can set a breakpoint on the function using the function pointer (for example, `bp -c *0x4001d310`). ModelSim will hit this breakpoint as you continue through initialization.

Completing Design Load

If you are through looking at the initialization code you can select **Tools > C Debug > Complete load** at any time, and ModelSim will continue loading the design without stopping. The one exception to this is if you have set a breakpoint in a `LoadDone` callback and also specified **Keep user init bps** in the C Debug setup dialog.

Debugging Functions when Quitting Simulation

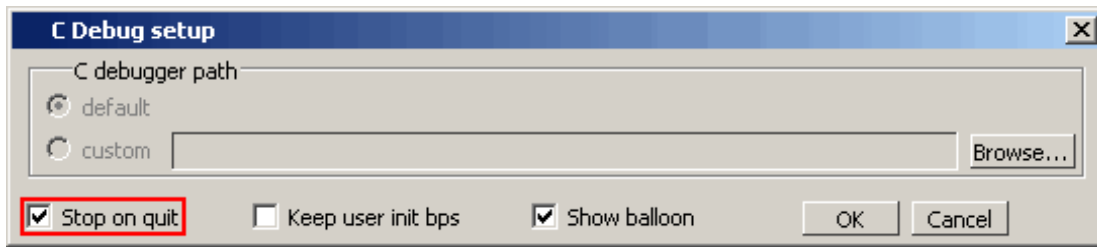
Stop on quit mode allows you to debug functions that are called when the simulator exits. Such functions include those referenced by one of the following:

- **mti_AddQuitCB** function in FLI code
- **miscf** function called by a `quit` or `$finish` in PLI code
- **cbEndofSimulation** function called by a `quit` or `$finish` in VPI code.

To enable **Stop on quit** mode, follow these steps:

1. Start C Debug by choosing **Tools > C Debug > Start C Debug** from the main menu.
2. Choose **Select Tools > C Debug > C Debug Setup** from the main menu.
3. Select **Stop on quit** in the C Debug setup dialog box ([Figure 19-8](#)).
4. Click OK.

Figure 19-8. Stop on quit Button in Dialog



With this mode enabled, if you have set a breakpoint in a quit callback function, C Debug will stop at the breakpoint after you issue the quit command in ModelSim. This allows you to step and examine the code in the quit callback function.

Invoke **run -continue** when you are done looking at the C code. When simulation completes, ModelSim automatically quits C-debugger and the GUI (whether or not a C breakpoint was hit and you return to the VSIM> prompt).

C Debug Command Reference

The table below provides a brief description of the commands that can be invoked when C Debug is running. Follow the links to the Reference Manual for complete command syntax.

Table 19-3. Command Reference for C Debug

Command	Description	Corresponding menu command
bd	deletes a previously set C breakpoint	right click breakpoint in Source window and select Remove Breakpoint
bp -c	sets a C breakpoint	click in the line number column next to the desired line number in the Source window
change	changes the value of a C variable	none
describe	prints the type information of a C variable	select the C variable name in the Source window and select Tools > Describe or right click and select Describe.
disablebp	disables a previously set C breakpoint	right click breakpoint in Source window and select Disable Breakpoint
enablebp	enables a previously disabled C breakpoint	right click breakpoint in Source window and select Enable Breakpoint

Table 19-3. Command Reference for C Debug

Command	Description	Corresponding menu command
examine	prints the value of a C variable	select the C variable name in the Source window and select Tools > Examine or right click and select Examine
gdb dir	sets the source directory search path for the C debugger	none
pop	moves the specified number of call frames up the C callstack	none
push	moves the specified number of call frames down the C callstack	none
run -continue	continues running the simulation after stopping	click the run -continue button on the Main or Source window toolbar
run -finish	continues running the simulation until control returns to the calling function	Tools > C Debug > Run > Finish
show	displays the names and types of the local variables and arguments of the current C function	Tools > C Debug > Show
step	single step in the C debugger to the next executable line of C code; step goes into function calls, whereas step -over does not	click the step or step -over button on the Main or Source window toolbar
tb	displays a stack trace of the C call stack	Tools > C Debug > Traceback

Chapter 20

Profiling Performance and Memory Use

The ModelSim profiler combines a statistical sampling profiler with a memory allocation profiler to provide instance specific execution and memory allocation data. It allows you to quickly determine how your memory is being allocated and easily identify areas in your simulation where performance can be improved. The profiler can be used at all levels of design simulation – Functional, RTL, and Gate Level – and has the potential to save hours of regression test time. In addition, ASIC and FPGA design flows benefit from the use of this tool.

Note



The functionality described in this chapter requires a profiler license feature in your ModelSim license file. Please contact your Mentor Graphics sales representative if you currently do not have such a feature.

Introducing Performance and Memory Profiling

The profiler provides an interactive graphical representation of both memory and CPU usage on a per instance basis. It shows you what part of your design is consuming resources (CPU cycles or memory), allowing you to more quickly find problem areas in your code.

The profiler enables those familiar with the design and validation environment to find first-level improvements in a matter of minutes. For example, the statistical sampling profiler might show the following:

- non-accelerated VITAL library cells that are impacting simulation run time
- objects in the sensitivity list that are not required, resulting in a process that consumes more simulation time than necessary
- a test bench process that is active even though it is not needed
- an inefficient C module
- random number processes that are consuming simulation resources in a test bench running in non-random mode

With this information, you can make changes to the VHDL or Verilog source code that will speed up the simulation.

The memory allocation profiler provides insight into how much memory different parts of the design are consuming. The two major areas of concern are typically: 1) memory usage during elaboration, and 2) during simulation. If memory is exhausted during elaboration, for example,

memory profiling may provide insights into what part(s) of the design are memory intensive. Or, if your HDL or PLI/FLI code is allocating memory and not freeing it when appropriate, the memory profiler will indicate excessive memory use in particular portions of the design.

Statistical Sampling Profiler

The profiler's statistical sampling profiler samples the current simulation at a user-determined rate (every <n> milliseconds of real or "wall-clock" time, not simulation time) and records what is executing at each sample point. The advantage of statistical sampling is that an entire simulation need not be run to get good information about what parts of your design are using the most simulation time. A few thousand samples, for example, can be accumulated before pausing the simulation to see where simulation time is being spent.

The statistical profiler reports only on the samples that it can attribute to user code. For example, if you use the `-nodebug` argument to `vcom` or `vlog`, it cannot report sample results.

Memory Allocation Profiler

The profiler's memory allocation profiler records every memory allocation and deallocation that takes place in the context of elaborating and simulating the design. It makes a record of the design element that is active at the time of allocation so memory resources can be attributed to appropriate parts of the design. This provides insights into memory usage that can help you re-code designs to, for example, minimize memory use, correct memory leaks, and change optimization parameters used at compile time.

Getting Started with the Profiler

Memory allocation profiling and statistical sampling are enabled separately.

Note



It is suggested that you not run the memory allocation and statistical sampling profilers at the same time. The analysis of the memory allocation can skew the results of the statistical sampling profiler.

Enabling the Memory Allocation Profiler

To record memory usage during elaboration and simulation, enable memory allocation profiling when the design is loaded with the `-memprof` argument to the `vsim` command.

```
vsim -memprof <design_unit>
```

Note that profile-data collection for the call tree is off by default. See [Calltree Window](#) for additional information on collecting call-stack data.

You can use the graphic user interface as follows to perform the same task.

1. Select **Simulate > Start Simulation** or the Simulate icon, to open the Start Simulation dialog box.
2. Select the Others tab.
3. Click the **Enable memory profiling** checkbox to select it.
4. Click **OK** to load the design with memory allocation profiling enabled.

If memory allocation during elaboration is not a concern, the memory allocation profiler can be enabled at any time after the design is loaded by doing any one of the following:

- select **Tools > Profile > Memory**
- use the -m argument with the [profile on](#) command

```
profile on -m
```

- click the Memory Profiling icon 

Handling Large Files

To allow memory allocation profiling of large designs, where the design itself plus the data required to keep track of memory allocation exceeds the memory available on the machine, the memory profiler allows you to route raw memory allocation data to an external file. This allows you to save the memory profile with minimal memory impact on the simulator, regardless of the size of your design.

The external data file is created during elaboration by using either the `-memprof+file=<filename>` or the `-memprof+fileonly=<filename>` argument with the [vsim](#) command.

The `-memprof+file=<filename>` option will collect memory profile data during both elaboration and simulation and save it to the named external file *and* makes the data available for viewing and reporting during the current simulation.

The `-memprof+fileonly=<filename>` option will collect memory profile data during both elaboration and simulation and save it to *only* the named external file. No data is saved for viewing and reporting during the current simulation, which reduces the overall amount of memory required by memory allocation profiling.

Alternatively, you can save memory profile data from the simulation only by using either the `-m -file <filename>` or the `-m -fileonly <filename>` argument with the [profile on](#) command.


The `-m -file <filename>` option saves memory profile data from simulation to the designated external file *and* makes the data available for viewing and reporting during the current simulation.

The `-m -fileonly <filename>` option saves memory profile data from simulation to *only* the designated external file. No data is saved for viewing and reporting during the current simulation, which reduces the overall amount of memory required by memory allocation profiling.

After elaboration and/or simulation is complete, a separate session can be invoked and the profile data can be read in with the `profile reload` command for analysis. It should be noted, however, that this command will clear all performance and memory profiling data collected to that point (implicit `profile clear`). Any currently loaded design will be unloaded (implicit `quit -sim`), and run-time profiling will be turned off (implicit `profile off -m -p`). If a new design is loaded after you have read the raw profile data, then all internal profile data is cleared (implicit `profile clear`), but run-time profiling is not turned back on.

Enabling the Statistical Sampling Profiler

To enable the profiler's statistical sampling profiler prior to a simulation run, do any one of the following:

- select **Tools > Profile > Performance**
- use the `profile on` command
- click the Performance Profiling icon 

Collecting Memory Allocation and Performance Data

Both memory allocation profiling and statistical sampling occur during the execution of a ModelSim `run` command. With profiling enabled, all subsequent `run` commands will collect memory allocation data and performance statistics. Profiling results are cumulative – each `run` command performed with profiling enabled will add new information to the data already gathered. To clear this data, select **Tools > Profile > Clear Profile Data** or use the `profile clear` command.

With the profiler enabled and a `run` command initiated, the simulator will provide a "Profiling" message in the transcript to indicate that profiling has started.

If the statistical sampling profiler and the memory allocation profiler are on, the status bar will display the number of Profile Samples collected and the amount of memory allocated, as shown below. Each profile sample will become a data point in the simulation's performance profile.

Figure 20-1. Status Bar: Profile Samples

Now: 100 ps Delta: 0 Profile Samples: 18 Memory: 65.4KB

Turning Profiling Off

You can turn off the statistical sampling profiler or the memory allocation profiler by doing any one of the following:

- deselect the **Performance** and/or **Memory** options in the **Tools > Profile menu**
- deselect the Performance Profiling and Memory Profiling icons in the toolbar
- use the [profile off](#) command with the -p or -m arguments.

Any ModelSim [run](#) commands that follow will not be profiled.

Running the Profiler on Windows with PLI/VPI Code

If you need to run the profiler under Windows on a design that contains FLI/PLI/VPI code, add these two switches to the compiling/linking command:

```
/DEBUG /DEBUGTYPE:COFF
```

These switches add symbols to the *.dll* file that the profiler can use in its report.

Interpreting Profiler Data

The utility of the data supplied by the profiler depends in large part on how your code is written. In cases where a single model or instance consumes a high percentage of simulation time or requires a high percentage of memory, the statistical sampling profiler or the memory allocation profiler quickly identifies that object, allowing you to implement a change that runs faster or requires less memory.

More commonly, simulation time or memory allocation will be spread among a handful of modules or entities – for example, 30% of simulation time split between models X, Y, and Z; or 20% of memory allocation going to models A, B, C and D. In such situations, careful examination and improvement of each model may result in overall speed improvement or more efficient memory allocation.

There are times, however, when the statistical sampling and memory allocation profilers tell you nothing more than that simulation time or memory allocation is fairly equally distributed throughout your design. In such situations, the profiler provides little helpful information and improvement must come from a higher level examination of how the design can be changed or optimized.

Viewing Profiler Results

The profiler provides four views of the collected data – *Ranked*, *Design Units*, *Call Tree* and *Structural*. All four views are enabled by selecting **View > Profiling**.

Note



The Ranked, Design Units, Calltree, and Structural windows, by default, only show performance and memory profile data equal to or greater than 1 percent. You can change this with the Profile Cutoff tool in the profile toolbar group.

Ranked Window

The Ranked window displays the results of the statistical performance profiler and the memory allocation profiler for each function or instance. By default, ranked profiler results are sorted by values in the *In%* column, which shows the percentage of the total samples collected for each function or instance. You can sort ranked results by any other column by simply clicking the column heading. Click the down arrow to the left of the Name column to open a Configure Columns dialog, which allows you to select which columns are to be hidden or displayed.

The use of colors in the display provides an immediate visual indication of where your design is spending most of its simulation time. By default, red text indicates functions or instances that are consuming 5% or more of simulation time.

Figure 20-2. Ranked Window

Name	Under(raw)	In(raw)	Under(%)	In(%)
test_sm.v:105	44	17	45.4%	17.5%
Tcl_OpenTcpServer	17	17	17.5%	17.5%
Tcl_WaitForEvent	5	5	5.2%	5.2%
sm.v:73	8	3	8.2%	3.1%
TclpHasSockets	4	3	4.1%	3.1%
test_sm.v:136	3	3	3.1%	3.1%
Tcl_GetTime	2	2	2.1%	2.1%
TclpLocaltime	2	2	2.1%	2.1%
test_sm.v	2	2	2.1%	2.1%
test_sm.v:103	2	2	2.1%	2.1%
test_sm.v:84	2	2	2.1%	2.1%
test_sm.v:92	2	2	2.1%	2.1%
TclWinOpenConsoleChannel	1	1	1.0%	1.0%

The Ranked tab does not provide hierarchical, function-call information.

Design Units Window

The Design Units window displays the profiler results, aggregated for the different design units. This window provides information similar to the Structural window, but organized by design unit, rather than hierarchically.

Figure 20-3. Design Units Window

Name	Count	Under(raw)	In(raw)	Under(%)	In(%)	%Parent
- sm_seq	1	3	3	3.1%	3.1%	...
sm_seq.v:55		1	1	1.0%	1.0%	33%
test_sm.v:136		1	1	1.0%	1.0%	33%
sm_seq.v:61		1	1	1.0%	1.0%	33%
- sm	1	10	10	10.3%	10.3%	...
sm.v:73		8	3	8.2%	3.1%	80%
- Tcd_Flush		4	0	4.1%	0.0%	50%
+ Tcd_Close		4	0	4.1%	0.0%	100%
+ Tcd_DoOneEvent		1	0	1.0%	0.0%	13%
sm.v:51		1	1	1.0%	1.0%	10%
sm.v:40		1	1	1.0%	1.0%	10%
+ beh_sram	1	1	1	1.0%	1.0%	...
+ test_sm	1	54	54	55.7%	55.7%	...

Calltree Window

Data collection for the call tree is off by default, due to the fact that it will increase the simulation time and resource usage. Collection can be turned on from the VSIM command prompt with **profile option collect_calltrees on** and off with **profile option collect_calltrees off**. Call stack data collection can also be turned on with the `-memprof+call` argument to the `vsim` command.

By default, profiler results in the Call Tree window are sorted according to the *Under(%)* column, which shows the percentage of the total samples collected for each function or instance and all supporting routines or instances. Sort results by any other column by clicking the column heading. As in the Ranked window, red object names indicate functions or instances that, by default, are consuming 5% or more of simulation time.

The Call Tree window differs from the Ranked window in two important respects.

- Entries in the Name column of the Calltree window are indented in hierarchical order to indicate which functions or routines call which others.
- A *%Parent* column in the Calltree window allows you to see what percentage of a parent routine's simulation time is used in which subroutines.

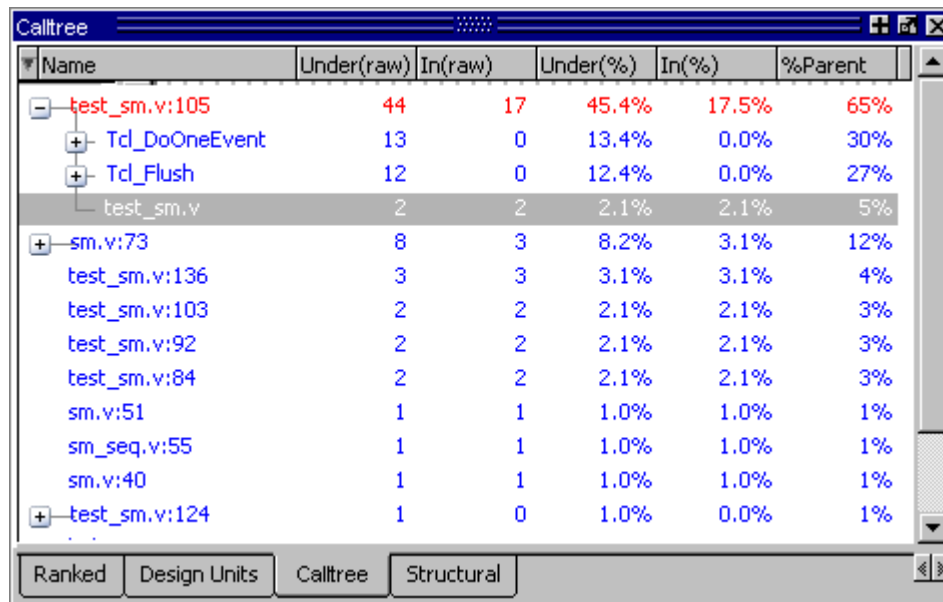
The Calltree window presents data in a call-stack format that provides more context than does the Ranked window about where simulation time is spent. For example, your models may contain several instances of a utility function that computes the maximum of 3-delay values. A Ranked window might reveal that the simulation spent 60% of its time in this utility function, but would not tell you which routine or routines were making the most use of it. The Calltree window will reveal which line is calling the function most frequently. Using this information,

you might decide that instead of calling the function every time to compute the maximum of the 3-delays, this spot in your VHDL code can be used to compute it just once. You can then store the maximum delay value in a local variable.

The two *%Parent* columns in the Calltree window show the percent of simulation time or allocated memory a given function or instance is using of its parent's total simulation time or available memory. From these columns, you can calculate the percentage of total simulation time or memory taken up by any function. For example, if a particular parent entry used 10% of the total simulation time or allocated memory, and it called a routine that used 80% of its simulation time or memory, then the percentage of total simulation time spent in, or memory allocated to, that routine would be 80% of 10%, or 8%.

In addition to these differences, the Ranked window displays any particular function only once, regardless of where it was used. In the Calltree window, the function can appear multiple times – each time in the context of where it was used.

Figure 20-4. Calltree Window



Name	Under(raw)	In(raw)	Under(%)	In(%)	%Parent
- test_sm.v:105	44	17	45.4%	17.5%	65%
+ Tcd_DoOneEvent	13	0	13.4%	0.0%	30%
+ Tcd_Flush	12	0	12.4%	0.0%	27%
- test_sm.v	2	2	2.1%	2.1%	5%
+ sm.v:73	8	3	8.2%	3.1%	12%
test_sm.v:136	3	3	3.1%	3.1%	4%
test_sm.v:103	2	2	2.1%	2.1%	3%
test_sm.v:92	2	2	2.1%	2.1%	3%
test_sm.v:84	2	2	2.1%	2.1%	3%
sm.v:51	1	1	1.0%	1.0%	1%
sm_seq.v:55	1	1	1.0%	1.0%	1%
sm.v:40	1	1	1.0%	1.0%	1%
+ test_sm.v:124	1	0	1.0%	0.0%	1%

Structural Window

The Structural window displays instance-specific performance and memory profile information in a hierarchical structure format identical to the Structure window. It contains the same information found in the Calltree window but adds an additional dimension with which to categorize performance samples and memory allocation. It shows how call stacks are associated with different instances in the design.

Figure 20-5. Structural Window

Name	Under(raw)	In(raw)	Under(%)	In(%)	%Parent
test_sm	68	54	70.1%	55.7%	...
sm_seq0	13	3	13.4%	3.1%	19.1%
sm_0	10	10	10.3%	10.3%	76.9%
sram_0	1	1	1.0%	1.0%	1.5%

In the Calltree and Structural windows, you can expand and collapse the various levels to hide data that is not useful to the current analysis and/or is cluttering the display. Click on the '+' box next to an object name to expand the hierarchy and show supporting functions and/or instances beneath it. Click the '-' box to collapse all levels beneath the entry.

Note that profile-data collection for the call tree is off by default. See [Calltree Window](#) for additional information on collecting call-stack data.

You can also right click any function or instance in the Calltree and Structural windows to obtain popup menu selections for rooting the display to the currently selected item, to ascend the displayed root one level, or to expand and collapse the hierarchy.

Toggling Display of Call Stack Entries

By default call stack entries do not display in the Structural window. To display call stack entries, right-click in the pane and select **Show Calls**.

Viewing Profile Details

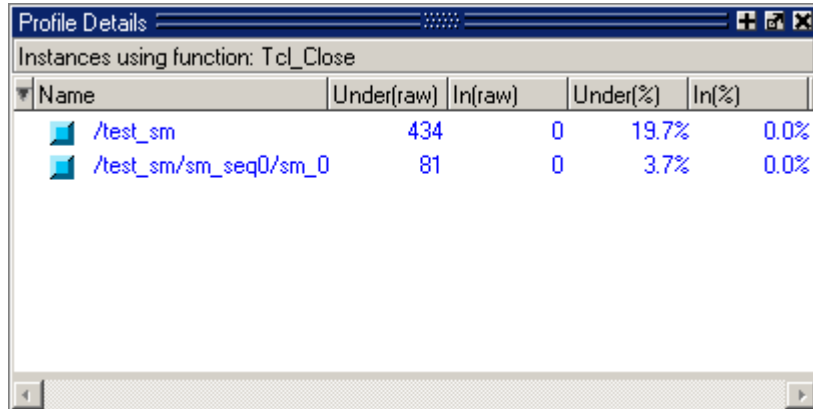
The Profiler increases visibility into simulation performance and memory usage with dynamic links to the Source window and the Profile Details window. The Profile Details window is enabled by selecting **View > Windows > Profile Details** or by entering the **view profiledetails** command at the VSIM prompt. You can also right-click any function or instance in the Ranked, Call Tree, or Structural tabs to open a popup menu that includes options for viewing profile details. The following options are available:

- View Source — opens the Source window to the location of the selected function.

- View Instantiation — opens the Source window to the location of the instantiation.
- Function Usage — opens the Profile Details window and displays all instances using the selected function.

In the Profile Details window shown below, all the instances using function *Tcl_Close* are displayed. The statistical performance and memory allocation data shows how much simulation time and memory is used by *Tcl_Close* in each instance.

Figure 20-6. Profile Details Window: Function Usage

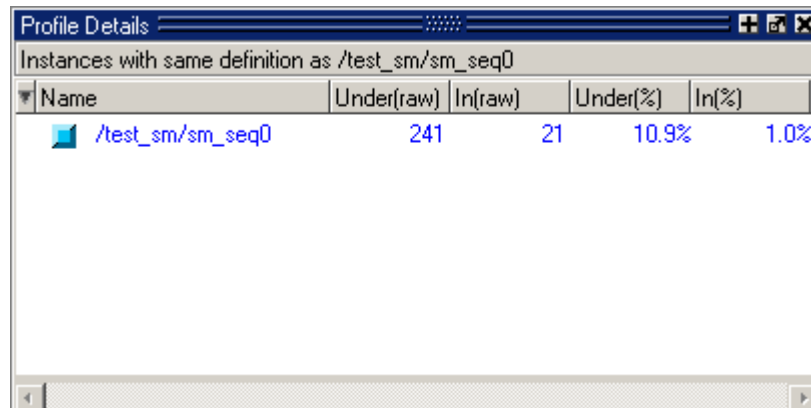


The screenshot shows a window titled "Profile Details" with a subtitle "Instances using function: Tcl_Close". It contains a table with the following data:

Name	Under(raw)	In(raw)	Under(%)	In(%)
/test_sm	434	0	19.7%	0.0%
/test_sm/sm_seq0/sm_0	81	0	3.7%	0.0%

- Instance Usage — opens the Profile Details window and displays all instances with the same definition as the selected instance.

Figure 20-7. Profile Details Window: Instance Usage



The screenshot shows a window titled "Profile Details" with a subtitle "Instances with same definition as /test_sm/sm_seq0". It contains a table with the following data:

Name	Under(raw)	In(raw)	Under(%)	In(%)
/test_sm/sm_seq0	241	21	10.9%	1.0%

- View Instantiation — opens the Source window to the point in the source code where the selected instance is instantiated.
- Callers and Callees — opens the Profile Details window and displays the callers and callees for the selected function. Items above the selected function are callers; items below are callees.

The selected function is distinguished with an arrow on the left and in 'hotForeground' color as shown below.

Figure 20-8. Profile Details Window: Callers and Callees

The screenshot shows a window titled 'Profile Details' with a subtitle 'Callers and callees of 'Tcl_OpenTcpServer''. It contains a table with the following data:

Name	Under(raw)	In(raw)	Under(%)	In(%)
Tcl_Flush	54	1	9.5%	0.2%
Tcl_Close	515	0	90.5%	0.0%
→ Tcl_OpenTcpServer	568	568	100.0%	100.0%

- Display in Call Tree — expands the Calltree window and displays all occurrences of the selected function and puts the selected function into a search buffer so you can easily cycle across all occurrences of that function.

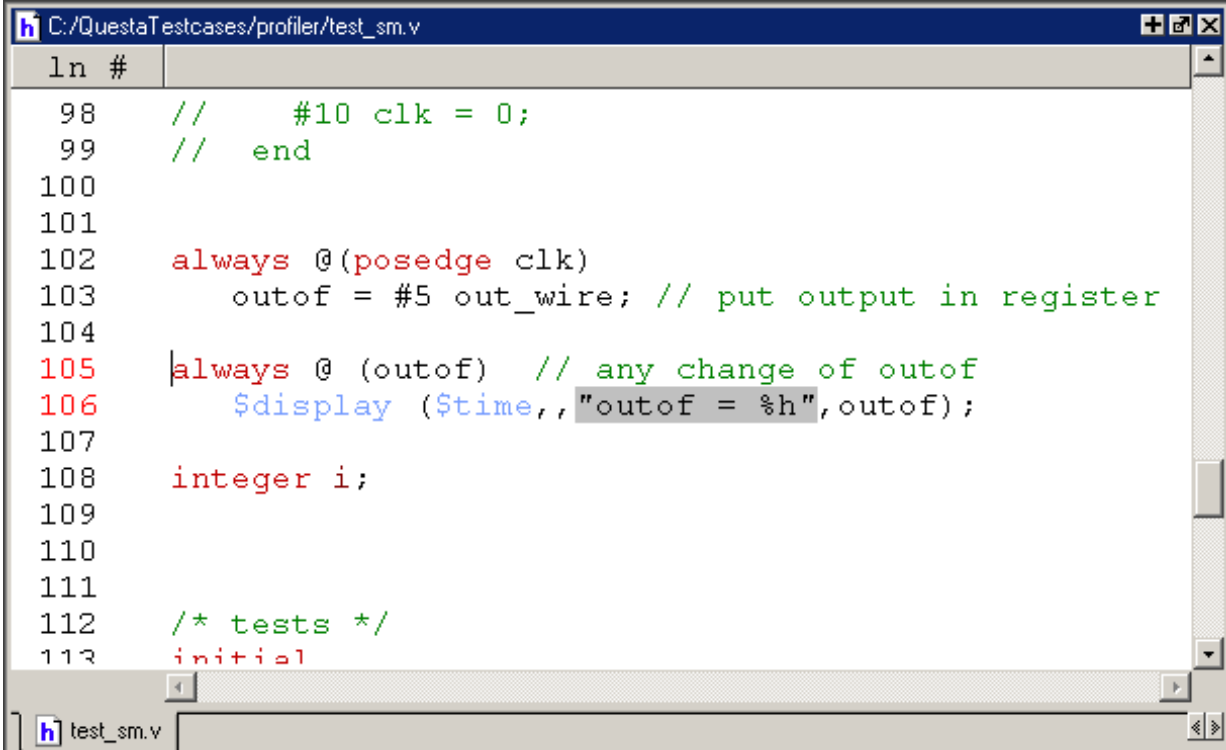
Note that profile-data collection for the call tree is off by default. See [Calltree Window](#) for additional information on collecting call-stack data.

- Display in Structural — expands the Structural window and displays all occurrences of the selected function and puts the selected function into a search buffer so you can easily cycle across all occurrences of that function.

Integration with Source Windows

The Ranked, Design Unit, Call Tree, and Structural windows are all dynamically linked to Source window. You can double-click any function or instance in these windows to bring up that object in a Source window with the selected line highlighted.

Figure 20-9. Accessing Source from Profile Views



```
C:/QuestaTestcases/profiler/test_sm.v
ln #
98 // #10 clk = 0;
99 // end
100
101
102 always @(posedge clk)
103     outof = #5 out_wire; // put output in register
104
105 always @ (outof) // any change of outof
106     $display ($time, "outof = %h", outof);
107
108 integer i;
109
110
111
112 /* tests */
113 initial
```

You can perform the same task by right-clicking any function or instance in any one of the four Profile views and selecting View Source from the popup menu that opens.

When you right-click an instance in the Structural window, the View Instantiation selection will become active in the popup menu. Selecting this option opens the instantiation in a Source window and highlights it.

The right-click popup menu also allows you to change the root instance of the display, ascend to the next highest root instance, or reset the root instance to the top level instance.

The selection of a context in the structure window will cause the root display to be set in the Structural window.

Analyzing C Code Performance

You can include C code in your design via SystemC, the Verilog PLI/VPI, or the ModelSim FLI. The profiler can be used to determine the impact of these C modules on simulator performance. Factors that can affect simulator performance when a design includes C code are as follows:

- PLI/FLI applications with large sensitivity lists
- Calling operating system functions from C code

- Calling the simulator's command interpreter from C code
- Inefficient C code

In addition, the Verilog PLI/VPI requires maintenance of the simulator's internal data structures as well as the PLI/VPI data structures for portability. (VHDL does not have this problem in ModelSim because the FLI gets information directly from the simulator.)

Reporting Profiler Results

You can create performance and memory profile reports using the Profile Report dialog or the [profile report](#) command.

For example, the command

```
profile report -calltree -file calltree.rpt -cutoff 2
```

will produce a Call Tree profile report in a text file called *calltree.rpt*, as shown here.

Figure 20-10. Profile Report Example

```

C:/QuestaTestcases/profiler/calltree.rpt
ln #
3 Platform: win32
4 Calltree profile generated Mon Oct 09 16:44:17 2006
5 Number of samples: 2206
6 Number of samples in user code: 1668 (76%)
7 Cutoff percentage: 2%
8
9 Name Under (raw) In (raw) U
10 ----
11 test_sm.v:105 1192 354
12 Tcl_Flush 428 0
13 Tcl_Close 428 0
14 Tcl_OpenTcpServer 428 428
15 Tcl_DoOneEvent 403 0
16 TclpHasSockets 150 149
17 Tcl_ServiceEvent 150 3
18 TclpHasSockets 145 87
19 Tcl_NotifyChannel 58 0
20 Tcl_Read 48 0
21 TclCopyChannel 48 0
22 Tcl_Flush 48 1
23 Tcl_OpenTcpServer 47 47
24 Tcl_DeleteTimerHandler 53 1
25 Tcl_GetTime 46 46
26 Tcl_WaitForEvent 49 47
27 sm.v:73 209 56
28 Tcl_Flush 79 0
  
```

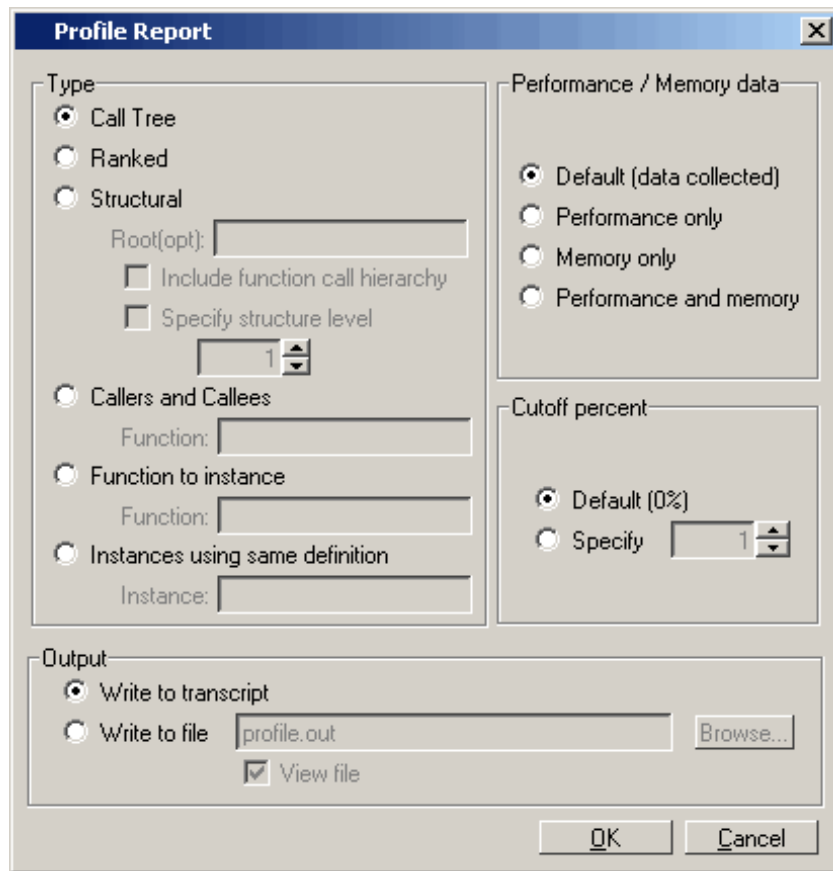
Select **Tools > Profile > Profile Report** to open the Profile Report dialog. The Profile Report dialog allows you to select the following performance profile type for reporting: Calltree, Ranked, Structural, Callers and Callees, Function to Instance, and Instances using the same definition. When the Structural profile type is selected, you can designate the root instance pathname, include function call hierarchy, and specify the structure level to be reported.

You can elect to report performance information only, memory information only, or a both. By default, all data collected will be reported.

Both performance and memory data will be displayed with a default cutoff of 0% - meaning, the report will contain any functions or instances that use simulation time or memory - unless you specify a different cutoff percentage.

You may elect to write the report directly to the Transcript window or to a file. If the "View file" box is selected, the profile report will be generated and immediately displayed in Notepad when the OK button is clicked.

Figure 20-11. Profile Report Dialog Box



Capacity Analysis

This section describes how to display memory usage (capacity) data that ModelSim collects for the following types of SystemVerilog constructs in the current design:

- Classes
- Queues, dynamic arrays, and associative arrays (QDAS)
- Assertions and cover directives
- Covergroups
- Solver (calls to randomize ())

ModelSim updates memory usage data at the end of every time step of the simulation and collects the number of objects allocated, the current memory allocated for the class object, the peak memory allocated, and the time at which peak memory occurred.

You can display this data in column format in the Capacity window of the user interface ([Obtaining a Graphical Interface \(GUI\) Display](#)) or as a text-based report in the Transcript window ([Writing a Text-Based Report](#)), which you can also write to a text file.

Enabling or Disabling Capacity Analysis

When you invoke ModelSim, you can use arguments to the `vsim` command to select one of the following levels of capacity analysis before loading your design:

- No analysis. Specify `-nocapacity`, along with any other `vsim` arguments you want to use.
- Coarse-grain analysis. Enabled by default (no additional `vsim` argument required).
- Fine-grain analysis: Specify `-capacity`, along with any other `vsim` arguments you want to use.

Note



Coarse-level and fine-level analyses are described in [Levels of Capacity Analysis](#).

In addition, you can use various other commands to enable collection of memory capacity data, along with viewing and reporting that data. [Table 20-1](#) summarizes the different ways to enable, view, and report memory capacity data.

Refer to the [ModelSim Reference Manual](#) for more information on using the commands listed in [Table 20-1](#).

Table 20-1. How to Enable and View Capacity Analysis

Action	Result	Description
<code>vsim <filename></code>	Collects coarse-grain analysis data.	No need to explicitly specify a coarse-grain analysis; enabled by default.
<code>vsim -capacity <filename></code>	Collects fine-grain analysis data.	Overrides default coarse-grain analysis.
<code>vsim -nocapacity <filename></code>	Disables capacity analysis.	No capacity data is collected.
<code>view capacity</code>	Displays the Capacity window containing capacity data.	Same as choosing View > Capacity from main menu.
<code>write report</code> { [-capacity [-l -s] [-assertions -classes -cvg -qdas -solver]] }	Reports data on memory capacity in either the Transcript window or to a file.	Use the -capacity switch along with other switches for object types to display memory data.
<code>profile on</code> { -solver -qdas -classes -cvg -assertions }	Enables fine-grain analysis.	Use this command after you have already loaded the design; you can specify multiple command switches.
<code>profile off</code> { -solver -qdas -classes -cvg -assertions }	Disables fine-grain analysis.	Use this command after you have already loaded the design; you can specify multiple command switches.
<code>coverage report -memory</code>	Reports coarse-grain data in either the Transcript window or to a file.	Use with -cvg and -details switches to obtain fine-grain data for covergroups.
<code>vcover report -memory</code>	Reports coarse-grain data from a previously saved code or functional coverage run in either the Transcript window or to a file.	Use with -cvg and -details switches to obtain fine-grain data for covergroups.
<code>vcover stats -memory</code>	Reports coarse-grain data from a previously saved code or functional coverage run in either the Transcript window or to a file.	No fine-grain analysis available.

Table 20-1. How to Enable and View Capacity Analysis (cont.)

Action	Result	Description
Choose View > Capacity from main menu	Displays the Capacity window containing capacity data.	Same as entering the view capacity command.

Levels of Capacity Analysis

ModelSim collects data as either a coarse-grain analysis or a fine-grain analysis of memory capacity. The main difference between the two levels is the amount of capacity data collected.

Coarse-grain Analysis

The coarse-grain analysis data is enabled by default when you run the vsim command.

The purpose of this analysis is to provide a simple display of the number of objects, the memory allocated for each class of design objects, the peak memory allocated, and the time at which peak memory occurred.

You can display the results of a coarse-grain analysis as either a graphical display in the user interface (see [Obtaining a Graphical Interface \(GUI\) Display](#)) or as a text report (see [Writing a Text-Based Report](#)).

Fine-grain Analysis

When you enable a fine-grain analysis, ModelSim collects more capacity data that you can use to dig deeper into the area where memory consumption is problematic. The details about each type of object are further quantified.

The display of the Capacity tab expands the coarse-grain categories and shows the count, current and peak memory allocation per class type, per assertions, per coverage groups/bins and per dynamic array objects.

Classes — displays aggregate information for each class type, including the current filename and line number where the allocation occurred.

QDAS — displays aggregate information for each type (queues, dynamic, associative), including the current filename and line number where the allocation has occurred.

Assertions — displays the assertion full name, number of threads allocated, current memory, peak memory and peak time.

Covergroups — displays the covergroup full name, number of coverpoints and crosses allocated, current memory, peak memory and peak time.

Solver — displays file name and line number of randmize() calls grouped by file name, line number, current memory, peak memory and peak time.

To enable fine-grain analysis, use either of the following commands:

```
vsim -capacity
profile on {-solver | -qdas | -classes | -cvg | -assertions}
```

Note that turning off fine-grain analysis reverts to coarse-grain analysis.

Obtaining a Graphical Interface (GUI) Display

To display a tabular listing of memory capacity data, choose View > Capacity from the main menu or enter the view command with “capacity” as the window type:

```
view capacity
```

This creates the Capacity window that displays memory data for the current design.

[Figure 20-12](#) shows an example of a coarse-level analysis that displays the following columns for each design object:

Count — quantity of design objects analyzed, depending on group type:

- classes: number currently allocated
- QDAS: number currently allocated
- cvg: number currently allocated
- assertions: number of threads allocated
- solver: number of times randmize() is called

Current Memory (bytes) — current amount of memory allocated for each group listed

Peak Memory (bytes) — peak amount of memory allocated for each group listed

Peak Time (ns) — the time at which peak memory was reached

Figure 20-12. Example of Memory Data in the Capacity Tab

Type/Object	Count	Current Memory	Peak Memory	Peak Time
Classes	159	16136	16136	4450
/std::semaphore	18	504	504	1650
/std::process	8	256	320	1658
/defs::Packet	97	12416	12416	4450
/test_router_sv_unit::scoreboard	1	168	168	1650
/test_router_sv_unit::monitor	8	1024	1024	1650
/test_router_sv_unit::driver	8	608	608	1650
/test_router_sv_unit::stimulus	8	416	416	1650
/test_router_sv_unit::test_env	1	144	144	1650
/std::mailbox::mailbox_1	8	480	480	1650
/std::mailbox::mailbox_1	2	120	120	1650
QDAS	310	3078	3091	4450
Dynamic arrays	300	2170	2183	4450
Queues	9	888	888	1657
Associative	1	20	20	1650
Assertions	0	0	0	0
Covergroups	3	1696	1696	1650
/test_router_sv_unit::scoreboard::cov1	3	1696	1696	1650
Solver	97	2072816	2081036	1651
./test_router.sv(311)	97	2072500	2080720	1651

Displaying Capacity Data in the Wave Window

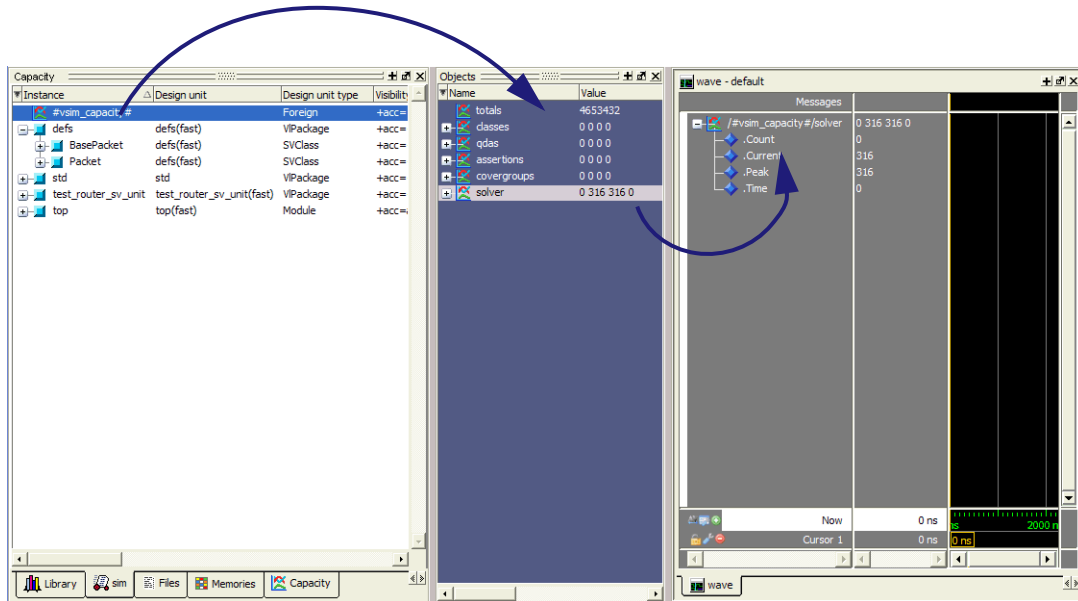
In addition, you can add the signals from the Capacity window to the Wave window like any other signal, either by drag-and-drop in the Main window or from the command line.

To drag-and-drop, do the following:

1. Click the Structure (sim) window tab.
2. Select the Instance labeled #vsim_capacity#. Selecting this instance displays a set of capacity types in the Objects window (see [Figure 20-13](#)).

3. Select one or more objects in the Objects window. Note that you can click on the [+] indicator to expand the listing of data below any type.
4. Drag and drop the selected objects to the Wave window.

Figure 20-13. Displaying Capacity Objects in the Wave Window



You can also display capacity objects in the Wave window from the command line, according to the following:

```
add wave /#vsim_capacity#{assertions | classes | covergroups | qdas | solver}.
[{{Count | Current | Peak | Time}}
```

For example to display the count for classes in the Wave window, enter the following:

```
add wave /#vsim_capacity#/classes.Count
```

Writing a Text-Based Report

To generate a text-based report of the capacity data, you can use the write report command:

```
write report -capacity [-l | -s] [-classes | -qdas | -assertions | -cvg | -solver]
```

When you specify `-s` or no other switch, it reports coarse-grain analysis. When you specify `-l`, it reports the fine-grain analysis.

For example:

```
write report -capacity -l
```

produces a report with the following format (all memory numbers are in bytes):

```
# write report -capacity -l
# CAPACITY REPORT Generated on Wed Dec 31 16:00:00 1969
#
# Total Memory Allocated:3866920
# TYPE: (COUNT, CURRENT MEM, PEAK MEM, PEAK MEM TIME)
# Classes: (159, 16136, 16136, 4450 ns)
#   /std::semaphore: (18, 504, 504, 1650 ns)
#     verilog_src/std/std.sv(25): (10, 280, 280, 1650 ns)
#     verilog_src/std/std.sv(27): (8, 224, 224, 1650 ns)
#   /std::process: (8, 256, 320, 1658 ns)
#     c:/dev/mainline/modeltech/win32/./verilog_src/std/std.sv: (8,
256, 320, 1658 ns)
#   /defs::Packet: (97, 12416, 12416, 4450 ns)
#     src/test_router.sv(309): (97, 12416, 12416, 4450 ns)
#   /test_router_sv_unit::scoreboard: (1, 168, 168, 1650 ns)
#     src/test_router.sv(355): (1, 168, 168, 1650 ns)
#   /test_router_sv_unit::monitor: (8, 1024, 1024, 1650 ns)
#     src/test_router.sv(362): (8, 1024, 1024, 1650 ns)
#   /test_router_sv_unit::driver: (8, 608, 608, 1650 ns)
#     src/test_router.sv(361): (8, 608, 608, 1650 ns)
#   /test_router_sv_unit::stimulus: (8, 416, 416, 1650 ns)
#     src/test_router.sv(360): (8, 416, 416, 1650 ns)
#   /test_router_sv_unit::test_env: (1, 144, 144, 1650 ns)
#     src/test_router.sv(408): (1, 144, 144, 1650 ns)
#   /std::mailbox::mailbox__1: (8, 480, 480, 1650 ns)
#     src/test_router.sv(363): (8, 480, 480, 1650 ns)
#   /std::mailbox::mailbox__1: (2, 120, 120, 1650 ns)
#     src/test_router.sv(353): (1, 60, 60, 1650 ns)
```

```

#          src/test_router.sv(354): (1, 60, 60, 1650 ns)
# QDAS: (310, 3078, 3091, 4450 ns)
#   Arrays: (300, 2170, 2183, 4450 ns)
#          src/test_router.sv(355): (1, 40, 40, 1650 ns)
#          c:/dev/mainline/modeltech/win32/./verilog_src/std/std.sv: (9,
117, 130, 1657 ns)
#          src/test_router.sv(309): (89, 1157, 1170, 4450 ns)
#          src/test_router.sv(355): (3, 26, 36, 1650 ns)
#          src/defs.sv(24): (97, 194, 194, 4450 ns)
#          src/test_router.sv(295): (91, 456, 458, 1657 ns)
#          <NOFILE>: (15, 26, 26, 4450 ns)
#          src/test_router.sv(386): (174, 300, 300, 4450 ns)
#          src/test_router.sv(351): (1, 32, 32, 1650 ns)
#          src/test_router.sv(348): (1, 32, 32, 1650 ns)
#          src/test_router.sv(349): (1, 32, 32, 1650 ns)
#          src/test_router.sv(350): (1, 32, 32, 1650 ns)
#   Queues: (9, 888, 888, 1657 ns)
#          c:/dev/mainline/modeltech/win32/./verilog_src/std/std.sv(39):
(9, 888, 888, 1657 ns)
#   Associative: (1, 20, 20, 1650 ns)
#          src/test_router.sv(355): (1, 20, 20, 1650 ns)
# Assertions/Cover Directives: (0, 0, 0, 0 ns)
# Covergroups: (3, 1696, 1696, 1650 ns)
#   /test_router_sv_unit::scoreboard::cov1: (3, 1696, 1696, 1650 ns)
# Solver: (97, 2072816, 2081036, 1651 ns)
#          src/test_router.sv(311): (97, 2891148, 2891148, 4450 ns)

```

Reporting Capacity Analysis Data From a UCDB File

By default, coarse-grain analysis data is saved into a UCDB file, along with the simulation coverage data using the coverage save command.

You can report this data from UCDB file using vcover report or the vcover stats commands in the following forms:

```
vcover report -memory <UCDB_filename>
```

```
vcover stats -memory <UCDB_filename>
```

Currently the fine-grain analysis data is not available from this report except as details related to covergroup memory usage. To report the covergroup memory usage details, you can use the vcover report command with the following arguments:

```
vcover report -cvg -details -memory
```

Example

```
vcover report -memory test.ucdb
```

```
COVERGROUP MEMORY USAGE: Total 13.3 KBytes, Peak 13.3 KBytes at time 0 ns  
for total 4 coverpoints/crosses.
```

```
ASSERT/COVER MEMORY USAGE: Total Memory 0 Bytes.
```

```
CONSTRAINT SOLVER MEMORY USAGE: Total 1.1 MBytes, Peak 1.1 MBytes at time  
0 ns for total 100 randomize() calls.
```

```
CLASS OBJECTS MEMORY USAGE: Total Memory 68 Bytes and Peak Memory 68 Bytes  
used at time 0 ns for total 1 class objects.
```

```
DYNAMIC OBJECTS MEMORY USAGE: Total Memory 35 Bytes and Peak Memory 35  
Bytes used at time 0 ns for total 2 dynamic objects.
```

Chapter 21

Signal Spy

The Verilog language allows access to any signal from any other hierarchical block without having to route it via the interface. This means you can use hierarchical notation to either assign or determine the value of a signal in the design hierarchy from a test bench. This capability fails when a Verilog test bench attempts to reference a signal in a VHDL block or reference a signal in a Verilog block through a VHDL level of hierarchy.

This limitation exists because VHDL does not allow hierarchical notation. In order to reference internal hierarchical signals, you have to resort to defining signals in a global package and then utilize those signals in the hierarchical blocks in question. But, this requires that you keep making changes depending on the signals that you want to reference.

The Signal Spy procedures and system tasks overcome the aforementioned limitations. They allow you to monitor (spy), drive, force, or release hierarchical objects in a VHDL or mixed design.

The VHDL procedures are provided via the [VHDL Utilities Package \(util\)](#) within the *modelsim_lib* library. To access the procedures you would add lines like the following to your VHDL code:

```
library modelsim_lib;  
use modelsim_lib.util.all;
```

The Verilog tasks and SystemC functions are available as built-in [System Tasks and Functions](#).

Table 21-1. Signal Spy Reference Comparison

Refer to:	VHDL procedures	Verilog system tasks	SystemC function
disable_signal_spy	disable_signal_spy()	\$disable_signal_spy()	disable_signal_spy()
enable_signal_spy	enable_signal_spy()	\$enable_signal_spy()	enable_signal_spy()
init_signal_driver	init_signal_driver()	\$init_signal_driver()	init_signal_driver()
init_signal_spy	init_signal_spy()	\$init_signal_spy()	init_signal_spy()
signal_force	signal_force()	\$signal_force()	signal_force()
signal_release	signal_release()	\$signal_release()	signal_release()

Designed for Test Benches

Signal Spy limits the portability of your code. HDL code with Signal Spy procedures or tasks works only in Questa and Modelsim. We therefore recommend using Signal Spy only in test benches, where portability is less of a concern, and the need for such a tool is more applicable.

SignalSpy Supported Types

SignalSpy supports the following SystemVerilog types and user-defined SystemC types.

- SystemVerilog types
 - All scalar and integer SV types (bit, logic, int, shortint, longint, integer, byte, both signed and unsigned variations of these types)
 - Real and Shortreal
 - User defined types (packed/unpacked structures including nested structures, packed/unpacked unions, enums)
 - Arrays and Multi-D arrays of all supported types.
- SystemC types
 - Primitive C floating point types (double, float)
 - User defined types (structures including nested structures, unions, enums)

Cross-language type-checks and mappings have been implemented to support these types across all the possible language combinations:

- SystemC-SystemVerilog
- SystemC-SystemC
- SystemC-VHDL
- VHDL-SystemVerilog
- SystemVerilog-SystemVerilog

In addition to referring to the complete signal, you can also address the bit-selects, field-selects and part-selects of the supported types. For example:

```
/top/myInst/my_record[2].my_field1[4].my_vector[8]
```

disable_signal_spy

This reference section describes the following:

- VHDL Procedure — `disable_signal_spy()`
- Verilog Task — `$disable_signal_spy()`
- SystemC Function— `disable_signal_spy()`

The `disable_signal_spy` call disables the associated `init_signal_spy`. The association between the `disable_signal_spy` call and the `init_signal_spy` call is based on specifying the same *src_object* and *dest_object* arguments to both. The `disable_signal_spy` call can only affect `init_signal_spy` calls that had their *control_state* argument set to "0" or "1".

By default this command uses a forward slash (/) as a path separator. You can change this behavior with the [SignalSpyPathSeparator](#) variable in the *modelsim.ini* file.

VHDL Syntax

```
disable_signal_spy(<src_object>, <dest_object>, <verbose>)
```

Verilog Syntax

```
$disable_signal_spy(<src_object>, <dest_object>, <verbose>)
```

SystemC Syntax

```
disable_signal_spy(<src_object>, <dest_object>, <verbose>)
```

Returns

Nothing

Arguments

- `src_object`
Required string. A full hierarchical path (or relative downward path with reference to the calling block) to a VHDL signal, SystemVerilog or Verilog register/net, or SystemC signal. This path should match the path that was specified in the `init_signal_spy` call that you wish to disable.
- `dest_object`
Required string. A full hierarchical path (or relative downward path with reference to the calling block) to a VHDL signal, SystemVerilog or Verilog register/net, or SystemC signal. This path should match the path that was specified in the `init_signal_spy` call that you wish to disable.
- `verbose`
Optional integer. Specifies whether you want a message reported in the transcript stating that a disable occurred and the simulation time that it occurred.

0 — Does not report a message. Default.

1 — Reports a message.

Related procedures

[init_signal_spy](#), [enable_signal_spy](#)

Example

See [init_signal_spy Example](#) or [\\$init_signal_spy Example](#)

enable_signal_spy

This reference section describes the following:

- VHDL Procedure — enable_signal_spy()
- Verilog Task — \$enable_signal_spy()
- SystemC Function— enable_signal_spy()

The enable_signal_spy() call enables the associated init_signal_spy call. The association between the enable_signal_spy call and the init_signal_spy call is based on specifying the same src_object and dest_object arguments to both. The enable_signal_spy call can only affect init_signal_spy calls that had their control_state argument set to "0" or "1".

By default this command uses a forward slash (/) as a path separator. You can change this behavior with the [SignalSpyPathSeparator](#) variable in the *modelsim.ini* file.

VHDL Syntax

```
enable_signal_spy(<src_object>, <dest_object>, <verbose>)
```

Verilog Syntax

```
$enable_signal_spy(<src_object>, <dest_object>, <verbose>)
```

SystemC Syntax

```
enable_signal_spy(<src_object>, <dest_object>, <verbose>)
```

Returns

Nothing

Arguments

- src_object
Required string. A full hierarchical path (or relative downward path with reference to the calling block) to a VHDL signal, SystemVerilog or Verilog register/net, or SystemC signal. This path should match the path that was specified in the init_signal_spy call that you wish to enable.
- dest_object
Required string. A full hierarchical path (or relative downward path with reference to the calling block) to a VHDL signal, SystemVerilog or Verilog register/net, or SystemC signal. This path should match the path that was specified in the init_signal_spy call that you wish to enable.
- verbose
Optional integer. Possible values are 0 or 1. Specifies whether you want a message reported in the transcript stating that an enable occurred and the simulation time that it occurred.
0 — Does not report a message. Default.

1 — Reports a message.

Related tasks

[init_signal_spy](#), [disable_signal_spy](#)

Example

See [\\$init_signal_spy Example](#) or [init_signal_spy Example](#)

init_signal_driver

This reference section describes the following:

- VHDL Procedure — `init_signal_driver()`
- Verilog Task — `$init_signal_driver()`
- SystemC Function— `init_signal_driver()`

The `init_signal_driver()` call drives the value of a VHDL signal, Verilog net, or SystemC (called the `src_object`) onto an existing VHDL signal or Verilog net (called the `dest_object`). This allows you to drive signals or nets at any level of the design hierarchy from within a VHDL architecture or Verilog or SystemC module (for example, a test bench).

Note



Destination SystemC signals are not supported.

The `init_signal_driver` procedure drives the value onto the destination signal just as if the signals were directly connected in the HDL code. Any existing or subsequent drive or force of the destination signal, by some other means, will be considered with the `init_signal_driver` value in the resolution of the signal.

By default this command uses a forward slash (/) as a path separator. You can change this behavior with the [SignalSpyPathSeparator](#) variable in the `modelsim.ini` file.

Call only once

The `init_signal_driver` procedure creates a persistent relationship between the source and destination signals. Hence, you need to call `init_signal_driver` only once for a particular pair of signals. Once `init_signal_driver` is called, any change on the source signal will be driven on the destination signal until the end of the simulation.

For VHDL, we recommend that you place all `init_signal_driver` calls in a VHDL process. You need to code the VHDL process correctly so that it is executed only once. The VHDL process should not be sensitive to any signals and should contain only `init_signal_driver` calls and a simple wait statement. The process will execute once and then wait forever. See the example below.

For Verilog we recommend that you place all `$init_signal_driver` calls in a Verilog initial block. See the example below.

VHDL Syntax

```
init_signal_driver(<src_object>, <dest_object>, <delay>, <delay_type>, <verbose>)
```

Verilog Syntax

```
$init_signal_driver(<src_object>, <dest_object>, <delay>, <delay_type>, <verbose>)
```

SystemC Syntax

init_signal_driver(<src_object>, <dest_object>, <delay>, <delay_type>, <verbose>)

Returns

Nothing

Arguments

- **src_object**
Required string. A full hierarchical path (or relative downward path with reference to the calling block) to a VHDL signal, Verilog net, or SystemC signal. Use the path separator to which your simulation is set (for example, "/" or "."). A full hierarchical path must begin with a "/" or ".". The path must be contained within double quotes.
- **dest_object**
Required string. A full hierarchical path (or relative downward path with reference to the calling block) to an existing VHDL signal or Verilog net. Use the path separator to which your simulation is set (for example, "/" or "."). A full hierarchical path must begin with a "/" or ".". The path must be contained within double quotes.
- **delay**
Optional time value. Specifies a delay relative to the time at which the src_object changes. The delay can be an inertial or transport delay. If no delay is specified, then a delay of zero is assumed.
- **delay_type**
Optional del_mode or integer. Specifies the type of delay that will be applied.
For the VHDL init_signal_driver Procedure, The value must be either:
 - mti_inertial (default)
 - mti_transportFor the Verilog \$init_signal_driver Task, The value must be either:
 - 0 — inertial (default)
 - 1 — transportFor the SystemC init_signal_driver Function, The value must be either:
 - 0 — inertial (default)
 - 1 — transport
- **verbose**
Optional integer. Possible values are 0 or 1. Specifies whether you want a message reported in the Transcript stating that the src_object is driving the dest_object.
 - 0 — Does not report a message. Default.
 - 1 — Reports a message.

Related procedures

[init_signal_spy](#), [signal_force](#), [signal_release](#)

Limitations

- For the VHDL `init_signal_driver` procedure, when driving a Verilog net, the only *delay_type* allowed is `inertial`. If you set the delay type to `mti_transport`, the setting will be ignored and the delay type will be `mti_inertial`.
- For the Verilog `$init_signal_driver` task, when driving a Verilog net, the only *delay_type* allowed is `inertial`. If you set the delay type to `1` (transport), the setting will be ignored, and the delay type will be `inertial`.
- For the SystemC `init_signal_driver` function, when driving a Verilog net, the only *delay_type* allowed is `inertial`. If you set the delay type to `1` (transport), the setting will be ignored, and the delay type will be `inertial`.
- Any delays that are set to a value less than the simulator resolution will be rounded to the nearest resolution unit; no special warning will be issued.
- Verilog memories (arrays of registers) are not supported.

`$init_signal_driver` Example

This example creates a local clock (*clk0*) and connects it to two clocks within the design hierarchy. The `.../blk1/clk` will match local *clk0* and a message will be displayed. The `.../blk2/clk` will match the local *clk0* but be delayed by 100 ps. For the second call to work, the `.../blk2/clk` must be a VHDL based signal, because if it were a Verilog net a 100 ps inertial delay would consume the 40 ps clock period. Verilog nets are limited to only inertial delays and thus the setting of `1` (transport delay) would be ignored.

```
`timescale 1 ps / 1 ps

module testbench;

reg clk0;

initial begin
    clk0 = 1;
    forever begin
        #20 clk0 = ~clk0;
    end
end

initial begin
    $init_signal_driver("clk0", "/testbench/uut/blk1/clk", , , 1);
    $init_signal_driver("clk0", "/testbench/uut/blk2/clk", 100, 1);
end

...

endmodule
```

init_signal_driver Example

This example creates a local clock (*clk0*) and connects it to two clocks within the design hierarchy. The *.../blk1/clk* will match local *clk0* and a message will be displayed. The *open* entries allow the default delay and delay_type while setting the verbose parameter to a 1. The *.../blk2/clk* will match the local *clk0* but be delayed by 100 ps.

```
library IEEE, modelsim_lib;
use IEEE.std_logic_1164.all;
use modelsim_lib.util.all;

entity testbench is
end;

architecture only of testbench is
    signal clk0 : std_logic;
begin
    gen_clk0 : process
    begin
        clk0 <= '1' after 0 ps, '0' after 20 ps;
        wait for 40 ps;
    end process gen_clk0;

    drive_sig_process : process
    begin
        init_signal_driver("clk0", "/testbench/uut/blk1/clk", open, open, 1);
        init_signal_driver("clk0", "/testbench/uut/blk2/clk", 100 ps,
            mti_transport);

        wait;
    end process drive_sig_process;
    ...
end;
```

init_signal_spy

This reference section describes the following:

- VHDL Procedure — `init_signal_spy()`
- Verilog Task — `$init_signal_spy()`
- SystemC Function— `init_signal_spy()`

The `init_signal_spy()` call mirrors the value of a VHDL signal, SystemVerilog or Verilog register/net, or SystemC signal (called the `src_object`) onto an existing VHDL signal, Verilog register, or SystemC signal (called the `dest_object`). This allows you to reference signals, registers, or nets at any level of hierarchy from within a VHDL architecture or Verilog or SystemC module (for example, a test bench).

The `init_signal_spy` call only sets the value onto the destination signal and does not drive or force the value. Any existing or subsequent drive or force of the destination signal, by some other means, will override the value that was set by `init_signal_spy`.

By default this command uses a forward slash (/) as a path separator. You can change this behavior with the [SignalSpyPathSeparator](#) variable in the `modelsim.ini` file.

Call only once

The `init_signal_spy` call creates a persistent relationship between the source and destination signals. Hence, you need to call `init_signal_spy` once for a particular pair of signals. Once `init_signal_spy` is called, any change on the source signal will mirror on the destination signal until the end of the simulation unless the `control_state` is set.

However, you can place simultaneous read/write calls on the same signal using multiple `init_signal_spy` calls, for example:

```
init_signal_spy ("/sc_top/sc_sig", "/top/hdl_INST/hdl_sig");  
init_signal_spy ("/top/hdl_INST/hdl_sig", "/sc_top/sc_sig");
```

The `control_state` determines whether the mirroring of values can be enabled/disabled and what the initial state is. Subsequent control of whether the mirroring of values is enabled/disabled is handled by the `enable_signal_spy` and `disable_signal_spy` calls.

For VHDL procedures, we recommend that you place all `init_signal_spy` calls in a VHDL process. You need to code the VHDL process correctly so that it is executed only once. The VHDL process should not be sensitive to any signals and should contain only `init_signal_spy` calls and a simple wait statement. The process will execute once and then wait forever, which is the desired behavior. See the example below.

For Verilog tasks, we recommend that you place all `$init_signal_spy` tasks in a Verilog initial block. See the example below.

VHDL Syntax

```
init_signal_spy(<src_object>, <dest_object>, <verbose>, <control_state>)
```

Verilog Syntax

`$init_signal_spy(<src_object>, <dest_object>, <verbose>, <control_state>)`

SystemC Syntax

`init_signal_spy(<src_object>, <dest_object>, <verbose>, <control_state>)`

Returns

Nothing

Arguments

- `src_object`
Required string. A full hierarchical path (or relative downward path with reference to the calling block) to a VHDL signal or SystemVerilog or Verilog register/net. Use the path separator to which your simulation is set (for example, "/" or "."). A full hierarchical path must begin with a "/" or ".". The path must be contained within double quotes.
- `dest_object`
Required string. A full hierarchical path (or relative downward path with reference to the calling block) to an existing VHDL signal or Verilog register. Use the path separator to which your simulation is set (for example, "/" or "."). A full hierarchical path must begin with a "/" or ".". The path must be contained within double quotes.
- `verbose`
Optional integer. Possible values are 0 or 1. Specifies whether you want a message reported in the Transcript stating that the `src_object`'s value is mirrored onto the `dest_object`.
 - 0 — Does not report a message. Default.
 - 1 — Reports a message.
- `control_state`
Optional integer. Possible values are -1, 0, or 1. Specifies whether or not you want the ability to enable/disable mirroring of values and, if so, specifies the initial state.
 - 1 — no ability to enable/disable and mirroring is enabled. (default)
 - 0 — turns on the ability to enable/disable and initially disables mirroring.
 - 1 — turns on the ability to enable/disable and initially enables mirroring.

Related procedures

[init_signal_driver](#), [signal_force](#), [signal_release](#), [enable_signal_spy](#), [disable_signal_spy](#)

Limitations

- When mirroring the value of a SystemVerilog or Verilog register/net onto a VHDL signal, the VHDL signal must be of type bit, bit_vector, std_logic, or std_logic_vector.
- Verilog memories (arrays of registers) are not supported.

init_signal_spy Example

In this example, the value of */top/uut/inst1/sig1* is mirrored onto */top/top_sig1*. A message is issued to the transcript. The ability to control the mirroring of values is turned on and the `init_signal_spy` is initially enabled.

The mirroring of values will be disabled when `enable_sig` transitions to a '0' and enable when `enable_sig` transitions to a '1'.

```
library ieee;
library modelsim_lib;
use ieee.std_logic_1164.all;
use modelsim_lib.util.all;
entity top is
end;
architecture only of top is
    signal top_sig1 : std_logic;
begin
    ...
    spy_process : process
    begin
        init_signal_spy("/top/uut/inst1/sig1", "/top/top_sig1", 1, 1);
        wait;
    end process spy_process;
    ...
    spy_enable_disable : process(enable_sig)
    begin
        if (enable_sig = '1') then
            enable_signal_spy("/top/uut/inst1/sig1", "/top/top_sig1", 0);
        elsif (enable_sig = '0')
            disable_signal_spy("/top/uut/inst1/sig1", "/top/top_sig1", 0);
        end if;
    end process spy_enable_disable;
    ...
end;
```

\$init_signal_spy Example

In this example, the value of *.top.uut.inst1.sig1* is mirrored onto *.top.top_sig1*. A message is issued to the transcript. The ability to control the mirroring of values is turned on and the `init_signal_spy` is initially enabled.

The mirroring of values will be disabled when `enable_reg` transitions to a '0' and enabled when `enable_reg` transitions to a '1'.

```
module top;
    ...
    reg top_sig1;
    reg enable_reg;
    ...
    initial
    begin
        $init_signal_spy(".top.uut.inst1.sig1", ".top.top_sig1", 1, 1);
    end
```

Signal Spy **init_signal_spy**

```
    always @ (posedge enable_reg)
    begin
        $enable_signal_spy(".top.uut.inst1.sig1", ".top.top_sig1", 0);
    end
    always @ (negedge enable_reg)
    begin
        $disable_signal_spy(".top.uut.inst1.sig1", ".top.top_sig1", 0);
    end
    ...
endmodule
```

signal_force

This reference section describes the following:

- VHDL Procedure — `signal_force()`
- Verilog Task — `$signal_force()`
- SystemC Function— `signal_force()`

The `signal_force()` call forces the value specified onto an existing VHDL signal, Verilog register or net, or SystemC signal (called the `dest_object`). This allows you to force signals, registers, or nets at any level of the design hierarchy from within a VHDL architecture or Verilog or SystemC module (for example, a test bench).

A `signal_force` works the same as the `force` command with the exception that you cannot issue a repeating force. The force will remain on the signal until a `signal_release`, a force or release command, or a subsequent `signal_force` is issued. `Signal_force` can be called concurrently or sequentially in a process.

This command displays any signals using your `radix` setting (either the default, or as you specify) unless you specify the radix in the *value* you set.

By default this command uses a forward slash (/) as a path separator. You can change this behavior with the `SignalSpyPathSeparator` variable in the `modelsim.ini` file.

VHDL Syntax

```
signal_force(<dest_object>, <value>, <rel_time>, <force_type>, <cancel_period>, <verbose>)
```

Verilog Syntax

```
$signal_force(<dest_object>, <value>, <rel_time>, <force_type>, <cancel_period>,  
<verbose>)
```

SystemC Syntax

```
signal_force(<dest_object>, <value>, <rel_time>, <force_type>, <cancel_period>, <verbose>)
```

Returns

Nothing

Arguments

- `dest_object`
Required string. A full hierarchical path (or relative downward path with reference to the calling block) to an existing VHDL signal, SystemVerilog or Verilog register/net or SystemC signal. Use the path separator to which your simulation is set (for example, "/" or "."). A full hierarchical path must begin with a "/" or ".". The path must be contained within double quotes.

- value

Required string. Specifies the value to which the `dest_object` is to be forced. The specified value must be appropriate for the type. The *value* can be a sequence of character literals or as a based number with a radix of 2, 8, 10 or 16. For example, the following values are equivalent for a signal of type `bit_vector (0 to 3)`:

- 1111 — character literal sequence
- 2#1111 — binary radix
- 10#15 — decimal radix
- 16#F — hexadecimal radix

- rel_time

Optional time. Specifies a time relative to the current simulation time for the force to occur. The default is 0.

- force_type

Optional forcetype or integer. Specifies the type of force that will be applied.

For the VHDL procedure, the value must be one of the following;

default — which is "freeze" for unresolved objects or "drive" for resolved objects
deposit
drive
freeze.

For the Verilog task, the value must be one of the following;

0 — default, which is "freeze" for unresolved objects or "drive" for resolved objects
1 — deposit
2 — drive
3 — freeze

For the SystemC function, the value must be one of the following;

0 — default, which is "freeze" for unresolved objects or "drive" for resolved objects
1 — deposit
2 — drive
3 — freeze

See the force command for further details on force type.

- cancel_period

Optional time or integer. Cancels the `signal_force` command after the specified period of time units. Cancellation occurs at the last simulation delta cycle of a time unit.

For the VHDL procedure, a value of zero cancels the force at the end of the current time period. Default is -1 ms. A negative value means that the force will not be cancelled.

For the Verilog task, A value of zero cancels the force at the end of the current time period. Default is -1. A negative value means that the force will not be cancelled.

For the SystemC function, A value of zero cancels the force at the end of the current time period. Default is -1. A negative value means that the force will not be cancelled.

- verbose

Optional integer. Possible values are 0 or 1. Specifies whether you want a message reported in the Transcript stating that the value is being forced on the `dest_object` at the specified time.

0 — Does not report a message. Default.

1 — Reports a message.

Related procedures

[init_signal_driver](#), [init_signal_spy](#), [signal_release](#)

Limitations

- You cannot force bits or slices of a register; you can force only the entire register.
- Verilog memories (arrays of registers) are not supported.

\$signal_force Example

This example forces `reset` to a "1" from time 0 ns to 40 ns. At 40 ns, `reset` is forced to a "0", 200000 ns after the second `$signal_force` call was executed.

```
`timescale 1 ns / 1 ns

module testbench;

  initial
  begin
    $signal_force("/testbench/uut/blk1/reset", "1", 0, 3, , 1);
    $signal_force("/testbench/uut/blk1/reset", "0", 40, 3, 200000, 1);
  end

  ...

endmodule
```

signal_force Example

This example forces `reset` to a "1" from time 0 ns to 40 ns. At 40 ns, `reset` is forced to a "0", 2 ms after the second `signal_force` call was executed.

If you want to skip parameters so that you can specify subsequent parameters, you need to use the keyword "open" as a placeholder for the skipped parameter(s). The first `signal_force`

procedure illustrates this, where an "open" for the cancel_period parameter means that the default value of -1 ms is used.

```
library IEEE, modelsim_lib;
use IEEE.std_logic_1164.all;
use modelsim_lib.util.all;

entity testbench is
end;

architecture only of testbench is
begin

    force_process : process
    begin
        signal_force("/testbench/uut/blk1/reset", "1", 0 ns, freeze, open, 1);
        signal_force("/testbench/uut/blk1/reset", "0", 40 ns, freeze, 2 ms,
1);
        wait;
    end process force_process;

    ...

end;
```

signal_release

This reference section describes the following:

- VHDL Procedure — `signal_release()`
- Verilog Task — `$signal_release()`
- SystemC Function— `signal_release()`

The `signal_release()` call releases any force that was applied to an existing VHDL signal, SystemVerilog or Verilog register/net, or SystemC signal (called the `dest_object`). This allows you to release signals, registers or nets at any level of the design hierarchy from within a VHDL architecture or Verilog or SystemC module (for example, a test bench).

A `signal_release` works the same as the `noforce` command. `Signal_release` can be called concurrently or sequentially in a process.

By default this command uses a forward slash (/) as a path separator. You can change this behavior with the `SignalSpyPathSeparator` variable in the `modelsim.ini` file.

VHDL Syntax

```
signal_release(<dest_object>, <verbose>)
```

Verilog Syntax

```
$signal_release(<dest_object>, <verbose>)
```

SystemC Syntax

```
signal_release(<dest_object>, <verbose>)
```

Returns

Nothing

Arguments

- `dest_object`

Required string. A full hierarchical path (or relative downward path with reference to the calling block) to an existing VHDL signal, SystemVerilog or Verilog register/net, or SystemC signal. Use the path separator to which your simulation is set (for example, "/" or "."). A full hierarchical path must begin with a "/" or ".". The path must be contained within double quotes.

- `verbose`

Optional integer. Possible values are 0 or 1. Specifies whether you want a message reported in the Transcript stating that the signal is being released and the time of the release.

0 — Does not report a message. Default.

1 — Reports a message.

Related procedures

[init_signal_driver](#), [init_signal_spy](#), [signal_force](#)

Limitations

- You cannot release a bit or slice of a register; you can release only the entire register.

signal_release Example

This example releases any forces on the signals *data* and *clk* when the signal *release_flag* is a "1". Both calls will send a message to the transcript stating which signal was released and when.

```
library IEEE, modelsim_lib;
use IEEE.std_logic_1164.all;
use modelsim_lib.util.all;

entity testbench is
end;

architecture only of testbench is

    signal release_flag : std_logic;

begin

    stim_design : process
    begin
        ...
        wait until release_flag = '1';
        signal_release("/testbench/dut/blk1/data", 1);
        signal_release("/testbench/dut/blk1/clk", 1);
        ...
    end process stim_design;

    ...

end;
```

\$signal_release Example

This example releases any forces on the signals *data* and *clk* when the register *release_flag* transitions to a "1". Both calls will send a message to the transcript stating which signal was released and when.


```
module testbench;

reg release_flag;

always @(posedge release_flag) begin
    $signal_release("/testbench/dut/blk1/data", 1);
    $signal_release("/testbench/dut/blk1/clock", 1);
end

...

endmodule
```


Chapter 22

Monitoring Simulations with JobSpy

This chapter describes JobSpy™, a tool for monitoring and controlling batch simulations and simulation farms.

Designers frequently run multiple simulation jobs in batch mode once verification reaches the regression testing stage. They face the problem that simulation farms and batch-mode runs offer little visibility into and control over simulation jobs. JobSpy helps alleviate this problem by allowing you to interact with batch jobs. By creating a process external to the running simulator, JobSpy can send and receive information about the running jobs.

Some applications of JobSpy include the following:

- Checking the progress of a simulation.
- Examining internal signal values to check if the design is functioning correctly, without stopping the simulation.
- Suspending one job to release a license for a more important job, also allowing you to restart the suspended job later.
- Instructing the running batch job to do a checkpoint of the job and then continue the run. If the workstation that was running a batch job were to fail at sometime in the future, you would could restart the job again from the saved checkpoint file.

You can run JobSpy from the command line, from within the ModelSim GUI, or from a standalone GUI. The actual commands that are sent and received across the communication pipe are the same for all modes of operation. The standalone GUI simply provides a dialog box where you can see all the running jobs.

Basic JobSpy Flow

The basic steps for setting up and using JobSpy are as follows:

1. Set JOBSPY_DAEMON environment variable.
2. Start JobSpy daemon.

Command line: **jobspsy -startd**

GUI: **Tools > JobSpy > Daemon > Start Daemon**

3. Start simulation jobs as you normally would. The tool will communicate with the JobSpy daemon through the use of the JOBSPY_DAEMON environment variable.

4. Use **jobspy** command or Job Manager GUI to monitor results.

Starting the JobSpy Daemon

You must start the JobSpy daemon prior to launching any simulation jobs. The daemon tracks jobs by setting up a communication pipe with each running simulation. When a simulation job starts, the daemon opens a TCP/IP port for the job and then records to a file:

- port number
- host name that the job was started on
- working directory

With a connection to the job established, you can invoke various commands via the command line or GUI to monitor or control the job. There are two steps to starting the daemon:

1. Set the **JOBSPY_DAEMON** environment variable.

The environment variable is set with the following syntax:

```
JOBSPY_DAEMON=<port_NUMBER>@<host>
```

For example,

```
JOBSPY_DAEMON=1301@mymachine
```

Every user who will run JobSpy must set this environment variable. You will typically set this in a start-up script, such as your *.cshrc* file, so that every new shell has access to the daemon.

2. Invoke the daemon using the **jobspy -startd** command or by selecting **Tools > JobSpy > Daemon > Start Daemon** from within ModelSim.

Any person who knows what port@host to set their **JOBSPY_DAEMON** variable to can control jobs submitted to that host. The intended use is that a person would set their **JOBSPY_DAEMON** variable, start the daemon, and then only they could control their jobs (unless they told somebody what port@host to use). Each user can use his/her own port id to monitor only their jobs.

Setting the JOBSPY_DAEMON Variable as a Directory

As an alternative to using a TCP/IP port, you can instruct the JobSpy Daemon to communicate with simulation jobs via a directory and file structure. Although a directory location is not technically a Daemon, for ease of use we will be referring to it as one in this document.

To specify a directory as your JobSpy Daemon, you would use the **JOBSPY_DAEMON** environment variable similar to the following:

`JOBSPY_DAEMON=/server/directory/subdirectory`

This instructs any simulation job invoked with the same `$JOBSPY_DAEMON` to create files containing communication and run information in the specified directory, which enables communication between JobSpy and the simulation jobs.

The `jobspy` command behaves similarly regardless of your using a TCP/IP port or a directory name for your JobSpy Daemon.

Running JobSpy from the Command Line

The JobSpy command-line interface is accessible from a shell prompt or within the ModelSim GUI, where the syntax is:

`jobspy [-gui] [-killd] [-startd] | jobs | status | <jobid> <command>`

See the [jobspy](#) command for complete syntax. The most common invocations are:

- **`jobspy -startd`** — invokes the daemon
- **`jobspy jobs`** — lists all jobs and their id numbers; you need the ids in order to execute commands on the jobs
- **`<jobid> <command>`** — allows you to issue commands to a job; only certain commands can be used, as noted below

Simulation Commands Available to JobSpy

You can perform a select number of simulator commands on jobs via JobSpy. The table below lists the available commands with a brief description.

Table 22-1. Simulation Commands You can Issue from JobSpy

Command	Description
stop	stops a simulation
go	resumes a stopped job
checkpoint or check	checkpoints a simulation
savewlf	saves simulation results to a WLF file; see Viewing Results During Active Simulation ; by default this command uses the pathname from the remote machine
examine	prints the value of a signal in the remote job
force	forces signal values in the remote job
log	logs signals in the waveform log file (.wlf)
nolog	removes logged signals from the waveform log file (.wlf)

Table 22-1. Simulation Commands You can Issue from JobSpy

Command	Description
now	prints job's current simulation time
profile on	enable profiling of remote job
profile off	disable profiling of remote job
profile save [<filename>]	save a profile of remote job. Default <filename> is <i>job<jobid>.prof</i>
pwd	prints the job's current working directory
quit	exits a simulation (terminates job)
savecov [<filename>]	writes out a coverage data UCDB file, equivalent to the coverage save command. Default <filename> is <i>Job_<gridtype>_<jobid>.ucdb</i> where <gridtype> is mti, sge, lsf or vov.
set	sets a TCL variable in the remote job's interpreter
simstatus	shows current status of the simulation
suspend	suspends job (releases license)
unsuspend	un-suspends job (reacquires license)

Example Session

The following example illustrates a session of JobSpy:

```

$ JOBSPY_DAEMON=1300@time //sets the daemon to a port@host
$ export JOBSPY_DAEMON //exports the environment variable

$ jobspy -startd //start the daemon

$ jobspy jobs // print list of jobs
JobID Type Sim Status Sim Time user Host PID Start Time Directory
5 mti Running 1,200ns alla time 24710 Mon Dec 27. /u/alla/z
11 mti Running 3,433ns mcar larg 24915 Tue Dec 28. /u/mcar/x

$ jobspy 11 checkpoint //checkpoint job 11
Checkpointing Job

$ jobspy 11 cont //resume job 11
continuing

$ jobspy 5 dataset save sim snap.wlf // saving waveforms from job 5
Dataset "sim" exported as WLF file: snap.wlf. @ 1,200ns

$ vsim -view snap.wlf // viewing waveforms from job 5

```

Running the JobSpy GUI

JobSpy includes a GUI called Job Manager that you can invoke from within ModelSim or separately as a stand-alone tool. The Job Manager shows all active simulations in real time and provides convenient access to JobSpy commands.

Starting Job Manager

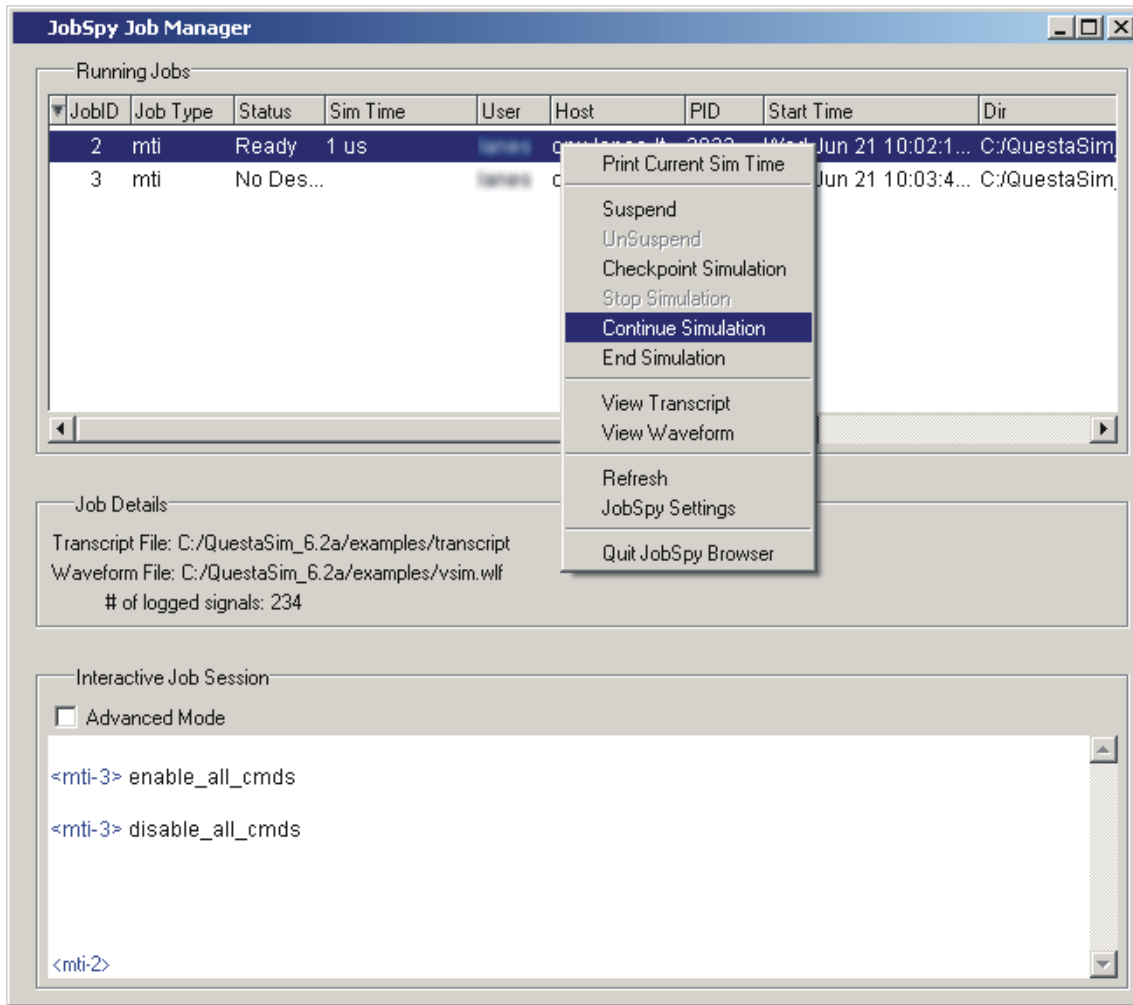
You can start Job Manager from a shell prompt or from within ModelSim:

- Shell Prompt — **jobs Spy -gui**
- GUI— **Tools > JobSpy > JobSpy Job Manager**

Invoking Simulation Commands in Job Manager

You can invoke simulation commands in Job Manager via a right-click menu or from the prompt in the Interactive Job Session window. Right-click a job in the list to access menu commands:

Figure 22-1. JobSpy Job Manager



Interactive Job Session Pane

The Interactive Job Session pane provides a command line for interacting with jobs. Commands you enter affect the job currently selected in the Running Jobs portion of the dialog box. See [Table 22-1](#) for a list of commands you can enter in the Interactive Job Session pane.

Note



If you check Advanced Mode, you can enter any ModelSim command at the prompt. However, you need to be careful as many ModelSim commands will not function properly with JobSpy.

View Commands and Pathnames

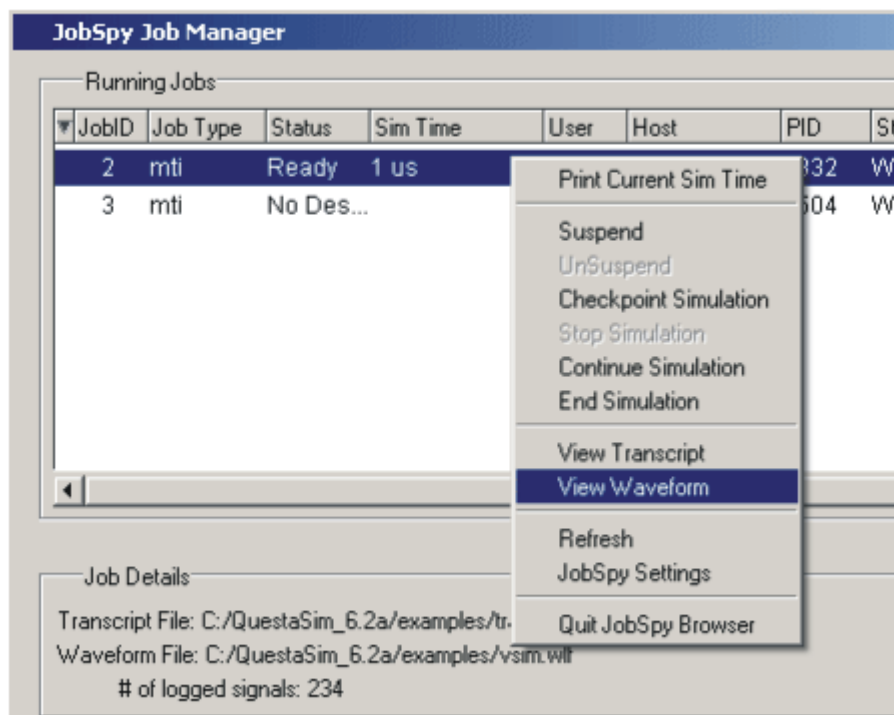
The **View Transcript** and **View Waveform** commands display files (*transcript* and *<name>.wlf*, respectively) that are output by the simulator. These commands use the pathname

from the remote machine to locate the required file. Depending on how your network is organized, the pathname may be different or inaccessible from the machine which is running JobSpy. In such cases, these commands will not work. The work around is to use **jobspy savewlf** to specify a known location for the WLF file or **cp** to copy the Transcript file to a known location.

Viewing Results During Active Simulation

You may want to check simulation results while your simulation jobs are still running. You can do this via the GUI or by using the **savewlf** command. To view waveforms from the JobSpy GUI, right-click a job and select **View Waveform**.

Figure 22-2. Job Manager View Waveform



Here are two important points to remember about viewing waveforms from the GUI:

- You must first log signals before you can view them as waveforms. If you haven't logged any signals, the View Waveform command in the GUI will be disabled.
- View Waveform uses the pathname from the remote machine to access a WLF file. The command may not work on some networks. See [View Commands and Pathnames](#) for details.

Viewing Waveforms from the Command Line

From the command line, there are three steps to viewing waveforms:

1. Log the appropriate signals

```
add log *
```

2. Save a dataset

```
$ jobspy 1204 savewlf snap.wlf  
Dataset "sim" exported as WLF file: snap.wlf. @ 84,785,547 ns
```

3. View the dataset

```
vsim -view snap.wlf
```

Licensing and Job Suspension

When you suspend a job via JobSpy, the simulation license is released by default. You can change this behavior by modifying the `MTI_RELEASE_ON_SUSPEND` environment variable. By default the variable is set to 10 (in seconds), which releases the license 10 seconds after receiving a suspend signal. If you change the value to 0 (off), simulation licenses will not be released upon job suspension.

Checkpointing Jobs

Checkpointing allows you to save the state of a simulation and restore it at a later time. There are three primary reasons for checkpointing jobs:

- Free up a license for a more important job
- Migrate a job from one machine to another
- Backup a job in case of a hardware crash or failure

In the case of freeing up a license, you should use the `suspend` command instead. Job suspension does not have the restrictions that checkpointing does.

If you need to checkpoint a job for migration or backup, keep in mind the following restrictions:

- The job must be restored on the same platform and exact OS on which the job was checkpointed.
- If your job includes any foreign C code (such as PLI or FLI), the foreign application must be written to support checkpointing. See [The PLI Callback reason Argument](#) for more information on checkpointing with PLI applications. See the Foreign Language Interface Reference Manual for information on checkpointing with FLI applications.

Connecting to Load-Sharing Software

Load-sharing software, such as Platform Computing's LSF or Sun's Grid Engine, centralize management of distributed computing resources. JobSpy can access and monitor simulation runs that were submitted to these load-managing products.

With the exception of checkpointing (discussed below), the only requirement for connecting to load-sharing software is that the JobSpy daemon be running prior to submitting the jobs. If the daemon is running, the jobs will show up in JobSpy automatically.

JobSpy supports Sun Grid Engine's task arrays, where the simulation jobs use the `JOB_ID` and the `SGE_TASK_ID` environment variables. The `jobspsy` command can reference these jobs as "`<taskId>.<jobId>`".

Checkpointing with Load-Sharing Software

Some additional steps are required to configure load-sharing software for checkpointing **vsim** jobs. The configuration depends on which load-sharing software you run.

Configuring LSF for Checkpointing

Do the following to enable **vsim** checkpointing with LSF:

- Set the environment variable `LSB_ECHKPNT_METHOD_DIR` to point to `<install_dir>/modeltech/<platform>`
`<platform>` refers to the VCO for the ModelSim installation (for example, `linux`, `sunos5`, and so forth). See the *Installation Guide* for a complete list.
- Set the environment variable `LSB_ECHKPNT_METHOD` to "modelsim"

With these environment variables set, you can use standard LSF commands to checkpoint **vsim** jobs. Consult LSF documentation for information on those commands.

Configuring Flowtracer for Checkpointing

Flowtracer does not support checkpointing of **vsim** jobs.

Configuring Grid Engine for Checkpointing

To checkpoint **vsim** jobs with Grid Engine, you must create a Checkpoint Object, taking note of the following settings:

- Set Interface to:
`APPLICAITON-LEVEL.`
- Set the Checkpoint Command field to:

```
<install_dir>/modeltech/<platform>/jobspy -check
```

where <platform> refers to the VCO for the ModelSim installation (for example, linux, sunos5, and so forth). See the *Installation Guide* for a complete list.

- Set the Migration Command field to:

```
<install_dir>/modeltech/<platform>/jobspy -check k
```

Consult the Grid Engine documentation for additional information.

Chapter 23

Generating Stimulus with Waveform Editor

The ModelSim Waveform Editor offers a simple method for creating design stimulus. You can generate and edit waveforms in a graphical manner and then drive the simulation with those waveforms. With Waveform Editor you can do the following:

- Create waveforms using four predefined patterns: clock, random, repeater, and counter. See [Creating Waveforms from Patterns](#).
- Edit waveforms with numerous functions including inserting, deleting, and stretching edges; mirroring, inverting, and copying waveform sections; and changing waveform values on-the-fly. See [Editing Waveforms](#).
- Drive the simulation directly from the created waveforms
- Save created waveforms to four stimulus file formats: Tcl force format, extended VCD format, Verilog module, or VHDL architecture. The HDL formats include code that matches the created waveforms and can be used in test benches to drive a simulation. See [Exporting Waveforms to a Stimulus File](#)

Limitations

The current version does not support the following:

- Enumerated signals, records, multi-dimensional arrays, and memories
- User-defined types
- SystemC or SystemVerilog

Getting Started with the Waveform Editor

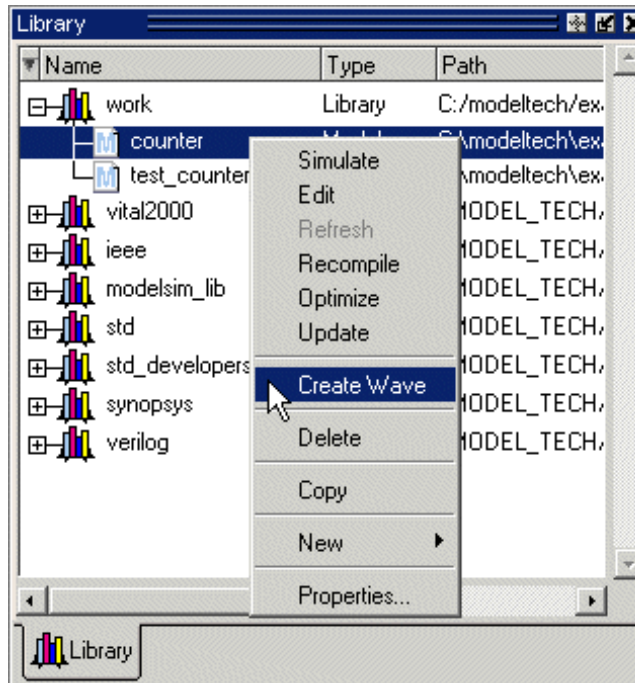
You can use Waveform Editor before or after loading a design. Regardless of which method you choose, you will select design objects and use them as the basis for created waveforms.

Using Waveform Editor Prior to Loading a Design

Here are the basic steps for using waveform editor prior to loading a design:

1. Right-click a design unit on the Library Window and select Create Wave .

Figure 23-1. Waveform Editor: Library Window



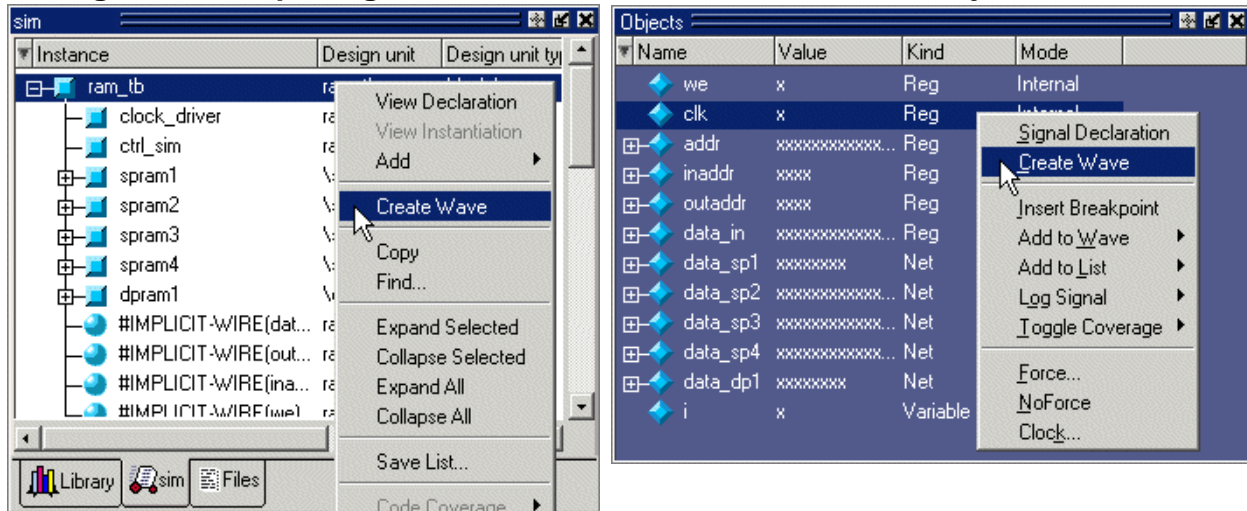
2. Edit the waveforms in the Wave window. See [Editing Waveforms](#) for more details.
3. Run the simulation (see [Simulating Directly from Waveform Editor](#)) or save the created waveforms to a stimulus file (see [Exporting Waveforms to a Stimulus File](#)).

Using Waveform Editor After Loading a Design

Here are the basic steps for using waveform editor after loading a design:

1. Right-click a block in the structure window or an object in the Object pane and select **Create Wave**.

Figure 23-2. Opening Waveform Editor from Structure or Objects Windows



2. Use the Create Pattern wizard to create the waveforms (see [Creating Waveforms from Patterns](#)).
3. Edit the waveforms as required (see [Editing Waveforms](#)).
4. Run the simulation (see [Simulating Directly from Waveform Editor](#)) or save the created waveforms to a stimulus file (see [Exporting Waveforms to a Stimulus File](#)).

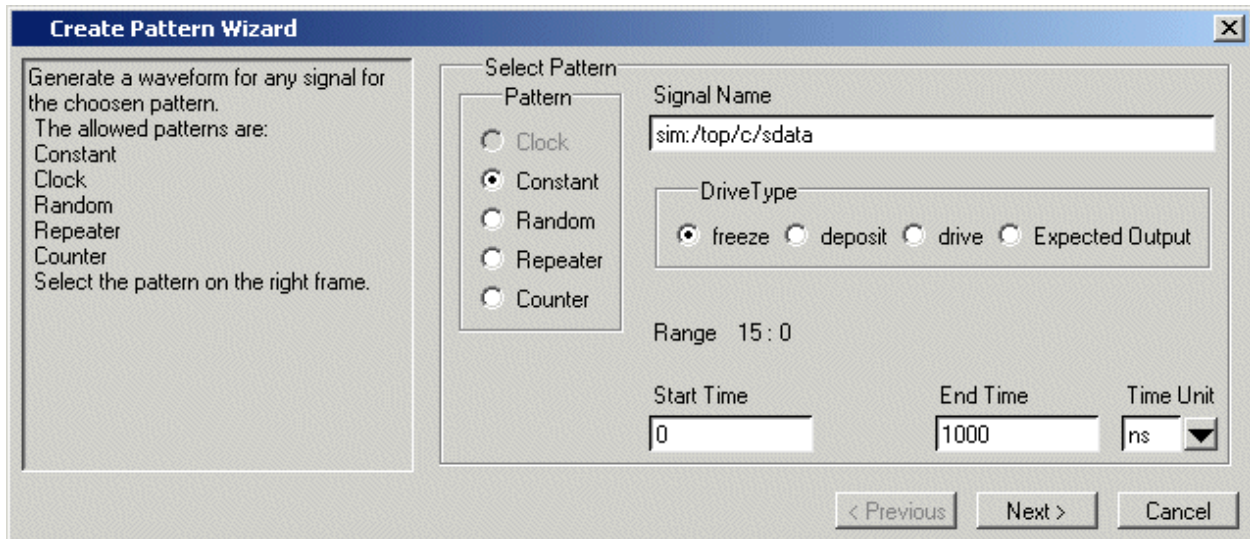
Creating Waveforms from Patterns

Waveform Editor includes a Create Pattern wizard that walks you through the process of creating waveforms. To access the wizard:

- Right-click an object in the Objects pane or structure pane (that is, sim tab of the Workspace pane) and select **Create Wave**.
- Right-click a signal already in the Wave window and select Create/Modify Waveform. (Only possible before simulation is run.)

The graphic below shows the initial dialog in the wizard. Note that the Drive Type field is not present for input and output signals.

Figure 23-3. Create Pattern Wizard



In this dialog you specify the signal that the waveform will be based upon, the Drive Type (if applicable), the start and end time for the waveform, and the pattern for the waveform.

The second dialog in the wizard lets you specify the appropriate attributes based on the pattern you select. The table below shows the five available patterns and their attributes:

Table 23-1. Signal Attributes in Create Pattern Wizard

Pattern	Description
Clock	Specify an initial value, duty cycle, and clock period for the waveform.
Constant	Specify a value.
Random	Generates different patterns depending upon the seed value. Specify the type (normal or uniform), an initial value, and a seed value. If you don't specify a seed value, ModelSim uses a default value of 5.
Repeater	Specify an initial value and pattern that repeats. You can also specify how many times the pattern repeats.
Counter	Specify start and end values, time period, type (Range, Binary, Gray, One Hot, Zero Hot, Johnson), counter direction, step count, and repeat number.

Creating Waveforms with Wave Create Command

The `wave create` command gives you the ability to generate clock, constant, random, repeater, and counter waveform patterns from the command line. You can then modify the waveform

interactively in the GUI and use the results to drive simulation. See the [wave create](#) command in the Command Reference for correct syntax, argument descriptions, and examples.

Editing Waveforms

You can edit waveforms interactively with menu commands, mouse actions, or by using the [wave edit](#) command.

To edit waveforms in the Wave window, follow these steps:

1. Create an editable pattern as described under [Creating Waveforms from Patterns](#).
2. Enter editing mode by right-clicking a blank area of the toolbar and selecting **Wave_edit** from the toolbar popup menu.

This will open the Wave Edit toolbar. For details about the Wave Edit toolbar, please refer to [Wave Edit Toolbar](#).

Figure 23-4. Wave Edit Toolbar



3. Select an edge or a section of the waveform with your mouse. See [Selecting Parts of the Waveform](#) for more details.
4. Select a command from the **Wave > Wave Editor** menu when the Wave window is docked, from the **Edit > Wave** menu when the Wave window is undocked, or right-click on the waveform and select a command from the **Wave** context menu.

The table below summarizes the editing commands that are available.

Table 23-2. Waveform Editing Commands

Operation	Description
Cut	Cut the selected portion of the waveform to the clipboard
Copy	Copy the selected portion of the waveform to the clipboard
Paste	Paste the contents of the clipboard over the selected section or at the active cursor location
Insert Pulse	Insert a pulse at the location of the active cursor
Delete Edge	Delete the edge at the active cursor
Invert	Invert the selected waveform section
Mirror	Mirror the selected waveform section
Value	Change the value of the selected portion of the waveform

Table 23-2. Waveform Editing Commands (cont.)

Operation	Description
Stretch Edge	Move an edge forward/backward by "stretching" the waveform; see Stretching and Moving Edges for more information
Move Edge	Move an edge forward/backward without changing other edges; see Stretching and Moving Edges for more information
Extend All Waves	Extend all created waveforms by the specified amount or to the specified simulation time; ModelSim cannot undo this edit or any edits done prior to an extend command
Change Drive Type	Change the drive type of the selected portion of the waveform
Undo	Undo waveform edits (except changing drive type and extending all waves)
Redo	Redo previously undone waveform edits

These commands can also be accessed via toolbar buttons. See [Wave Edit Toolbar](#) for more information.

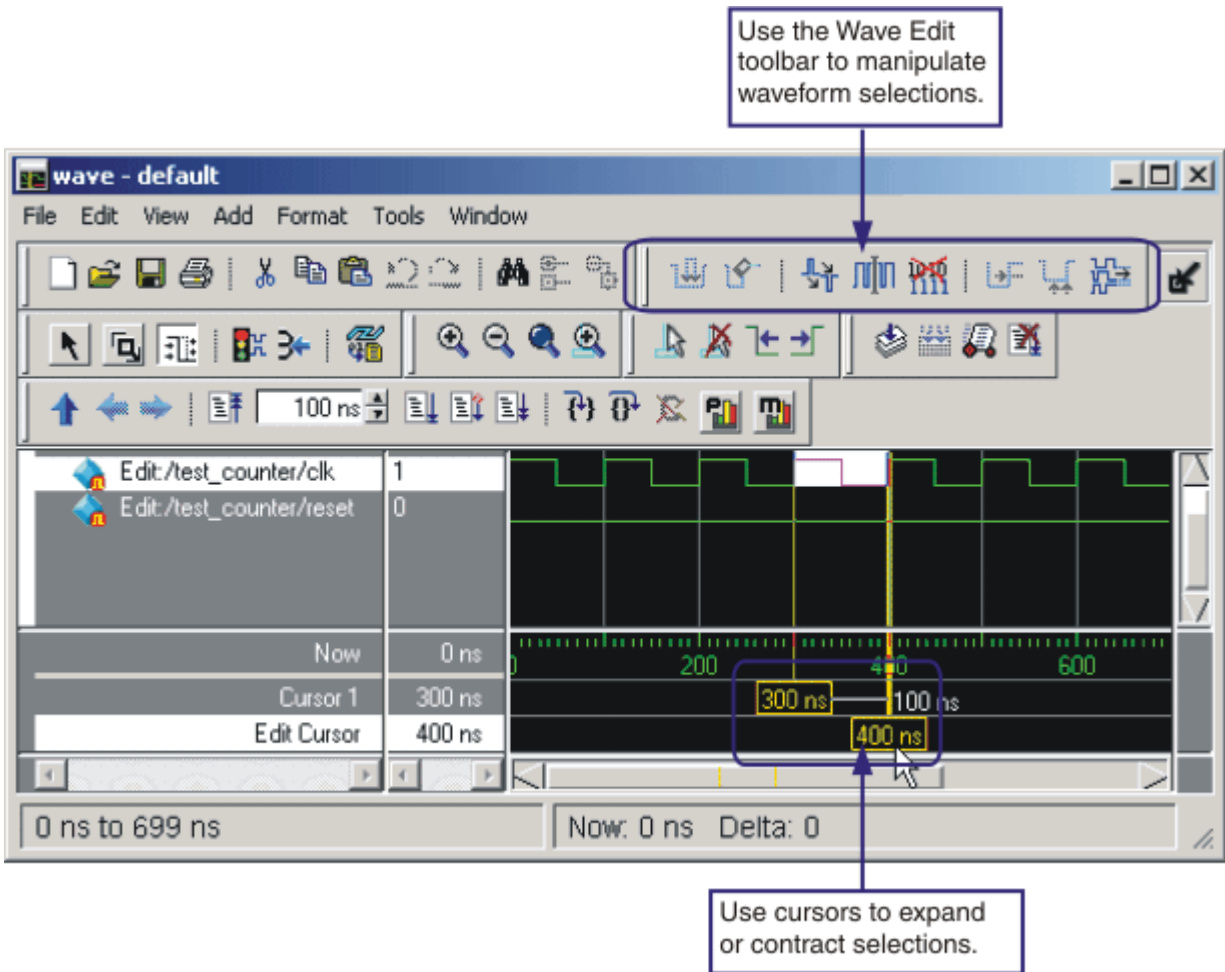
Selecting Parts of the Waveform

There are several methods for selecting edges or sections of a waveform. The table and graphic below describe the various options.

Table 23-3. Selecting Parts of the Waveform

Action	Method
Select a waveform edge	Click on or just to the right of the waveform edge
Select a section of the waveform	Click-and-drag the mouse pointer in the waveform pane
Select a section of multiple waveforms	Click-and-drag the mouse pointer while holding the <Shift> key
Extend/contract the selection size	Drag a cursor in the cursor pane
Extend/contract selection from edge-to-edge	Click Next Transition/Previous Transition icons after selecting section

Figure 23-5. Manipulating Waveforms with the Wave Edit Toolbar and Cursors



Selection and Zoom Percentage

You may find that you cannot select the exact range you want because the mouse moves more than one unit of simulation time (for example, 228 ns to 230 ns). If this happens, zoom in on the Wave display (see [Zooming the Wave Window Display](#)), and you should be able to select the range you want.

Auto Snapping of the Cursor

When you click just to the right of a waveform edge in the waveform pane, the cursor automatically "snaps" to the nearest edge. This behavior is controlled by the Snap Distance setting in the Wave window preferences dialog.

Stretching and Moving Edges

There are mouse and keyboard shortcuts for moving and stretching edges:

Table 23-4. Wave Editor Mouse/Keyboard Shortcuts

Action	Mouse/keyboard shortcut
Stretch an edge	Hold the <Ctrl> key and drag the edge
Move an edge	Hold the <Ctrl> key and drag the edge with the 2nd (middle) mouse button

Here are some points to keep in mind about stretching and moving edges:

- If you stretch an edge forward, more waveform is inserted at the beginning of simulation time.
- If you stretch an edge backward, waveform is deleted at the beginning of simulation time.
- If you move an edge past another edge, either forward or backward, the edge you moved past is deleted.

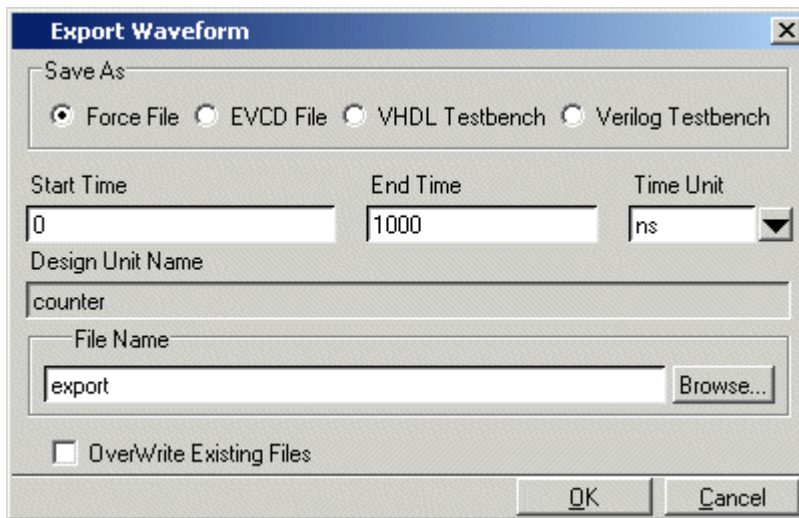
Simulating Directly from Waveform Editor

You need not save the waveforms in order to use them as stimulus for a simulation. Once you have configured all the waveforms, you can run the simulation as normal by selecting **Simulate > Start Simulation** in the Main window or using the `vsim` command. ModelSim automatically uses the created waveforms as stimulus for the simulation. Furthermore, while running the simulation you can continue editing the waveforms to modify the stimulus for the part of the simulation yet to be completed.

Exporting Waveforms to a Stimulus File

Once you have created and edited the waveforms, you can save the data to a stimulus file that can be used to drive a simulation now or at a later time. To save the waveform data, select **File > Export > Waveform** or use the `wave export` command.

Figure 23-6. Export Waveform Dialog



You can save the waveforms in four different formats:

Table 23-5. Formats for Saving Waveforms

Format	Description
Force format	Creates a Tcl script that contains force commands necessary to recreate the waveforms; source the file when loading the simulation as described under Driving Simulation with the Saved Stimulus File
EVCD format	Creates an extended VCD file which can be reloaded using the Import > EVCD File command or can be used with the -vcdstim argument to vsim to simulate the design
VHDL Testbench	Creates a VHDL architecture that you load as the top-level design unit
Verilog Testbench	Creates a Verilog module that you load as the top-level design unit

Driving Simulation with the Saved Stimulus File

The method for loading the stimulus file depends upon what type of format you saved. In each of the following examples, assume that the top-level of your block is named "top" and you saved the waveforms to a stimulus file named "mywaves" with the default extension.

Table 23-6. Examples for Loading a Stimulus File

Format	Loading example
Force format	<code>vsim top -do mywaves.do</code>

Table 23-6. Examples for Loading a Stimulus File (cont.)

Format	Loading example
Extended VCD format ¹	<code>vsim top -vcdstim mywaves.vcd</code>
VHDL Testbench	<code>vcom mywaves.vhd</code> <code>vsim mywaves</code>
Verilog Testbench	<code>vlog mywaves.v</code> <code>vsim mywaves</code>

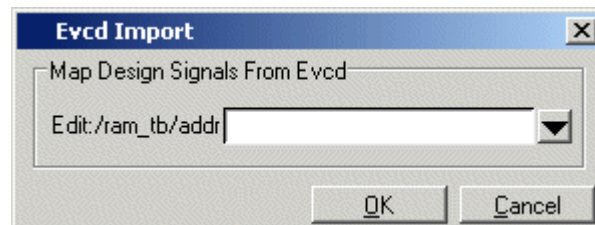
1. You can also use the **Import > EVCD** command from the Wave window. See below for more details on working with EVCD files.

Signal Mapping and Importing EVCD Files

When you import a previously saved EVCD file, ModelSim attempts to map the signals in the EVCD file to the signals in the loaded design. It matches signals based on name and width.

If ModelSim can't map the signals automatically, you can do the mapping yourself by selecting one or more signals, right-clicking a selected signal, and then selecting Map to Design Signal.

Figure 23-7. Evcd Import Dialog



Select a signal from the drop-down arrow and click OK. You will repeat this process for each signal you selected.

Note



This command works only with extended VCD files created with ModelSim.

Using Waveform Compare with Created Waveforms

The Waveform Compare feature compares two or more waveforms and displays the differences in the Wave window (see [Waveform Compare](#) for details). This feature can be used in tandem with Waveform Editor. The combination is most useful in situations where you know the expected output of a signal and want to compare visually the differences between expected output and simulated output.

The basic procedure for using the two features together is as follows:

- Create a waveform based on the signal of interest with a drive type of expected output
- Add the design signal of interest to the Wave window and then run the design
- Start a comparison and use the created waveform as the reference dataset for the comparison. Use the text "Edit" to designate a create waveform as the reference dataset. For example:

```
compare start Edit sim  
compare add -wave /test_counter/count  
compare run
```

Saving the Waveform Editor Commands

When you create and edit waveforms in the Wave window, ModelSim tracks the underlying Tcl commands and reports them to the transcript. You can save those commands to a DO file that can be run at a later time to recreate the waveforms.

To save your waveform editor commands, select **File > Save**.

Chapter 24

Standard Delay Format (SDF) Timing Annotation

This chapter covers the ModelSim implementation of SDF (Standard Delay Format) timing annotation. Included are sections on VITAL SDF and Verilog SDF, plus troubleshooting.

Verilog and VHDL VITAL timing data can be annotated from SDF files by using the simulator's built-in SDF annotator.

ASIC and FPGA vendors usually provide tools that create SDF files for use with their cell libraries. Refer to your vendor's documentation for details on creating SDF files for your library. Many vendors also provide instructions on using their SDF files and libraries with ModelSim.

The SDF specification was originally created for Verilog designs, but it has also been adopted for VHDL VITAL designs. In general, the designer does not need to be familiar with the details of the SDF specification because the cell library provider has already supplied tools that create SDF files that match their libraries.

Note



ModelSim can read SDF files that were compressed using gzip. Other compression formats (for example, Unix zip) are not supported.

Specifying SDF Files for Simulation

ModelSim supports SDF versions 1.0 through 4.0 (IEEE 1497), except the NETDELAY and LABEL statements. The simulator's built-in SDF annotator automatically adjusts to the version of the file. Use the following `vsim` command line options to specify the SDF files, the desired timing values, and their associated design instances:

```
-sdfmin [<instance>=]<filename>  
-sdftyp [<instance>=]<filename>  
-sdfmax [<instance>=]<filename>
```

Any number of SDF files can be applied to any instance in the design by specifying one of the above options for each file. Use **-sdfmin** to select minimum, **-sdftyp** to select typical, and **-sdfmax** to select maximum timing values from the SDF file.

Instance Specification

The instance paths in the SDF file are relative to the instance to which the SDF is applied. Usually, this instance is an ASIC or FPGA model instantiated under a test bench. For example, to annotate maximum timing values from the SDF file *myasic.sdf* to an instance *u1* under a top-level named *testbench*, invoke the simulator as follows:

```
vsim -sdfmax /testbench/u1=myasic.sdf testbench
```

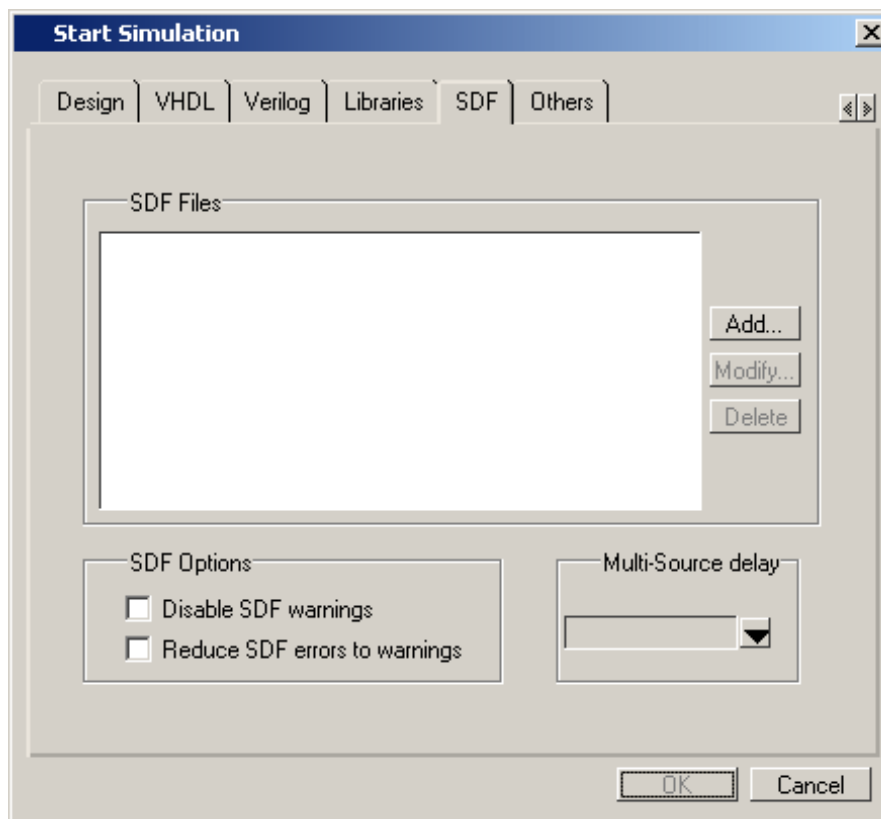
If the instance name is omitted then the SDF file is applied to the top-level. *This is usually incorrect* because in most cases the model is instantiated under a test bench or within a larger system level simulation. In fact, the design can have several models, each having its own SDF file. In this case, specify an SDF file for each instance. For example,

```
vsim -sdfmax /system/u1=asic1.sdf -sdfmax /system/u2=asic2.sdf system
```

SDF Specification with the GUI

As an alternative to the command line options, you can specify SDF files in the **Start Simulation** dialog box under the SDF tab.

Figure 24-1. SDF Tab in Start Simulation Dialog



You can access this dialog by invoking the simulator without any arguments or by selecting **Simulate > Start Simulation**.

For Verilog designs, you can also specify SDF files by using the `$sdf_annotate` system task. See [\\$sdf_annotate](#) for more details.

Errors and Warnings

Errors issued by the SDF annotator while loading the design prevent the simulation from continuing, whereas warnings do not.

- Use either the `-sdfnoerror` or the `+nosdferror` option with `vsim` to change SDF errors to warnings so that the simulation can continue.
- Use either the `-sdfnowarn` or the `+nosdfwarn` option with `vsim` to suppress warning messages.

Another option is to use the **SDF** tab from the **Start Simulation** dialog box (Figure 24-1). Select **Disable SDF warnings** (`-sdfnowarn +nosdfwarn`) to disable warnings, or select **Reduce SDF errors to warnings** (`-sdfnoerror`) to change errors to warnings.

See [Troubleshooting](#) for more information on errors and warnings and how to avoid them.

Compiling SDF Files

The `sdfcom` command compiles SDF files. Compiled SDF can be annotated to Verilog and VHDL regions, including those regions hierarchically underneath SystemC modules. However, compiled SDF cannot be targeted to a SystemC node directly (even if the intended annotation objects underneath the SystemC node are Verilog and/or VHDL).

In situations where the same SDF file is used for multiple simulation runs, the elaboration time will be reduced significantly.

Note



When compiled SDF files are used, the annotator behaves as if the `-v2k_int_delays` switch for the `vsim` command has been specified.

Simulating with Compiled SDF Files

Compiled SDF files may be specified on the `vsim` line with the `-sdfmin`, `-sdftyp`, and `-sdfmax` arguments. Alternatively, they may be specified as the filename in a `$sdf_annotate()` system task in the Verilog source.

Using \$sdf_annotate() with Compiled SDF

The following limitations exist when using compiled SDF files with \$sdf_annotate():

- The \$sdf_annotate() call cannot be made from a delayed initial block:

```
initial #10 $sdf_annotate(...); // Not allowed
```

- The \$sdf_annotate() call cannot be made from an if statement:

```
reg doSdf = 1'b1;
initial begin
    if (doSdf) $sdf_annotate(...); // Not allowed
end
```

- If the annotation order of multiple \$sdf_annotate() calls is important, you must have all of them in a single initial block.

VHDL VITAL SDF

VHDL SDF annotation works on VITAL cells only. The IEEE 1076.4 VITAL ASIC Modeling Specification describes how cells must be written to support SDF annotation. Once again, the designer does not need to know the details of this specification because the library provider has already written the VITAL cells and tools that create compatible SDF files. However, the following summary may help you understand simulator error messages. For additional VITAL specification information, see [VITAL Usage and Compliance](#).

SDF to VHDL Generic Matching

An SDF file contains delay and timing constraint data for cell instances in the design. The annotator must locate the cell instances and the placeholders (VHDL generics) for the timing data. Each type of SDF timing construct is mapped to the name of a generic as specified by the VITAL modeling specification. The annotator locates the generic and updates it with the timing value from the SDF file. It is an error if the annotator fails to find the cell instance or the named generic. The following are examples of SDF constructs and their associated generic names:

Table 24-1. Matching SDF to VHDL Generics

SDF construct	Matching VHDL generic name
(IOPATH a y (3))	tpd_a_y
(IOPATH (posedge clk) q (1) (2))	tpd_clk_q_posedge
(INTERCONNECT u1/y u2/a (5))	tipd_a
(SETUP d (posedge clk) (5))	tsetup_d_clk_noedge_posedge
(HOLD (negedge d) (posedge clk) (5))	thold_d_clk_negedge_posedge
(SETUPHOLD d clk (5) (5))	tsetup_d_clk & thold_d_clk

Table 24-1. Matching SDF to VHDL Generics (cont.)

SDF construct	Matching VHDL generic name
(WIDTH (COND (reset==1'b0) clk) (5))	tpw_clk_reset_eq_0

The SDF statement CONDELSE, when targeted for Vital cells, is annotated to a **tpd** generic of the form **tpd_<inputPort>_<outputPort>**.

Resolving Errors

If the simulator finds the cell instance but not the generic then an error message is issued. For example,

```
** Error (vsim-SDF-3240) myasic.sdf(18):
Instance '/testbench/dut/u1' does not have a generic named 'tpd_a_y'
```

In this case, make sure that the design is using the appropriate VITAL library cells. If it is, then there is probably a mismatch between the SDF and the VITAL cells. You need to find the cell instance and compare its generic names to those expected by the annotator. Look in the VHDL source files provided by the cell library vendor.

If none of the generic names look like VITAL timing generic names, then perhaps the VITAL library cells are not being used. If the generic names do look like VITAL timing generic names but don't match the names expected by the annotator, then there are several possibilities:

- The vendor's tools are not conforming to the VITAL specification.
- The SDF file was accidentally applied to the wrong instance. In this case, the simulator also issues other error messages indicating that cell instances in the SDF could not be located in the design.
- The vendor's library and SDF were developed for the older VITAL 2.2b specification. This version uses different name mapping rules. In this case, invoke **vsim** with the **-vital2.2b** option:

```
vsim -vital2.2b -sdfmax /testbench/u1=myasic.sdf testbench
```

For more information on resolving errors see [Troubleshooting](#).

Verilog SDF

Verilog designs can be annotated using either the simulator command line options or the **\$sdf_annotate** system task (also commonly used in other Verilog simulators). The command line options annotate the design immediately after it is loaded, but before any simulation events take place. The **\$sdf_annotate** task annotates the design at the time it is called in the Verilog source code. This provides more flexibility than the command line options.

\$sdf_annotate

Syntax

```
$sdf_annotate  
  ["<sdffile>"], [<instance>], ["<config_file>"], ["<log_file>"], ["<mtm_spec>"],  
  ["<scale_factor>"], ["<scale_type>"]];
```

Arguments

- "<sdffile>"
String that specifies the SDF file. Required.
- <instance>
Hierarchical name of the instance to be annotated. Optional. Defaults to the instance where the \$sdf_annotate call is made.
- "<config_file>"
String that specifies the configuration file. Optional. Currently not supported, this argument is ignored.
- "<log_file>"
String that specifies the logfile. Optional. Currently not supported, this argument is ignored.
- "<mtm_spec>"
String that specifies the delay selection. Optional. The allowed strings are "minimum", "typical", "maximum", and "tool_control". Case is ignored and the default is "tool_control". The "tool_control" argument means to use the delay specified on the command line by +mindelays, +typdelays, or +maxdelays (defaults to +typdelays).
- "<scale_factor>"
String that specifies delay scaling factors. Optional. The format is "<min_mult>:<typ_mult>:<max_mult>". Each multiplier is a real number that is used to scale the corresponding delay in the SDF file.
- "<scale_type>"
String that overrides the <mtm_spec> delay selection. Optional. The <mtm_spec> delay selection is always used to select the delay scaling factor, but if a <scale_type> is specified, then it will determine the min/typ/max selection from the SDF file. The allowed strings are "from_min", "from_minimum", "from_typ", "from_typical", "from_max", "from_maximum", and "from_mtm". Case is ignored, and the default is "from_mtm", which means to use the <mtm_spec> value.

Examples

Optional arguments can be omitted by using commas or by leaving them out if they are at the end of the argument list. For example, to specify only the SDF file and the instance to which it applies:

```
$sdf_annotate("myasic.sdf", testbench.u1);
```

To also specify maximum delay values:

```
$sdf_annotate("myasic.sdf", testbench.u1, , , "maximum");
```

SDF to Verilog Construct Matching

The annotator matches SDF constructs to corresponding Verilog constructs in the cells. Usually, the cells contain path delays and timing checks within specify blocks. For each SDF construct, the annotator locates the cell instance and updates each specify path delay or timing check that matches. An SDF construct can have multiple matches, in which case each matching specify statement is updated with the SDF timing value. SDF constructs are matched to Verilog constructs as follows.

- **IOPATH** is matched to specify path delays or primitives:

Table 24-2. Matching SDF IOPATH to Verilog

SDF	Verilog
(IOPATH (posedge clk) q (3) (4))	(posedge clk => q) = 0;
(IOPATH a y (3) (4))	buf u1 (y, a);

The IOPATH construct usually annotates path delays. If ModelSim can't locate a corresponding specify path delay, it returns an error unless you use the +sdf_iopath_to_prim_ok argument to **vsim**. If you specify that argument and the module contains no path delays, then all primitives that drive the specified output port are annotated.

- **INTERCONNECT** and **PORT** are matched to input ports:

Table 24-3. Matching SDF INTERCONNECT and PORT to Verilog

SDF	Verilog
(INTERCONNECT u1.y u2.a (5))	input a;
(PORT u2.a (5))	inout a;

Both of these constructs identify a module input or inout port and create an internal net that is a delayed version of the port. This is called a Module Input Port Delay (MIPD). All primitives, specify path delays, and specify timing checks connected to the original port are reconnected to the new MIPD net.

- **PATHPULSE** and **GLOBALPATHPULSE** are matched to specify path delays:

Table 24-4. Matching SDF PATHPULSE and GLOBALPATHPULSE to Verilog

SDF	Verilog
(PATHPULSE a y (5) (10))	(a => y) = 0;
(GLOBALPATHPULSE a y (30) (60))	(a => y) = 0;

If the input and output ports are omitted in the SDF, then all path delays are matched in the cell.

- **DEVICE** is matched to primitives or specify path delays:

Table 24-5. Matching SDF DEVICE to Verilog

SDF	Verilog
(DEVICE y (5))	and u1(y, a, b);
(DEVICE y (5))	(a => y) = 0; (b => y) = 0;

If the SDF cell instance is a primitive instance, then that primitive's delay is annotated. If it is a module instance, then all specify path delays are annotated that drive the output port specified in the DEVICE construct (all path delays are annotated if the output port is omitted). If the module contains no path delays, then all primitives that drive the specified output port are annotated (or all primitives that drive any output port if the output port is omitted).

SETUP is matched to \$setup and \$setuphold:

Table 24-6. Matching SDF SETUP to Verilog

SDF	Verilog
(SETUP d (posedge clk) (5))	\$setup(d, posedge clk, 0);
(SETUP d (posedge clk) (5))	\$setuphold(posedge clk, d, 0, 0);

- **HOLD** is matched to \$hold and \$setuphold:

Table 24-7. Matching SDF HOLD to Verilog

SDF	Verilog
(HOLD d (posedge clk) (5))	\$hold(posedge clk, d, 0);
(HOLD d (posedge clk) (5))	\$setuphold(posedge clk, d, 0, 0);

- **SETUPHOLD** is matched to \$setup, \$hold, and \$setuphold:

Table 24-8. Matching SDF SETUPHOLD to Verilog

SDF	Verilog
(SETPHOLD d (posedge clk) (5) (5))	\$setup(d, posedge clk, 0);
(SETPHOLD d (posedge clk) (5) (5))	\$hold(posedge clk, d, 0);
(SETPHOLD d (posedge clk) (5) (5))	\$setuphold(posedge clk, d, 0, 0);

- **RECOVERY** is matched to \$recovery:

Table 24-9. Matching SDF RECOVERY to Verilog

SDF	Verilog
(RECOVERY (negedge reset) (posedge clk) (5))	\$recovery(negedge reset, posedge clk, 0);

- **REMOVAL** is matched to \$removal:

Table 24-10. Matching SDF REMOVAL to Verilog

SDF	Verilog
(REMOVAL (negedge reset) (posedge clk) (5))	\$removal(negedge reset, posedge clk, 0);

- **RECREM** is matched to \$recovery, \$removal, and \$crem:

Table 24-11. Matching SDF RECREM to Verilog

SDF	Verilog
(RECREM (negedge reset) (posedge clk) (5) (5))	\$recovery(negedge reset, posedge clk, 0);
(RECREM (negedge reset) (posedge clk) (5) (5))	\$removal(negedge reset, posedge clk, 0);
(RECREM (negedge reset) (posedge clk) (5) (5))	\$crem(negedge reset, posedge clk, 0);

- **SKEW** is matched to \$skew:

Table 24-12. Matching SDF SKEW to Verilog

SDF	Verilog
(SKEW (posedge clk1) (posedge clk2) (5))	\$skew(posedge clk1, posedge clk2, 0);

- **WIDTH** is matched to \$width:

Table 24-13. Matching SDF WIDTH to Verilog

SDF	Verilog
(WIDTH (posedge clk) (5))	\$width(posedge clk, 0);

- **PERIOD** is matched to \$period:

Table 24-14. Matching SDF PERIOD to Verilog

SDF	Verilog
(PERIOD (posedge clk) (5))	\$period(posedge clk, 0);

- **NOCHANGE** is matched to \$nochange:

Table 24-15. Matching SDF NOCHANGE to Verilog

SDF	Verilog
(NOCHANGE (negedge write) addr (5) (5))	\$nochange(negedge write, addr, 0, 0);

To see complete mappings of SDF and Verilog constructs, please consult IEEE Standard 1364-2005, Chapter 16 - Back Annotation Using the Standard Delay Format (SDF).

Optional Edge Specifications

Timing check ports and path delay input ports can have optional edge specifications. The annotator uses the following rules to match edges:

- A match occurs if the SDF port does not have an edge.
- A match occurs if the specify port does not have an edge.
- A match occurs if the SDF port edge is identical to the specify port edge.
- A match occurs if explicit edge transitions in the specify port edge overlap with the SDF port edge.

These rules allow SDF annotation to take place even if there is a difference between the number of edge-specific constructs in the SDF file and the Verilog specify block. For example, the Verilog specify block may contain separate setup timing checks for a falling and rising edge on data with respect to clock, while the SDF file may contain only a single setup check for both edges:

Table 24-16. Matching Verilog Timing Checks to SDF SETUP

SDF	Verilog
(SETUP data (posedge clock) (5))	\$setup(posedge data, posedge clk, 0);
(SETUP data (posedge clock) (5))	\$setup(negedge data, posedge clk, 0);

In this case, the cell accommodates more accurate data than can be supplied by the tool that created the SDF file, and both timing checks correctly receive the same value.

Likewise, the SDF file may contain more accurate data than the model can accommodate.

Table 24-17. SDF Data May Be More Accurate Than Model

SDF	Verilog
(SETUP (posedge data) (posedge clock) (4))	\$setup(data, posedge clk, 0);
(SETUP (negedge data) (posedge clock) (6))	\$setup(data, posedge clk, 0);

In this case, both SDF constructs are matched and the timing check receives the value from the last one encountered.

Timing check edge specifiers can also use explicit edge transitions instead of posedge and negedge. However, the SDF file is limited to posedge and negedge. For example,

Table 24-18. Matching Explicit Verilog Edge Transitions to Verilog

SDF	Verilog
(SETUP data (posedge clock) (5))	\$setup(data, edge[01, 0x] clk, 0);

The explicit edge specifiers are 01, 0x, 10, 1x, x0, and x1. The set of [01, 0x, x1] is equivalent to posedge, while the set of [10, 1x, x0] is equivalent to negedge. A match occurs if any of the explicit edges in the specify port match any of the explicit edges implied by the SDF port.

Optional Conditions

Timing check ports and path delays can have optional conditions. The annotator uses the following rules to match conditions:

- A match occurs if the SDF does not have a condition.
- A match occurs for a timing check if the SDF port condition is semantically equivalent to the specify port condition.
- A match occurs for a path delay if the SDF condition is lexically identical to the specify condition.

Timing check conditions are limited to very simple conditions, therefore the annotator can match the expressions based on semantics. For example,

Table 24-19. SDF Timing Check Conditions

SDF	Verilog
(SETUP data (COND (reset!=1) (posedge clock)) (5))	\$setup(data, posedge clk &&& (reset==0),0);

The conditions are semantically equivalent and a match occurs. In contrast, path delay conditions may be complicated and semantically equivalent conditions may not match. For example,

Table 24-20. SDF Path Delay Conditions

SDF	Verilog
(COND (r1 r2) (IOPATH clk q (5)))	if (r1 r2) (clk => q) = 5; // matches
(COND (r1 r2) (IOPATH clk q (5)))	if (r2 r1) (clk => q) = 5; // does not match

The annotator does not match the second condition above because the order of r1 and r2 are reversed.

Rounded Timing Values

The SDF **TIMESCALE** construct specifies time units of values in the SDF file. The annotator rounds timing values from the SDF file to the time precision of the module that is annotated. For example, if the SDF **TIMESCALE** is 1ns and a value of .016 is annotated to a path delay in a module having a time precision of 10ps (from the timescale directive), then the path delay receives a value of 20ps. The SDF value of 16ps is rounded to 20ps. Interconnect delays are rounded to the time precision of the module that contains the annotated MIPD.

SDF for Mixed VHDL and Verilog Designs

Annotation of a mixed VHDL and Verilog design is very flexible. VHDL VITAL cells and Verilog cells can be annotated from the same SDF file. This flexibility is available only by using the simulator's SDF command line options. The Verilog \$sdf_annotate system task can annotate Verilog cells only. See the [vsim](#) command for more information on SDF command line options.

Interconnect Delays

An interconnect delay represents the delay from the output of one device to the input of another. ModelSim can model single interconnect delays or multisource interconnect delays for Verilog, VHDL/VITAL, or mixed designs. See the [vsim](#) command for more information on the relevant command line arguments.

Timing checks are performed on the interconnect delayed versions of input ports. This may result in misleading timing constraint violations, because the ports may satisfy the constraint while the delayed versions may not. If the simulator seems to report incorrect violations, be sure to account for the effect of interconnect delays.

Disabling Timing Checks

ModelSim offers a number of options for disabling timing checks on a global or individual basis. The table below provides a summary of those options. See the command and argument descriptions in the Reference Manual for more details.

Table 24-21. Disabling Timing Checks

Command and argument	Effect
<code>tcheck_set</code>	modifies reporting or X generation status on one or more timing checks
<code>tcheck_status</code>	prints to the Transcript the current status of one or more timing checks
vlog +notimingchecks	disables timing check system tasks for all instances in the specified Verilog design
vlog +nospecify	disables specify path delays and timing checks for all instances in the specified Verilog design
vopt +notimingchecks	removes all timing check entries from the design as it is parsed; fixes the TimingChecksOn generic for all Vital models to FALSE; As a consequence, using vsim +notimingchecks at simulation may not have any effect on the simulation depending on the optimization of the model.
vsim +no_neg_tchk	disables negative timing check limits by setting them to zero for all instances in the specified design
vsim +no_notifier	disables the toggling of the notifier register argument of the timing check system tasks for all instances in the specified design
vsim +no_tchk_msg	disables error messages issued by timing check system tasks when timing check violations occur for all instances in the specified design
vsim +notimingchecks	disables Verilog and VITAL timing checks for all instances in the specified design; sets generic TimingChecksOn to FALSE for all VHDL Vital models with the Vital_level0 or Vital_level1 attribute. Setting this generic to FALSE disables the actual calls to the timing checks along with anything else that is present in the model's timing check block.
vsim +nospecify	disables specify path delays and timing checks for all instances in the specified design

Troubleshooting

Specifying the Wrong Instance

By far, the most common mistake in SDF annotation is to specify the wrong instance to the simulator's SDF options. The most common case is to leave off the instance altogether, which is the same as selecting the top-level design unit. This is generally wrong because the instance paths in the SDF are relative to the ASIC or FPGA model, which is usually instantiated under a top-level test bench. See [Instance Specification](#) for an example.

Simple examples for both a VHDL and a Verilog test bench are provided below. For simplicity, these test bench examples do nothing more than instantiate a model that has no ports.

VHDL Test Bench

```
entity testbench is end;  
architecture only of testbench is  
    component myasic  
    end component;  
begin  
    dut : myasic;  
end;
```

Verilog Test Bench

```
module testbench;  
    myasic dut();  
endmodule
```

The name of the model is *myasic* and the instance label is *dut*. For either test bench, an appropriate simulator invocation might be:

```
vsim -sdfmax /testbench/dut=myasic.sdf testbench
```

Optionally, you can leave off the name of the top-level:

```
vsim -sdfmax /dut=myasic.sdf testbench
```

The important thing is to select the instance for which the SDF is intended. If the model is deep within the design hierarchy, an easy way to find the instance name is to first invoke the simulator without SDF options, view the structure pane, navigate to the model instance, select it, and enter the [environment](#) command. This command displays the instance name that should be used in the SDF command line option.

Matching a Single Timing Check

SDF annotation of `RECREM` or `SETUPHOLD` matching only a single setup, hold, recovery, or removal timing check will result in a Warning message.

Mistaking a Component or Module Name for an Instance Label

Another common error is to specify the component or module name rather than the instance label. For example, the following invocation is wrong for the above test benches:

```
vsim -sdfmax /testbench/myasic=myasic.sdf testbench
```

This results in the following error message:

```
** Error (vsim-SDF-3250) myasic.sdf(0):  
Failed to find INSTANCE '/testbench/myasic'.
```

Forgetting to Specify the Instance

If you leave off the instance altogether, then the simulator issues a message for each instance path in the SDF that is not found in the design. For example,

```
vsim -sdfmax myasic.sdf testbench
```

Results in:

```
** Error (vsim-SDF-3250) myasic.sdf(0):  
Failed to find INSTANCE '/testbench/u1'  
** Error (vsim-SDF-3250) myasic.sdf(0):  
Failed to find INSTANCE '/testbench/u2'  
** Error (vsim-SDF-3250) myasic.sdf(0):  
Failed to find INSTANCE '/testbench/u3'  
** Error (vsim-SDF-3250) myasic.sdf(0):  
Failed to find INSTANCE '/testbench/u4'  
** Error (vsim-SDF-3250) myasic.sdf(0):  
Failed to find INSTANCE '/testbench/u5'  
** Warning (vsim-SDF-3432) myasic.sdf:  
This file is probably applied to the wrong instance.  
** Warning (vsim-SDF-3432) myasic.sdf:  
Ignoring subsequent missing instances from this file.
```

After annotation is done, the simulator issues a summary of how many instances were not found and possibly a suggestion for a qualifying instance:

```
** Warning (vsim-SDF-3440) myasic.sdf:  
Failed to find any of the 358 instances from this file.  
** Warning (vsim-SDF-3442) myasic.sdf:  
Try instance '/testbench/dut'. It contains all instance paths from this  
file.
```

The simulator recommends an instance only if the file was applied to the top-level and a qualifying instance is found one level down.

Also see [Resolving Errors](#) for specific VHDL VITAL SDF troubleshooting.

Chapter 25

Value Change Dump (VCD) Files

The Value Change Dump (VCD) file format is supported for use by ModelSim and is specified in the IEEE 1364-2005 standard. A VCD file is an ASCII file that contains information about value changes on selected variables in the design stored by VCD system tasks. This includes header information, variable definitions, and variable value changes.

VCD is in common use for Verilog designs and is controlled by VCD system task calls in the Verilog source code. ModelSim provides equivalent commands for these system tasks and extends VCD support to SystemC and VHDL designs. You can use these ModelSim VCD commands on Verilog, VHDL, SystemC, or mixed designs.

Extended VCD supports Verilog and VHDL ports in a mixed-language design containing SystemC. However, extended VCD does not support SystemC ports in a mixed-language design.

If you need vendor-specific ASIC design-flow documentation that incorporates VCD, contact your ASIC vendor.

Creating a VCD File

ModelSim provides two general methods for creating a VCD file:

- **Four-State VCD File** — produces a four-state VCD file with variable changes in 0, 1, x, and z with no strength information.
- **Extended VCD File** — produces an extended VCD file with variable changes in all states and strength information and port driver data.

Both methods also capture port driver changes unless you filter them out with optional command-line arguments.

Four-State VCD File

First, compile and load the design:

```
% cd <installDir>/examples/tutorials/verilog/basicSimulation
% vlib work
% vlog counter.v tcounter.v
% vopt test_counter +acc -o test_counter_opt
% vsim test_counter_opt
```

Next, with the design loaded, specify the VCD file name with the `vcd file` command and add objects to the file with the `vcd add` command:

```
VSIM 1> vcd file myvcdfile.vcd
VSIM 2> vcd add /test_counter/dut/*
VSIM 3> run
VSIM 4> quit -f
```

Upon quitting the simulation, there will be a VCD file in the working directory.

Extended VCD File

First, compile and load the design:

```
% cd <installDir>/examples/tutorials/verilog/basicSimulation
% vlib work
% vlog counter.v tcounter.v
% vopt test_counter +acc -o test_counter_opt
% vsim test_counter_opt
```

Next, with the design loaded, specify the VCD file name and objects to add with the `vcd dumpports` command:

```
VSIM 1> vcd dumpports -file myvcdfile.vcd /test_counter/dut/*
VSIM 3> run
VSIM 4> quit -f
```

Upon quitting the simulation, there will be an extended VCD file called *myvcdfile.vcd* in the working directory.

Note



There is an internal limit to the number of ports that can be listed with the `vcd dumpports` command. If that limit is reached, use the `vcd add` command with the `-dumpports` option to name additional ports.

Case Sensitivity

Verilog designs are case-sensitive, so ModelSim maintains case when it produces a VCD file. However, VHDL is not case-sensitive, so ModelSim converts all signal names to lower case when it produces a VCD file.

Checkpoint/Restore and Writing VCD Files

If a checkpoint occurs while ModelSim is writing a VCD file, the entire VCD file is copied into the checkpoint file. Since VCD files can be very large, it is possible that disk space problems may occur. Consequently, ModelSim issues a warning in this situation.

Using Extended VCD as Stimulus

You can use an extended VCD file as stimulus to re-simulate your design. There are two ways to do this:

1. Simulate the top level of a design unit with the input values from an extended VCD file.
2. Specify one or more instances in a design to be replaced with the output values from the associated VCD file.

Simulating with Input Values from a VCD File

When simulating with inputs from an extended VCD file, you can simulate only one design unit at a time. In other words, you can apply the VCD file inputs only to the top level of the design unit for which you captured port data.

The general procedure includes two steps:

1. Create a VCD file for a single design unit using the `vcd dumpports` command.
2. Resimulate the single design unit using the `-vcdstim` argument to `vsim`. Note that `-vcdstim` works only with VCD files that were created by a ModelSim simulation.

Example 25-1. Verilog Counter

First, create the VCD file for the single instance using `vcd dumpports`:

```
% cd <installDir>/examples/tutorials/verilog/basicSimulation
% vlib work
% vlog counter.v tcounter.v
% vopt test_counter +acc -o test_counter_opt
% vsim test_counter_opt +dumpports+nocollapse
VSIM 1> vcd dumpports -file counter.vcd /test_counter/dut/*
VSIM 2> run
VSIM 3> quit -f
```

Next, rerun the counter without the test bench, using the `-vcdstim` argument:

```
% vsim -vcdstim counter.vcd counter
VSIM 1> add wave /*
VSIM 2> run 200
```

Example 25-2. VHDL Adder

First, create the VCD file using `vcd dumpports`:

```
% cd <installDir>/examples/misc
% vlib work
% vcom gates.vhd adder.vhd stimulus.vhd
% vopt testbench2 +acc -o testbench2_opt
% vsim testbench2_opt +dumpports+nocollapse
VSIM 1> vcd dumpports -file addern.vcd /testbench2/uut/*
VSIM 2> run 1000
VSIM 3> quit -f
```

Next, rerun the adder without the test bench, using the **-vcdstim** argument:

```
% vsim -vcdstim addern.vcd addern -gn=8 -do "add wave /*; run 1000"
```

Example 25-3. Mixed-HDL Design

First, create three VCD files, one for each module:

```
% cd <installDir>/examples/tutorials/mixed/projects
% vlib work
% vlog cache.v memory.v proc.v
% vcom util.vhd set.vhd top.vhd
% vopt top +acc -o top_opt
% vsim top_opt +dumpports+nocollapse
VSIM 1> vcd dumpports -file proc.vcd /top/p/*
VSIM 2> vcd dumpports -file cache.vcd /top/c/*
VSIM 3> vcd dumpports -file memory.vcd /top/m/*
VSIM 4> run 1000
VSIM 5> quit -f
```

Next, rerun each module separately, using the captured VCD stimulus:

```
% vsim -vcdstim proc.vcd proc -do "add wave /*; run 1000"
VSIM 1> quit -f

% vsim -vcdstim cache.vcd cache -do "add wave /*; run 1000"
VSIM 1> quit -f

% vsim -vcdstim memory.vcd memory -do "add wave /*; run 1000"
VSIM 1> quit -f
```

Note



When using VCD files as stimulus, the VCD file format does not support recording of delta delay changes – delta delays are not captured and any delta delay ordering of signal changes is lost. Designs relying on this ordering may produce unexpected results.

Replacing Instances with Output Values from a VCD File

Replacing instances with output values from a VCD file lets you simulate without the instance's source or even the compiled object. The general procedure includes two steps:

1. Create VCD files for one or more instances in your design using the [vcd dumpports](#) command. If necessary, use the **-vcdstim** switch to handle port order problems (see below).

2. Re-simulate your design using the `-vcdstim <instance>=<filename>` argument to `vsim`. Note that this works only with VCD files that were created by a ModelSim simulation.

Example 25-4. Replacing Instances

In the following example, the three instances `/top/p`, `/top/c`, and `/top/m` are replaced in simulation by the output values found in the corresponding VCD files.

First, create VCD files for all instances you want to replace:

```
vcd dumpports -vcdstim -file proc.vcd /top/p/*
vcd dumpports -vcdstim -file cache.vcd /top/c/*
vcd dumpports -vcdstim -file memory.vcd /top/m/*
run 1000
```

Next, simulate your design and map the instances to the VCD files you created:

```
vsim top_opt -vcdstim /top/p=proc.vcd -vcdstim /top/c=cache.vcd
-vcdstim /top/m=memory.vcd
quit -f
```

Note



When using VCD files as stimulus, the VCD file format does not support recording of delta delay changes – delta delays are not captured and any delta delay ordering of signal changes is lost. Designs relying on this ordering may produce unexpected results.

Port Order Issues

The `-vcdstim` argument to the `vcd dumpports` command ensures the order that port names appear in the VCD file matches the order that they are declared in the instance's module or entity declaration. Consider the following module declaration:

```
module proc(clk, addr, data, rw, strb, rdy);
  input  clk, rdy;
  output addr, rw, strb;
  inout  data;
```

The order of the ports in the module line (`clk, addr, data, ...`) does not match the order of those ports in the input, output, and inout lines (`clk, rdy, addr, ...`). In this case the `-vcdstim` argument to the `vcd dumpports` command needs to be used.

In cases where the order is the same, you do not need to use the `-vcdstim` argument to `vcd dumpports`. Also, module declarations of the form:

```
module proc(input clk, output addr, inout data, ...)
```

do not require use of the argument.

VCD Commands and VCD Tasks

ModelSim VCD commands map to IEEE Std 1364 VCD system tasks and appear in the VCD file along with the results of those commands. The table below maps the VCD commands to their associated tasks.

Table 25-1. VCD Commands and SystemTasks

VCD commands	VCD system tasks
<code>vcd add</code>	<code>\$dumpvars</code>
<code>vcd checkpoint</code>	<code>\$dumpall</code>
<code>vcd file</code>	<code>\$dumpfile</code>
<code>vcd flush</code>	<code>\$dumpflush</code>
<code>vcd limit</code>	<code>\$dumplimit</code>
<code>vcd off</code>	<code>\$dumpoff</code>
<code>vcd on</code>	<code>\$dumpon</code>

ModelSim also supports extended VCD (dumpports system tasks). The table below maps the VCD dumpports commands to their associated tasks.

Table 25-2. VCD Dumpport Commands and System Tasks

VCD dumpports commands	VCD system tasks
<code>vcd dumpports</code>	<code>\$dumpports</code>
<code>vcd dumpportsall</code>	<code>\$dumpportsall</code>
<code>vcd dumpportsflush</code>	<code>\$dumpportsflush</code>
<code>vcd dumpportslimit</code>	<code>\$dumpportslimit</code>
<code>vcd dumpportsoff</code>	<code>\$dumpportsoff</code>
<code>vcd dumpportson</code>	<code>\$dumpportson</code>

ModelSim supports multiple VCD files. This functionality is an extension of the IEEE Std 1364-2005 specification. The tasks behave the same as the IEEE equivalent tasks such as `$dumpfile`, `$dumpvar`, and so forth. The difference is that `$dumpfile` can be called multiple times to create more than one VCD file, and the remaining tasks require a filename argument to associate their actions with a specific file.

Table 25-3. VCD Commands and System Tasks for Multiple VCD Files

VCD commands	VCD system tasks
<code>vcd add -file <filename></code>	<code>\$dumpvars</code>
<code>vcd checkpoint <filename></code>	<code>\$dumpall</code>

Table 25-3. VCD Commands and System Tasks for Multiple VCD Files (cont.)

VCD commands	VCD system tasks
<code>vcd files <filename></code>	<code>\$fdumpfile</code>
<code>vcd flush <filename></code>	<code>\$fdumpflush</code>
<code>vcd limit <filename></code>	<code>\$fdumplimit</code>
<code>vcd off <filename></code>	<code>\$fdumpoff</code>
<code>vcd on <filename></code>	<code>\$fdumpon</code>

Using VCD Commands with SystemC

VCD commands are supported for the following SystemC signals:

`sc_signal<T>`
`sc_signal_resolved`
`sc_signal_rv<N>`

VCD commands are supported for the following SystemC signal ports:

`sc_in<T>`
`sc_out<T>`
`sc_inout<T>`
`sc_in_resolved`
`sc_out_resolved`
`sc_inout_resolved`
`sc_in_rv<N>`
`sc_out_rv<N>`
`sc_inout_rv<N>`

<T> can be any of types shown in [Table 25-4](#).

Table 25-4. SystemC Types

unsigned char	char	sc_int
unsigned short	short	sc_uint
unsigned int	int	sc_bigint
unsigned long	float	sc_biguint
unsigned long long	double	sc_signed

Table 25-4. SystemC Types

	enum	sc_unsigned
		sc_logic
		sc_bit
		sc_bv
		sc_lv

Unsupported types are the SystemC fixed point types, class, structures and unions.

Compressing Files with VCD Tasks

ModelSim can produce compressed VCD files using the **gzip** compression algorithm. Since we cannot change the syntax of the system tasks, we act on the extension of the output file name. If you specify a .gz extension on the filename, ModelSim will compress the output.

VCD File from Source to Output

The following example shows the VHDL source, a set of simulator commands, and the resulting VCD output.

VHDL Source Code

The design is a simple shifter device represented by the following VHDL source code:

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity SHIFTER_MOD is
  port (CLK, RESET, data_in  : IN STD_LOGIC;
        Q : INOUT STD_LOGIC_VECTOR(8 downto 0));
END SHIFTER_MOD ;

architecture RTL of SHIFTER_MOD is
begin
  process (CLK,RESET)
  begin
    if (RESET = '1') then
      Q <= (others => '0') ;
    elsif (CLK'event and CLK = '1') then
      Q <= Q(Q'left - 1 downto 0) & data_in ;
    end if ;
  end process ;
end ;
```

VCD Simulator Commands

At simulator time zero, the designer executes the following commands:


```
vcd file output.vcd
vcd add -r *
force reset 1 0
force data_in 0 0
force clk 0 0
run 100
force clk 1 0, 0 50 -repeat 100
run 100
vcd off
force reset 0 0
force data_in 1 0
run 100
vcd on
run 850
force reset 1 0
run 50
vcd checkpoint
quit -sim
```

VCD Output

The VCD file created as a result of the preceding scenario would be called *output.vcd*. The following pages show how it would look.

```

$date                               $end                               #700
  Thu Sep 18                         #100                              1!
11:07:43 2003                       1!                                1(
$end                                  #150                              #750
$version                              0!                                0!
  <Tool> Version                      #200                              #800
<version>                            1!                                1!
$end                                  $dumpoff                          1'
$timescale                           x!                                #850
  1ns                                 x"                                0!
$end                                  x#                                #900
$scope module                         x$                                1!
shifter_mod $end                     x%                                1&
$var wire 1 ! clk                     x&                                #950
$end                                  x'                                0!
$var wire 1 " reset                   x(                                #1000
$end                                  x)                                1!
$var wire 1 # data_in                 x*                                1%
$end                                  x+                                #1050
$var wire 1 $ q [8]                   x,                                0!
$end                                  $end                              #1100
$var wire 1 % q [7]                   #300                              1!
$end                                  $dumpon                          1$
$var wire 1 & q [6]                   1!                                #1150
$end                                  0"                                0!
$var wire 1 ' q [5]                   1#                                1"
$end                                  0$                                0,
$var wire 1 ( q [4]                   0%                                0+
$end                                  0&                                0*
$var wire 1 ) q [3]                   0'                                0)
$end                                  0(                                0(
$var wire 1 * q [2]                   0)                                0'
$end                                  0*                                0&
$var wire 1 + q [1]                   0+                                0%
$end                                  1,                                0$
$var wire 1 , q [0]                   $end                              #1200
$end                                  #350                              1!
$upscope $end                        0!                                $dumpall
$enddefinitions $end                 #400                              1!
#0                                    1!                                1"
$dumpvars                             1+                                1#
0!                                    #450                              0$
1"                                    0!                                0%
0#                                    #500                              0&
0$                                    1!                                0'
0%                                    1*                                0(
0&                                    #550                              0)
0'                                    0!                                0*
0(                                    #600                              0+
0)                                    1!                                0,
0*                                    1)                                $end
0+                                    #650
0,                                    0!

```

VCD to WLF

The ModelSim `vcd2wlf` command is a utility that translates a `.vcd` file into a `.wlf` file that can be displayed in ModelSim using the `vsim -view` argument. This command only works on VCD files containing positive time values.

Capturing Port Driver Data

Some ASIC vendors' toolkits read a VCD file format that provides details on port drivers. This information can be used, for example, to drive a tester. For more information on a specific toolkit, refer to the ASIC vendor's documentation.

In ModelSim use the `vcd dumpports` command to create a VCD file that captures port driver data. Each time an external or internal port driver changes values, a new value change is recorded in the VCD file with the following format:

```
p<state> <0 strength> <1 strength> <identifier_code>
```

Driver States

Table 25-5 shows the driver states recorded as TSSI states if the direction is known.

Table 25-5. Driver States

Input (testfixture)	Output (dut)
D low	L low
U high	H high
N unknown	X unknown
Z tri-state	T tri-state
d low (two or more drivers active)	l low (two or more drivers active)
u high (two or more drivers active)	h high (two or more drivers active)

If the direction is unknown, the state will be recorded as one of the following:

Table 25-6. State When Direction is Unknown

Unknown direction
0 low (both input and output are driving low)
1 high (both input and output are driving high)
? unknown (both input and output are driving unknown)

Table 25-6. State When Direction is Unknown (cont.)

Unknown direction	
F	three-state (input and output unconnected)
A	unknown (input driving low and output driving high)
a	unknown (input driving low and output driving unknown)
B	unknown (input driving high and output driving low)
b	unknown (input driving high and output driving unknown)
C	unknown (input driving unknown and output driving low)
c	unknown (input driving unknown and output driving high)
f	unknown (input and output three-stated)

Driver Strength

The recorded 0 and 1 strength values are based on Verilog strengths:

Table 25-7. Driver Strength

Strength	VHDL std_logic mappings
0 highz	'Z'
1 small	
2 medium	
3 weak	
4 large	
5 pull	'W', 'H', 'L'
6 strong	'U', 'X', '0', '1', '-'
7 supply	

Identifier Code

The <identifier_code> is an integer preceded by < that starts at zero and is incremented for each port in the order the ports are specified. Also, the variable type recorded in the VCD header is "port".

Resolving Values

The resolved values written to the VCD file depend on which options you specify when creating the file.

Default Behavior

By default, ModelSim generates VCD output according to the *IEEE Standard for Verilog[®] Hardware Description Language*, IEEE 1364[™]-2005. This standard states that the values 0 (both input and output are active with value 0) and 1 (both input and output are active with value 1) are conflict states. The standard then defines two strength ranges:

- Strong: strengths 7, 6, and 5
- Weak: strengths 4, 3, 2, 1

The rules for resolving values are as follows:

- If the input and output are driving the same value with the same range of strength, the resolved value is 0 or 1, and the strength is the stronger of the two.
- If the input is driving a strong strength and the output is driving a weak strength, the resolved value is D, d, U or u, and the strength is the strength of the input.
- If the input is driving a weak strength and the output is driving a strong strength, the resolved value is L, l, H or h, and the strength is the strength of the output.

Extended Data Type for VHDL (vl_logic)

Mentor Graphics has created an additional VHDL data type for use in mixed-language designs, in case you need access to the full Verilog state set. The vl_logic type is an enumeration that defines the full set of VHDL values for Verilog nets, as defined for Logic Strength Modeling in IEEE 1364[™]-2005.

This specification defines the following driving strengths for signals propagated from gate outputs and continuous assignment outputs:

Supply, Strong, Pull, Weak, HiZ

This specification also defines three charge storage strengths for signals originating in the trireg net type:

Large, Medium, Small

Each of these strengths can assume a strength level ranging from 0 to 7 (expressed as a binary value from 000 to 111), combined with the standard four-state values of 0, 1, X, and Z. This results in a set of 256 strength values, which preserves Verilog strength values going through the VHDL portion of the design and allows a VCD in extended format for any downstream application.

The `vl_logic` type is defined in the following file installed with ModelSim, where you can view the 256 strength values:

```
<install_dir>/vhdl_src/verilog/vltypes.vhd
```

This location is a pre-compiled **verilog** library provided in your installation directory, along with the other pre-compiled libraries (**std** and **ieee**).

Note



The Wave window display and WLF do not support the full range of `vl_logic` values for VHDL signals.

Ignoring Strength Ranges

You may wish to ignore strength ranges and have ModelSim handle each strength separately. Any of the following options will produce this behavior:

- Use the `-no_strength_range` argument to the `vcd dumptports` command
- Use an optional argument to `$dumptports` (see [Extended \\$dumptports Syntax](#) below)
- Use the `+dumptports+no_strength_range` argument to `vsim` command

In this situation, ModelSim reports strengths for both the zero and one components of the value if the strengths are the same. If the strengths are different, ModelSim reports only the “winning” strength. In other words, the two strength values either match (for example, pA 5 5 !) or the winning strength is shown and the other is zero (for instance, pH 0 5 !).

Extended \$dumptports Syntax

ModelSim extends the `$dumptports` system task in order to support exclusion of strength ranges. The extended syntax is as follows:

```
$dumptports (scope_list, file_pathname, ncsim_file_index, file_format)
```

The `nc_sim_index` argument is required yet ignored by ModelSim. It is required only to be compatible with NCSim’s argument list.

The `file_format` argument accepts the following values or an ORed combination thereof (see examples below):

Table 25-8. Values for file_format Argument

File_format value	Meaning
0	Ignore strength range
2	Use strength ranges; produces IEEE 1364-compliant behavior

Table 25-8. Values for file_format Argument (cont.)

File_format value	Meaning
4	Compress the EVCD output
8	Include port direction information in the EVCD file header; same as using -direction argument to <code>vcd dumpports</code>

Here are some examples:

```
// ignore strength range
$dumpports(top, "filename", 0, 0)
// compress and ignore strength range
$dumpports(top, "filename", 0, 4)
// print direction and ignore strength range
$dumpports(top, "filename", 0, 8)
// compress, print direction, and ignore strength range
$dumpports(top, "filename", 0, 12)
```

Example 25-5. VCD Output from vcd dumpports

This example demonstrates how `vcd dumpports` resolves values based on certain combinations of driver values and strengths and whether or not you use strength ranges. [Table 25-9](#) is sample driver data.

Table 25-9. Sample Driver Data

time	in value	out value	in strength value (range)	out strength value (range)
0	0	0	7 (strong)	7 (strong)
100	0	0	6 (strong)	7 (strong)
200	0	0	5 (strong)	7 (strong)
300	0	0	4 (weak)	7 (strong)
900	1	0	6 (strong)	7 (strong)
27400	1	1	5 (strong)	4 (weak)
27500	1	1	4 (weak)	4 (weak)
27600	1	1	3 (weak)	4 (weak)

Given the driver data above and use of 1364 strength ranges, here is what the VCD file output would look like:

Value Change Dump (VCD) Files
Capturing Port Driver Data

```
#0  
p0 7 0 <0  
#100  
p0 7 0 <0  
#200  
p0 7 0 <0  
#300  
pL 7 0 <0  
#900  
pB 7 6 <0  
#27400  
pU 0 5 <0  
#27500  
p1 0 4 <0  
#27600  
p1 0 4 <0
```


Chapter 26

Tcl and Macros (DO Files)

Tcl is a scripting language for controlling and extending ModelSim. Within ModelSim you can develop implementations from Tcl scripts without the use of C code. Because Tcl is interpreted, development is rapid; you can generate and execute Tcl scripts on the fly without stopping to recompile or restart ModelSim. In addition, if ModelSim does not provide the command you need, you can use Tcl to create your own commands.

Tcl Features

Using Tcl with ModelSim gives you these features:

- command history (like that in C shells)
- full expression evaluation and support for all C-language operators
- a full range of math and trig functions
- support of lists and arrays
- regular expression pattern matching
- procedures
- the ability to define your own commands
- command substitution (that is, commands may be nested)
- robust scripting language for macros

Tcl References

Two books about Tcl are *Tcl and the Tk Toolkit* by John K. Ousterhout, published by Addison-Wesley Publishing Company, Inc., and *Practical Programming in Tcl and Tk* by Brent Welch published by Prentice Hall. You can also consult the following online references:

- Select **Help > Tcl Man Pages**.

Tcl Commands

For complete information on Tcl commands, select **Help > Tcl Man Pages**. Also see [Simulator GUI Preferences](#) for information on Tcl preference variables.

ModelSim command names that conflict with Tcl commands have been renamed or have been replaced by Tcl commands, as shown in [Table 26-1](#).

Table 26-1. Changes to ModelSim Commands

Previous ModelSim command	Command changed to (or replaced by)
continue	run with the <code>-continue</code> option
format list wave	write format with either list or wave specified
if	replaced by the Tcl if command, see If Command Syntax for more information
list	add list
nolist nowave	delete with either list or wave specified
set	replaced by the Tcl set command, see set Command Syntax for more information
source	vsource
wave	add wave

Tcl Command Syntax

The following eleven rules define the syntax and semantics of the Tcl language. Additional details on [If Command Syntax](#) and [set Command Syntax](#) follow.

1. A Tcl script is a string containing one or more commands. Semi-colons and newlines are command separators unless quoted as described below. Close brackets ("]") are command terminators during command substitution (see below) unless quoted.
2. A command is evaluated in two steps. First, the Tcl interpreter breaks the command into words and performs substitutions as described below. These substitutions are performed in the same way for all commands. The first word is used to locate a command procedure to carry out the command, then all of the words of the command are passed to the command procedure. The command procedure is free to interpret each of its words in any way it likes, such as an integer, variable name, list, or Tcl script. Different commands interpret their words differently.
3. Words of a command are separated by white space (except for newlines, which are command separators).
4. If the first character of a word is a double-quote (") then the word is terminated by the next double-quote character. If semi-colons, close brackets, or white space characters (including newlines) appear between the quotes then they are treated as ordinary characters and included in the word. Command substitution, variable substitution, and backslash substitution are performed on the characters between the quotes as described below. The double-quotes are not retained as part of the word.

5. If the first character of a word is an open brace ({) then the word is terminated by the matching close brace (}). Braces nest within the word: for each additional open brace there must be an additional close brace (however, if an open brace or close brace within the word is quoted with a backslash then it is not counted in locating the matching close brace). No substitutions are performed on the characters between the braces except for backslash-newline substitutions described below, nor do semi-colons, newlines, close brackets, or white space receive any special interpretation. The word will consist of exactly the characters between the outer braces, not including the braces themselves.
6. If a word contains an open bracket ([) then Tcl performs command substitution. To do this it invokes the Tcl interpreter recursively to process the characters following the open bracket as a Tcl script. The script may contain any number of commands and must be terminated by a close bracket (]). The result of the script (that is, the result of its last command) is substituted into the word in place of the brackets and all of the characters between them. There may be any number of command substitutions in a single word. Command substitution is not performed on words enclosed in braces.
7. If a word contains a dollar-sign (\$) then Tcl performs variable substitution: the dollar-sign and the following characters are replaced in the word by the value of a variable. Variable substitution may take any of the following forms:
 - o \$name
Name is the name of a scalar variable; the name is terminated by any character that isn't a letter, digit, or underscore.
 - o \$name(index)
Name gives the name of an array variable and index gives the name of an element within that array. Name must contain only letters, digits, and underscores. Command substitutions, variable substitutions, and backslash substitutions are performed on the characters of index.
 - o \${name}
Name is the name of a scalar variable. It may contain any characters whatsoever except for close braces.

There may be any number of variable substitutions in a single word. Variable substitution is not performed on words enclosed in braces.
8. If a backslash (\) appears within a word then backslash substitution occurs. In all cases but those described below the backslash is dropped and the following character is treated as an ordinary character and included in the word. This allows characters such as double quotes, close brackets, and dollar signs to be included in words without

triggering special processing. [Table 26-2](#) lists the backslash sequences that are handled specially, along with the value that replaces each sequence.

Table 26-2. Tcl Backslash Sequences

Sequence	Value
<code>\a</code>	Audible alert (bell) (0x7)
<code>\b</code>	Backspace (0x8)
<code>\f</code>	Form feed (0xc).
<code>\n</code>	Newline (0xa)
<code>\r</code>	Carriage-return (0xd)
<code>\t</code>	Tab (0x9)
<code>\v</code>	Vertical tab (0xb)
<code>\<newline>whiteSpace</code>	A single space character replaces the backslash, newline, and all spaces and tabs after the newline. This backslash sequence is unique in that it is replaced in a separate pre-pass before the command is actually parsed. This means that it will be replaced even when it occurs between braces, and the resulting space will be treated as a word separator if it isn't in braces or quotes.
<code>\\</code>	Backslash (" <code>\</code> ")
<code>\ooo</code>	The digits <code>ooo</code> (one, two, or three of them) give the octal value of the character.
<code>\xhh</code>	The hexadecimal digits <code>hh</code> give the hexadecimal value of the character. Any number of digits may be present.

Backslash substitution is not performed on words enclosed in braces, except for backslash-newline as described above.

9. If a pound sign (#) appears at a point where Tcl is expecting the first character of the first word of a command, then the pound sign and the characters that follow it, up through the next newline, are treated as a comment and ignored. The # character denotes a comment only when it appears at the beginning of a command.
10. Each character is processed exactly once by the Tcl interpreter as part of creating the words of a command. For example, if variable substitution occurs then no further substitutions are performed on the value of the variable; the value is inserted into the word verbatim. If command substitution occurs then the nested command is processed entirely by the recursive call to the Tcl interpreter; no substitutions are performed before making the recursive call and no additional substitutions are performed on the result of the nested script.

11. Substitutions do not affect the word boundaries of a command. For example, during variable substitution the entire value of the variable becomes part of a single word, even if the variable's value contains spaces.

If Command Syntax

The Tcl **if** command executes scripts conditionally. Note that in the syntax below the question mark (?) indicates an optional argument.

Syntax

```
if expr1 ?then? body1 elseif expr2 ?then? body2 elseif ... ?else? ?bodyN?
```

Description

The **if** command evaluates *expr1* as an expression. The value of the expression must be a boolean (a numeric value, where 0 is false and anything else is true, or a string value such as **true** or **yes** for true and **false** or **no** for false); if it is true then *body1* is executed by passing it to the Tcl interpreter. Otherwise *expr2* is evaluated as an expression and if it is true then *body2* is executed, and so on. If none of the expressions evaluates to true then *bodyN* is executed. The **then** and **else** arguments are optional "noise words" to make the command easier to read. There may be any number of **elseif** clauses, including zero. *bodyN* may also be omitted as long as **else** is omitted too. The return value from the command is the result of the body script that was executed, or an empty string if none of the expressions was non-zero and there was no *bodyN*.

set Command Syntax

The Tcl **set** command returns or sets the values of variables.

Syntax

```
set <varName> [<value>]
```

Arguments

- <varName> — (required) The name of a Tcl variable. The variable name relates to the following:
 - GUI preference variables. You can view a complete list of these variables within the GUI from the **Tools > Edit Preferences** menu selection.
 - Simulator control variables.

UserTimeUnit

IgnoreNote

CheckpointCompressMode

RunLength

IgnoreNote

NumericStdNoWarnings

IterationLimit

IgnoreError

StdArithNoWarnings

BreakOnAssertion

IgnoreFailure

PathSeparator

DefaultForceKind

DefaultRadix

WLFFilename

DelayFileOpen

WLFTimeLimit

WLFSizeLimit

If you do not specify a <value> this command will return the value of the <varName> you specify.

- <value> — (optional) The value to be assigned to the variable.

When you specify <value> you will change the current state of the <varName> you specify.

Description

Returns the value of variable *varName*. If you specify *value*, the command sets the value of *varName* to *value*, creating a new variable if one doesn't already exist, and returns its value. If *varName* contains an open parenthesis and ends with a close parenthesis, then it refers to an array element: the characters before the first open parenthesis are the name of the array, and the characters between the parentheses are the index within the array. Otherwise *varName* refers to a scalar variable. Normally, *varName* is unqualified (does not include the names of any containing namespaces), and the variable of that name in the current namespace is read or written. If *varName* includes namespace qualifiers (in the array name if it refers to an array element), the variable in the specified namespace is read or written.

If no procedure is active, then *varName* refers to a namespace variable (global variable if the current namespace is the global namespace). If a procedure is active, then *varName* refers to a parameter or local variable of the procedure unless the global command was invoked to declare *varName* to be global, or unless a Tcl **variable** command was invoked to declare *varName* to be a namespace variable.

Command Substitution

Placing a command in square brackets ([]) will cause that command to be evaluated first and its results returned in place of the command. An example is:

```
set a 25
set b 11
set c 3
echo "the result is [expr ($a + $b)/$c]"
```

will output:

```
"the result is 12"
```

This feature allows VHDL variables and signals, and Verilog nets and registers to be accessed using:

```
[examine -<radix> name]
```

The %name substitution is no longer supported. Everywhere %name could be used, you now can use [examine -value -<radix> name] which allows the flexibility of specifying command options. The radix specification is optional.

Command Separator

A semicolon character (;) works as a separator for multiple commands on the same line. It is not required at the end of a line in a command sequence.

Multiple-Line Commands

With Tcl, multiple-line commands can be used within macros and on the command line. The command line prompt will change (as in a C shell) until the multiple-line command is complete.

In the example below, note the way the opening brace '}' is at the end of the if and else lines. This is important because otherwise the Tcl scanner won't know that there is more coming in the command and will try to execute what it has up to that point, which won't be what you intend.

```
if { [exa sig_a] == "0011ZZ" } {  
    echo "Signal value matches"  
    do macro_1.do  
} else {  
    echo "Signal value fails"  
    do macro_2.do  
}
```

Evaluation Order

An important thing to remember when using Tcl is that anything put in braces ({}) is not evaluated immediately. This is important for if-then-else statements, procedures, loops, and so forth.

Tcl Relational Expression Evaluation

When you are comparing values, the following hints may be useful:

- Tcl stores all values as strings, and will convert certain strings to numeric values when appropriate. If you want a literal to be treated as a numeric value, don't quote it.

```
if {[exa var_1] == 345}...
```

The following will also work:

```
if {[exa var_1] == "345"}...
```

- However, if a literal cannot be represented as a number, you *must* quote it, or Tcl will give you an error. For instance:

```
if {[exa var_2] == 001Z}...
```

will give an error.

```
if {[exa var_2] == "001Z"}...
```

will work okay.

- Don't quote single characters in single quotes:

```
if {[exa var_3] == 'X'}...
```

will give an error

```
if {[exa var_3] == "X"}...
```

will work okay.

- For the equal operator, you must use the C operator (==). For not-equal, you must use the C operator (!=).

Variable Substitution

When a `$<var_name>` is encountered, the Tcl parser will look for variables that have been defined either by ModelSim or by you, and substitute the value of the variable.

Note



Tcl is case sensitive for variable names.

To access environment variables, use the construct:

```
$env(<var_name>)  
echo My user name is $env(USER)
```

Environment variables can also be set using the env array:

```
set env(SHELL) /bin/csh
```

See [modelsim.ini Variables](#) for more information about ModelSim-defined variables.

System Commands

To pass commands to the UNIX shell or DOS window, use the Tcl **exec** command:

```
echo The date is [exec date]
```


Simulator State Variables

Unlike other variables that must be explicitly set, simulator state variables return a value relative to the current simulation. Simulator state variables can be useful in commands, especially when used within ModelSim DO files (macros). The variables are referenced in commands by prefixing the name with a dollar sign (\$).

argc

This variable returns the total number of parameters passed to the current macro.

architecture

This variable returns the name of the top-level architecture currently being simulated; for an optimized Verilog module, returns architecture name; for a configuration or non-optimized Verilog module, this variable returns an empty string.

configuration

This variable returns the name of the top-level configuration currently being simulated; returns an empty string if no configuration.

delta

This variable returns the number of the current simulator iteration.

entity

This variable returns the name of the top-level VHDL entity or Verilog module currently being simulated.

library

This variable returns the library name for the current region.

MacroNestingLevel

This variable returns the current depth of macro call nesting.

n

This variable represents a macro parameter, where n can be an integer in the range 1-9.

Now

This variable always returns the current simulation time with time units (for example, 110,000 ns) Note: will return a comma between thousands.

now

This variable when time resolution is a unary unit (that is, 1ns, 1ps, 1fs): returns the current simulation time without time units (for example, 100000) when time resolution is a multiple of the unary unit (that is, 10ns, 100ps, 10fs): returns the current simulation time with time units (for example, 110000 ns) Note: will not return comma between thousands.

resolution

This variable returns the current simulation time resolution.

Referencing Simulator State Variables

Variable values may be referenced in simulator commands by preceding the variable name with a dollar sign (\$). For example, to use the **now** and **resolution** variables in an **echo** command type:

```
echo "The time is $now $resolution."
```

Depending on the current simulator state, this command could result in:

```
The time is 12390 ps 10ps.
```

If you do not want the dollar sign to denote a simulator variable, precede it with a backslash (\). For example, `\$now` will not be interpreted as the current simulator time.

Special Considerations for the now Variable

For the **when** command, special processing is performed on comparisons involving the **now** variable. If you specify "when { \$now=100 }...", the simulator will stop at time 100 regardless of the multiplier applied to the time resolution.

You must use 64-bit time operators if the time value of **now** will exceed 2147483647 (the limit of 32-bit numbers). For example:

```
if { [gtTime $now 2us] } {  
.  
:  
.
```

See [Simulator Tcl Time Commands](#) for details on 64-bit time operators.

List Processing

In Tcl a "list" is a set of strings in curly braces separated by spaces. Several Tcl commands are available for creating lists, indexing into lists, appending to lists, getting the length of lists and shifting lists, as shown in [Table 26-3](#).

Table 26-3. Tcl List Commands

Command syntax	Description
lappend var_name val1 val2 ...	appends val1, val2, and so forth, to list var_name
lindex list_name index	returns the index-th element of list_name; the first element is 0
linsert list_name index val1 val2 ...	inserts val1, val2, and so forth, just before the index-th element of list_name
list val1, val2 ...	returns a Tcl list consisting of val1, val2, and so forth.
llength list_name	returns the number of elements in list_name
lrange list_name first last	returns a sublist of list_name, from index first to index last; first or last may be "end", which refers to the last element in the list
lreplace list_name first last val1, val2, ...	replaces elements first through last with val1, val2, and so forth.

Two other commands, **lsearch** and **lsort**, are also available for list manipulation. See the Tcl man pages ([Help > Tcl Man Pages](#)) for more information on these commands.

See also the ModelSim Tcl command: [lecho](#)

Reading Variable Values From the INI File

You can read values from the *modelsim.ini* file with the following function:

```
GetPrivateProfileString <section> <key> <defaultValue>
```

Reads the string value for the specified variable in the specified section. Optionally provides a default value if no value is present.

Setting Tcl variables with values from the *modelsim.ini* file is one use of these Tcl functions. For example,

```
set MyCheckpointCompressMode [GetPrivateProfileString vsim
                             CheckpointCompressMode 1 modelsim.ini ]

set PrefMain(file) [GetPrivateProfileString vsim TranscriptFile ""
                                             modelsim.ini]
```

Simulator Tcl Commands

These additional commands enhance the interface between Tcl and ModelSim. Only brief descriptions are provided in [Table 26-4](#). For more information and command syntax see [Commands](#).

Table 26-4. Simulator-Specific Tcl Commands

Command	Description
alias	creates a new Tcl procedure that evaluates the specified commands; used to create a user-defined alias
find	locates incrTcl classes and objects
lecho	takes one or more Tcl lists as arguments and pretty-prints them to the Transcript pane
lshift	takes a Tcl list as argument and shifts it in-place one place to the left, eliminating the 0th element
lsublist	returns a sublist of the specified Tcl list that matches the specified Tcl glob pattern
printenv	echoes to the Transcript pane the current names and values of all environment variables

Simulator Tcl Time Commands

ModelSim Tcl time commands make simulator-time-based values available for use within other Tcl procedures.

Time values may optionally contain a units specifier where the intervening space is also optional. If the space is present, the value must be quoted (for example, 10ns, "10 ns"). Time values without units are taken to be in the UserTimeScale. Return values are always in the current Time Scale Units. All time values are converted to a 64-bit integer value in the current Time Scale. This means that values smaller than the current Time Scale will be truncated to 0.

Conversions

Table 26-5. Tcl Time Conversion Commands

Command	Description
intToTime <intHi32> <intLo32>	converts two 32-bit pieces (high and low order) into a 64-bit quantity (Time in ModelSim is a 64-bit integer)
RealToTime <real>	converts a <real> number to a 64-bit integer in the current Time Scale
scaleTime <time> <scaleFactor>	returns the value of <time> multiplied by the <scaleFactor> integer

Relations

Table 26-6. Tcl Time Relation Commands

Command	Description
eqTime <time> <time>	evaluates for equal
neqTime <time> <time>	evaluates for not equal
gtTime <time> <time>	evaluates for greater than
gteTime <time> <time>	evaluates for greater than or equal
ltTime <time> <time>	evaluates for less than
lteTime <time> <time>	evaluates for less than or equal

All relation operations return 1 or 0 for true or false respectively and are suitable return values for TCL conditional expressions. For example,

```
if {[eqTime $Now 1750ns]} {
    ...
}
```

Arithmetic

Table 26-7. Tcl Time Arithmetic Commands

Command	Description
addTime <time> <time>	add time
divTime <time> <time>	64-bit integer divide
mulTime <time> <time>	64-bit integer multiply
subTime <time> <time>	subtract time

Tcl Examples

[Example 26-1](#) uses the Tcl **while** loop to copy a list from variable *a* to variable *b*, reversing the order of the elements along the way:

Example 26-1. Tcl while Loop

```
set b [list]
set i [expr {[length $a] - 1}]
while {$i >= 0} {
    lappend b [lindex $a $i]
    incr i -1
}
```

[Example 26-2](#) uses the Tcl **for** command to copy a list from variable *a* to variable *b*, reversing the order of the elements along the way:

Example 26-2. Tcl for Command

```
set b [list]
for {set i [expr {[length $a] - 1}]} {$i >= 0} {incr i -1} {
    lappend b [lindex $a $i]
}
```

[Example 26-3](#) uses the Tcl **foreach** command to copy a list from variable *a* to variable *b*, reversing the order of the elements along the way (the **foreach** command iterates over all of the elements of a list):

Example 26-3. Tcl foreach Command

```
set b [list]
foreach i $a { set b [linsert $b 0 $i] }
```

[Example 26-4](#) shows a list reversal as above, this time aborting on a particular element using the Tcl **break** command:

Example 26-4. Tcl break Command

```
set b [list]
foreach i $a {
    if {$i = "ZZZ"} break
    set b [linsert $b 0 $i]
}
```

[Example 26-5](#) is a list reversal that skips a particular element by using the Tcl **continue** command:

Example 26-5. Tcl continue Command

```
set b [list]
foreach i $a {
    if {$i = "ZZZ"} continue
    set b [linsert $b 0 $i]
}
```

[Example 26-6](#) works in UNIX only. In a Windows environment, the Tcl **exec** command will execute compiled files only, not system commands.) The example shows how you can access system information and transfer it into VHDL variables or signals and Verilog nets or registers. When a particular HDL source breakpoint occurs, a Tcl function is called that gets the date and time and deposits it into a VHDL signal of type STRING. If a particular environment variable (DO_ECHO) is set, the function also echoes the new date and time to the transcript file by examining the VHDL variable.

Example 26-6. Access and Transfer System Information

(in VHDL source):

```
signal datetime : string(1 to 28) := " ";# 28 spaces
```

(on VSIM command line or in macro):

```
proc set_date {} {
    global env
    set do_the_echo [set env(DO_ECHO)]
    set s [clock format [clock seconds]]
    force -deposit datetime $s
    if {do_the_echo} {
        echo "New time is [examine -value datetime]"
    }
}

bp src/waveadd.vhd 133 {set_date; continue}
--sets the breakpoint to call set_date
```

[Example 26-7](#) specifies the compiler arguments and lets you compile any number of files.

Example 26-7. Tcl Used to Specify Compiler Arguments

```
set Files [list]
set nbrArgs $argc
for {set x 1} {$x <= $nbrArgs} {incr x} {
    set lappend Files $1
    shift
}
eval vcom -93 -explicit -noaccel $Files
```

[Example 26-8](#) is an enhanced version of the last one. The additional code determines whether the files are VHDL or Verilog and uses the appropriate compiler and arguments depending on the file type. Note that the macro assumes your VHDL files have a *.vhd* file extension.

Example 26-8. Tcl Used to Specify Compiler Arguments—Enhanced

```
set vhdFiles [list]
set vFiles [list]
set nbrArgs $argc
for {set x 1} {$x <= $nbrArgs} {incr x} {
    if {[string match *.vhd $1]} {
        lappend vhdFiles $1
    } else {
        lappend vFiles $1
    }
    shift
}
if {[llength $vhdFiles] > 0} {
    eval vcom -93 -explicit -noaccel $vhdFiles
}
if {[llength $vFiles] > 0} {
    eval vlog $vFiles
}
```

Macros (DO Files)

ModelSim macros (also called DO files) are simply scripts that contain ModelSim and, optionally, Tcl commands. You invoke these scripts with the **Tools > TCL > Execute Macro** menu selection or the `do` command.

Creating DO Files

You can create DO files, like any other Tcl script, by typing the required commands in any editor and saving the file. Alternatively, you can save the transcript as a DO file (see [Saving the Transcript File](#)).

All "event watching" commands (for example, `onbreak`, `onerror`, and so forth) must be placed before `run` commands within the macros in order to take effect.

The following is a simple DO file that was saved from the transcript. It is used in the dataset exercise in the ModelSim Tutorial. This DO file adds several signals to the Wave window, provides stimulus to those signals, and then advances the simulation.

```
add wave ld
add wave rst
add wave clk
add wave d
add wave q
force -freeze clk 0 0, 1 {50 ns} -r 100
force rst 1
force rst 0 10
force ld 0
force d 1010
onerror {cont}
run 1700
force ld 1
run 100
force ld 0
run 400
force rst 1
run 200
force rst 0 10
run 1500
```

Using Parameters with DO Files

You can increase the flexibility of DO files by using parameters. Parameters specify values that are passed to the corresponding parameters \$1 through \$9 in the macro file. For example say the macro "testfile" contains the line **bp** \$1 \$2. The command below would place a breakpoint in the source file named *design.vhd* at line 127:

```
do testfile design.vhd 127
```

There is no limit on the number of parameters that can be passed to macros, but only nine values are visible at one time. You can use the [shift](#) command to see the other parameters.

Deleting a File from a.do Script

To delete a file from a .do script, use the Tcl **file** command as follows:

```
file delete myfile.log
```

This will delete the file "myfile.log."

You can also use the **transcript file** command to perform a deletion:

```
transcript file ()  
transcript file my file.log
```

The first line will close the current log file. The second will open a new log file. If it has the same name as an existing file, it will replace the previous one.

Making Macro Parameters Optional

If you want to make macro parameters optional (that is, be able to specify fewer parameter values with the do command than the number of parameters referenced in the macro), you must use the **argc** simulator state variable. The **argc** simulator state variable returns the number of parameters passed. The examples below show several ways of using **argc**.

Example 26-9. Specifying Files to Compile With **argc** Macro

This macro specifies the files to compile and handles 0-2 compiler arguments as parameters. If you supply more arguments, ModelSim generates a message.

```
switch $argc {
  0 {vcom file1.vhd file2.vhd file3.vhd }
  1 {vcom $1 file1.vhd file2.vhd file3.vhd }
  2 {vcom $1 $2 file1.vhd file2.vhd file3.vhd }
  default {echo Too many arguments. The macro accepts 0-2 args. }
}
```

Example 26-10. Specifying Compiler Arguments With Macro

This macro specifies the compiler arguments and lets you compile any number of files.

```
variable Files ""
set nbrArgs $argc
for {set x 1} {$x <= $nbrArgs} {incr x} {
  set Files [concat $Files $1]
  shift
}
eval vcom -93 -explicit -noaccel $Files
```

Example 26-11. Specifying Compiler Arguments With Macro—Enhanced

This macro is an enhanced version of the one shown in example 2. The additional code determines whether the files are VHDL or Verilog and uses the appropriate compiler and arguments depending on the file type. Note that the macro assumes your VHDL files have a *.vhd* file extension.

```

variable vhdFiles ""
variable vFiles ""
set nbrArgs $argc
set vhdFilesExist 0
set vFilesExist 0
for {set x 1} {$x <= $nbrArgs} {incr x} {
    if {[string match *.vhd $1]} {
        set vhdFiles [concat $vhdFiles $1]
        set vhdFilesExist 1
    } else {
        set vFiles [concat $vFiles $1]
        set vFilesExist 1
    }
    shift
}
if {$vhdFilesExist == 1} {
    eval vcom -93 -explicit -noaccel $vhdFiles
}
if {$vFilesExist == 1} {
    eval vlog $vFiles
}

```

Useful Commands for Handling Breakpoints and Errors

If you are executing a macro when your simulation hits a breakpoint or causes a run-time error, ModelSim interrupts the macro and returns control to the command line. The commands in [Table 26-8](#) may be useful for handling such events. (Any other legal command may be executed as well.)

Table 26-8. Commands for Handling Breakpoints and Errors in Macros

command	result
run -continue	continue as if the breakpoint had not been executed, completes the run that was interrupted
resume	continue running the macro
onbreak	specify a command to run when you hit a breakpoint within a macro
onElabError	specify a command to run when an error is encountered during elaboration
onerror	specify a command to run when an error is encountered within a macro
status	get a traceback of nested macro calls when a macro is interrupted
abort	terminate a macro once the macro has been interrupted or paused

Table 26-8. Commands for Handling Breakpoints and Errors in Macros

command	result
pause	cause the macro to be interrupted; the macro can be resumed by entering a resume command via the command line
transcript	control echoing of macro commands to the Transcript pane

You can also set the `OnErrorDefaultAction` Tcl variable to determine what action ModelSim takes when an error occurs. To set the variable on a permanent basis, you must define the variable in a *modelsim.tcl* file (see [The modelsim.tcl File](#) for details).

Error Action in DO Files

If a command in a macro returns an error, ModelSim does the following:

1. If an [onerror](#) command has been set in the macro script, ModelSim executes that command. The `onerror` command must be placed prior to the run command in the DO file to take effect.
2. If no [onerror](#) command has been specified in the script, ModelSim checks the `OnErrorDefaultAction` variable. If the variable is defined, its action will be invoked.
3. If neither 1 or 2 is true, the macro aborts.

Using the Tcl Source Command with DO Files

Either the `do` command or Tcl source command can execute a DO file, but they behave differently.

With the Tcl source command, the DO file is executed exactly as if the commands in it were typed in by hand at the prompt. Each time a breakpoint is hit, the Source window is updated to show the breakpoint. This behavior could be inconvenient with a large DO file containing many breakpoints.

When a `do` command is interrupted by an error or breakpoint, it does not update any windows, and keeps the DO file "locked". This keeps the Source window from flashing, scrolling, and moving the arrow when a complex DO file is executed. Typically an [onbreak](#) resume command is used to keep the macro running as it hits breakpoints. Add an [onbreak](#) abort command to the DO file if you want to exit the macro and update the Source window.

The Tcl Debugger

We would like to thank Gregor Schmid for making TDebug available for use in the public domain.

This program is distributed in the hope that it will be useful, but WITHOUT ANY WARRANTY; without even the implied warranty of FITNESS FOR A PARTICULAR PURPOSE.

Starting the Debugger

Select **Tools > TCL > Tcl Debugger** to run the debugger. Make sure you use the ModelSim and TDebug menu selections to invoke and close the debugger. If you would like more information on the configuration of TDebug see **Help > Technotes > tdebug**.

The following text is an edited summary of the README file distributed with TDebug.

How it Works

TDebug works by parsing and redefining Tcl/Tk-procedures, inserting calls to ``td_eval'` at certain points, which takes care of the display, stepping, breakpoints, variables and so forth. The advantages are that TDebug knows which statement in which procedure is currently being executed and can give visual feedback by highlighting it. All currently accessible variables and their values are displayed as well. Code can be evaluated in the context of the current procedure. Breakpoints can be set and deleted with the mouse.

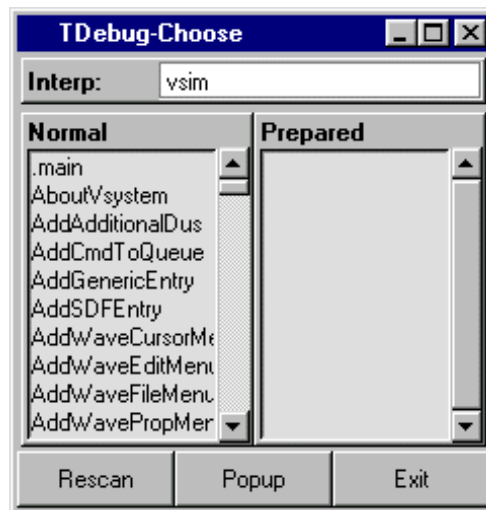
Unfortunately there are drawbacks to this approach. Preparation of large procedures is slow and due to Tcl's dynamic nature there is no guarantee that a procedure can be prepared at all. This problem has been alleviated somewhat with the introduction of partial preparation of procedures. There is still no possibility to get at code running in the global context.

The Chooser

Select **Tools > TCL > Tcl Debugger** to open the TDebug chooser.

The TDebug chooser has three parts. At the top the current interpreter, *vsim.op_*, is shown. In the main section there are two list boxes. All currently defined procedures are shown in the left list box. By clicking the left mouse button on a procedure name, the procedure gets prepared for debugging and its name is moved to the right list box. Clicking a name in the right list box returns a procedure to its normal state.

Figure 26-1. TDebug Choose Dialog



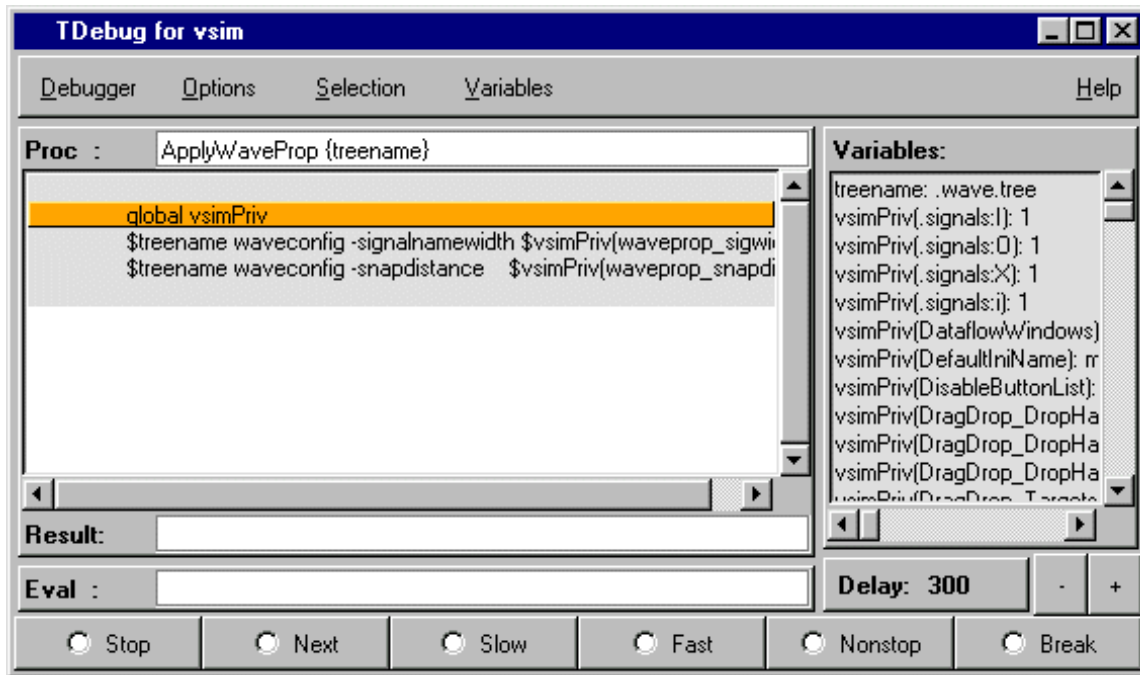
Press the right mouse button on a procedure in either list box to get its program code displayed in the main debugger window.

The three buttons at the bottom let you force a **Rescan** of the available procedures, **Popup** the debugger window or **Exit** TDebug. Exiting from TDebug doesn't terminate ModelSim, it merely detaches from *vsim.op_*, restoring all prepared procedures to their unmodified state.

The Debugger

Select the **Popup** button in the Chooser to open the debugger window ([Figure 26-2](#)).

Figure 26-2. Tcl Debugger for vsim



The debugger window is divided into the main region with the name of the current procedure (**Proc**), a listing in which the expression just executed is highlighted, the **Result** of this execution and the currently available **Variables** and their values, an entry to **Eval** expressions in the context of the current procedure, and some button controls for the state of the debugger.

A procedure listing displayed in the main region will have a darker background on all lines that have been prepared. You can prepare or restore additional lines by selecting a region (<Button-1>, standard selection) and choosing **Selection > Prepare Proc** or **Selection > Restore Proc** from the debugger menu (or by pressing ^P or ^R).

When using `Prepare' and `Restore', try to be smart about what you intend to do. If you select just a single word (plus some optional white space) it will be interpreted as the name of a procedure to prepare or restore. Otherwise, if the selection is owned by the listing, the corresponding lines will be used.

Be careful with partial prepare or restore! If you prepare random lines inside a `switch' or `bind' expression, you may get surprising results on execution, because the parser doesn't know about the surrounding expression and can't try to prevent problems.

There are seven possible debugger states, one for each button and an `idle` or `waiting` state when no button is active. The button-activated states are shown in [Table 26-9](#).

Table 26-9. Tcl Debug States

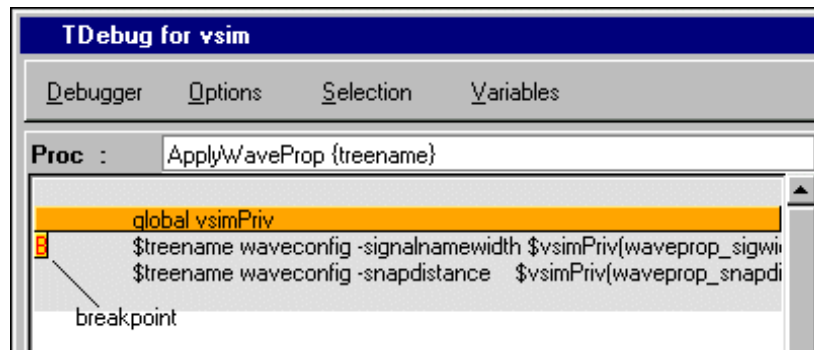
Button	Description
Stop	stop after next expression, used to get out of slow/fast/nonstop mode
Next	execute one expression, then revert to idle
Slow	execute until end of procedure, stopping at breakpoints or when the state changes to stop; after each execution, stop for `delay` milliseconds; the delay can be changed with the `+` and `-` buttons
Fast	execute until end of procedure, stopping at breakpoints
Nonstop	execute until end of procedure without stopping at breakpoints or updating the display
Break	terminate execution of current procedure

Closing the debugger doesn't quit it, it only does `wm withdraw`. The debugger window will pop up the next time a prepared procedure is called. Make sure you close the debugger with **Debugger > Close**.

Breakpoints

To set/unset a breakpoint, double-click inside the listing. The breakpoint will be set at the innermost available expression that contains the position of the click. Conditional or counted breakpoints aren't supported.

Figure 26-3. Setting a Breakpoint in the Debugger

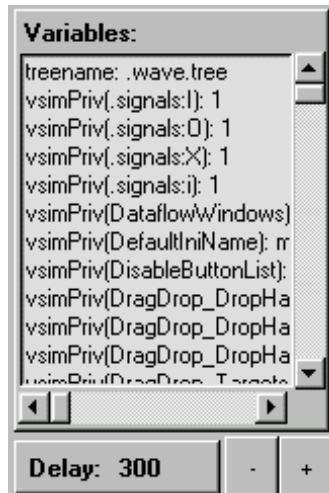


The **Eval** entry supports a simple history mechanism available via the <Up_arrow> and <Down_arrow> keys. If you evaluate a command while stepping through a procedure, the command will be evaluated in the context of the procedure; otherwise it will be evaluated at the

global level. The result will be displayed in the result field. This entry is useful for a lot of things, but especially to get access to variables outside the current scope.

Try entering the line ``global td_priv'` and watch the **Variables** box (with global and array variables enabled of course).

Figure 26-4. Variables Dialog Box



Configuration

You can customize TDebug by setting up a file named `.tdebugrc` in your home directory. See the TDebug README at **Help > Technotes > tdebug** for more information on the configuration of TDebug.

TclPro Debugger

The Tools menu in the Main window contains a selection for the TclPro Debugger from Scriptics Corporation. This debugger and any available documentation can be acquired from Scriptics. Once acquired, do the following steps to use the TclPro Debugger:

1. Make sure the TclPro bin directory is in your PATH.
2. In TclPro Debugger, create a new project with Remote Debugging enabled.
3. Start ModelSim and select **Tools > TclPro Debugger**.
4. Press the Stop button in the debugger in order to set breakpoints, and so forth.

Note



TclPro Debugger version 1.4 does not work with ModelSim.

Chapter A

modelsim.ini Variables

This chapter covers the contents and modification of the *modelsim.ini* file.

- [Organization of the modelsim.ini File](#) — A list of the different sections of the *modelsim.ini* file.
- [Making Changes to the modelsim.ini File](#) — How to modify variable settings in the *modelsim.ini* file.
- [Variables](#) — An alphabetized list of *modelsim.ini* variables and their properties.
- [Commonly Used modelsim.ini Variables](#) — A discussion of the most frequently used variables and their settings.

Organization of the modelsim.ini File

The *modelsim.ini* file is the default initialization file and contains control variables that specify reference library paths, optimization, compiler and simulator settings, and various other functions. It is located in your install directory and is organized into the following sections.

- The [library] section contains variables that specify paths to various libraries used by ModelSim.
- The [vcom] section contains variables that control the compilation of VHDL files.
- The [vlog] section contains variables that control the compilation of Verilog files.
- The [scom] section contains variables that control the compilation of SystemC files.
- The [vopt] section contains variables that control optimization.
- The [vsim] section contains variables that control the simulator.
- The [lmc] section contains variables that control the interface between the simulator and Logic Modeling's SmartModel SWIFT software.
- The [msg_system] section contains variables that control the severity of notes, warnings, and errors that come from vcom, vlog and vsim.

The [scom], [vcom], and [vlog] sections contain compiler control variables.

The [vopt] section contains optimization variables.

The [vsim] section contains simulation control variables.

The System Initialization chapter contains [Environment Variables](#).

Making Changes to the modelsim.ini File

Modify *modelsim.ini* variables by:

- Changing the settings in the [The Runtime Options Dialog](#).
- [Editing modelsim.ini Variables](#).

The Read-only attribute must be turned off to save changes to the *modelsim.ini* file.

Changing the modelsim.ini Read-Only Attribute

When first installed, the *modelsim.ini* file is protected as a Read-only file. In order to make and save changes to the file the Read-only attribute must first be turned off in the *modelsim.ini* Properties dialog box.

Procedure

1. Navigate to the location of the *modelsim.ini* file.
2. <install directory>/modelsim.ini
3. Right-click on the *modelsim.ini* file and choose **Properties** from the popup menu.
4. This displays the *modelsim.ini* Properties dialog box.
5. Uncheck the Attribute: **Read-only**.
6. Click **OK**

To protect the *modelsim.ini* file after making changes, follow the above steps and at step 5, check the **Read-only** attribute.

The Runtime Options Dialog

To access, select **Simulate > Runtime Options** in the Main window. The dialog contains three tabs - Defaults, Assertions, and WLF Files.

The **Runtime Options** dialog writes changes to the active *modelsim.ini* file that affect the current session. If the read-only attribute for the *modelsim.ini* file is turned off, the changes are saved, and affect all future sessions. See [Changing the modelsim.ini Read-Only Attribute](#).

Figure A-1. Runtime Options Dialog: Defaults Tab

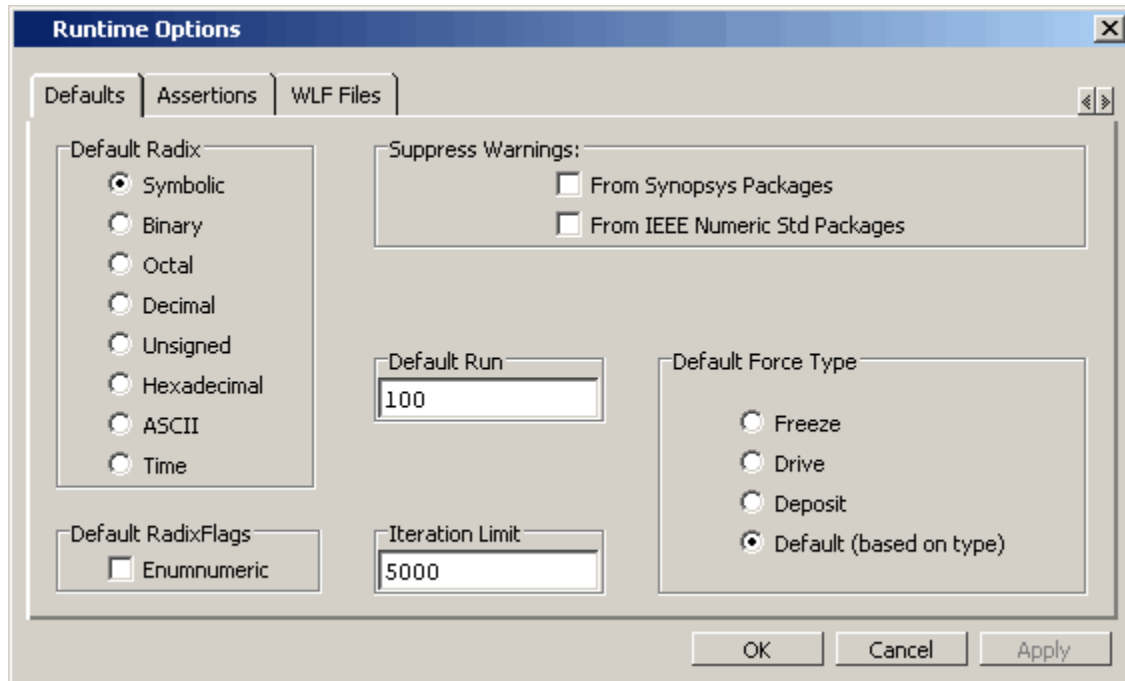


Table A-1. Runtime Option Dialog: Defaults Tab Contents

Option	Description
Default Radix	Sets the default radix for the current simulation run. The chosen radix is used for all commands (<i>force</i> , <i>examine</i> , <i>change</i> are examples) and for displayed values in the Objects, Locals, Dataflow, List, and Wave windows. The corresponding <i>modelsim.ini</i> variable is DefaultRadix . You can override this variable with the radix command.
Default RadixFlags	Displays SystemVerilog and SystemC enums as numbers rather than strings. This option overrides the global setting of the default radix. You can override this variable with the add list -radixenumsymbolic .
Suppress Warnings	<p>From Synopsys Packages suppresses warnings generated within the accelerated Synopsys <i>std_arith</i> packages. The corresponding <i>modelsim.ini</i> variable is StdArithNoWarnings.</p> <p>From IEEE Numeric Std Packages suppresses warnings generated within the accelerated <i>numeric_std</i> and <i>numeric_bit</i> packages. The corresponding <i>modelsim.ini</i> variable is NumericStdNoWarnings.</p>

Table A-1. Runtime Option Dialog: Defaults Tab Contents

Option	Description
Default Run	Sets the default run length for the current simulation. The corresponding <i>modelsim.ini</i> variable is RunLength . You can override this variable by specifying the run command.
Iteration Limit	Sets a limit on the number of deltas within the same simulation time unit to prevent infinite looping. The corresponding <i>modelsim.ini</i> variable is IterationLimit .
Default Force Type	Selects the default force type for the current simulation. The corresponding <i>modelsim.ini</i> variable is DefaultForceKind . You can override this variable by specifying the switches -default, -deposit, -drive, or -freeze with the force command.

Figure A-2. Runtime Options Dialog Box: Assertions Tab

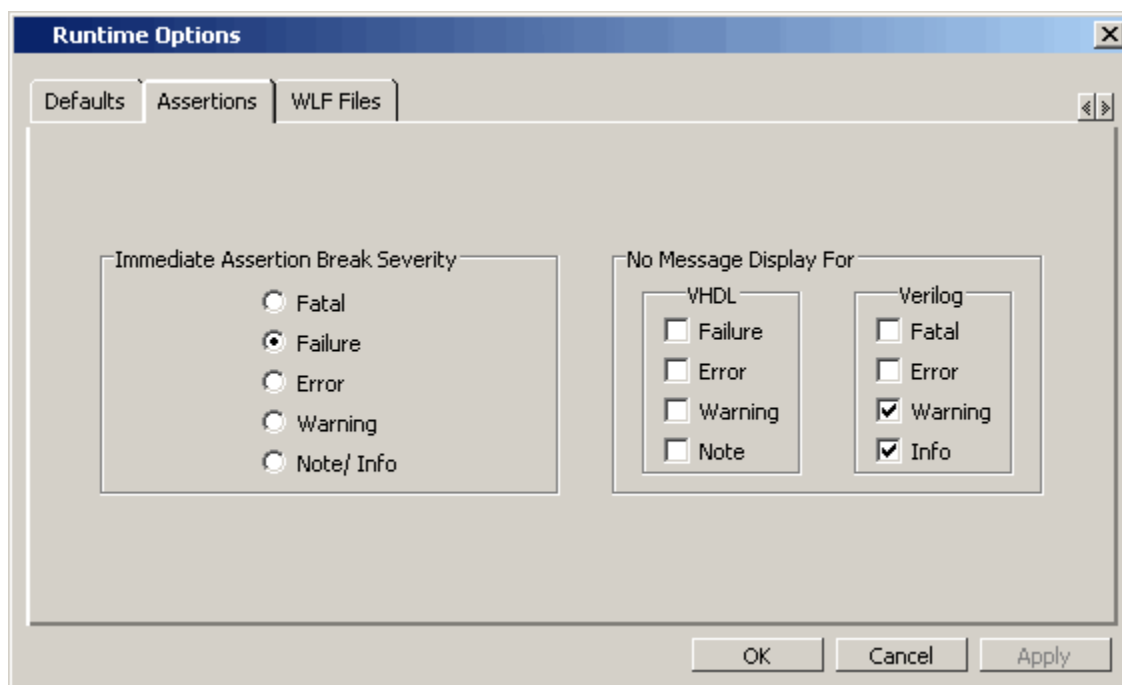


Table A-2. Runtime Option Dialog: Assertions Tab Contents

Option	Description
No Message Display For -VHDL	Selects the VHDL assertion severity for which messages will not be displayed (even if break on assertion is set for that severity). Multiple selections are possible. The corresponding <i>modelsim.ini</i> variables are IgnoreFailure , IgnoreError , IgnoreWarning , and IgnoreNote .

Figure A-3. Runtime Options Dialog Box: WLF Files Tab

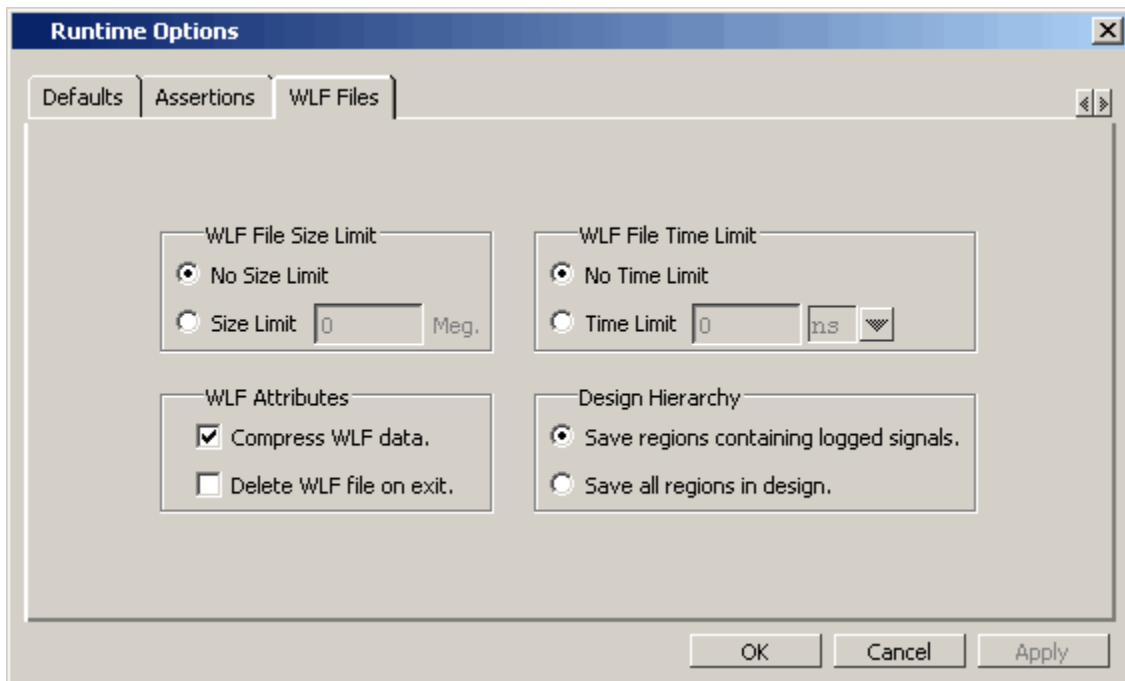


Table A-3. Runtime Option Dialog: WLF Files Tab Contents

Option	Description
WLF File Size Limit	Limits the WLF file by size (as closely as possible) to the specified number of megabytes. If both size and time limits are specified, the most restrictive is used. Setting it to 0 results in no limit. The corresponding <i>modelsim.ini</i> variable is WLFSizeLimit .
WLF File Time Limit	Limits the WLF file by size (as closely as possible) to the specified amount of time. If both time and size limits are specified, the most restrictive is used. Setting it to 0 results in no limit. The corresponding <i>modelsim.ini</i> variable is WLFTimeLimit .
WLF Attributes	Specifies whether to compress WLF files and whether to delete the WLF file when the simulation ends. You would typically only disable compression for troubleshooting purposes. The corresponding <i>modelsim.ini</i> variables are WLFCompress for compression and WLFDeleteOnQuit for WLF file deletion.
Design Hierarchy	Specifies whether to save all design hierarchy in the WLF file or only regions containing logged signals. The corresponding <i>modelsim.ini</i> variable is WLFSaveAllRegions .

Editing modelsim.ini Variables

The syntax for variables in the file is:

<variable> = <value>

Procedure

1. Open the *modelsim.ini* file with a text editor.
2. Find the variable you want to edit in the appropriate section of the file.
3. Type the new value for the variable after the equal (=) sign.
4. If the variable is commented out with a simicolon (;) remove the semicolon.
5. Save.

Overriding the Default Initialization File

You can make changes to the working environment during a work session by loading an alternate initialization file that replaces the the default *modelsim.ini* file. This file overrides the file and path specified by the MODELSIM environment variable.

Procedure

1. Open the *modelsim.ini* file with a text editor.
2. Make changes to the modelsim.ini variables.
3. Save the file with an alternate name to any directory.
4. After start up of the tool, specify the -modelsimini <ini_filepath> switch with one of the following commands:

Table A-4. Commands for Overriding the Default Initialization File

Simulator Commands	Compiler Commands	Utility Commands
vsim	scom vcom vlog vopt	scgenmod vcover attribute vcover merge vcover ranktest vcover report vcover stats vcover testnames vdel vdir vgencomp vmake xml2ucdb

See the <command> -modelsimini switch description for further information.

Variables

The *modelsim.ini* variables are listed in order alphabetically. The following information is given for each variable.

- A short description of how the variable functions.
- The location of the variable, by section, in the *modelsim.ini* file.
- The syntax for the variable.
- A listing of all values and the default value where applicable.
- Related switches that are entered on the command line to override variable settings. Commands entered at the command line always take precedence over *modelsim.ini* settings. Not all variables have related switches.
- Related topics and links to further information about the variable.

AcceptLowerCasePragmaOnly

This variable instructs the Verilog compiler to accept only lower case pragmas in Verilog source files.

Section [vlog]

Syntax

AcceptLowerCasePragmaOnly = {0 | 1}

0 — Off (default)

1 — On

You can override this variable by specifying **vlog** -lowercasepragma.

AmsStandard

This variable specifies whether **vcom** adds the declaration of REAL_VECTOR to the STANDARD package. This is useful for designers using VHDL-AMS to test digital parts of their model.

Section [vcom]

Syntax

AmsStandard = {0 | 1}

0 — Off (default)

1 — On

You can override this variable by specifying `vcom` `{-amsstd | -noamsstd}`.

Related Topics

[MGC_AMS_HOME](#)

AssertFile

This variable specifies an alternative file for storing VHDL assertion messages. By default, assertion messages are output to the file specified by the [TranscriptFile](#) variable in the *modelsim.ini* file (refer to “[Creating a Transcript File](#)”). If the `AssertFile` variable is specified, all assertion messages will be stored in the specified file, not in the transcript.

Section [vsim]

Syntax

`AssertFile = <filename>`

`<filename>` — Any valid file name containing assertion messages, where the default name is *assert.log*.

You can override this variable by specifying `vsim -assertfile`.

AssertionDebug

This variable specifies that SVA assertion passes are reported.

Section [vsim]

Syntax

`AssertionDebug = {0 | 1}`

0 — Off (default)

1 — On

You can override this variable by specifying `vsim -assertdebug`.

AssertionFailAction

This variable sets an action for a PSL/SVA failure event.

Section [vsim]

Syntax

`AssertionFailAction = {0 | 1 | 2}`

0 — Continue (default)

1 — Break

2 — Exit

You can override this variable by specifying [assertion fail](#) -action.

AssertionFailEnable

This variable enables failure tracking for PSL/SVA assertions.

Section [vsim]

Syntax

AssertionFailEnable = {0 | 1}

0 — Off

1 — On (default)

You can override this variable by specifying [assertion fail](#) -disable.

AssertionFailLimit

This variable sets a limit for the number of times ModelSim responds to a PSL/SVA assertion failure event. ModelSim disables an assertion after reaching the limit.

Section [vsim]

Syntax

AssertionFailLimit = <n>

<n> — Any positive integer where the default is -1 (unlimited).

You can override this variable by specifying [assertion fail](#) -limit.

AssertionFailLocalVarLog

This variable prints SVA concurrent assertion local variable values corresponding to failed assertion threads when the [vsim](#) command is run with the -assertdebug switch.

Section [vsim]

Syntax

AssertionFailLocalVarLog = {0 | 1}

0 — Off

1 — On (default)

You can override this variable by specifying [assertion fail](#) -lvlog.

AssertionFailLog

This variable enables transcript logging for PSL assertion failure events.

Section [vsim]

Syntax

AssertionFailLog = {0 | 1}

0 — Off

1 — On (default)

You can override this variable by specifying [assertion fail -log](#).

AssertionPassEnable

This variable enables pass tracking for PSL/SVA assertions.

Section [vsim]

Syntax

AssertionPassEnable = {0 | 1}

0 — Off

1 — On (default)

You can override this variable by specifying [assertion pass -disable](#).

AssertionPassLimit

This variable sets the limit for the number of times ModelSim responds to a PSL/SVA assertion pass event. ModelSim disables an assertion after reaching the limit.

Section [vsim]

Syntax

AssertionPassLimit = <n>

<n> — Any positive integer where the default is -1 (unlimited).

You can override this variable by specifying [assertion pass -limit](#).

AssertionPassLog

This variable enables transcript logging for PSL assertion pass events.

Section [vsim]

Syntax

AssertionPassLog = {0 | 1}

0 — Off (default)

1 — On

You can override this variable by specifying [assertion pass -log](#).

AutoExclusionsDisable

This variable is used to control automatic code coverage exclusions. By default, assertions and FSMs are excluded from the code coverage. For FSMs, all transitions to and from excluded states are also automatically excluded. When “all” is selected, code coverage is enabled for both assertions and FSMs.

Section [vsim]

Syntax

AutoExclusionsDisable = {assertions | fsm | all}

assertions — Enable code coverage for assertions.

fsm — Enable code coverage for FSMs.

all — Enable code coverage for all automatic exclusions.

To enable multiple values, use a comma or space separated list.

You can override this variable by specifying [vsim -autoexclusionsdisable](#).

BindAtCompile

This variable instructs ModelSim to perform VHDL default binding at compile time rather than load time.

Section [vcom]

Syntax

BindAtCompile = {0 | 1}

0 — Off (default)

1 — On

You can override this variable by specifying [vcom {-bindAtCompile | -bindAtLoad}](#).

Related Topics

[Default Binding](#)

[RequireConfigForAllDefaultBinding](#)

BreakOnAssertion

This variable defines the severity of VHDL assertions that cause a simulation break. It also controls any messages in the source code that use *assertion_failure_**. For example, since most

Variables

runtime messages use some form of `assertion_failure_*`, any runtime error will cause the simulation to break if the user sets `BreakOnAssertion = 2` (error).

Section [vsim]

Syntax

`BreakOnAssertion = {0 | 1 | 2 | 3 | 4}`

0 — Note

1 — Warning

2 — Error

3 — Failure (default)

4 — Fatal

Related Topics

You can set this variable in the [The Runtime Options Dialog](#).

You can set this variable interactively with the [Tcl set Command Syntax](#).

CheckPlusargs

This variable defines the simulator's behavior when encountering unrecognized plusargs. The simulator checks the syntax of all system-defined plusargs to ensure they conform to the syntax defined in the Reference Manual. By default, the simulator does not check syntax or issue warnings for unrecognized plusargs (including accidentally misspelled, system-defined plusargs), because there is no way to distinguish them from a user-defined plusarg.

Section [vsim]

Syntax

`CheckPlusargs = {0 | 1 | 2}`

0 — Ignore (default)

1 — Issues a warning and simulates while ignoring.

2 — Issues an error and exits.

CheckpointCompressMode

This variable specifies that checkpoint files are written in compressed format.

Section [vsim]

Syntax

`CheckpointCompressMode = {0 | 1}`

0 — Off

1 — On (default)

Related Topics

You can set this variable interactively with the Tcl [set Command Syntax](#).

CheckSynthesis

This variable turns on limited synthesis rule compliance checking, which includes checking only signals used (read) by a process and understanding only combinational logic, not clocked logic.

Section [vcom]

Syntax

CheckSynthesis = {0 | 1}

0 — Off (default)

1 — On

You can override this variable by specifying `vcom -check_synthesis`.

CommandHistory

This variable specifies the name of a file in which to store the Main window command history.

Section [vsim]

Syntax

CommandHistory = <filename>

<filename> — Any string representing a valid filename.

The default setting for this variable is to comment it out with a semicolon (;).

ConcurrentFileLimit

This variable controls the number of VHDL files open concurrently. This number should be less than the current limit setting for maximum file descriptors.

Section [vsim]

Syntax

ConcurrentFileLimit = <n>

<n> — Any non-negative integer where 0 is unlimited and 40 is the default.

Related Topics

[Syntax for File Declaration](#)

CoverageSub

This variable controls the collection of code coverage statistics in VHDL subprograms.

Section [vcom]

Syntax

CoverageSub = {0 | 1}

0 — Off

1 — On (default)

CoverCells

This variable enables code coverage of Verilog modules defined by 'celldefine and 'endcelldefine compiler directives.

Section [vlog]

Syntax

CoverCells = {0 | 1}

0 — Off (default)

1 — On

You can override this variable by specifying **vlog** {-covercells |-nocovercells} or **vopt** {-covercells |-nocovercells}.

Related Topics

[Verilog-XL Compatible Compiler Arguments](#)

CoverCountAll

This variable applies to condition and expression coverage UDP tables. If this variable is turned off (0) and a match occurs in more than one row, none of the counts for all matching rows is incremented. By default, counts are incremented for all matching rows.

Section [vsim]

Syntax

CoverCountAll = {0 | 1}

0 — Off

1 — On (default)

You can override this variable by specifying `vsim -covercountnone`.

Related Topics

[Verilog-XL Compatible Compiler Arguments](#)

CoverExcludeDefault

This variable excludes code coverage data collection from the default branch of case statements.

Sections [vcom], [vlog]

Syntax

CoverExcludeDefault = {0 | 1}

0 — Off (default)

1 — On

CoverFEC

This variable controls the collection of code coverage for focused expression and condition coverage statistics.

Sections [vcom], [vlog]

Syntax

CoverFEC = {0 | 1}

0 — Off

1 — On (default)

CoverMaxFECRows

This variable controls the maximum number of rows allowed in an FEC truth table for a code coverage condition or expression. Increasing the number of rows includes more expressions for coverage but also increases the compile time. Depending on the total number of rows, the increase can be quite dramatic.

Sections [vcom], [vlog], [vopt]

Syntax

CoverMaxFECRows = <n>

<n> — Any integer where the default is 192.

CoverMaxUDPRows

This variable controls the maximum number of rows allowed in a UDP truth table for a code coverage condition or expression. Increasing the number of rows includes more expressions for coverage but also increases the compile time. Depending on the total number of rows, the increase can be quite dramatic.

Section [vcom], [vlog], [vopt]

Syntax

CoverMaxUDPRows = <n>

<n> — Any integer where the default is 192.

CoverOpt

This variable controls the default level of optimizations for compilations with code coverage.

Sections [vcom], [vlog], [vopt]

Syntax

CoverOpt = {1 | 2 | 3 | 4}

- 1 — Turns off all optimizations that affect coverage reports.
- 2 — Allows optimizations that provide large performance improvements by invoking sequential processes only when the data changes. Allows VHDL flip-flop recognition. This setting may result in major reductions in coverage counts.
- 3 — (default) Allows all optimizations in 2, and allows optimizations that may change expressions or remove some statements. Also allows constant propagation and VHDL subprogram inlining.
- 4 — Allows all optimizations in 2 and 3, and allows optimizations that may remove major regions of code by changing assignments to built-ins or removing unused signals. It also changes Verilog gates to continuous assignments. Allows VHDL subprogram inlining.

You can override this variable by specifying the [vcom](#), [vlog](#), or [vopt](#) command with the `-coveropt` argument.

Related Topics

+cover switch with the [vlog](#) command.

CoverRespectHandL

This variable specifies whether you want the VHDL 'H' and 'L' input values on conditions and expressions to be automatically converted to '1' and '0', respectively.

This variable controls the default level of optimizations for compilations with code coverage.

Section: [vcom]

Syntax

CoverRespectHandL = {0 | 1}

0 — On

1 — Off (default) H and L values are not automatically converted.

If you are not using 'H' and 'L' values and do not want the additional UDP rows that are difficult to cover — you can:

- Change your VHDL expressions of the form (a = '1') to (to_x01(a) = '1') or to std_match(a,'1'). These functions are recognized and used to simplify the UDP tables.
- Override this variable by specifying [vcom](#) -nocoverrespecthandl.

CoverShortCircuit

This variable enables short circuiting of expressions when coverage is enabled.

Sections [vcom], [vlog]

Syntax

CoverShortCircuit = {0 | 1}

0 — Off

1 — On (default)

You can override this variable by specifying either the [vcom](#) or [vlog](#) command with the argument -nocovershort.

CppOptions

This variable adds any specified C++ compiler options to the sccom command line at the time of invocation.

Section [sccom]

Syntax

CppOptions = <options>

<options> — Any normal C++ compiler options.

You turn this variable off by commenting the variable line in the *modelsim.ini* file.

Related Topics

[sccom](#) <CPP compiler options>

CppPath

This variable should point directly to the location of the g++ executable, such as:

```
% CppPath/usr/bin/g++
```

This variable is not required when running SystemC designs. By default, you should install and use the built-in g++ compiler that comes with ModelSim.

Section [sccom]

Syntax

CppPath = <path>

<path> — The path to the g++ executable.

DatasetSeparator

This variable specifies the dataset separator for fully-rooted contexts, for example:

```
sim:/top
```

The variable for DatasetSeparator must not be the same character as the [PathSeparator](#) variable, or the [SignalSpyPathSeparator](#) variable.

Section [vsim]

Syntax

DatasetSeparator = <character>

<character> — Any character except special characters, such as \, {, }, and so forth, where the default is a colon (:).

DefaultForceKind

This variable defines the kind of force used when not otherwise specified.

Section [vsim]

Syntax

DefaultForceKind = {default | deposit | drive | freeze}

default — Uses the signal kind to determine the force kind.

deposit — Sets the object to the specified value.

drive — Default for resolved signals.

freeze — Default for unresolved signals.

You can override this variable by specifying **force** {-default | -deposit | -drive | -freeze}.

Related Topics

You can set this variable in the [The Runtime Options Dialog](#).

You can set this variable interactively with the Tcl [set Command Syntax](#).

DefaultRadix

This variable allows a numeric radix to be specified as a name or number. For example, you can specify binary as “binary” or “2” or octal as “octal” or “8”.

Section [vsim]

Syntax

DefaultRadix = {ascii | binary | decimal | hexadecimal | octal | symbolic | unsigned}

ascii — Display values in 8-bit character encoding.

binary— Display values in binary format. You can also specify 2.

decimal or 10 — Display values in decimal format. You can also specify 10.

hexadecimal— Display values in hexadecimal format. You can also specify 16.

octal— Display values in octal format. You can also specify 8.

symbolic — (default) Display values in a form closest to their natural format.

unsigned — Display values in unsigned decimal format.

You can override this variable by specifying **radix** {ascii | binary | decimal | hexadecimal | octal | symbolic | unsigned}.

Related Topics

You can set this variable in the [The Runtime Options Dialog](#) [Changing Radix \(base\) for the Wave Window](#)

You can set this variable interactively with the Tcl [set Command Syntax](#).

DefaultRestartOptions

This variable sets the default behavior for the restart command.

Section [vsim]

Syntax

```
DefaultRestartOptions = {-force | -noassertions | -nobreakpoint | -nofcovers | -nolist | -nolog | -nowave}
```

- force — Restart simulation without requiring confirmation in a popup window.
- noassertions — Restart simulation without maintaining the current assert directive configurations.
- nobreakpoint — Restart simulation with all breakpoints removed.
- nofcovers — Restart without maintaining the current cover directive configurations.
- nolist — Restart without maintaining the current List window environment.
- nolog — Restart without maintaining the current logging environment.
- nowave — Restart without maintaining the current Wave window environment.
- semicolon (;) — Default is to prevent initiation of the variable by commenting the variable line.

You can specify one or more value in a space separated list.

You can override this variable by specifying `restart` {-force | -noassertions | -nobreakpoint | -nofcovers | -nolist | -nolog | -nowave}.

Related Topics

[checkpoint](#) command [vsim -restore](#)

[Checkpointing and Restoring Simulations](#)

DelayFileOpen

This variable instructs ModelSim to open VHDL87 files on first read or write, else open files when elaborated.

Section [vsim]

Syntax

DelayFileOpen = {0 | 1}
0 — On (default)
1 — Off

Related Topics

You can set this variable interactively with the Tcl [set Command Syntax](#).

displaymsgmode

This variable controls where the simulator outputs system task messages. The display system tasks displayed with this functionality include: \$display, \$strobe, \$monitor, \$write as well as the analogous file I/O tasks that write to STDOUT, such as \$fwrite or \$fdisplay.

Section [msg_system]

Syntax

displaymsgmode = {both | tran | wlf}
both — Outputs messages to both the transcript and the WLF file.
tran — (default) Outputs messages only to the transcript, therefore they are unavailable in the Message Viewer.
wlf — Outputs messages only to the WLF file/Message Viewer, therefore they are unavailable in the transcript.

You can override this variable by specifying [vsim -displaymsgmode](#).

Related Topics

[Message Viewer Window](#)

DpiOutOfTheBlue

This variable enables DPI out-of-the-blue function calls and debugging support for a SystemC method and a SystemC thread. The C functions must not be declared as import tasks or functions.

Section [vsim]

Syntax

DpiOutOfTheBlue = {0 | 1 | 2}
0 — Support for DPI out-of-the-blue calls is disabled.
1 — (default) Support for DPI out-of-the-blue calls is enabled, but debugging support is not available.

2 — Support for DPI out-of-the-blue calls is enabled with debugging support for a SystemC thread.

To turn on debugging support in a SystemC method, you set `DpiOutOfTheBlue = 2`, then specify `vsim -scdpidebug`.

You can override this variable by specifying `vsim -dpioutoftheblue`.

Related Topics

`-dpioutoftheblue` switch to the `vsim` command. `-scdpidebug` switch to the `vsim` command

[Making Verilog Function Calls from non-DPI C Models](#)

DumpportsCollapse

This variable collapses vectors (VCD id entries) in dumpports output.

Section [`vsim`]

Syntax

`DumpportsCollapse = {0 | 1}`

0 — Off

1 — On (default)

You can override this variable by specifying `vsim {+dumpports+collapse | +dumpports+nocollapse}`.

error

This variable changes the severity of the listed message numbers to "error".

Section [`msg_system`]

Syntax

`error = <msg_number>...`

`<msg_number>...`— An unlimited list of message numbers, comma separated.

You can override this variable by specifying the `scom`, `vcom`, `vlog`, `vopt`, or `vsim` command with the `-error argument`.

Related Topics

[verror](#) <msg number> prints a detailed description about a message number.

[fatal](#), [note](#), [suppress](#), [warning](#)

[Changing Message Severity Level](#)

ErrorFile

This variable specifies an alternative file for storing error messages. By default, error messages are output to the file specified by the [TranscriptFile](#) variable in the *modelsim.ini* file. If the `ErrorFile` variable is specified, all error messages will be stored in the specified file, not in the transcript.

Section [vsim]

Syntax

`ErrorFile = <filename>`

<filename> — Any valid filename where the default is *error.log*.

You can override this variable by specifying [vsim](#) -errorfile.

Related Topics

[Creating a Transcript File](#)

Explicit

This variable enables the resolving of ambiguous function overloading in favor of the "explicit" function declaration (not the one automatically created by the compiler for each type declaration). Using this variable makes QuestaSim compatible with common industry practice.

Section [vcom]

Syntax

`Explicit = {0 | 1}`

0 — Off

1 — On (default)

You can override this variable by specifying [vcom](#) -explicit.

fatal

This variable changes the severity of the listed message numbers to "fatal".

Section [msg_system]

Syntax

`fatal = <msg_number>...`

`<msg_number>...`— An unlimited list of message numbers, comma separated.

You can override this variable by specifying the [sccom](#), [vcom](#), [vlog](#), [vopt](#), or [vsim](#) command with the `-fatal` argument.

Related Topics

[verror <msg number>](#) prints a detailed description about a message number.

[Changing Message Severity Level](#)

[error](#), [note](#), [suppress](#), [warning](#)

FsmResetTrans

This variable controls the recognition of asynchronous reset transitions in FSMs.

Sections [[vcom](#)], [[vlog](#)]

Syntax

`FsmResetTrans = { 0 | 1 }`

0 — Off

1 — On (default)

Related Topics

[vcom -fsmresettrans](#) | [-nofsmresettrans](#)

[vlog -fsmresettrans](#) | [-nofsmresettrans](#)

FsmSingle

This variable controls the recognition of FSMs with a single-bit current state variable.

Section [[vcom](#)], [[vlog](#)]

Syntax

`FsmSingle = { 0 | 1 }`

0 — Off

1 — On (default)

Related Topics

vcom -fmsmsingle | -nofmsmsingle
vlog -fmsmsingle | -nofmsmsingle

FsmXAssign

This variable controls the recognition of FSMs where a current-state or next-state variable has been assigned “X” in a case statement.

Section [vlog]

Syntax

FsmXAssign = { 0 | 1 }
0 — Off
1 — On (default)

Related Topics

vlog -fsmxassign | -nofsmxassign

GenerateFormat

This variable controls the format of a generate statement label for each iteration. Do not enclose the argument in quotation marks.

Section [vsim]

Syntax

GenerateFormat = <non-quoted string>

<non-quoted string> — Default is %s_%d. Any non-quoted string containing at a minimum a %s followed by a %d. The format string must contain the conversion codes %s and %d, in that order, and no other conversion codes. The %s represents the generate_label; the %d represents the generate parameter value at a particular generate iteration. Application of the format must result in a unique scope name over all such names in the design so that name lookup can function properly.

GenerateLoopIterationMax

This variable specifies the maximum number of iterations permitted for a generate loop; restricting this permits the implementation to recognize infinite generate loops.

Section [vlog]

Syntax

GenerateLoopIterationMax = <n>

<n> — Any natural integer greater than or equal to 0, where the default is 100000.

GenerateRecursionDepthMax

This variable specifies the maximum depth permitted for a recursive generate instantiation; restricting this permits the implementation to recognize infinite recursions.

Section [vlog]

Syntax

GenerateRecursionDepthMax = <n>

<n> — Any natural integer greater than or equal to 0, where the default is 200.

GenerousIdentifierParsing

Controls parsing of identifiers input to the simulator. If this variable is on (value = 1), either VHDL extended identifiers or Verilog escaped identifier syntax may be used for objects of either language kind. This provides backward compatibility with older *.do* files, which often contain pure VHDL extended identifier syntax, even for escaped identifiers in Verilog design regions.

Section [vsim]

Syntax

GenerousIdentifierParsing = {0 | 1}

0 — Off

1 — On (default)

GlobalSharedObjectsList

This variable instructs ModelSim to load the specified PLI/FLI shared objects with global symbol visibility.

Section [vsim]

Syntax

GlobalSharedObjectsList = <filename>

<filename> — A comma separated list of filenames.

semicolon (;) — (default) Prevents initiation of the variable by commenting the variable line.

You can override this variable by specifying `vsim -gblso`.

Hazard

This variable turns on Verilog hazard checking (order-dependent accessing of global variables).

Section [vlog]

Syntax

Hazard = {0 | 1}

0 — Off (default)

1 — On

ieee

This variable sets the path to the library containing IEEE and Synopsys arithmetic packages.

Section [library]

Syntax

ieee = <path>

<path> — Any valid path, including environment variables where the default is \$MODEL_Tech/./ieee.

IgnoreError

This variable instructs ModelSim to disable runtime error messages.

Section [vsim]

Syntax

IgnoreError = {0 | 1}

0 — Off (default)

1 — On

Related Topics

You can set this variable in the [The Runtime Options Dialog](#).

You can set this variable interactively with the Tcl [set Command Syntax](#).

IgnoreFailure

This variable instructs ModelSim to disable runtime failure messages.

Section [vsim]

Syntax

IgnoreFailure = {0 | 1}

0 — Off (default)

1 — On

Related Topics

You can set this variable in the [The Runtime Options Dialog](#).

You can set this variable interactively with the Tcl [set Command Syntax](#).

IgnoreNote

This variable instructs ModelSim to disable runtime note messages.

Section [vsim]

Syntax

IgnoreNote = {0 | 1}

0 — Off (default)

1 — On

Related Topics

Set this variable in the [The Runtime Options Dialog](#)

You can set this variable interactively with the Tcl [set Command Syntax](#).

IgnoreVitalErrors

This variable instructs ModelSim to ignore VITAL compliance checking errors.

Section [vcom]

Syntax

IgnoreVitalErrors = {0 | 1}

0 — Off, (default) Allow VITAL compliance checking errors.

1 — On

You can override this variable by specifying [vcom -ignorevitalerrors](#).

IgnoreWarning

This variable instructs ModelSim to disable runtime warning messages.

Section [vsim]

Syntax

IgnoreWarning = {0 | 1}

0 — Off, (default) Enable runtime warning messages.

1 — On

Related Topics

You can set this variable in the [The Runtime Options Dialog](#).

You can set this variable interactively with the Tcl [set Command Syntax](#).

ImmediateContinuousAssign

This variable instructs ModelSim to run continuous assignments before other normal priority processes that are scheduled in the same iteration. This event ordering minimizes race differences between optimized and non-optimized designs and is the default behavior.

Section [vsim]

Syntax

ImmediateContinuousAssign = {0 | 1}

0 — Off,

1 — On (default)

You can override this variable by specifying vsim -noimmedca.

IterationLimit

This variable specifies a limit on simulation kernel iterations allowed without advancing time.

Section [vlog]

Syntax

IterationLimit= <n>

<n> — Any positive integer where the default is 5000.

Related Topics

You can set this variable in the [The Runtime Options Dialog](#).

You can set this variable interactively with the Tcl [set Command Syntax](#).

LibrarySearchPath

This variable defines a space separated list of path entries that describe where to find a resource library containing a precompiled package. The behavior of this variable is identical to specifying `vlog -L`.

Section [vlog]

Syntax

LibrarySearchPath= <path ..>

<path> — Any path where the default is \$MODEL_TECH/./avm.

Related Topics

[Specifying Resource Libraries](#).

License

This variable controls the license file search.

Section [vsim]

Syntax

License = <license_option>

<license_option> — One or more license options separated by spaces where the default is to search all licenses.

Table A-5. License Variable: License Options

license_option	Description
lnonly	only use msimhdlsim
mixedonly	exclude single language licenses
noInl	exclude language neutral licenses
nomix	exclude msimhdlmix
noqueue	do not wait in license queue if no licenses are available
noslvhdl	exclude qhsimvh

Table A-5. License Variable: License Options

license_option	Description
noslvlog	exclude qhsimvl
plus	only use PLUS license
vlog	only use VLOG license
vhdl	only use VHDL license

You can override this variable by specifying `vsim <license_option>`.

MaxReportRhsCrossProducts

This variable specifies a maximum limit for the number of Cross (bin) products reported against a Cross when a XML or UCDB report is generated. The warning is issued if the limit is crossed.

Section [vsim]

Syntax

MaxReportRhsCrossProducts = <n>

<n> — Any positive integer where the default is 1000.

MessageFormat

This variable defines the format of VHDL assertion messages as well as normal error messages.

Section [vsim]

Syntax

MessageFormat = <% value>

<% value> — One or more of the variables from [Table A-6](#) where the default is:

```
** %S: %R\n Time: %T Iteration: %D%i\n.
```

Table A-6. MessageFormat Variable: Accepted Values

Variable	Description
%S	severity level
%R	report message
%T	time of assertion
%D	delta
%I	instance or region pathname (if available)
%i	instance pathname with process
%O	process name

Table A-6. MessageFormat Variable: Accepted Values

Variable	Description
%K	kind of object path points to; returns Instance, Signal, Process, or Unknown
%P	instance or region path without leaf process
%F	file
%L	line number of assertion, or if from subprogram, line from which call is made
%%	print '%' character

MessageFormatBreak

This variable defines the format of messages for VHDL assertions that trigger a breakpoint.

Section [vsim]

Syntax

MessageFormatBreak = <% value>

<% value> — One or more of the variables from [Table A-6](#) where the default is:

```
** %S: %R\n Time: %T Iteration: %D %K: %i File: %F\n
```

MessageFormatBreakLine

This variable defines the format of messages for VHDL assertions that trigger a breakpoint. %L specifies the line number of the assertion or, if the breakpoint is from a subprogram, the line from which the call is made.

Section [vsim]

Syntax

MessageFormatBreakLine = <% value>

<% value> — One or more of the variables from [Table A-6](#) where the default is:

```
** %S: %R\n Time: %T Iteration: %D %K: %i File: %F Line: %L\n
```

MessageFormatError

This variable defines the format of all error messages.

If undefined, MessageFormat is used unless the error causes a breakpoint in which case [MessageFormatBreak](#) is used.

Section [vsim]

Syntax

MessageFormatError = <%value>

<%value> — One or more of the variables from [Table A-6](#) where the default is:

```
** %S: %R\n Time: %T Iteration: %D %K: %i File: %F\n
```

MessageFormatFail

This variable defines the format of messages for VHDL Fail assertions.

If undefined, MessageFormat is used unless assertion causes a breakpoint in which case [MessageFormatBreak](#) is used.

Section [vsim]

Syntax

MessageFormatFail = <%value>

<%value> — One or more of the variables from [Table A-6](#) where the default is:

```
** %S: %R\n Time: %T Iteration: %D %K: %i File: %F\n
```

MessageFormatFatal

This variable defines the format of messages for VHDL Fatal assertions.

If undefined, MessageFormat is used unless assertion causes a breakpoint in which case [MessageFormatBreak](#) is used.

Section [vsim]

Syntax

MessageFormatFatal = <%value>

<%value> — One or more of the variables from [Table A-6](#) where the default is:

```
** %S: %R\n Time: %T Iteration: %D %K: %i File: %F\n
```

MessageFormatNote

This variable defines the format of messages for VHDL Note assertions.

If undefined, MessageFormat is used unless assertion causes a breakpoint in which case [MessageFormatBreak](#) is used.

Section [vsim]

Syntax

MessageFormatNote = <%value>

<%value> — One or more of the variables from [Table A-6](#) where the default is:

```
** %S: %R\n Time: %T Iteration: %D%I\n
```

MessageFormatWarning

This variable defines the format of messages for VHDL Warning assertions.

If undefined, MessageFormat is used unless assertion causes a breakpoint in which case [MessageFormatBreak](#) is used.

Section [vsim]

Syntax

MessageFormatWarning = <%value>

<%value> — One or more of the variables from [Table A-6](#) where the default is:

```
** %S: %R\n Time: %T Iteration: %D%I\n
```

modelsim_lib

This variable sets the path to the library containing Mentor Graphics VHDL utilities such as Signal Spy.

Section [library]

Syntax

modelsim_lib = <path>

<path> — Any valid path where the default is \$MODEL_TECH/./modelsim_lib. May include environment variables.

msgmode

This variable controls where the simulator outputs elaboration and runtime messages.

Section [msg_system]

Syntax

msgmode = {tran | wlf | both}

both — (default) Transcript and wlf files.

tran — Messages appear only in the transcript.

wlf — Messages are sent to the wlf file and can be viewed in the MsgViewer.

You can override this variable by specifying [vsim](#) -msgmode.

Related Topics

[Message Viewer Window](#)

MultiFileCompilationUnit

This variable controls whether Verilog files are compiled separately or concatenated into a single compilation unit.

Section [vlog]

Syntax

MultiFileCompilationUnit = {0 | 1}

0 — (default) Single File Compilation Unit (SFCU) mode.

1 — Multi File Compilation Unit (MFCU) mode.

You can override this variable by specifying `vlog {-mfcu | -sfcu}`.

Related Topics

[SystemVerilog Multi-File Compilation](#)

NoAutoSDFCompile

This variable is used to disable automatic SDF compiling for flows that support it.

Section [vsim]

Syntax

NoAutoSDFCompile = {0 | 1}

0 — Off

1 — On (default)

NoCaseStaticError

This variable changes case statement static errors to warnings.

Section [vcom]

Syntax

NoCaseStaticError = {0 | 1}

0 — Off (default)

1 — On

You can override this variable by specifying `vcom -nocasestaticerror`.

Related Topics

[vcom -pedanticerrors](#)

[PedanticErrors](#)

NoDebug

This variable controls inclusion of debugging info within design units.

Sections [vcom], [vlog]

Syntax

NoDebug = {0 | 1}

0 — Off (default)

1 — On

NoIndexCheck

This variable controls run time index checks.

Section [vcom]

Syntax

NoIndexCheck = {0 | 1}

0 — Off (default)

1 — On

You can override NoIndexCheck = 0 by specifying [vcom -noindexcheck](#).

Related Topics

[Range and Index Checking](#)

NoOthersStaticError

This variable disables errors caused by aggregates that are not locally static.

Section [vcom]

Syntax

NoOthersStaticError = {0 | 1}

0 — Off (default)

1 — On

You can override this variable by specifying [vcom -noothersstaticerror](#).

Related Topics

[Changing Message Severity Level](#)

[PedanticErrors](#)

NoRangeCheck

This variable disables run time range checking. In some designs this results in a 2x speed increase.

Section [vcom]

Syntax

NoRangeCheck = {0 | 1}

0 — Off (default)

1 — On

You can override this NoRangeCheck = 1 by specifying [vcom -rangecheck](#).

Related Topics

[Range and Index Checking](#)

note

This variable changes the severity of the listed message numbers to "note".

Section [msg_system]

Syntax

note = <msg_number>...

<msg_number>... — An unlimited list of message numbers, comma separated.

You can override this variable setting by specifying the [sccom](#), [vcom](#), [vlog](#), [vopt](#), or [vsim](#) command with the -note argument.

Related Topics

[verror <msg number>](#) prints a detailed description about a message number.

[Changing Message Severity Level](#)

[error](#), [fatal](#), [suppress](#), [warning](#)

NoVital

This variable disables acceleration of the VITAL packages.

Section [vcom]

Syntax

NoVital = {0 | 1}

0 — Off (default)

1 — On

You can override this variable by specifying `vcom -novital`.

NoVitalCheck

This variable disables VITAL level 0 and Vital level 1 compliance checking.

Section [vcom]

Syntax

NoVitalCheck = {0 | 1}

0 — Off (default)

1 — On

You can override this variable by specifying `vcom -novitalcheck`.

Related Topics

Section 4 of the Vital-95 Spec (IEEE std 1076.4-1995)

NumericStdNoWarnings

This variable disables warnings generated within the accelerated `numeric_std` and `numeric_bit` packages.

Section [vsim]

Syntax

NumericStdNoWarnings = {0 | 1}

0 — Off (default)

1 — On

Related Topics

You can set this variable in the [The Runtime Options Dialog](#).

You can set this variable interactively with the Tcl [set Command Syntax](#).

OnFinish

This variable controls the behavior of ModelSim when it encounters either an assertion failure, a \$finish, or an sc_stop() in the design code.

Section [vsim]

Syntax

OnFinish = {ask | exit | final | stop}

ask — (default) In batch mode, the simulation exits. In GUI mode, a dialog box pops up and asks for user confirmation on whether to quit the simulation.

stop — Causes the simulation to stay loaded in memory. This can make some post-simulation tasks easier.

exit — The simulation exits without asking for any confirmation.

final — The simulation executes all final blocks then exits the simulation.

You can override this variable by specifying `vsim -onfinish`.

OnFinishPendingAssert

This variable prints pending deferred assertion messages. Deferred assertion messages may be scheduled after the \$finish in the same time step. Deferred assertions scheduled to print after the \$finish are printed to the Transcript before exiting. They are printed with severity level NOTE because it is not known whether the assertion is still valid due to being printed in the active region instead of the reactive region where they are normally printed.

Section [vsim]

Syntax

OnFinishPendingAssert = {0 | 1}

0 — Off (default)

1 — On

Optimize_1164

This variable disables optimization for the IEEE std_logic_1164 package.

Section [vcom]

Syntax

Optimize_1164 = {0 | 1}

0 — Off

1 — On (default)

PathSeparator

This variable specifies the character used for hierarchical boundaries of HDL modules. This variable does not affect file system paths. The argument to PathSeparator must not be the same character as DatasetSeparator. This variable setting is also the default for the [SignalSpyPathSeparator](#) variable.

This variable is used by the [vsim](#) and [vopt](#) commands.

Note



When creating a virtual bus, the PathSeparator variable must be set to either a period (.) or a forward slash (/). For more information on creating virtual buses, refer to the section “[Combining Objects into Buses](#)”.

Section [vsim]

Syntax

PathSeparator = <n>

<n> — Any character except special characters, such as \, {, }, and so forth, where the default is a forward slash (/).

Related Topics

[Using Escaped Identifiers](#)

[Preserving Design Visibility with the Learn Flow](#)

You can set this variable interactively with the Tcl [set Command Syntax](#).

PedanticErrors

This variable forces display of an error message (rather than a warning) on a variety of conditions. It overrides the [NoCaseStaticError](#) and [NoOthersStaticError](#) variables.

Section [vcom]

Syntax

PedanticErrors = {0 | 1}

0 — Off (default)

1 — On

Related Topics

[vcom -nocasestaticerror](#)

[vcom -noothersstaticerror](#)

[Enforcing Strict 1076 Compliance](#)

PliCompatDefault

This variable specifies the VPI object model behavior within vsim.

Section [vsim]

Syntax

PliCompatDefault = {1995 | 2001 | 2005 | 2009 | latest}

1995 — Instructs vsim to use the object models as defined in IEEE Std 1364-1995.

When you specify this argument, SystemVerilog objects will not be accessible.

Aliases include:

95

1364v1995

1364V1995

VL1995

VPI_COMPATIBILITY_VERSION_1364v1995

1 — On

2001 — Instructs vsim to use the object models as defined in IEEE Std 1364-2001.

When you specify this argument, SystemVerilog objects will not be accessible.

Aliases include:

01

1364v2001

1364V2001

VL2001

VPI_COMPATIBILITY_VERSION_1364v2001

Note



There are a few cases where the 2005 VPI object model is incompatible with the 2001 model, which is inherent in the specifications.

2005 — Instructs vsim to use the object models as defined in IEEE Std 1800-2005 and IEEE Std 1364-2005. Aliases include:

05

1800v2005

Variables

1800V2005

SV2005

VPI_COMPATIBILITY_VERSION_1800v2005

2009 — Instructs vsim to use the object models as defined in IEEE Std P1800-2009 (unapproved draft standard). Aliases include:

09

1800v2009

1800V2009

SV2009

VPI_COMPATIBILITY_VERSION_1800v2009

latest — (default) This is equivalent to the "2009" argument. This is the default behavior if you do not specify this switch or if you specify the switch without an argument.

You can override this variable by specifying [vsim -plicompatdefault](#).

Related Topics

[Verilog Interfaces to C](#)

PrintSimStats

This variable instructs the simulator to print out simulation statistics at the end of the simulation before it exits.

Section [vsim]

Syntax

PrintSimStats = {0 | 1}

0 — Off (default)

1 — On

You can override this variable by specifying [vsim -printsimstats](#).

Related Topics

[simstats](#)

PrintSVPackageLoadingAttribute

This variable prints the attribute placed upon SV packages during package import when true (1). The attribute will be ignored when this variable entry is false (0). The attribute name is "package_load_message." The value of this attribute is a string literal.

Section [vlog]

Syntax

PrintSVPackageLoadingAttribute = {0 | 1}

- 0 — False
- 1 — True (default)

Protect

This variable enables protect directive processing.

Section [vlog]

Syntax

Protect = {0 | 1}

- 0 — Off (default)
- 1 — On

Related Topics

[Compiler Directives](#)

Quiet

This variable turns off "loading..." messages.

Sections [vcom], [vlog]

Syntax

Quiet = {0 | 1}

- 0 — Off (default)
- 1 — On

You can override this variable by specifying **vlog** -quiet or **vcom** -quiet.

RequireConfigForAllDefaultBinding

This variable instructs the compiler not to generate a default binding during compilation.

Section [vcom]

Syntax

RequireConfigForAllDefaultBinding = {0 | 1}

- 0 — Off (default)
- 1 — On

You can override RequireConfigForAllDefaultBinding = 1 by specifying **vcom** -performdefaultbinding.

Related Topics

[Default Binding](#)

[BindAtCompile](#)

[vcom -ignoredefaultbinding](#)

Resolution

This variable specifies the simulator resolution. The argument must be less than or equal to the [UserTimeUnit](#) and must not contain a space between value and units.

Section [vsim]

Syntax

Resolution = {[n]<time_unit>}

[n] — Optional prefix specifying number of time units as 1, 10, or 100.

<time_unit> — fs, ps, ns, us, ms, or sec where the default is ns ps.

The argument must be less than or equal to the [UserTimeUnit](#) and must not contain a space between value and units, for example:

```
Resolution = 10fs
```

You can override this variable by specifying [vsim -t](#). You should set a smaller resolution if your delays get truncated.

Related Topics

[Time](#) command

RunLength

This variable specifies the default simulation length in units specified by the [UserTimeUnit](#) variable.

Section [vsim]

Syntax

RunLength = <n>

<n> — Any positive integer where the default is 100.

You can override this variable by specifying the [run](#) command.

Related Topics

You can set this variable in the [The Runtime Options Dialog](#).

You can set this variable interactively with the Tcl [set Command Syntax](#).

ScalarOpts

This variable activates optimizations on expressions that do not involve signals, waits, or function/procedure/task invocations.

Sections [vcom], [vlog]

Syntax

ScalarOpts = {0 | 1}

0 — Off (default)

1 — On

SccomLogfile

This variable creates a log file for sccom.

Section [sccom]

Syntax

SccomLogfile = {0 | 1}

0 — Off (default)

1 — On

You can override this variable by specifying [sccom -log](#).

SccomVerbose

This variable prints the name of each sc_module encountered during compilation.

Section [sccom]

Syntax

SccomVerbose = {0 | 1}

0 — Off (default)

1 — On

You can override this variable by specifying [sccom -verbose](#).

ScEnableScSignalWriteCheck

This variable enables a check for multiple writers on a SystemC signal.

Section [vsim]

Syntax

ScEnableScSignalWriteCheck = {0 | 1}

0 — Off (default)

1 — On

ScMainFinishOnQuit

This variable determines when the `sc_main` thread exits. This variable is used to turn off the execution of remainder of `sc_main` upon quitting the current simulation session. Disabling this variable (0) has the following effect: If the cumulative length of `sc_main()` in simulation time units is less than the length of the current simulation run upon quit or restart, `sc_main()` is aborted in the middle of execution. This can cause the simulator to crash if the code in `sc_main` is dependent on a particular simulation state.

On the other hand, one drawback of not running `sc_main` till the end is potential memory leaks for objects created by `sc_main`. By default, the remainder of `sc_main` is executed regardless of delays.

Section [vsim]

Syntax

ScMainFinishOnQuit = {0 | 1}

0 — Off

1 — On (default)

ScMainStackSize

This variable sets the stack size for the `sc_main()` thread process.

Section [vsim]

Syntax

ScMainStackSize = <n>{Kb | Mb | Gb}

<n> — An integer followed by Kb, Mb, Gb where the default is 10Mb.

ScShowIeeeDeprecationWarnings

This variable displays warning messages for many of the deprecated features in Annex C of the IEEE 1666 SystemC Language Reference Manual.

Section [vsim]

Syntax

ScShowIeeeDeprecationWarnings = {0 | 1}

0 — Off (default)

1 — On

ScTimeUnit

This variable sets the default time unit for SystemC simulations.

Section [vsim]

Syntax

ScTimeUnit = {[n]<time_unit>}

[n] — Optional prefix specifying number of time units as 1, 10, or 100.

<time_unit> — fs, ps, ns, us, ms, or sec where the default is 1 ns.

ScvPhaseRelationName

This variable changes the precise name used by SCV to specify “phase” transactions in the WLF file.

Section [vsim]

Syntax

ScvPhaseRelationName = <string>

<string> — Any legal string where the default is mti_phase. Legal C-language identifiers are recommended.

Related Topics

[Parallel Transactions](#)

[Recording Phase Transactions](#)

Show_BadOptionWarning

This variable instructs ModelSim to generate a warning whenever an unknown plus argument is encountered.

Section [vlog]

Syntax

Show_BadOptionWarning = {0 | 1}

0 — Off (default)

1 — On

Show_Lint

This variable instructs ModelSim to display lint warning messages.

Sections [vcom], [vlog]

Syntax

Show_Lint = {0 | 1}

0 — Off (default)

1 — On

You can override this variable by specifying `vlog -lint` or `vcom -lint`.

Show_source

This variable shows source line containing error.

Sections [vcom], [vlog]

Syntax

Show_source = {0 | 1}

0 — Off (default)

1 — On

You can override this variable by specifying the `vlog -source` or `vcom -source`.

Show_VitalChecksWarnings

This variable enables VITAL compliance-check warnings.

Section [vcom]

Syntax

Show_VitalChecksWarnings = {0 | 1}

0 — Off

1 — On (default)

Show_Warning1

This variable enables unbound-component warnings.

Section [vcom]

Syntax

Show_Warning1 = {0 | 1}

0 — Off

1 — On (default)

Show_Warning2

This variable enables process-without-a-wait-statement warnings.

Section [vcom]

Syntax

Show_Warning2 = {0 | 1}

0 — Off

1 — On (default)

Show_Warning3

This variable enables null-range warnings.

Section [vcom]

Syntax

Show_Warning3 = {0 | 1}

0 — Off

1 — On (default)

Show_Warning4

This variable enables no-space-in-time-literal warnings.

Section [vcom]

Syntax

Show_Warning4 = {0 | 1}

0 — Off

1 — On (default)

Show_Warning5

This variable enables multiple-drivers-on-unresolved-signal warnings.

Section [vcom]

Syntax

Show_Warning5 = {0 | 1}

0 — Off

1 — On (default)

ShowConstantImmediateAsserts

This variable controls the display of immediate assertions with constant expressions. By default, immediate assertions with constant expressions are displayed in the GUI, in reports, and in the UCDB.

Section [vcom], [vlog], [vopt]

Syntax

ShowConstantImmediateAsserts = {0 | 1}

0 — Off

1 — On (default)

ShowFunctions

This variable sets the format for Breakpoint and Fatal error messages. When set to 1 (the default value), messages will display the name of the function, task, subprogram, module, or architecture where the condition occurred, in addition to the file and line number. Set to 0 to revert messages to the previous format.

Section [vsim]

Syntax

ShowFunctions = {0 | 1}

0 — Off

1 — On (default)

ShowUnassociatedScNameWarning

This variable instructs ModelSim to display unassociated SystemC name warnings.

Section [vsim]

Syntax

ShowUnassociatedScNameWarning = {0 | 1}

0 — Off (default)

1 — On

ShowUndebuggableScTypeWarning

This variable instructs ModelSim to display undebuggable SystemC type warnings.

Section [vsim]

Syntax

ShowUndebuggableScTypeWarning = {0 | 1}

0 — Off

1 — On (default)

ShutdownFile

This variable calls the [write format restart](#) command upon exit and executes the *.do* file created by that command. This variable should be set to the name of the file to be written, or the value "--disable-auto-save" to disable this feature. If the filename contains the pound sign character (#), then the filename will be sequenced with a number replacing the #. For example, if the file is "restart#.do", then the first time it will create the file "restart1.do" and the second time it will create "restart2.do", and so forth.

Section [vsim]

Syntax

ShutdownFile = <filename>.do | <filename>#.do | --disable-auto-save }

<filename>.do — A user defined filename.

<filename>#.do — A user defined filename with a sequencing character.

--disable-auto-save — Disables auto save.

SignalSpyPathSeparator

This variable specifies a unique path separator for the Signal Spy functions. The argument to SignalSpyPathSeparator must not be the same character as the [DatasetSeparator](#) variable.

Section [vsim]

Syntax

SignalSpyPathSeparator = <character>

<character> — Any character except special characters, such as \, {, }, and so forth, where the default is to use the [PathSeparator](#) variable or a forward slash (/).

Related Topics

[Signal Spy](#)

SparseMemThreshold

This variable specifies the size at which memories will automatically be marked as sparse memory. A memory with depth equal to or more than the sparse memory threshold gets marked as sparse automatically, unless specified otherwise in source code or by the +nonsparse switch to vlog or vopt commands.

Section [vlog]

Syntax

SparseMemThreshold = <n>

<n> — Any non-negative integer where the default is 1048576.

Related Topics

[Sparse Memory Modeling](#)

Startup

This variable specifies a simulation startup macro.

Section [vsim]

Syntax

Startup = {do <DO filename>}

<DO filename> — Any valid macro (do) file where the default is to comment out the line (;).

Related Topics

[do command](#)

[Using a Startup File](#)

std

This variable sets the path to the VHDL STD library.

Section [library]

Syntax

std = <path>

<path> — Any valid path where the default is \$MODEL_TECH/./std. May include environment variables.

std_developerskit

This variable sets the path to the libraries for Mentor Graphics standard developer's kit.

Section [library]

Syntax

std_developerskit = <path>

<path> — Any valid path where the default is \$MODEL_TECH/./std_developerskit. May include environment variables.

StdArithNoWarnings

This variable suppresses warnings generated within the accelerated Synopsys std_arith packages.

Section [vsim]

Syntax

StdArithNoWarnings = {0 | 1}

0 — Off (default)

1 — On

Related Topics

You can set this variable in the [The Runtime Options Dialog](#).

You can set this variable interactively with the Tcl [set Command Syntax](#).

suppress

This variable suppresses the listed message numbers and/or message code strings (displayed in square brackets).

Section [msg_system]

Syntax

suppress = <msg_number>...

<msg_number>...— An unlimited list of message numbers, comma separated.

You can override this variable setting by specifying the [sccom](#), [vcom](#), [vlog](#), [vopt](#), or [vsim](#) command with the -suppress argument.

Related Topics

[verror <msg number>](#) prints a detailed description about a message number.

[Changing Message Severity Level](#)

[error](#), [fatal](#), [note](#), [warning](#)

sv_std

This variable sets the path to the SystemVerilog STD library.

Section [library]

Syntax

sv_std = <path>

<path> — Any valid path where the default is \$MODEL_TECH/./sv_std. May include environment variables.



SVFileExtensions

This variable defines one or more filename suffixes that identify a file as a SystemVerilog file. To insert white space in an extension, use a backslash (\) as a delimiter. To insert a backslash in an extension, use two consecutive backslashes (\\).

Section [vlog]

Syntax

SVFileExtensions = sv svp svh

On — Uncomment the variable.

Off — Comment the variable (;).

Svlog

This variable instructs the vlog compiler to compile in SystemVerilog mode. This variable does not exist in the default *modelsim.ini* file, but is added when you select Use SystemVerilog in the Compile Options dialog box > Verilog and SystemVerilog tab.

Section [vlog]

Syntax

Svlog = {0 | 1}

0 — Off (default)

1 — On

synopsys

This variable sets the path to the accelerated arithmetic packages.

Section [vsim]

Syntax

synopsys = <library>

<path> — Any valid path where the default is \$MODEL_TECH/./synopsys. May include environment variables.

ToggleCountLimit

This variable limits the toggle coverage count for a toggle node. After the limit is reached, further activity on the node will be ignored for toggle coverage. All possible transition edges must reach this count for the limit to take effect. For example, if you are collecting toggle data on 0->1 and 1->0 transitions, both transition counts must reach the limit. If you are collecting full data on 6 edge transitions, all 6 must reach the limit. If the limit is set to zero, then it is treated as unlimited.

Section [vsim]

Syntax

ToggleCountLimit = <n>

<n> — Any non-negative integer with a maximum positive value of a 32-bit signed integer and a default of 1.

You can override this variable by specifying [vsim -togglecountlimit](#) or [toggle add -countlimit](#).

ToggleFixedSizeArray

This variable is used to control whether Verilog fixed-size arrays are included for toggle coverage.

Section [vsim]

Syntax

ToggleFixedSizeArray = {0 | 1}

0 — Off (default)

1 — On

You can override this variable by specifying [vsim {-togglefixedsizearray | -notogglefixedsizearray}](#).

Related Topics

You can set this variable interactively with the Tcl [set Command Syntax](#).

ToggleMaxFixedSizeArray

This variable is used to control the limit on the size of Verilog fixed-size arrays that are included for toggle coverage.

Section [vsim]

Syntax

ToggleMaxFixedSizeArray = <n>

<n> — Any positive integer where the default is 100.

You can override this variable by specifying [vsim -togglemaxfixedsizearray](#).

Related Topics

You can set this variable interactively with the Tcl [set Command Syntax](#).

ToggleMaxIntValues

This variable sets the maximum number of unique VHDL integer values to record with toggle coverage.

Section [vsim]

Syntax

ToggleMaxIntValues = <n>

<n> — Any positive integer where the default is 100.

You can override this variable by specifying [vsim -togglemaxintvalues](#).

Related Topics

You can set this variable interactively with the Tcl [set Command Syntax](#).

ToggleMaxRealValues

This variable sets the maximum number of unique SystemVerilog real values to record with toggle coverage.

Section [vsim]

Syntax

ToggleMaxIntValues = <n>

<n> — Any positive integer where the default is 100.

You can override this variable by specifying [vsim -togglemaxrealvalues](#).

Related Topics

You can set this variable interactively with the Tcl [set Command Syntax](#).

ToggleNoIntegers

This variable controls the automatic inclusion of VHDL integer types in toggle coverage.

Section [vsim]

Syntax

ToggleNoIntegers = {0 | 1}

0 — Off

1 — On (default)

You can override this variable by specifying [vsim -notoggoints](#).

TogglePackedAsVec

This variable controls the treatment of packed vectors and structures as reg-vectors in toggle coverage.

Short Description

Section [vsim]

Syntax

TogglePackedAsVec = {0 | 1}

0 — Off (default)

1 — On

You can override this variable by specifying the [vcom](#), [vlog](#) or [vsim](#) command with the `-togglepackedasvec` argument.

ToggleVlogEnumBits

This variable controls toggle coverage for SystemVerilog enumerated types.

Section [vsim]

Syntax

ToggleVlogEnumBits = {0 | 1}

0 — Off (default)

1 — On

You can override this variable by specifying [vsim](#) `-togglevlogenumbits`.

ToggleVlogIntegers

This variable controls toggle coverage for SystemVerilog integer types (that is, byte, shortint, int, longint, but not enumeration types).

Section [vsim]

Syntax

ToggleVlogIntegers = {0 | 1}

0 — Off

1 — On (default)

You can override this variable by specifying [vsim](#) `[-togglevlogints | -notogglevlogints]`.

ToggleVlogReal

This variable controls toggle coverage for SystemVerilog real value types.

Section [vsim]

Syntax

ToggleVlogReal = {0 | 1}

0 — Off (default)

1 — On

You can override this variable by specifying `vsim {-togglevlogreal | nottogglevlogreal}`.

ToggleWidthLimit

This variable limits the width of signals that are automatically added to toggle coverage with the `+cover=t` argument for `vcom` or `vlog`. The limit applies to Verilog registers and VHDL arrays. A value of 0 is taken as unlimited.

Section [vsim]

Syntax

ToggleWidthLimit = <n>

<n> — Any non-negative integer with a maximum positive value of a 32-bit signed integer and a default of 128.

You can override this variable by specifying `vsim -togglewidthlimit`.

Related Topics

-togglewidthlimit switch with the `vcom` and `vlog` commands

TranscriptFile

This variable specifies a file for saving a command transcript. You can specify environment variables in the pathname.

Section [vsim]

Syntax

TranscriptFile = {<filename> | transcript}

<filename> — Any valid filename where transcript is the default.

Related Topics

[transcript file](#) command

[AssertFile](#)

UCDBFilename

This variable specifies the default unified coverage database file name that is written at the end of the simulation. If this variable is set, the UCDB is saved automatically at the end of simulation. All coverage statistics are saved to the specified *.ucdb* file.

Section [vsim]

Syntax

UCDBFilename = {<filename> | *vsim.ucdb*}

<filename> — Any valid filename where *vsim.ucdb* is the default.

UnbufferedOutput

This variable controls VHDL and Verilog files open for write.

Section [vsim]

Syntax

UnbufferedOutput = {0 | 1}

0 — Off, Buffered (default)

1 — On, Unbuffered

UpCase

This variable instructs ModelSim to activate the conversion of regular Verilog identifiers to uppercase and allows case insensitivity for module names.

Section [vlog]

Syntax

UpCase = {0 | 1}

0 — Off (default)

1 — On

Related Topics

[Verilog-XL Compatible Compiler Arguments](#)

UserTimeUnit

This variable specifies the multiplier for simulation time units and the default time units for commands such as [force](#) and [run](#). Generally, you should set this variable to default, in which case it takes the value of the [Resolution](#) variable.

Note

The value you specify for UserTimeUnit does not affect the display in the Wave window. To change the time units for the X-axis in the Wave window, choose Wave > Wave Preferences > Grid & Timeline from the main menu and specify a value for Grid Period.

Section [vsim]

Syntax

UserTimeUnit = {<time_unit> | default}
<time_unit> — fs, ps, ns, us, ms, sec, or default.

Related Topics

[RunLength](#) variable.

You can set this variable interactively with the Tcl [set Command Syntax](#).

UseScv

This variable enables the use of SCV include files and verification library.

Section [sccom]

Syntax

UseScv = {0 | 1}
0 — Off (default)
1 — On

You can override this variable by specifying [sccom -scv](#).

verilog

This variable sets the path to the library containing VHDL/Verilog type mappings.

Section [library]

Syntax

verilog = <path>

<path> — Any valid path where the default is \$MODEL_TECH/./verilog. May include environment variables.

Veriuser

This variable specifies a list of dynamically loadable objects for Verilog PLI/VPI applications.

Section [vsim]

Syntax

Veriuser = <name>

<name> — One or more valid shared object names where the default is to comment out the variable.

Related Topics

-pli switch to the [vsim](#) command. [restart](#) command.

[Registering PLI Applications](#)

VHDL93

This variable enables support for VHDL language version.

Section [vcom]

Syntax

VHDL93 = {0 | 1 | 2 | 3 | 1987 | 1993 | 2002 | 2008}

0 — Support for VHDL-1987. You can also specify 1987.

1 — Support for VHDL-1993. You can also specify 1993.

2 — Support for VHDL-2002 (default). You can also specify 2002.

3 — Support for VHDL-2008. You can also specify 2008.

You can override this variable by specifying [vcom](#) {-87 | -93 | -2002 | -2008}.

vital2000

This variable sets the path to the VITAL 2000 library.

Section [library]

Syntax

vital2000 = <path>

<path> — Any valid path where the default is \$MODEL_TECH/./vital2000. May include environment variables.

vlog95compat

This variable instructs ModelSim to disable SystemVerilog and Verilog 2001 support, making the compiler revert to IEEE Std 1364-1995 syntax.

Section [vlog]

Syntax

vlog95compat = {0 | 1}

0 — Off (default)

1 — On

You can override this variable by specifying `vlog -vlog95compat`.

VoptAutoSDFCompile

This variable controls whether or not SDF files are compiled as part of the design-wide optimizations vopt performs when automatic optimizations are performed.

This functionality applies only to SDF files specified with the `-sdftyp` switch on the `vsim` command line. It does not apply to `$sdf_annotate` system tasks, which will always be compiled.

Section [vsim]

Syntax

VoptAutoSDFCompile = {0 | 1}

0 — Off, SDF files are not compiled in with the design.

1 — On (default), SDF files are compiled as part of design-wide optimizations.

Related Topics

[Performing Optimization on Designs Containing SDF](#)

VoptFlow

This variable controls whether ModelSim operates in optimized mode or full visibility mode.

Section [vsim]

Syntax

VoptFlow = {0 | 1}

Variables

0 — Off, Design is compiled and simulated without optimizations, maintaining full visibility.

1 — On (default), vopt is invoked automatically on the design and the design is fully optimized.

You can override VoptFlow = 0 by specifying [vsim -vopt](#).

Related Topics

[Optimizing Designs with vopt](#)

[Using SV Bind With or Without vopt](#)

WarnConstantChange

This variable controls whether a warning is issued when the change command changes the value of a VHDL constant or generic.

Section [vsim]

Syntax

WarnConstantChange = {0 | 1}

0 — Off

1 — On (default)

Related Topics

[change](#) command

warning

This variable changes the severity of the listed message numbers to "warning".

Section [msg_system]

Syntax

warning = <msg_number>...

<msg_number>... — An unlimited list of message numbers, comma separated.

You can override this variable setting by specifying the [sccom](#), [vcom](#), [vlog](#), [vopt](#), or [vsim](#) command with the -warning argument.

Related Topics

[verror <msg number>](#) prints a detailed description about a message number.

[error](#), [fatal](#), [note](#), [suppress](#)

[Changing Message Severity Level](#)

WaveSignalNameWidth

This variable controls the number of visible hierarchical regions of a signal name shown in the [Wave Window](#).

Section [vsim]

Syntax

WaveSignalNameWidth = <n>

<n> — Any non-negative integer where the default is 0 (display full path). 1 displays only the leaf path element, 2 displays the last two path elements, and so on.

You can override this variable by specifying [configure -signalnamewidth](#).

WLFCacheSize

This variable sets the number of megabytes for the WLF reader cache. WLF reader caching caches blocks of the WLF file to reduce redundant file I/O.

Section [vsim]

Syntax

WLFCacheSize = <n>

<n> — Any non-negative integer where the default is 0.

You can override this variable by specifying [vsim -wlf cachesize](#).

Related Topics

[WLF File Parameter Overview](#)

WLFCollapseMode

This variable controls when the WLF file records values.

Section [vsim]

Syntax

WLFCollapseMode = {0 | 1 | 2}

0 — Preserve all events and event order. Same as [vsim -wlf nocollapse](#).

Variables

- 1 — (default) Only record values of logged objects at the end of a simulator iteration. Same as `vsim -wlfcollapsedelta`.
- 2 — Only record values of logged objects at the end of a simulator time step. Same as `vsim -wlfcollapsetime`.

You can override this variable by specifying `vsim {-wlfnocollapse | -wlfcollapsedelta | -wlfcollapsetime}`.

Related Topics

[WLF File Parameter Overview](#)

WLFCompress

This variable enables WLF file compression.

Section [vsim]

Syntax

WLFCompress = {0 | 1}

0 — Off

1 — On (default)

You can override this variable by specifying `vsim -wlfnocompress`.

Related Topics

[WLF File Parameter Overview](#)

`vsim -wlfcompress`.

You can set this variable in the [The Runtime Options Dialog](#).

WLFDeleteOnQuit

This variable specifies whether a WLF file should be deleted when the simulation ends.

Section [vsim]

Syntax

WLFDeleteOnQuit = {0 | 1}

0 — Off (default), Do not delete.

1 — On

You can override this variable by specifying `vsim -wlfnodeleteonquit`.

Related Topics

[WLF File Parameter Overview](#)

`vsim -wlfdeleteonquit`.

You can set this variable in the [The Runtime Options Dialog](#).

WLFfilename

This variable specifies the default WLF file name.

Section [vsim]

Syntax

WLFfilename = {<filename> | *vsim.wlf*}

<filename> — User defined WLF file to create.

vsim.wlf — (default) filename

You can override this variable by specifying `vsim -wlf`.

Related Topics

[WLF File Parameter Overview](#)

You can set this variable interactively with the Tcl [set Command Syntax](#).

WLFIndex

This variable determines whether or not a WLF file should be indexed during simulation.

Section [vsim]

Syntax

WLFIndex = {0 | 1}

0 — Off

1 — On (default), Index.

WLFOptimize

This variable specifies whether the viewing of waveforms is optimized.

Section [vsim]

Syntax

WLFOptimize = {0 | 1}

0 — Off

1 — On (default)

You can override this variable by specifying [vsim -wlfnoopt](#).

Related Topics

[WLF File Parameter Overview](#)

[vsim -wlfopt](#).

WLFSaveAllRegions

This variable specifies the regions to save in the WLF file.

Section [vsim]

Syntax

WLFSaveAllRegions= {0 | 1}

0 — (default), Only save regions containing logged signals.

1 — Save all design hierarchy.

Related Topics

You can set this variable in the [The Runtime Options Dialog](#).

WLFSimCacheSize

This variable sets the number of megabytes for the WLF reader cache for the current simulation dataset only. WLF reader caching caches blocks of the WLF file to reduce redundant file I/O. This makes it easier to set different sizes for the WLF reader cache used during simulation, and those used during post-simulation debug. If neither [vsim -wlfsimcachesize](#), nor the [WLFCacheSize](#) variable is specified, the [WLFCacheSize](#) variable is used.

Section [vsim]

Syntax

WLFSimCacheSize = <n>

<n> — Any non-negative integer where the default is 0.

You can override this variable by specifying [vsim -wlfsimcachesize](#).

Related Topics

[WLF File Parameter Overview](#)

WLFSizeLimit

This variable limits the WLF file by size (as closely as possible) to the specified number of megabytes; if both size ([WLFSizeLimit](#)) and time ([WLFTimeLimit](#)) limits are specified the most restrictive is used.

Section [vsim]

Syntax

WLFSizeLimit = <n>

<n> — Any non-negative integer in units of MB where the default is 0 (unlimited).

You can override this variable by specifying [vsim -wlfslim](#).

Related Topics

[WLF File Parameter Overview](#)

[Limiting the WLF File Size](#)

You can set this variable interactively with the Tcl [set Command Syntax](#).

WLFTimeLimit

This variable limits the WLF file by time (as closely as possible) to the specified amount of time. If both time and size limits are specified the most restrictive is used.

Section [vsim]

Syntax

WLFTimeLimit = <n>

<n> — Any non-negative integer in units of MB where the default is 0 (unlimited).

You can override this variable by specifying [vsim -wlfslim](#).

Related Topics

[WLF File Parameter Overview](#)

[Limiting the WLF File Size](#)

You can set this variable in the [The Runtime Options Dialog](#).

You can set this variable interactively with the Tcl [set Command Syntax](#).

WLFUseThreads

This variable specifies whether the logging of information to the WLF file is performed using multithreading.

Section [vsim]

Syntax

WLFUseThreads = {0 | 1}

0 — Off, Windows systems only, or when one processor is available.

1 — On, Linux or Solaris systems only, with more than one processor on the system. When this behavior is enabled, the logging of information is performed by the secondary processor while the simulation and other tasks are performed by the primary processor.

You can override this variable by specifying [vsim](#) {-wlfthreads | -wlfnothreads}.

ZeroIn

This variable instructs vsim to automatically invoke 0in ccl.

Sections [vcom], [vlog], [vsim]

Syntax

ZeroIn = {0 | 1}

0 — Off (default)

1 — On

You can override this variable by specifying [vsim](#) -0in.

ZeroInOptions

This variable passes options to 0in ccl.

Section [vcom], [vlog], [vsim]

Syntax

ZeroInOptions = <option>

<option> — Any valid 0-in options where the default is quotation marks (“”).

You can override this variable by specifying `vsim -0in_options`.

Commonly Used modelsim.ini Variables

Several of the more commonly used *modelsim.ini* variables are further explained below.



Tip: When a design is loaded, you can use the `where` command to display which *modelsim.ini* or ModelSim Project File (*.mpf*) file is in use.

Common Environment Variables

You can use environment variables in an initialization file. Insert a dollar sign (\$) before the name of the environment variable so that its defined value is used. For example:

```
[Library]
work = $HOME/work_lib
test_lib = ./$TESTNUM/work
...
[vsim]
IgnoreNote = $IGNORE_ASSERTS
IgnoreWarning = $IGNORE_ASSERTS
IgnoreError = 0
IgnoreFailure = 0
```

Note



The `MODEL_TECH` environment variable is a special variable that is set by ModelSim (it is not user-definable). ModelSim sets this value to the name of the directory from which the `VCOM` or `VLOG` compilers or the `VSIM` simulator was invoked. This directory is used by other ModelSim commands and operations to find the libraries.

Hierarchical Library Mapping

By adding an "others" clause to your *modelsim.ini* file, you can have a hierarchy of library mappings. If the ModelSim tools do not find a mapping in the *modelsim.ini* file, then they will search only the library section of the initialization file specified by the "others" clause. For example:

```
[Library]
asic_lib = /cae/asic_lib
work = my_work
others = /install_dir/modeltech/modelsim.ini
```

Since the file referred to by the "others" clause may itself contain an "others" clause, you can use this feature to chain a set of hierarchical INI files for library mappings.

Creating a Transcript File

A feature in the system initialization file allows you to keep a record of everything that occurs in the transcript: error messages, assertions, commands, command outputs, and so forth. To do this, set the value for the [TranscriptFile](#) line in the *modelsim.ini* file to the name of the file in which you would like to record the ModelSim history.

```
; Save the command window contents to this file
TranscriptFile = trnsrpt
```

You can disable the creation of the transcript file by using the following ModelSim command immediately after ModelSim starts:

```
transcript file ""
```

Using a Startup File

The system initialization file allows you to specify a command or a *do* file that is to be executed after the design is loaded. For example:

```
; VSIM Startup command
Startup = do mystartup.do
```

The line shown above instructs ModelSim to execute the commands in the macro file named *mystartup.do*.

```
; VSIM Startup command
Startup = run -all
```

The line shown above instructs VSIM to run until there are no events scheduled.

See the [do](#) command for additional information on creating do files.

Turning Off Assertion Messages

You can turn off assertion messages from your VHDL code by setting a switch in the *modelsim.ini* file. This option was added because some utility packages print a huge number of warnings.

```
[vsim]
IgnoreNote = 1
IgnoreWarning = 1
IgnoreError = 1
IgnoreFailure = 1
```

Turning off Warnings from Arithmetic Packages

You can disable warnings from the Synopsys and numeric standard packages by adding the following lines to the [vsim] section of the *modelsim.ini* file.

```
[vsim]
NumericStdNoWarnings = 1
StdArithNoWarnings = 1
```

These variables can also be set interactively using the Tcl [set Command Syntax](#). This capability provides an answer to a common question about disabling warnings at time 0. You might enter commands like the following in a DO file or at the ModelSim prompt:

```
set NumericStdNoWarnings 1
run 0
set NumericStdNoWarnings 0
run -all
```

Force Command Defaults

The [force](#) command has -freeze, -drive, and -deposit options. When none of these is specified, then -freeze is assumed for unresolved signals and -drive is assumed for resolved signals. But if you prefer -freeze as the default for both resolved and unresolved signals, you can change the defaults in the *modelsim.ini* file.

```
[vsim]
; Default Force Kind
; The choices are freeze, drive, or deposit
DefaultForceKind = freeze
```

Restart Command Defaults

The [restart](#) command has -force, -nobreakpoint, -nofcovers, -nolist, -nolog, and -nowave options. You can set any of these as defaults by entering the following line in the *modelsim.ini* file:

```
DefaultRestartOptions = <options>
```

where <options> can be one or more of -force, -nobreakpoint, -nofcovers, -nolist, -nolog, and -nowave.

Example:

```
DefaultRestartOptions = -nolog -force
```

VHDL Standard

You can specify which version of the 1076 Std ModelSim follows by default using the [VHDL93](#) variable:

Commonly Used modelsim.ini Variables

```
[vcom]
; VHDL93 variable selects language version as the default.
; Default is VHDL-2002.
; Value of 0 or 1987 for VHDL-1987.
; Value of 1 or 1993 for VHDL-1993.
; Default or value of 2 or 2002 for VHDL-2002.
VHDL93 = 2002
```

Opening VHDL Files

You can delay the opening of VHDL files with an entry in the *INI* file if you wish. Normally VHDL files are opened when the file declaration is elaborated. If the [DelayFileOpen](#) option is enabled, then the file is not opened until the first read or write to that file.

```
[vsim]
DelayFileOpen = 1
```

Appendix B

Location Mapping

Pathnames to source files are recorded in libraries by storing the working directory from which the compile is invoked and the pathname to the file as specified in the invocation of the compiler. The pathname may be either a complete pathname or a relative pathname.

Referencing Source Files with Location Maps

ModelSim tools that reference source files from the library locate a source file as follows:

- If the pathname stored in the library is complete, then this is the path used to reference the file.
- If the pathname is relative, then the tool looks for the file relative to the current working directory. If this file does not exist, then the path relative to the working directory stored in the library is used.

This method of referencing source files generally works fine if the libraries are created and used on a single system. However, when multiple systems access a library across a network, the physical pathnames are not always the same and the source file reference rules do not always work.

Using Location Mapping

Location maps are used to replace prefixes of physical pathnames in the library with environment variables. The location map defines a mapping between physical pathname prefixes and environment variables.

ModelSim tools open the location map file on invocation if the [MGC_LOCATION_MAP](#) environment variable is set. If [MGC_LOCATION_MAP](#) is not set, ModelSim will look for a file named *"mgc_location_map"* in the following locations, in order:

- the current directory
- your home directory
- the directory containing the ModelSim binaries
- the ModelSim installation directory

Use these two steps to map your files:

1. Set the environment variable `MGC_LOCATION_MAP` to the path of your location map file.
2. Specify the mappings from physical pathnames to logical pathnames:

```
$SRC
/home/vhdl/src
/usr/vhdl/src

$IEEE
/usr/modeltech/ieee
```

Pathname Syntax

The logical pathnames must begin with `$` and the physical pathnames must begin with `/`. The logical pathname is followed by one or more equivalent physical pathnames. Physical pathnames are equivalent if they refer to the same physical directory (they just have different pathnames on different systems).

How Location Mapping Works

When a pathname is stored, an attempt is made to map the physical pathname to a path relative to a logical pathname. This is done by searching the location map file for the first physical pathname that is a prefix to the pathname in question. The logical pathname is then substituted for the prefix. For example, `"/usr/vhdl/src/test.vhd"` is mapped to `"$SRC/test.vhd"`. If a mapping can be made to a logical pathname, then this is the pathname that is saved. The path to a source file entry for a design unit in a library is a good example of a typical mapping.

For mapping from a logical pathname back to the physical pathname, ModelSim expects an environment variable to be set for each logical pathname (with the same name). ModelSim reads the location map file when a tool is invoked. If the environment variables corresponding to logical pathnames have not been set in your shell, ModelSim sets the variables to the first physical pathname following the logical pathname in the location map. For example, if you don't set the `SRC` environment variable, ModelSim will automatically set it to `"/home/vhdl/src"`.

Mapping with TCL Variables

Two Tcl variables may also be used to specify alternative source-file paths; `SourceDir` and `SourceMap`. You would define these variables in a `modelsim.tcl` file. See [The modelsim.tcl File](#) for details.

Appendix C

Error and Warning Messages

Message System

The ModelSim message system helps you identify and troubleshoot problems while using the application. The messages display in a standard format in the Transcript pane. Accordingly, you can also access them from a saved transcript file (see [Saving the Transcript File](#) for more details).

Message Format

The format for the messages is:

```
** <SEVERITY LEVEL>: ([<Tool>[-<Group>]]-<MsgNum>) <Message>
```

- **SEVERITY LEVEL** — may be one of the following:

Table C-1. Severity Level Types

severity level	meaning
Note	This is an informational message.
Warning	There may be a problem that will affect the accuracy of your results.
Error	The tool cannot complete the operation.
Fatal	The tool cannot complete execution.
INTERNAL ERROR	This is an unexpected error that should be reported to your support representative.

- **Tool** — indicates which ModelSim tool was being executed when the message was generated. For example, tool could be vcom, vdel, vsim, and so forth.
- **Group** — indicates the topic to which the problem is related. For example group could be PLI, VCD, and so forth.

Example

```
# ** Error: (vsim-PLI-3071) ./src/19/testfile(77): $fdumplimit : Too few arguments.
```

Getting More Information

Each message is identified by a unique MsgNum id. You can access additional information about a message using the unique id and the [verror](#) command. For example:

```
% verror 3071
Message # 3071:
Not enough arguments are being passed to the specified system task or
function.
```

Changing Message Severity Level

You can suppress or change the severity of notes, warnings, and errors that come from **vcom**, **vlog**, and **vsim**. You cannot change the severity of or suppress Fatal or Internal messages.

There are three ways to modify the severity of or suppress notes, warnings, and errors:

- Use the `-error`, `-fatal`, `-note`, `-suppress`, and `-warning` arguments to [sccom](#), [vcom](#), [vlog](#), [vopt](#), or [vsim](#). See the command descriptions in the Reference Manual for details on those arguments.
- Use the [suppress](#) command.
- Set a permanent default in the `[msg_system]` section of the *modelsim.ini* file. See [modelsim.ini Variables](#) for more information.

Suppressing Warning Messages

You can suppress some warning messages. For example, you may receive warning messages about unbound components about which you are not concerned.

Suppressing VCOM Warning Messages

Use the `-nowarn <category_number>` argument with the [vcom command](#) to suppress a specific warning message. For example:

```
vcom -nowarn 1
```

suppresses unbound component warning messages.

Alternatively, warnings may be disabled for all compiles via the Main window **Compile > Compile Options** menu selections or the *modelsim.ini* file (see [modelsim.ini Variables](#)).

The warning message category numbers are:


```
1 = unbound component
2 = process without a wait statement
3 = null range
4 = no space in time literal
5 = multiple drivers on unresolved signal
6 = VITAL compliance checks ("VitalChecks" also works)
7 = VITAL optimization messages
8 = lint checks
9 = signal value dependency at elaboration
10 = VHDL-1993 constructs in VHDL-1987 code
13 = constructs that coverage can't handle
14 = locally static error deferred until simulation run
```

These numbers are unrelated to **vcom** arguments that are specified by numbers, such as **vcom -87** – which disables support for VHDL-1993 and 2002.

Suppressing VLOG Warning Messages

As with the **vcom** command, you can use the **-nowarn <category_number>** argument with the **vlog** command to suppress a specific warning message. The warning message category numbers for **vlog** are:

```
12 = non-LRM compliance in order to match Cadence behavior
13 = constructs that coverage can't handle
```

Or, you can use the **+nowarn<CODE>** argument with the **vlog** command to suppress a specific warning message. Warnings that can be disabled include the **<CODE>** name in square brackets in the warning message. For example:

```
vlog +nowarnDECAY
```

suppresses decay warning messages.

Suppressing VOPT Warning Messages

Use the **-nowarn <category_number>** argument with the **vopt** command to suppress a specific warning message. For example:

```
vopt -nowarn 1
```

suppresses unbound component warning messages.

Alternatively, warnings may be disabled for all compiles via the Main window **Compile > Compile Options** menu selections or the *modelsim.ini* file (see [modelsim.ini Variables](#)).

The warning message category numbers are:

Exit Codes

```

1 = unbound component
2 = process without a wait statement
3 = null range
4 = no space in time literal
5 = multiple drivers on unresolved signal
6 = VITAL compliance checks ("VitalChecks" also works)
7 = VITAL optimization messages
8 = lint checks
9 = signal value dependency at elaboration
10 = VHDL-1993 constructs in VHDL-1987 code
12 = non-LRM compliance in order to match Cadence behavior
13 = constructs that coverage can't handle
14 = locally static error deferred until simulation run

```

Or, you can use the **+nowarn<CODE>** argument with the **vopt** command to suppress a specific warning message. Warnings that can be disabled include the **<CODE>** name in square brackets in the warning message. For example:

```
vopt +nowarnDECAY
```

suppresses decay warning messages.

Suppressing VSIM Warning Messages

Use the **+nowarn<CODE>** argument to **vsim** to suppress a specific warning message. Warnings that can be disabled include the **<CODE>** name in square brackets in the warning message. For example:

```
vsim +nowarnTFMPC
```

suppresses warning messages about too few port connections.

Exit Codes

The table below describes exit codes used by ModelSim tools.

Table C-2. Exit Codes

Exit code	Description
0	Normal (non-error) return
1	Incorrect invocation of tool
2	Previous errors prevent continuing
3	Cannot create a system process (execv, fork, spawn, and so forth.)
4	Licensing problem
5	Cannot create/open/find/read/write a design library

Table C-2. Exit Codes

Exit code	Description
6	Cannot create/open/find/read/write a design unit
7	Cannot open/read/write/dup a file (open, lseek, write, mmap, munmap, fopen, fdopen, fread, dup2, and so forth.)
8	File is corrupted or incorrect type, version, or format of file
9	Memory allocation error
10	General language semantics error
11	General language syntax error
12	Problem during load or elaboration
13	Problem during restore
14	Problem during refresh
15	Communication problem (Cannot create/read/write/close pipe/socket)
16	Version incompatibility
19	License manager not found/unreadable/unexecutable (vlm/mgvlm)
22	SystemC link error
23	SystemC DPI internal error
24	SystemC archive error
42	Lost license
43	License read/write failure
44	Modeltech daemon license checkout failure #44
45	Modeltech daemon license checkout failure #45
90	Assertion failure (SEVERITY_QUIT)
99	Unexpected error in tool
100	GUI Tcl initialization failure
101	GUI Tk initialization failure
102	GUI IncrTk initialization failure
111	X11 display error
202	Interrupt (SIGINT)
204	Illegal instruction (SIGILL)
205	Trace trap (SIGTRAP)

Table C-2. Exit Codes

Exit code	Description
206	Abort (SIGABRT)
208	Floating point exception (SIGFPE)
210	Bus error (SIGBUS)
211	Segmentation violation (SIGSEGV)
213	Write on a pipe with no reader (SIGPIPE)
214	Alarm clock (SIGALRM)
215	Software termination signal from kill (SIGTERM)
216	User-defined signal 1 (SIGUSR1)
217	User-defined signal 2 (SIGUSR2)
218	Child status change (SIGCHLD)
230	Exceeded CPU limit (SIGXCPU)
231	Exceeded file size limit (SIGXFSZ)

Miscellaneous Messages

This section describes miscellaneous messages which may be associated with ModelSim.

Compilation of DPI Export TFs Error

```
# ** Fatal: (vsim-3740) Can't locate a C compiler for compilation of  
DPI export tasks/functions.
```

- Description — ModelSim was unable to locate a C compiler to compile the DPI exported tasks or functions in your design.
- Suggested Action — Make sure that a C compiler is visible from where you are running the simulation.

Empty port name warning

```
# ** WARNING: [8] <path/file_name>: empty port name in port list.
```

- Description — ModelSim reports these warnings if you use the **-lint** argument to **vlog**. It reports the warning for any NULL module ports.
- Suggested action — If you wish to ignore this warning, do not use the **-lint** argument.

Lock message

waiting for lock by user@user. Lockfile is <library_path>/_lock

- Description — The `_lock` file is created in a library when you begin a compilation into that library, and it is removed when the compilation completes. This prevents simultaneous updates to the library. If a previous compile did not terminate properly, ModelSim may fail to remove the `_lock` file.
- Suggested action — Manually remove the `_lock` file after making sure that no one else is actually using that library.

Metavalue detected warning

Warning: NUMERIC_STD.">": metavalue detected, returning FALSE

- Description — This warning is an assertion being issued by the IEEE `numeric_std` package. It indicates that there is an 'X' in the comparison.
- Suggested action — The message does not indicate which comparison is reporting the problem since the assertion is coming from a standard package. To track the problem, note the time the warning occurs, restart the simulation, and run to one time unit before the noted time. At this point, start stepping the simulator until the warning appears. The location of the blue arrow in a Source window will be pointing at the line following the line with the comparison.

These messages can be turned off by setting the `NumericStdNoWarnings` variable to 1 from the command line or in the `modelsim.ini` file.

Sensitivity list warning

signal is read by the process but is not in the sensitivity list

- Description — ModelSim outputs this message when you use the `-check_synthesis` argument to `vcom`. It reports the warning for any signal that is read by the process but is not in the sensitivity list.
- Suggested action — There are cases where you may purposely omit signals from the sensitivity list even though they are read by the process. For example, in a strictly sequential process, you may prefer to include only the clock and reset in the sensitivity list because it would be a design error if any other signal triggered the process. In such cases, your only option is to not use the `-check_synthesis` argument.

Tcl Initialization error 2

```
Tcl_Init Error 2 : Can't find a usable Init.tcl in the following
directories :
../tcl/tcl8.3 .
```

- Description — This message typically occurs when the base file was not included in a Unix installation. When you install ModelSim, you need to download and install 3 files from the ftp site. These files are:

```
modeltech-base.mis  
modeltech-docs.mis  
install.<platform>
```

If you install only the <platform> file, you will not get the Tcl files that are located in the base file.

This message could also occur if the file or directory was deleted or corrupted.

- Suggested action — Reinstall ModelSim with all three files.

Too few port connections

```
# ** Warning (vsim-3017): foo.v(1422): [TFMPC] - Too few port  
connections. Expected 2, found 1.  
# Region: /foo/tb
```

- Description — This warning occurs when an instantiation has fewer port connections than the corresponding module definition. The warning doesn't necessarily mean anything is wrong; it is legal in Verilog to have an instantiation that doesn't connect all of the pins. However, someone that expects all pins to be connected would like to see such a warning.

Here are some examples of legal instantiations that will and will not cause the warning message.

Module definition:

```
module foo (a, b, c, d);
```

Instantiation that does not connect all pins but will not produce the warning:

```
foo inst1(e, f, g, ); // positional association  
foo inst1(.a(e), .b(f), .c(g), .d()); // named association
```

Instantiation that does not connect all pins but will produce the warning:

```
foo inst1(e, f, g); // positional association  
foo inst1(.a(e), .b(f), .c(g)); // named association
```

Any instantiation above will leave pin *d* unconnected but the first example has a placeholder for the connection. Here's another example:

```
foo inst1(e, , g, h);  
foo inst1(.a(e), .b(), .c(g), .d(h));
```

- Suggested actions —

- Check that there is not an extra comma at the end of the port list. (for example, `model(a,b,)`). The extra comma is legal Verilog and implies that there is a third port connection that is unnamed.
- If you are purposefully leaving pins unconnected, you can disable these messages using the `+nowarnTFMPC` argument to `vsim`.

VSIM license lost

```
Console output:  
Signal 0 caught... Closing vsim vlm child.  
vsim is exiting with code 4  
FATAL ERROR in license manager
```

```
transcript/vsim output:  
# ** Error: VSIM license lost; attempting to re-establish.  
#   Time: 5027 ns   Iteration: 2  
# ** Fatal: Unable to kill and restart license process.  
#   Time: 5027 ns   Iteration: 2
```

- Description — ModelSim queries the license server for a license at regular intervals. Usually these "License Lost" error messages indicate that network traffic is high, and communication with the license server times out.
- Suggested action — Anything you can do to improve network communication with the license server will probably solve or decrease the frequency of this problem.

Failed to find libswift entry

```
** Error: Failed to find LMC Smartmodel libswift entry in project file.  
# Fatal: Foreign module requested halt
```

- Description — ModelSim could not locate the **libswift** entry and therefore could not link to the Logic Modeling library.
- Suggested action — Uncomment the appropriate **libswift** entry in the [lmc] section of the `modelsim.ini` or project `.mpf` file. See [VHDL SmartModel Interface](#) for more information.

sccom Error Messages

This section describes [sccom](#) error messages which may be associated with ModelSim.

Failed to load sc lib error: undefined symbol

```
# ** Error: (vsim-3197) Load of  
  "/home/cmg/newport2_systemc/chip/vhdl/work/systemc.so"  
  failed:ld.so.1:  
  /home/icds_nut/modelsim/5.8a/sunos5/vsimk:  
  fatal: relocation error: file  
  /home/cmg/newport2_systemc/chip/vhdl/work/systemc.so:
```

```
symbol_Z28host_respond_to_vhdl_requestPm:
referenced symbol not found.
# ** Error: (vsim-3676) Could not load shared library
/home/cmg/newport2_systemc/chip/vhdl/work/systemc.so
for SystemC module 'host_xtor'.
```

- Description — The causes for such an error could be:
 - missing symbol definition
 - bad link order specified in `sccom -link`
 - multiply defined symbols (see [Multiple Symbol Definitions](#))
- 1. Suggested action —
 - If the undefined symbol is a C function in your code or a library you are linking with, be sure that you declared it as an external "C" function:

```
extern "C" void myFunc();
```
 - The order in which you place the `-link` option within the `sccom -link` command is critical. Make sure you have used it appropriately. See [sccom](#) for syntax and usage information. See [Misplaced -link Option](#) for further explanation of error and correction.

Multiply defined symbols

```
work/sc/gensrc/test_ringbuf.o: In function
`test_ringbuf::clock_generator(void)':
work/sc/gensrc/test_ringbuf.o(.text+0x4): multiple definition of
`test_ringbuf::clock_generator(void)'
work/sc/test_ringbuf.o(.text+0x4): first defined here
```

- Meaning — The most common type of error found during `sccom -link` operation is the multiple symbol definition error. This typically arises when the same global symbol is present in more than one `.o` file. Several causes are likely:
 - A common cause of multiple symbol definitions involves incorrect definition of symbols in header files. If you have an out-of-line function (one that isn't preceded by the "inline" keyword) or a variable defined (that is, not just referenced or prototyped, but truly defined) in a `.h` file, you can't include that `.h` file in more than one `.cpp` file.
 - Another cause of errors is due to ModelSim's name association feature. The name association feature automatically generates `.cpp` files in the work library. These files "include" your header files. Thus, while it might appear as though you have included your header file in only one `.cpp` file, from the linker's point of view, it is included in multiple `.cpp` files.
- Suggested action — Make sure you don't have any out-of-line functions. Use the "inline" keyword. See [Multiple Symbol Definitions](#).

Enforcing Strict 1076 Compliance

The optional **-pedanticerrors** argument to **vcom** enforces strict compliance to the IEEE 1076 Language Reference Manual (LRM) in the cases listed below. The default behavior for these cases is to issue an insuppressible warning message. If you compile with **-pedanticerrors**, the warnings change to an error, unless otherwise noted. Descriptions in quotes are actual warning/error messages emitted by **vcom**. As noted, in some cases you can suppress the warning using **-nowarn [level]**.

- Type conversion between array types, where the element subtypes of the arrays do not have identical constraints.
- "Extended identifier terminates at newline character (0xa)."
- "Extended identifier contains non-graphic character 0x%x."
- "Extended identifier \"%s\" contains no graphic characters."
- "Extended identifier \"%s\" did not terminate with backslash character."
- "An abstract literal and an identifier must have a separator between them."

This is for forming physical literals, which comprise an optional numeric literal, followed by a separator, followed by an identifier (the unit name). Warning is level 4, which means "-nowarn 4" will suppress it.

- In VHDL 1993 or 2002, a subprogram parameter was declared using VHDL 1987 syntax (which means that it was a class VARIABLE parameter of a file type, which is the only way to do it in VHDL 1987 and is illegal in later VHDLs). Warning is level 10.
- "Shared variables must be of a protected type." Applies to VHDL 2002 only.
- Expressions evaluated during elaboration cannot depend on signal values. Warning is level 9.
- "Non-standard use of output port '%s' in PSL expression." Warning is level 11.
- "Non-standard use of linkage port '%s' in PSL expression." Warning is level 11.
- Type mark of type conversion expression must be a named type or subtype, it can't have a constraint on it.
- When the actual in a PORT MAP association is an expression, it must be a (globally) static expression. The port must also be of mode IN.
- The expression in the CASE and selected signal assignment statements must follow the rules given in Section 8.8 of the 2002 VHDL LRM. In certain cases we can relax these rules, but **-pedanticerrors** forces strict compliance.
- A CASE choice expression must be a locally static expression. We allow it to be only globally static, but **-pedanticerrors** will check that it is locally static. Same rule for selected signal assignment statement choices. Warning level is 8.

- When making a default binding for a component instantiation, ModelSim's non-standard search rules found a matching entity. Section 5.2.2 of the 2002 VHDL LRM describes the standard search rules. Warning level is 1.
- Both FOR GENERATE and IF GENERATE expressions must be globally static. We allow non-static expressions unless **-pedanticerrors** is present.
- When the actual part of an association element is in the form of a conversion function call [or a type conversion], and the formal is of an unconstrained array type, the return type of the conversion function [type mark of the type conversion] must be of a constrained array subtype. We relax this (with a warning) unless **-pedanticerrors** is present when it becomes an error.
- OTHERS choice in a record aggregate must refer to at least one record element.
- In an array aggregate of an array type whose element subtype is itself an array, all expressions in the array aggregate must have the same index constraint, which is the element's index constraint. No warning is issued; the presence of **-pedanticerrors** will produce an error.
- Non-static choice in an array aggregate must be the only choice in the only element association of the aggregate.
- The range constraint of a scalar subtype indication must have bounds both of the same type as the type mark of the subtype indication.
- The index constraint of an array subtype indication must have index ranges each of whose both bounds must be of the same type as the corresponding index subtype.
- When compiling VHDL 1987, various VHDL 1993 and 2002 syntax is allowed. Use **-pedanticerrors** to force strict compliance. Warnings are all level 10.
- For a FUNCTION having a return type mark that denotes a constrained array subtype, a RETURN statement expression must evaluate to an array value with the same index range(s) and direction(s) as that type mark. This language requirement (Section 8.12 of the 2002 VHDL LRM) has been relaxed such that ModelSim displays only a compiler warning and then performs an implicit subtype conversion at run time.

To enforce the prior compiler behavior, use `vcom -pedanticerrors`.

Appendix D

Verilog Interfaces to C

This appendix describes the ModelSim implementation of the Verilog interfaces:

- Verilog PLI (Programming Language Interface)
- VPI (Verilog Procedural Interface)
- SystemVerilog DPI (Direct Programming Interface).

These three interfaces provide a mechanism for defining tasks and functions that communicate with the simulator through a C procedural interface. There are many third party applications available that interface to Verilog simulators through the PLI (see [Third Party PLI Applications](#)). In addition, you may write your own PLI/VPI/DPI applications.

Implementation Information

This chapter describes only the details of using the PLI/VPI/DPI with ModelSim Verilog and SystemVerilog.

- ModelSim SystemVerilog implements DPI as defined in IEEE Std P1800-2005.
- PLI Implementation — Verilog implements the PLI as defined in the IEEE Std 1364-2001, with the exception of the **acc_handle_datapath()** routine.

The **acc_handle_datapath()** routine is not implemented because the information it returns is more appropriate for a static timing analysis tool.

- VPI Implementation — The VPI is partially implemented as defined in the IEEE Std 1364-2005 and IEEE Std 1800-2005. The list of currently supported functionality can be found in the following file:

```
<install_dir>/docs/technotes/Verilog_VPI.note
```

The simulator allows you to specify whether it runs in a way compatible with the IEEE Std 1364-2001 object model or the combined IEEE Std 1364-2005/IEEE Std 1800-2005 object models. By default, the simulator uses the combined 2005 object models. This control is accessed through the **vsim** -plicompatdefault switch or the **PliCompatDefault** variable in the *modelsim.ini* file.

The following table outlines information you should know about when performing a simulation with VPI and HDL files using the two different object models.

Table D-1. VPI Compatibility Considerations

Simulator Compatibility: -plicompatdefault	VPI Files	HDL Files	Notes
2001	2001	2001	When your VPI and HDL are written based on the 2001 standard, be sure to specify, as an argument to vsim, “-plicompatdefault 2001”.
2005	2005	2005	When your VPI and HDL are written based on the 2005 standard, you do not need to specify any additional information to vsim because this is the default behavior
2001	2001	2005	New SystemVerilog objects in the HDL will be completely invisible to the application. This may be problematic, for example, for a delay calculator, which will not see SystemVerilog objects with delay on a net.
2001	2005	2001	It is possible to write a 2005 VPI that is backwards-compatible with 2001 behavior by using mode-neutral techniques. The simulator will reject 2005 requests if it is running in 2001 mode, so there may be VPI failures.
2001	2005	2005	You should only use this setup if there are other VPI libraries in use for which it is absolutely necessary to run the simulator in 2001-mode. This combination is not recommended when the simulator is capable of supporting the 2005 constructs.
2005	2001	2001	This combination is not recommended. You should change the -plicompatdefault argument to 2001.
2005	2001	2005	This combination is most likely to result in errors generated from the VPI as it encounters objects in the HDL that it does not understand.
2005	2005	2001	This combination should function without issues, as SystemVerilog is a superset of Verilog. All that is happening here is that the HDL design is not using the full subset of objects that both the simulator and VPI ought to be able to handle.

g++ Compiler Support for use with Interfaces

You must acquire the g++ compiler for your given platform as defined in the sections [Compiling and Linking C Applications for Interfaces](#) and [Compiling and Linking C++ Applications for Interfaces](#).

Registering PLI Applications

Each PLI application must register its system tasks and functions with the simulator, providing the name of each system task and function and the associated callback routines. Since many PLI applications already interface to Verilog-XL, ModelSim Verilog PLI applications make use of the same mechanism to register information about each system task and function in an array of `s_tfcell` structures. This structure is declared in the `veriusers.h` include file as follows:

```
typedef int (*p_tffn)();
typedef struct t_tfcell {
    short type; /* USERTASK, USERFUNCTION, or USERREALFUNCTION */
    short data; /* passed as data argument of callback function */
    p_tffn checktf; /* argument checking callback function */
    p_tffn sizetf; /* function return size callback function */
    p_tffn calltf; /* task or function call callback function */
    p_tffn misctf; /* miscellaneous reason callback function */
    char *tfname; /* name of system task or function */
    /* The following fields are ignored by ModelSim Verilog */
    int forwref;
    char *tfveritool;
    char *tferrmessage;
    int hash;
    struct t_tfcell *left_p;
    struct t_tfcell *right_p;
    char *namecell_p;
    int warning_printed;
} s_tfcell, *p_tfcell;
```

The various callback functions (`checktf`, `sizetf`, `calltf`, and `misctf`) are described in detail in the IEEE Std 1364. The simulator calls these functions for various reasons. All callback functions are optional, but most applications contain at least the `calltf` function, which is called when the system task or function is executed in the Verilog code. The first argument to the callback functions is the value supplied in the `data` field (many PLI applications don't use this field). The `type` field defines the entry as either a system task (`USERTASK`) or a system function that returns either a register (`USERFUNCTION`) or a real (`USERREALFUNCTION`). The `tfname` field is the system task or function name (it must begin with \$). The remaining fields are not used by ModelSim Verilog.

On loading of a PLI application, the simulator first looks for an `init_usertfs` function, and then a `veriusertfs` array. If `init_usertfs` is found, the simulator calls that function so that it can call `mti_RegisterUserTF()` for each system task or function defined. The `mti_RegisterUserTF()` function is declared in `veriusers.h` as follows:

```
void mti_RegisterUserTF(p_tfcell usertf);
```

The storage for each usertf entry passed to the simulator must persist throughout the simulation because the simulator de-references the usertf pointer to call the callback functions. We recommend that you define your entries in an array, with the last entry set to 0. If the array is named veriusertfs (as is the case for linking to Verilog-XL), then you don't have to provide an init_usertfs function, and the simulator will automatically register the entries directly from the array (the last entry must be 0). For example,

```
s_tfcell veriusertfs[] = {
    {usertask, 0, 0, 0, abc_calltf, 0, "$abc"},
    {usertask, 0, 0, 0, xyz_calltf, 0, "$xyz"},
    {0} /* last entry must be 0 */
};
```

Alternatively, you can add an init_usertfs function to explicitly register each entry from the array:

```
void init_usertfs()
{
    p_tfcell usertf = veriusertfs;
    while (usertf->type)
        mti_RegisterUserTF(usertf++);
}
```

It is an error if a PLI shared library does not contain a veriusertfs array or an init_usertfs function.

Since PLI applications are dynamically loaded by the simulator, you must specify which applications to load (each application must be a dynamically loadable library, see [Compiling and Linking C Applications for Interfaces](#)). The PLI applications are specified as follows (note that on a Windows platform the file extension would be .dll):

- As a list in the Veriuser entry in the *modelsim.ini* file:
Veriuser = pliapp1.so pliapp2.so pliappn.so
- As a list in the PLIOBJS environment variable:
% setenv PLIOBJS "pliapp1.so pliapp2.so pliappn.so"
- As a -pli argument to the simulator (multiple arguments are allowed):
-pli pliapp1.so -pli pliapp2.so -pli pliappn.so

The various methods of specifying PLI applications can be used simultaneously. The libraries are loaded in the order listed above. Environment variable references can be used in the paths to the libraries in all cases.

Registering VPI Applications

Each VPI application must register its system tasks and functions and its callbacks with the simulator. To accomplish this, one or more user-created registration routines must be called at simulation startup. Each registration routine should make one or more calls to `vpi_register_systf()` to register user-defined system tasks and functions and `vpi_register_cb()` to register callbacks. The registration routines must be placed in a table named `vlog_startup_routines` so that the simulator can find them. The table must be terminated with a 0 entry.

Example D-1. VPI Application Registration

```
PLI_INT32 MyFuncCalltf( PLI_BYTE8 *user_data )
{ ... }
PLI_INT32 MyFuncCompiletf( PLI_BYTE8 *user_data )
{ ... }
PLI_INT32 MyFuncSizetf( PLI_BYTE8 *user_data )
{ ... }
PLI_INT32 MyEndOfCompCB( p_cb_data cb_data_p )
{ ... }
PLI_INT32 MyStartOfSimCB( p_cb_data cb_data_p )
{ ... }
void RegisterMySystfs( void )
{

    vpiHandle tmpH;
    s_cb_data callback;
    s_vpi_systf_data systf_data;

    systf_data.type          = vpiSysFunc;
    systf_data.sysfunctype  = vpiSizedFunc;
    systf_data.tfname       = "$myfunc";
    systf_data.calltf       = MyFuncCalltf;
    systf_data.compiletf    = MyFuncCompiletf;
    systf_data.sizetf       = MyFuncSizetf;
    systf_data.user_data    = 0;
    tmpH = vpi_register_systf( &systf_data );
    vpi_free_object(tmpH);

    callback.reason         = cbEndOfCompile;
    callback.cb_rtn         = MyEndOfCompCB;
    callback.user_data      = 0;
    tmpH = vpi_register_cb( &callback );
    vpi_free_object(tmpH);

    callback.reason         = cbStartOfSimulation;
    callback.cb_rtn         = MyStartOfSimCB;
    callback.user_data      = 0;
    tmpH = vpi_register_cb( &callback );
    vpi_free_object(tmpH);
}
```

```
void (*vlog_startup_routines[ ] ) () = {  
    RegisterMySystfs,  
    0 /* last entry must be 0 */  
};
```

Loading VPI applications into the simulator is the same as described in [Registering PLI Applications](#).

Using PLI and VPI Together

PLI and VPI applications can co-exist in the same application object file. In such cases, the applications are loaded at startup as follows:

- If an `init_usertfs()` function exists, then it is executed and only those system tasks and functions registered by calls to `mti_RegisterUserTF()` will be defined.
- If an `init_usertfs()` function does not exist but a `veriusertfs` table does exist, then only those system tasks and functions listed in the `veriusertfs` table will be defined.
- If an `init_usertfs()` function does not exist and a `veriusertfs` table does not exist, but a `vlog_startup_routines` table does exist, then only those system tasks and functions and callbacks registered by functions in the `vlog_startup_routines` table will be defined.

As a result, when PLI and VPI applications exist in the same application object file, they must be registered in the same manner. VPI registration functions that would normally be listed in a `vlog_startup_routines` table can be called from an `init_usertfs()` function instead.

Registering DPI Applications

DPI applications do not need to be registered. However, each DPI imported or exported task or function must be identified using SystemVerilog ‘import “DPI-C”’ or ‘export “DPI-C”’ syntax. Examples of the syntax follow:

```
export "DPI-C" task t1;  
task t1(input int i, output int o);  
.  
.  
.  
end task  
import "DPI-C" function void f1(input int i, output int o);
```

Your code must provide imported functions or tasks, compiled with an external compiler. An imported task must return an `int` value, "1" indicating that it is returning due to a disable, or "0" indicating otherwise.

These imported functions or objects may then be loaded as a shared library into the simulator with either the command line option `-sv_lib <lib>` or `-sv_liblist <bootstrap_file>`. For example,


```
vlog dut.v  
gcc -shared -Bsymbolic -o imports.so imports.c  
vsim -sv_lib imports top -do <do_file>
```

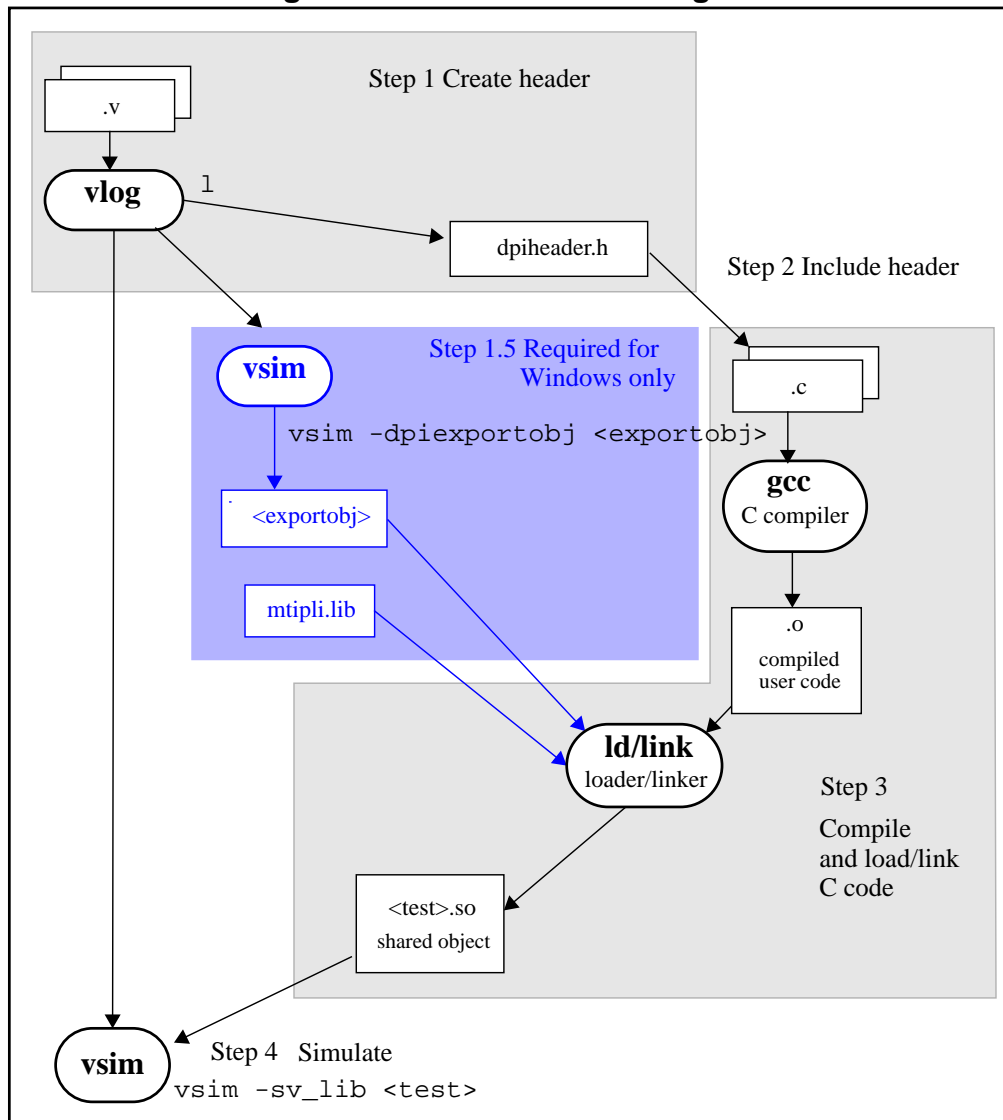
The **-sv_lib** option specifies the shared library name, without an extension. A file extension is added by the tool, as appropriate to your platform. For a list of file extensions accepted by platform, see [DPI File Loading](#).

You can also use the command line options **-sv_root** and **-sv_liblist** to control the process for loading imported functions and tasks. These options are defined in the IEEE Std P1800-2005 LRM.

DPI Use Flow

Correct use of ModelSim DPI depends on the flow presented in this section.

Figure D-1. DPI Use Flow Diagram



1. Run `vlog` to generate a `dpiheader.h` file.

This file defines the interface between C and ModelSim for exported and imported tasks and functions. Though the `dpiheader.h` is a user convenience file rather than a requirement, including `dpiheader.h` in your C code can immediately solve problems caused by an improperly defined interface. An example command for creating the header file would be:

```
vlog -dpiheader <dpiheader>.h files.v
```

2. **Required for Windows only;** Run a preliminary invocation of `vsim` with the `-dpiexportobj` switch.

Because of limitations with the linker/loader provided on Windows, this additional step is required. You must create the exported task/function compiled object file (*exportobj*) by running a preliminary vsim command, such as:

```
vsim -dpiexportobj exportobj top
```

3. Include the *dpiheader.h* file in your C code.

ModelSim recommends that any user DPI C code that accesses exported tasks/functions, or defines imported tasks/functions, should include the *dpiheader.h* file. This allows the C compiler to verify the interface between C and ModelSim.

4. Compile the C code into a shared object.

Compile your code, providing any *.a* or other *.o* files required.

For Windows users — In this step, the object file needs to be bound together with the *.obj* that you created using the **-dpiexportobj** switch, into a single *.dll* file.

5. Simulate the design.

When simulating, specify the name of the imported DPI C shared object (according to the SystemVerilog LRM). For example:

```
vsim -sv_lib <test> top
```

Integrating Export Wrappers into an Import Shared Object

Some workflows require you to generate export tf wrappers ahead of time with:

```
vsim -dpiexportobj <export_object_file>
```

In this case, you must manually integrate the resulting object code into the simulation by non-standard means, described as follows:

- Link the exportwrapper object file (*export_object_file*) directly into a shared object containing the DPI import code, and then load the shared object with **-sv_lib**. This process can only work in simple scenarios, specifically when there is only one **-sv_lib** library that calls exported SystemVerilog tasks or functions.
- Use the vsim **-gblso** switch to load the *export_object_file* before any import shared objects are loaded. This is the more general approach.

When you manually integrate the DPI *export_object_file* into the simulation database, the normal automatic integration flow must be disabled by using the vsim **-nodpiexports** option.

Another reason you may want to use this process is to simplify the set of shared objects that the OS is required to keep track of.

When Your DPI Export Function is Not Getting Called

This issue can arise in your C code due to the way the C linker resolves symbols. It happens if a name you choose for a SystemVerilog export function happens to match a function name in a custom, or even standard C library. In this case, your C compiler will bind calls to the function in that C library, rather than to the export function in the SystemVerilog simulator.

The symptoms of such a misbinding can be difficult to detect. Generally, the misbound function silently returns an unexpected or incorrect value.

To determine if you have this type of name aliasing problem, consult the C library documentation (either the online help or man pages) and look for function names that match any of your export function names. You should also review any other shared objects linked into your simulation and look for name aliases there. To get a comprehensive list of your export functions, you can use `vsim -dpiheader` option and review the generated header file.

Troubleshooting a Missing DPI Import Function

DPI uses C function linkage. If your DPI application is written in C++, it is important to remember to use `extern "C"` declaration syntax appropriately. Otherwise the C++ compiler will produce a mangled C++ name for the function, and the simulator is not able to locate and bind the DPI call to that function.

Also, if you do not use the `-Bsymbolic` argument on the command line for specifying a link, the system may bind to an incorrect function, resulting in unexpected behavior. For more information, see [Correct Linking of Shared Libraries with -Bsymbolic](#).

DPI and the qverilog Command

The `qverilog` performs a single-step compilation, optimization, and simulation (see [Platform Specific Information](#)). You can specify C/C++ files on the `qverilog` command line, and the command will invoke the correct C/C++ compiler based on the file type passed. For example, you can enter the following command:

```
qverilog verilog1.v verilog2.v mydpcode.c
```

This command:

1. Compiles the Verilog files with `vlog`
2. Compiles and links the C/C++ file
3. Creates the shared object `qv_dpi.so` in the `work/_dpi` directory.
4. Invokes the `vsim` with the `-sv_lib` argument and the shared object created in step 3.

For **-ccflags** and **-ldflags**, **qverilog** does not check the validity of the option(s) you specify. The options are directly passed on to the compiler and linker, and if they are not valid, an error message is generated by the compiler/linker.

You can also specify C/C++ files and options with the **-f** argument, and they will be processed the same way as Verilog files and options in a **-f** file.

Note

If your design contains export tasks and functions, it is recommended that you use the classic simulation flow (vlog/vsim).

Platform Specific Information

For designs containing only DPI import tasks and functions (no exports), the simplified **qverilog** flow with C/C++ files on the command line is supported on all platforms. On Win32, use the two step vlog/vsim flow for designs with export tasks and functions.

Simplified Import of Library Functions

In addition to the traditional method of importing FLI, PLI, and C library functions, a simplified method can be used: you can declare VPI and FLI functions as DPI-C imports. When you declare VPI and FLI functions as DPI-C imports, the DPI shared object is loaded at runtime automatically. Neither the C implementation of the import tf, nor the **-sv_lib** argument is required.

Also, on most platforms (see [Platform Specific Information](#)), you can declare most standard C library functions as DPI-C imports.

The following example is processed directly, without DPI C code:

```
package cmath;
    import "DPI-C" function real sin(input real x);
    import "DPI-C" function real sqrt(input real x);
endpackage

package fli;
    import "DPI-C" function mti_Cmd(input string cmd);
endpackage

module top;
    import cmath::*;
    import fli::*;
    int status, A;
    initial begin
        $display("sin(0.98) = %f", sin(0.98));
        $display("sqrt(0.98) = %f", sqrt(0.98));
        status = mti_Cmd("change A 123");
        $display("A = %ld, status = %ld", A, status);
    end
end
```

```
endmodule
```

To simulate, you would simply enter a command such as: **vsim top**.

Precompiled packages are available with that contain import declarations for certain commonly used C calls.

```
<installDir>/verilog_src/dpi_cpack/dpi_cpackages.sv
```

You do not need to compile this file, it is automatically available as a built-in part of the SystemVerilog simulator.

Platform Specific Information

On Windows, only FLI and PLI commands may be imported in this fashion. C library functions are not automatically importable. They must be wrapped in user DPI C functions, which are brought into the simulator using the **-sv_lib** argument.

Use Model for Locked Work Libraries

You may want to create the work library as a locked entity, which enables multiple users to simultaneously share the design library at runtime.

The **vsim** switch **-locklib** allows you to create a library that prevents compilers from recompiling or refreshing a target library.

To prevent **vsim** from creating objects in the library at runtime, the **vsim -dpiexportobj** flow is available on all platforms. Use this flow after compilation, but before you start simulation using the design library.

An example command sequence would be:

```
vlib work
vlog -dpiheader dpiheader.h test.sv
gcc -shared -Bsymbolic -o test.so test.c
vlib -locklib work
vsim -c -dpiexportobj work/_dpi/exportwrapper top
```

The `work/_dpi/exportwrapper` argument provides a basename for the shared object.

The library is now ready for simulation by multiple simultaneous users, as follows:

```
vsim top -sv_lib test
```

At runtime, **vsim** automatically checks to see if the file `work/_dpi/exportwrapper.so` is up-to-date with respect to its C source code. If it is out of date, an error message is issued and elaboration stops.

DPI Arguments of Parameterized Datatypes

DPI import and export TF's can be written with arguments of parameterized data types. For example, assuming T1 and T2 are type parameters:

```
import "DPI-C" function T1 impf(input T2 arg);
```

This feature is only supported when the **vopt** flow is used (see [Optimizing Designs with vopt](#)). On occasion, the tool may not be able to resolve type parameters while building the optimized design, in which case the workaround is to rewrite the function without using parameterized types. The LRM rules for tf signature matching apply to the finally resolved value of type parameters. See the P1800-2005 SystemVerilog LRM, Section 26.4.4 for further information on matching rules.

Making Verilog Function Calls from non-DPI C Models

Working in certain FLI or PLI C applications, you might want to interact with the simulator by directly calling Verilog DPI export functions. Such applications may include complex 3rd party integrations, or multi-threaded C test benches. Normally calls to export functions from PLI or FLI code are illegal. These calls are referred to as out-of-the-blue calls, since they do not originate in the controlled environment of a DPI import tf.

You can set the ModelSim tool to allow out-of-the-blue Verilog function calls either for all simulations (`DpiOutOfTheBlue = 1` in `modelsim.ini` file), or for a specific simulation (`vsim -dpioutoftheblue 1`). See [DpiOutOfTheBlue](#) for information about debugging support for a SystemC method or a SystemC thread.

One restriction applies: only Verilog functions may be called out-of-the-blue. It is illegal to call Verilog tasks in this way. The simulator issues an error if it detects such a call.

Calling C/C++ Functions Defined in PLI Shared Objects from DPI Code

In some instances you may need to share C/C++ code across different shared objects that contain PLI and/or DPI code. There are two ways you can achieve this goal:

- The easiest is to include the shared code in an object containing PLI code, and then make use of the `vsim -gblso` option.
- Another way is to define a standalone shared object that only contains shared function definitions, and load that using `vsim -gblso`. In this case, the process does not require PLI or DPI loading mechanisms, such as `-pli` or `-sv_lib`.

You should also take into consideration what happens when code in one global shared object needs to call code in another global shared object. In this case, place the `-gblso` argument for the calling code on the `vsim` command line *after* you place the `-gblso` argument for the called code.

This is because vsim loads the files in the specified order and you must load called code before calling code in all cases.

Circular references aren't possible to achieve. If you have that kind of condition, you are better off combining the two shared objects into a single one.

For more information about this topic please refer to the section "[Loading Shared Objects with Global Symbol Visibility](#)".

Compiling and Linking C Applications for Interfaces

The following platform-specific instructions show you how to compile and link your PLI/VPI/DPI C applications so that they can be loaded by ModelSim. Various native C/C++ compilers are supported on different platforms. The gcc compiler is supported on all platforms.

The following PLI/VPI/DPI routines are declared in the include files located in the ModelSim `<install_dir>/include` directory:

- `acc_user.h` — declares the ACC routines
- `veriusr.h` — declares the TF routines
- `vpi_user.h` — declares the VPI routines
- `svdpi.h` — declares DPI routines

The following instructions assume that the PLI, VPI, or DPI application is in a single source file. For multiple source files, compile each file as specified in the instructions and link all of the resulting object files together with the specified link instructions.

Although compilation and simulation switches are platform-specific, loading shared libraries is the same for all platforms. For information on loading libraries for PLI/VPI see [PLI and VPI File loading](#). For DPI loading instructions, see [DPI File Loading](#).

For all UNIX Platforms

The information in this section applies to all UNIX platforms.

`app.so`

If `app.so` is not in your current directory, you must tell the OS where to search for the shared object. You can do this one of two ways:

- Add a path before `app.so` in the command line option or control variable (The path may include environment variables.)

- Put the path in a UNIX shell environment variable:

LD_LIBRARY_PATH_32= <library path without filename> (for Solaris/Linux 32-bit)

or

LD_LIBRARY_PATH_64= <library path without filename> (for Solaris 64-bit)

Correct Linking of Shared Libraries with **-Bsymbolic**

In the examples shown throughout this appendix, the **-Bsymbolic** linker option is used with the compilation (**gcc** or **g++**) or link (**ld**) commands to correctly resolve symbols. This option instructs the linker to search for the symbol within the local shared library and bind to that symbol if it exists. If the symbol is not found within the library, the linker searches for the symbol within the vsimk executable and binds to that symbol, if it exists.

When using the **-Bsymbolic** option, the linker may warn about symbol references that are not resolved within the local shared library. It is safe to ignore these warnings, provided the symbols are present in other shared libraries or the vsimk executable. (An example of such a warning would be a reference to a common API call such as `vpi_printf()`).

Windows Platforms — C

- Microsoft Visual C 4.1 or Later

```
cl -c -I<install_dir>\modeltech\include app.c  

link -dll -export:<init_function> app.obj <install_dir>\win32\mtipli.lib -out:app.dll
```

For the Verilog PLI, the <init_function> should be "init_usertfs". Alternatively, if there is no init_usertfs function, the <init_function> specified on the command line should be "veriusertfs". For the Verilog VPI, the <init_function> should be "vlog_startup_routines". These requirements ensure that the appropriate symbol is exported, and thus ModelSim can find the symbol when it dynamically loads the DLL.

When executing **cl** commands in a DO file, use the **/NOLOGO** switch to prevent the Microsoft C compiler from writing the logo banner to stderr. Writing the logo causes Tcl to think an error occurred.

If you need to run the profiler (see [Profiling Performance and Memory Use](#)) on a design that contains PLI/VPI code, add these two switches to the link commands shown above:

```
/DEBUG /DEBUGTYPE:COFF
```

These switches add symbols to the *.dll* that the profiler can use in its report.

If you have Cygwin installed, make sure that the Cygwin *link.exe* executable is not in your search path ahead of the Microsoft Visual C *link* executable. If you mistakenly bind your dll's with the Cygwin *link.exe* executable, the *.dll* will not function properly. It may be best to rename or remove the Cygwin *link.exe* file to permanently avoid this scenario.

- MinGW gcc 3.2.3

```
gcc -c -I<install_dir>\include app.c  
gcc -shared -Bsymbolic -o app.dll app.o -L<install_dir>\win32 -lmtipli
```

The ModelSim tool requires the use of the MinGW gcc compiler rather than the Cygwin gcc compiler. MinGW gcc is available on the ModelSim FTP site. Remember to add the path to your gcc executable in the Windows environment variables.

DPI Imports on Windows Platforms — C

When linking the shared objects, be sure to specify one “link -export” option for each DPI imported task or function in your linking command line. You can use the **-isymfile** argument from the **vlog** command to obtain a complete list of all imported tasks/functions expected by ModelSim.

As an alternative to specifying one -export option for each imported task or function, you can make use of the `__declspec (dllexport)` macro supported by Visual C. You can place this macro before every DPI import task or function declaration in your C source. All the marked functions will be available for use by **vsim** as DPI import tasks and functions.

DPI Flow for Exported Tasks and Functions on Windows Platforms

Since the Windows platform lacks the necessary runtime linking capabilities, you must perform an additional manual step in order to prepare shared objects containing calls to exported SystemVerilog tasks or functions. You need to invoke a special run of **vsim**. The command is as follows:

```
vsim <top du list> -dpiexportobj <objname> <other args>
```

The **-dpiexportobj** generates an object file `<objname>.obj` that contains "glue" code for exported tasks and functions. You must add that object file to the link line for your `.dll`, listed after the other object files. For example, a link line for MinGW would be:

```
gcc -shared -Bsymbolic -o app.dll app.obj <objname>.obj  
-L<install_dir>\modeltech\win32 -lmtipli
```

and a link line for Visual C would be:

```
link -dll -export:<init_function> app.obj <objname>.obj\  
<install_dir>\modeltech\win32\mtipli.lib -out:app.dll
```

32-bit Linux Platform — C

If your PLI/VPI/DPI application uses anything from a system library, you will need to specify that library when you link your PLI/VPI/DPI application. For example, to use the standard C library, specify `-lc` to the `ld` command.

- GNU C Compiler version gcc 3.2 or later

```
gcc -c -I<install_dir>/modeltech/include app.c  
gcc -shared -Bsymbolic -o app.so app.o -lc
```

If you are using ModelSim with RedHat version 7.1 or below, you also need to add the **-noinherit-exec** switch when you specify **-Bsymbolic**.

The compiler switch **-freg-struct-return** must be used when compiling any FLI application code that contains foreign functions that return real or time values.

64-bit Linux for IA64 Platform — C

64-bit Linux is supported on RedHat Linux Advanced Workstation 2.1 for Itanium 2.

- GNU C Compiler version gcc 3.2 or later

```
gcc -c -fPIC -I<install_dir>/modeltech/include app.c  
gcc -shared -Bsymbolic -o app.so app.o
```

If your PLI/VPI/DPI application requires a user or vendor-supplied C library, or an additional system library, you will need to specify that library when you link your PLI/VPI/DPI application. For example, to use the system math library libm, specify **-lm** to the **ld** command:

```
gcc -c -fPIC -I<install_dir>/modeltech/include math_app.c  
gcc -shared -Bsymbolic -o math_app.so math_app.o -lm
```

64-bit Linux for Opteron/Athlon 64 and EM64T Platforms — C

64-bit Linux is supported on RedHat Linux EWS 3.0 for Opteron/Athlon 64 and EM64T.

- GNU C Compiler version gcc 3.2 or later

```
gcc -c -fPIC -I<install_dir>/modeltech/include app.c  
gcc -shared -Bsymbolic -o app.so app.o
```

To compile for 32-bit operation, specify the **-m32** argument on both the compile and link gcc command lines.

If your PLI/VPI/DPI application requires a user or vendor-supplied C library, or an additional system library, you will need to specify that library when you link your PLI/VPI/DPI application. For example, to use the system math library libm, specify **-lm** to the **ld** command:

```
gcc -c -fPIC -I<install_dir>/modeltech/include math_app.c  
gcc -shared -Bsymbolic -o math_app.so math_app.o -lm
```

32-bit Solaris UltraSPARC Platform — C

If your PLI/VPI/DPI application uses anything from a system library, you will need to specify that library when you link your PLI/VPI/DPI application. For example, to use the standard C library, specify '-lc' to the 'ld' command.

- GNU C Compiler version gcc 3.2 or later

```
gcc -c -fPIC -I<install_dir>/modeltech/include app.c  
/usr/ccs/bin/ld -G -Bsymbolic -o app.so app.o -lc
```

- Sun Studio C++ compiler

```
cc -c -KPIC -I<install_dir>/modeltech/include app.c  
/usr/ccs/bin/ld -G -Bsymbolic -o app.so app.o -lc
```

32-bit Solaris x86 Platform — C

If your PLI/VPI/DPI application uses anything from a system library, you will need to specify that library when you link your PLI/VPI/DPI application. For example, to use the standard C library, specify '-lc' to the 'ld' command.

- GNU C Compiler version gcc 3.2 or later

```
gcc -c -fPIC -I<install_dir>/questasim/include app.c  
gcc -shared -Bsymbolic -o app.so app.o -lc
```

- Sun Studio compiler

```
cc -c -I<install_dir>/questasim/include app.c  
/usr/ccs/bin/ld -G -Bsymbolic -o app.so app.o -lc
```

64-bit Solaris UltraSPARC Platform — C

- GNU C Compiler version gcc 3.2 or later

```
gcc -c -I<install_dir>/modeltech/include -m64 -fPIC app.c  
gcc -shared -m64 -Bsymbolic -o app.so app.o
```

This was tested with gcc 3.2.2. You may need to add the location of *libgcc_s.so.1* to the LD_LIBRARY_PATH_64 environment variable.

- Sun Studio compiler

```
cc -c -xarch=v9 -KPIC -O -I<install_dir>/modeltech/include -c app.c  
/usr/ccs/bin/ld -G -64 -Bsymbolic -o app.so app.o
```

64-bit Solaris x86 Platform — C

- GNU C Compiler version gcc 3.2 or later

```
gcc -c -m64 -fPIC -I<install_dir>/questasim/include app.c  
gcc -shared -m64 -Bsymbolic -o app.so app.o -lc
```

This was tested with gcc 3.2.2. You may need to add the location of *libgcc_s.so.1* to the LD_LIBRARY_PATH_64 environment variable.

- Sun Studio compiler

```
cc -c -xarch=amd64 -KPIC -I<install_dir>/questasim/include app.c  
/usr/ccs/bin/ld -G -64 -Bsymbolic -o app.so app.o -lc
```

Compiling and Linking C++ Applications for Interfaces

ModelSim does not have direct support for any language other than standard C; however, C++ code can be loaded and executed under certain conditions.

Since ModelSim's PLI/VPI/DPI functions have a standard C prototype, you must prevent the C++ compiler from mangling the PLI/VPI/DPI function names. This can be accomplished by using the following type of extern:

```
extern "C"  
{  
    <PLI/VPI/DPI application function prototypes>  
}
```

The header files *veriusertfs.h*, *acc_user.h*, and *vpi_user.h*, *svdpi.h*, and *dpiheader.h* already include this type of extern. You must also put the PLI/VPI/DPI shared library entry point (*veriusertfs*, *init_usertfs*, or *vlog_startup_routines*) inside of this type of extern.

You must also place an ‘extern “C”’ declaration immediately before the body of every import function in your C++ source code, for example:

```
extern "C"  
int myimport(int i)  
{  
    vpi_printf("The value of i is %d\n", i);  
}
```

The following platform-specific instructions show you how to compile and link your PLI/VPI/DPI C++ applications so that they can be loaded by ModelSim.

Although compilation and simulation switches are platform-specific, loading shared libraries is the same for all platforms. For information on loading libraries, see [DPI File Loading](#).

For PLI/VPI only

If *app.so* is not in your current directory you must tell Solaris where to search for the shared object. You can do this one of two ways:

- Add a path before *app.so* in the foreign attribute specification. (The path may include environment variables.)

- Put the path in a UNIX shell environment variable:
LD_LIBRARY_PATH_32= <library path without filename> (32-bit)
or
LD_LIBRARY_PATH_64= <library path without filename> (64-bit)

Windows Platforms — C++

- Microsoft Visual C++ 4.1 or Later

```
cl -c [-GX] -I<install_dir>\modeltech\include app.cxx
link -dll -export:<init_function> app.obj
                        <install_dir>\modeltech\win32\mtipli.lib /out:app.dll
```

The **-GX** argument enables exception handling.

For the Verilog PLI, the <init_function> should be "init_userdfs". Alternatively, if there is no init_userdfs function, the <init_function> specified on the command line should be "veriusertfs". For the Verilog VPI, the <init_function> should be "vlog_startup_routines". These requirements ensure that the appropriate symbol is exported, and thus ModelSim can find the symbol when it dynamically loads the DLL.

When executing **cl** commands in a DO file, use the **/NOLOGO** switch to prevent the Microsoft C compiler from writing the logo banner to stderr. Writing the logo causes Tcl to think an error occurred.

If you need to run the profiler (see [Profiling Performance and Memory Use](#)) on a design that contains PLI/VPI code, add these two switches to the link command shown above:

```
/DEBUG /DEBUGTYPE:COFF
```

These switches add symbols to the *.dll* that the profiler can use in its report.

If you have Cygwin installed, make sure that the Cygwin *link.exe* executable is not in your search path ahead of the Microsoft Visual C *link* executable. If you mistakenly bind your dll's with the Cygwin *link.exe* executable, the *.dll* will not function properly. It may be best to rename or remove the Cygwin *link.exe* file to permanently avoid this scenario.

- MinGW C++ Version 3.2.3

```
g++ -c -I<install_dir>\modeltech\include app.cpp
g++ -shared -Bsymbolic -o app.dll app.o -L<install_dir>\modeltech\win32 -lmtipli
```

ModelSim requires the use of the MinGW gcc compiler rather than the Cygwin gcc compiler.

DPI Imports on Windows Platforms — C++

When linking the shared objects, be sure to specify one **-export** option for each DPI imported task or function in your linking command line. You can use Verilog's **-isymfile** option to obtain a complete list of all imported tasks and functions expected by ModelSim.

DPI Special Flow for Exported Tasks and Functions

Since the Windows platform lacks the necessary runtime linking capabilities, you must perform an additional manual step in order to compile the HDL source files into the shared object file. You need to invoke a special run of vsim. The command is as follows:

```
vsim <top du list> -dpiexportobj <objname> <other args>
```

The `-dpiexportobj` generates the object file `<objname>.obj` that contains "glue" code for exported tasks and functions. You must add that object file to the link line, listed after the other object files. For example, if the object name was `dpi1`, the link line for MinGW would be:

```
g++ -shared -Bsymbolic -o app.dll app.obj <objname>.obj  
-L<install_dir>\modeltech\win32 -lmtipli
```

32-bit Linux Platform — C++

- GNU C++ Version 2.95.3 or Later

```
g++ -c -fPIC -I<install_dir>/modeltech/include app.cpp  
g++ -shared -Bsymbolic -fPIC -o app.so app.o
```

64-bit Linux for IA64 Platform — C++

64-bit Linux is supported on RedHat Linux Advanced Workstation 2.1 for Itanium 2.

- GNU C++ compiler version gcc 3.2 or later

```
g++ -c -fPIC -I<install_dir>/modeltech/include app.cpp  
g++ -shared -Bsymbolic -o app.so app.o
```

If your PLI/VPI application requires a user or vendor-supplied C library, or an additional system library, you will need to specify that library when you link your PLI/VPI application. For example, to use the system math library `libm`, specify `'-lm'`:

```
g++ -c -fPIC -I<install_dir>/modeltech/include math_app.cpp  
g++ -shared -Bsymbolic -o math_app.so math_app.o -lm
```

64-bit Linux for Opteron/Athlon 64 and EM64T Platforms — C++

64-bit Linux is supported on RedHat Linux EWS 3.0 for Opteron/Athlon 64 and EM64T.

- GNU C++ compiler version gcc 3.2 or later

```
g++ -c -fPIC -I<install_dir>/modeltech/include app.cpp  
g++ -shared -Bsymbolic -o app.so app.o
```

To compile for 32-bit operation, specify the `-m32` argument on both the `g++` compiler command line as well as the `g++ -shared` linker command line.

If your PLI/VPI/DPI application requires a user or vendor-supplied C library, or an additional system library, you will need to specify that library when you link your PLI/VPI/DPI application. For example, to use the system math library `libm`, specify `-lm` to the `ld` command:

```
g++ -c -fPIC -I<install_dir>/modeltech/include math_app.cpp  
g++ -shared -Bsymbolic -o math_app.so math_app.o -lm
```

32-bit Solaris UltraSPARC Platform — C++

If your PLI/VPI application uses anything from a system library, you will need to specify that library when you link your PLI/VPI application. For example, to use the standard C library, specify `-lc` to the `ld` command.

- GNU C++ compiler version gcc 3.2 or later

```
g++ -c -I<install_dir>/modeltech/include app.cpp  
g++ -shared -Bsymbolic -o app.so app.o -lc
```

- Sun Studio Compiler

```
CC -c -I<install_dir>/questasim/include app.cpp  
/usr/ccs/bin/ld -G -Bsymbolic -o app.so app.o -lc
```

32-bit Solaris x86 Platform — C++

If your PLI/VPI application uses anything from a system library, you will need to specify that library when you link your PLI/VPI application. For example, to use the standard C library, specify `-lc` to the `ld` command.

- GNU C++ compiler version gcc 3.2 or later

```
g++ -c -fPIC -I<install_dir>/questasim/include app.cpp  
g++ -shared -Bsymbolic -o app.so app.o -lc
```

- Sun Studio Compiler

```
CC -c -I<install_dir>/questasim/include app.cpp  
/usr/ccs/bin/ld -G -Bsymbolic -o app.so app.o -lc
```

64-bit Solaris UltraSPARC Platform — C++

- GNU C++ compiler version gcc 3.2 or later

```
g++ -c -I<install_dir>/modeltech/include -m64 -fPIC app.cpp  
g++ -shared -Bsymbolic -o app.so -m64 app.o
```

This was tested with gcc 3.2.2. You may need to add the location of `libgcc_s.so.1` to the `LD_LIBRARY_PATH_64` environment variable.

- Sun Studio compiler


```
CC -xarch=v9 -O -I<install_dir>/questasim/include -c app.cpp
/usr/ccs/bin/ld -G -64 -Bsymbolic app.o -o app.so
```

where v9 applies to UltraSPARC and amd64 applies to x86 platforms.

64-bit Solaris x86 Platform — C++

- GNU C++ compiler version gcc 3.2 or later

```
g++ -c -m64 -fPIC -I<install_dir>/questasim/include app.cpp
g++ -shared -m64 -Bsymbolic -o app.so app.o -lc
```

This was tested with gcc 3.2.2. You may need to add the location of *libgcc_s.so.1* to the LD_LIBRARY_PATH_64 environment variable.

- Sun Studio compiler

```
CC -c -xarch=amd64 -KPIC -I<install_dir>/questasim/include app.cpp
/usr/ccs/bin/ld -G -64 -Bsymbolic -o app.so app.o -lc
```

Specifying Application Files to Load

PLI and VPI file loading is identical. DPI file loading uses switches to the **vsim** command.

PLI and VPI File loading

The PLI/VPI applications are specified as follows:

- As a list in the Veriuser entry in the *modelsim.ini* file:
Veriuser = pliapp1.so pliapp2.so pliappn.so
- As a list in the PLIOBJS environment variable:
% setenv PLIOBJS "pliapp1.so pliapp2.so pliappn.so"
- As a **-pli** argument to the simulator (multiple arguments are allowed):
-pli pliapp1.so -pli pliapp2.so -pli pliappn.so

Note



On Windows platforms, the file names shown above should end with *.dll* rather than *.so*.

The various methods of specifying PLI/VPI applications can be used simultaneously. The libraries are loaded in the order listed above. Environment variable references can be used in the paths to the libraries in all cases.

See also [modelsim.ini Variables](#) for more information on the *modelsim.ini* file.

DPI File Loading

DPI applications are specified to **vsim** using the following SystemVerilog arguments:

Table D-2. vsim Arguments for DPI Application

Argument	Description
-sv_lib <name>	specifies a library name to be searched and used. No filename extensions must be specified. (The extensions ModelSim expects are: <i>.dll</i> for Win32, <i>.so</i> for all other platforms.)
-sv_root <name>	specifies a new prefix for shared objects as specified by -sv_lib
-sv_liblist	specifies a “bootstrap file” to use

When the simulator finds an imported task or function, it searches for the symbol in the collection of shared objects specified using these arguments.

For example, you can specify the DPI application as follows:

```
vsim -sv_lib dpiapp1 -sv_lib dpiapp2 -sv_lib dpiappn top
```

It is a mistake to specify DPI import tasks and functions (tf) inside PLI/VPI shared objects. However, a DPI import tf can make calls to PLI/VPI C code, providing that **vsim -gblso** was used to mark the PLI/VPI shared object with global symbol visibility. See [Loading Shared Objects with Global Symbol Visibility](#).

Loading Shared Objects with Global Symbol Visibility

On Unix platforms you can load shared objects such that all symbols in the object have global visibility. To do this, use the **-gblso** argument to **vsim** when you load your PLI/VPI application. For example:

```
vsim -pli obj1.so -pli obj2.so -gblso obj1.so top
```

The **-gblso** argument works in conjunction with the GlobalSharedObjectList variable in the *modelsim.ini* file. This variable allows user C code in other shared objects to refer to symbols in a shared object that has been marked as global. All shared objects marked as global are loaded by the simulator earlier than any non-global shared objects.

PLI Example

The following example is a trivial, but complete PLI application.

```
hello.c:
```

```

#include "veriusertfs.h"
static PLI_INT32 hello()
{
    io_printf("Hi there\n");
    return 0;
}
s_tfcell veriusertfs[] = {
    {usertask, 0, 0, 0, hello, 0, "$hello"},
    {0} /* last entry must be 0 */
};
hello.v:
module hello;
    initial $hello;
endmodule
Compile the PLI code for the Solaris operating system:
% cc -c -I<install_dir>/modeltech/include hello.c
% ld -G -Bsymbolic -o hello.sl hello.o
Compile the Verilog code:
% vlib work
% vlog hello.v
Simulate the design:
% vsim -c -pli hello.sl hello
# Loading work.hello
# Loading ./hello.sl
VSIM 1> run -all
# Hi there
VSIM 2> quit

```

VPI Example

The following example is a trivial, but complete VPI application. A general VPI example can be found in `<install_dir>/modeltech/examples/verilog/vpi`.

hello.c:

```

#include "vpi_user.h"
static PLI_INT32 hello(PLI_BYTE8 * param)
{
    vpi_printf( "Hello world!\n" );
    return 0;
}
void RegisterMyTfs( void )
{
    s_vpi_systf_data systf_data;
    vpiHandle systf_handle;
    systf_data.type = vpiSysTask;
    systf_data.sysfunctype = vpiSysTask;
    systf_data.tfname = "$hello";
    systf_data.calltf = hello;
    systf_data.compiletf = 0;
    systf_data.sizetf = 0;
    systf_data.user_data = 0;
    systf_handle = vpi_register_systf( &systf_data );
    vpi_free_object( systf_handle );
}

```

```
void (*vlog_startup_routines[])() = {
    RegisterMyTfs,
    0
};
hello.v:
module hello;
    initial $hello;
endmodule
Compile the VPI code for the Solaris operating system:
% gcc -c -I<install_dir>/include hello.c
% gcc -shared -Bsymbolic -o hello.sl hello.o
Compile the Verilog code:
% vlib work
% vlog hello.v
Simulate the design:
% vsim -c -pli hello.sl hello
# Loading work.hello
# Loading ./hello.sl
VSIM 1> run -all
# Hello world!
VSIM 2> quit
```

DPI Example

The following example is a trivial but complete DPI application. For win32 platforms an additional step is required. For additional examples, see the `<install_dir>/modeltech/examples/systemverilog/dpi` directory.

```
hello_c.c:
#include "svdpi.h"
#include "dpiheader.h"
int c_task(int i, int *o)
{
    printf("Hello from c_task()\n");
    verilog_task(i, o); /* Call back into Verilog */
    *o = i;
    return(0); /* Return success (required by tasks) */
}
hello.v:
module hello_top;
    int ret;
    export "DPI-C" task verilog_task;
    task verilog_task(input int i, output int o);
        #10;
        $display("Hello from verilog_task()");
    endtask
    import "DPI-C" context task c_task(input int i, output int o);
    initial
    begin
        c_task(1, ret); // Call the c task named 'c_task()'
    end
endmodule
Compile the Verilog code:
% vlib work
% vlog -sv -dpiheader dpiheader.h hello.v
```

```
Compile the DPI code for the Solaris operating system:
% gcc -c -I<install_dir>/include hello_c.c
% gcc -shared -Bsymbolic -o hello_c.so hello_c.o
Simulate the design:
% vsim -c -sv_lib hello_c hello_top -do "run -all; quit -f"
# Loading work.hello_c
# Loading ./hello_c.so
VSIM 1> run -all
# Hello from c_task()
# Hello from verilog_task()
VSIM 2> quit
```

The PLI Callback reason Argument

The second argument to a PLI callback function is the reason argument. The values of the various reason constants are defined in the *veriusers.h* include file. See IEEE Std 1364 for a description of the reason constants. The following details relate to ModelSim Verilog, and may not be obvious in the IEEE Std 1364. Specifically, the simulator passes the reason values to the *miscf* callback functions under the following circumstances:

`reason_endofcompile`

For the completion of loading the design.

`reason_finish`

For the execution of the `$finish` system task or the **quit** command.

`reason_startofsave`

For the start of execution of the **checkpoint** command, but before any of the simulation state has been saved. This allows the PLI application to prepare for the save, but it shouldn't save its data with calls to `tf_write_save()` until it is called with `reason_save`.

`reason_save`

For the execution of the **checkpoint** command. This is when the PLI application must save its state with calls to `tf_write_save()`.

`reason_startofrestart`

For the start of execution of the **restore** command, but before any of the simulation state has been restored. This allows the PLI application to prepare for the restore, but it shouldn't restore its state with calls to `tf_read_restart()` until it is called with `reason_restart`. The `reason_startofrestart` value is passed only for a restore command, and not in the case that the simulator is invoked with `-restore`.

`reason_restart`

For the execution of the **restore** command. This is when the PLI application must restore its state with calls to `tf_read_restart()`.

`reason_reset`

For the execution of the **restart** command. This is when the PLI application should free its memory and reset its state. We recommend that all PLI applications reset their internal state during a restart as the shared library containing the PLI code might not be

reloaded. (See the **-keeploaded** and **-keeploadedrestart** arguments to `vsim` for related information.)

`reason_endofreset`

For the completion of the **restart** command, after the simulation state has been reset but before the design has been reloaded.

`reason_interactive`

For the execution of the `$stop` system task or any other time the simulation is interrupted and waiting for user input.

`reason_scope`

For the execution of the **environment** command or selecting a scope in the structure window. Also for the call to `acc_set_interactive_scope()` if the `callback_flag` argument is non-zero.

`reason_paramvc`

For the change of value on the system task or function argument.

`reason_synch`

For the end of time step event scheduled by `tf_synchronize()`.

`reason_rosynch`

For the end of time step event scheduled by `tf_rosynchronize()`.

`reason_reactivate`

For the simulation event scheduled by `tf_setdelay()`.

`reason_paramdrc`

Not supported in ModelSim Verilog.

`reason_force`

Not supported in ModelSim Verilog.

`reason_release`

Not supported in ModelSim Verilog.

`reason_disable`

Not supported in ModelSim Verilog.

The `sizetf` Callback Function

A user-defined system function specifies the width of its return value with the `sizetf` callback function, and the simulator calls this function while loading the design. The following details on the `sizetf` callback function are not found in the IEEE Std 1364:

- If you omit the `sizetf` function, then a return width of 32 is assumed.
- The `sizetf` function should return 0 if the system function return value is of Verilog type "real".
- The `sizetf` function should return -32 if the system function return value is of Verilog type "integer".

PLI Object Handles

Many of the object handles returned by the PLI ACC routines are pointers to objects that naturally exist in the simulation data structures, and the handles to these objects are valid throughout the simulation, even after the `acc_close()` routine is called. However, some of the objects are created on demand, and the handles to these objects become invalid after `acc_close()` is called. The following object types are created on demand in ModelSim Verilog:

```
accOperator (acc_handle_condition)
accWirePath (acc_handle_path)
accTerminal (acc_handle_terminal, acc_next_cell_load, acc_next_driver, and
             acc_next_load)
accPathTerminal (acc_next_input and acc_next_output)
accTchkTerminal (acc_handle_tchkarg1 and acc_handle_tchkarg2)
accPartSelect (acc_handle_conn, acc_handle_pathin, and acc_handle_pathout)
```

If your PLI application uses these types of objects, then it is important to call `acc_close()` to free the memory allocated for these objects when the application is done using them.

If your PLI application places value change callbacks on `accRegBit` or `accTerminal` objects, *do not* call `acc_close()` while these callbacks are in effect.

Third Party PLI Applications

Many third party PLI applications come with instructions on using them with ModelSim Verilog. Even without the instructions, it is still likely that you can get it to work with ModelSim Verilog as long as the application uses standard PLI routines. The following guidelines are for preparing a Verilog-XL PLI application to work with ModelSim Verilog.

Generally, a Verilog-XL PLI application comes with a collection of object files and a `veriususer.c` file. The `veriususer.c` file contains the registration information as described above in [Registering PLI Applications](#). To prepare the application for ModelSim Verilog, you must compile the `veriususer.c` file and link it to the object files to create a dynamically loadable object (see [Compiling and Linking C Applications for Interfaces](#)). For example, if you have a `veriususer.c` file and a library archive `libapp.a` file that contains the application's object files, then the following commands should be used to create a dynamically loadable object for the Solaris operating system:

```
% cc -c -I<install_dir>/modeltech/include veriususer.c
% /usr/ccs/bin/ld -G -Bsymbolic -o app.sl veriususer.o libapp.a
```

The PLI application is now ready to be run with ModelSim Verilog. All that's left is to specify the resulting object file to the simulator for loading using the **Veriususer** entry in the `modesim.ini` file, the **-pli** simulator argument, or the `PLIOBJS` environment variable (see [Registering PLI Applications](#)).

Support for VHDL Objects

The PLI ACC routines also provide limited support for VHDL objects in either an all VHDL design or a mixed VHDL/Verilog design. The following table lists the VHDL objects for which handles may be obtained and their type and fulltype constants:

Table D-3. Supported VHDL Objects

Type	Fulltype	Description
accArchitecture	accArchitecture	instantiation of an architecture
accArchitecture	accEntityVitalLevel0	instantiation of an architecture whose entity is marked with the attribute VITAL_Level0
accArchitecture	accArchVitalLevel0	instantiation of an architecture which is marked with the attribute VITAL_Level0
accArchitecture	accArchVitalLevel1	instantiation of an architecture which is marked with the attribute VITAL_Level1
accArchitecture	accForeignArch	instantiation of an architecture which is marked with the attribute FOREIGN and which does not contain any VHDL statements or objects other than ports and generics
accArchitecture	accForeignArchMixed	instantiation of an architecture which is marked with the attribute FOREIGN and which contains some VHDL statements or objects besides ports and generics
accBlock	accBlock	block statement
accForLoop	accForLoop	for loop statement
accForeign	accShadow	foreign scope created by mti_CreateRegion()
accGenerate	accGenerate	generate statement
accPackage	accPackage	package declaration
accSignal	accSignal	signal declaration

The type and fulltype constants for VHDL objects are defined in the *acc_vhdl.h* include file. All of these objects (except signals) are scope objects that define levels of hierarchy in the structure window. Currently, the PLI ACC interface has no provision for obtaining handles to generics, types, constants, variables, attributes, subprograms, and processes.

However, some of these objects can be manipulated through the ModelSim VHDL foreign interface (mti_* routines). See the *PLI Reference Manual* for more information.

IEEE Std 1364 ACC Routines

ModelSim Verilog supports the following ACC routines:

Table D-4. Supported ACC Routines

Routines		
acc_append_delays	acc_free	acc_next
acc_append_pulsere	acc_handle_by_name	acc_next_bit
acc_close	acc_handle_calling_mod_m	acc_next_cell
acc_collect	acc_handle_condition	acc_next_cell_load
acc_compare_handles	acc_handle_conn	acc_next_child
acc_configure	acc_handle_hiconn	acc_next_driver
acc_count	acc_handle_interactive_scope	acc_next_hiconn
acc_fetch_argc	acc_handle_loconn	acc_next_input
acc_fetch_argv	acc_handle_modpath	acc_next_load
acc_fetch_attribute	acc_handle_notifier	acc_next_loconn
acc_fetch_attribute_int	acc_handle_object	acc_next_modpath
acc_fetch_attribute_str	acc_handle_parent	acc_next_net
acc_fetch_defname	acc_handle_path	acc_next_output
acc_fetch_delay_mode	acc_handle_pathin	acc_next_parameter
acc_fetch_delays	acc_handle_pathout	acc_next_port
acc_fetch_direction	acc_handle_port	acc_next_portout
acc_fetch_edge	acc_handle_scope	acc_next_primitive
acc_fetch_fullname	acc_handle_simulated_net	acc_next_scope
acc_fetch_fulltype	acc_handle_tchk	acc_next_specparam
acc_fetch_index	acc_handle_tchkarg1	acc_next_tchk
acc_fetch_location	acc_handle_tchkarg2	acc_next_terminal
acc_fetch_name	acc_handle_terminal	acc_next_topmod
acc_fetch_paramtype	acc_handle_tfarg	acc_object_in_typelist
acc_fetch_paramval	acc_handle_itfarg	acc_object_of_type
acc_fetch_polarity	acc_handle_tfinst	acc_product_type
acc_fetch_precision	acc_initialize	acc_product_version
acc_fetch_pulsere		acc_release_object
acc_fetch_range		acc_replace_delays
acc_fetch_size		acc_replace_pulsere
acc_fetch_tfarg		acc_reset_buffer
acc_fetch_itfarg		acc_set_interactive_scope
acc_fetch_tfarg_int		acc_set_pulsere
acc_fetch_itfarg_int		acc_set_scope
acc_fetch_tfarg_str		acc_set_value
acc_fetch_itfarg_str		acc_vcl_add
acc_fetch_timescale_info		acc_vcl_delete
acc_fetch_type		acc_version
acc_fetch_type_str		
acc_fetch_value		

`acc_fetch_paramval()` cannot be used on 64-bit platforms to fetch a string value of a parameter. Because of this, the function `acc_fetch_paramval_str()` has been added to the PLI for this use. `acc_fetch_paramval_str()` is declared in `acc_user.h`. It functions in a manner similar to `acc_fetch_paramval()` except that it returns a `char *`. `acc_fetch_paramval_str()` can be used on all platforms.

IEEE Std 1364 TF Routines

ModelSim Verilog supports the following TF (task and function) routines;

Table D-5. Supported TF Routines

Routines		
io_mcdprintf	tf_getrealtime	tf_scale_longdelay
io_printf	tf_igetrealtime	tf_scale_realdelay
mc_scan_plusargs	tf_gettime	tf_setdelay
tf_add_long	tf_igettime	tf_isetdelay
tf_asynchoff	tf_gettimeprecision	tf_setlongdelay
tf_iasynchoff	tf_igettimeprecision	tf_isetlongdelay
tf_asynchon	tf_gettimeunit	tf_setrealdelay
tf_iasynchon	tf_igettimeunit	tf_isetrealdelay
tf_clearalldelays	tf_getworkarea	tf_setworkarea
tf_iclearalldelays	tf_igetworkarea	tf_isetworkarea
tf_compare_long	tf_long_to_real	tf_sizep
tf_copypvc_flag	tf_longtime_tostr	tf_isizep
tf_icopypvc_flag	tf_message	tf_spname
tf_divide_long	tf_mipname	tf_ispname
tf_dofinish	tf_imipname	tf_strdelputp
tf_dostop	tf_movepvc_flag	tf_istrdelputp
tf_error	tf_imovepvc_flag	tf_strgetp
tf_evaluatep	tf_multiply_long	tf_istrgetp
tf_ievaluatep	tf_nodeinfo	tf_strgettime
tf_exprinfo	tf_inodeinfo	tf_strlongdelputp
tf_iexprinfo	tf_nump	tf_istrlongdelputp
tf_getcstringp	tf_inump	tf_strrealdelputp
tf_igetcstringp	tf_propagatep	tf_istrrealdelputp
tf_getinstance	tf_ipropagatep	tf_subtract_long
tf_getlongp	tf_putlongp	tf_synchronize
tf_igetlongp	tf_iputlongp	tf_isynchronize
tf_getlongtime	tf_putp	tf_testpvc_flag
tf_igetlongtime	tf_iputp	tf_itestpvc_flag
tf_getnextlongtime	tf_putrealp	tf_text
tf_getp	tf_iputrealp	tf_typep
tf_igetp	tf_read_restart	tf_itypep
tf_getpchange	tf_real_to_long	tf_unscale_longdelay
tf_igetpchange	tf_rosynchronize	tf_unscale_realdelay
tf_getrealp	tf_irosynchronize	tf_warning
tf_igetrealp		tf_write_save

SystemVerilog DPI Access Routines

ModelSim SystemVerilog supports all routines defined in the "svdpi.h" file defined in the IEEE Std 1800-2005.

Verilog-XL Compatible Routines

The following PLI routines are not defined in IEEE Std 1364, but ModelSim Verilog provides them for compatibility with Verilog-XL.

```
char *acc_decompile_exp(handle condition)
```

This routine provides similar functionality to the Verilog-XL **acc_decompile_expr** routine. The **condition** argument must be a handle obtained from the **acc_handle_condition** routine. The value returned by **acc_decompile_exp** is the string representation of the condition expression.

```
char *tf_dumpfilename(void)
```

This routine returns the name of the VCD file.

```
void tf_dumpflush(void)
```

A call to this routine flushes the VCD file buffer (same effect as calling **\$dumpflush** in the Verilog code).

```
int tf_getlongsimtime(int *aof_hightime)
```

This routine gets the current simulation time as a 64-bit integer. The low-order bits are returned by the routine, while the high-order bits are stored in the **aof_hightime** argument.

64-bit Support for PLI

The PLI function `acc_fetch_paramval()` cannot be used on 64-bit platforms to fetch a string value of a parameter. Because of this, the function `acc_fetch_paramval_str()` has been added to the PLI for this use. `acc_fetch_paramval_str()` is declared in `acc_user.h`. It functions in a manner similar to `acc_fetch_paramval()` except that it returns a `char *`. `acc_fetch_paramval_str()` can be used on all platforms.

Using 64-bit ModelSim with 32-bit Applications

If you have 32-bit PLI/VPI/DPI applications and wish to use 64-bit ModelSim, you will need to port your code to 64 bits by moving from the ILP32 data model to the LP64 data model. We strongly recommend that you consult the 64-bit porting guides for Sun.

PLI/VPI Tracing

The foreign interface tracing feature is available for tracing PLI and VPI function calls. Foreign interface tracing creates two kinds of traces: a human-readable log of what functions were called, the value of the arguments, and the results returned; and a set of C-language files that can be used to replay what the foreign interface code did.

The Purpose of Tracing Files

The purpose of the logfile is to aid you in debugging PLI or VPI code. The primary purpose of the replay facility is to send the replay files to support for debugging co-simulation problems, or debugging PLI/VPI problems for which it is impractical to send the PLI/VPI code. We still need you to send the VHDL/Verilog part of the design to actually execute a replay, but many problems can be resolved with the trace only.

Invoking a Trace

To invoke the trace, call `vsim` with the `-trace_foreign` argument:

Syntax

```
vsim
  -trace_foreign <action> [-tag <name>]
```

Arguments

<action>

Can be either the value 1, 2, or 3. Specifies one of the following actions:

Table D-6. Values for <action> Argument

Value	Operation	Result
1	create log only	writes a local file called "mti_trace_<tag>"
2	create replay only	writes local files called "mti_data_<tag>.c", "mti_init_<tag>.c", "mti_replay_<tag>.c" and "mti_top_<tag>.c"
3	create both log and replay	writes all above files

-tag <name>

Used to give distinct file names for multiple traces. Optional.

Examples

```
vsim -trace_foreign 1 mydesign
  Creates a logfile.
```

```
vsim -trace_foreign 3 mydesign
  Creates both a logfile and a set of replay files.
```

```
vsim -trace_foreign 1 -tag 2 mydesign
  Creates a logfile with a tag of "2".
```

The tracing operations will provide tracing during all user foreign code-calls, including PLI/VPI user tasks and functions (calltf, checktf, sizetf and mistf routines), and Verilog VCL callbacks.

Checkpointing and Interface Code

The checkpoint feature in ModelSim captures the state of PLI/VPI/DPI code. See [The PLI Callback reason Argument](#) for reason arguments that apply to checkpoint/restore.

Checkpointing Code that Works with Heap Memory

If checkpointing code that works with heap memory, use `mti_Malloc()` rather than `raw malloc()` or `new`. Any memory allocated with `mti_Malloc()` is guaranteed to be restored correctly. Any memory allocated with `raw malloc()` will not be restored correctly, and simulator crashes can result.

Debugging Interface Application Code

ModelSim offers the optional C Debug feature. This tool allows you to interactively debug SystemC/C/C++ source code with the open-source **`gdb`** debugger. See [C Debug](#) for details. If you don't have access to C Debug, continue reading for instructions on how to attach to an external C debugger.

In order to debug your PLI/VPI/DPI application code in a debugger, you must first:

1. Compile the application code with debugging information (using the **`-g`** option) and without optimizations (for example, don't use the **`-O`** option).
2. Load **`vsim`** into a debugger.

Even though **`vsim`** is stripped, most debuggers will still execute it. You can invoke the debugger directly on **`vsimk`**, the simulation kernel where your application code is loaded (for example, "ddd `which vsimk`"), or you can attach the debugger to an already running **`vsim`** process. In the second case, you must attach to the PID for **`vsimk`**, and you must specify the full path to the **`vsimk`** executable (for example, "gdb \$MTI_HOME/sunos5/vsimk 1234").

On Solaris and Linux systems you can use either **`gdb`** or **`ddd`**.

3. Set an entry point using breakpoint.

Since initially the debugger recognizes only **`vsim`**'s PLI/VPI/DPI function symbols, when invoking the debugger directly on **`vsim`** you need to place a breakpoint in the first PLI/VPI/DPI function that is called by your application code. An easy way to set an entry point is to put a call to `acc_product_version()` as the first executable statement in your application code. Then, after **`vsim`** has been loaded into the debugger, set a breakpoint in this function. Once you have set the breakpoint, run **`vsim`** with the usual arguments.

When the breakpoint is reached, the shared library containing your application code has been loaded.

4. In some debuggers, you must use the **share** command to load the application's symbols.

At this point all of the application's symbols should be visible. You can now set breakpoints in and single step through your application code.

Appendix E

Command and Keyboard Shortcuts

This appendix is a collection of the keyboard and command shortcuts available in the ModelSim GUI.

Command Shortcuts

- You may abbreviate command syntax, with the following limitation: the minimum number of characters required to execute a command are those that make it unique. Note that new commands may disable existing shortcuts. For this reason, ModelSim does not allow command name abbreviations in macro files. This minimizes your need to update macro files as new commands are added.
- You can enter multiple commands on one line if they are separated by semi-colons (;). For example:

```
vlog -nodebug=ports level3.v level2.v ; vlog -nodebug top.v
```

The return value of the last function executed is the only one printed to the transcript. This may cause some unexpected behavior in certain circumstances. Consider this example:

```
vsim -c -do "run 20 ; simstats ; quit -f" top
```

You probably expect the **simstats** results to display in the Transcript window, but they will not, because the last command is **quit -f**. To see the return values of intermediate commands, you must explicitly print the results. For example:

```
vsim -do "run 20 ; echo [simstats]; quit -f" -c top
```

Command History Shortcuts

You can review the simulator command history, or reuse previously entered commands with the following shortcuts at the ModelSim/VSIM prompt:

Table E-1. Command History Shortcuts

Shortcut	Description
!!	repeats the last command
!n	repeats command number n; n is the VSIM prompt number (for example, for this prompt: VSIM 12>, n =12)
!abc	repeats the most recent command starting with "abc"

Table E-1. Command History Shortcuts (cont.)

Shortcut	Description
^xyz^ab^	replaces "xyz" in the last command with "ab"
up arrow and down arrow keys	scrolls through the command history
click on prompt	left-click once on a previous ModelSim or VSIM prompt in the transcript to copy the command typed at that prompt to the active cursor
his or history	shows the last few commands (up to 50 are kept)

Main and Source Window Mouse and Keyboard Shortcuts

The following mouse actions and special keystrokes can be used to edit commands in the entry region of the Main window. They can also be used in editing the file displayed in the Source window and all **Notepad** windows (enter the **notepad** command within ModelSim to open the Notepad editor).

Table E-2. Mouse Shortcuts

Mouse - UNIX and Windows	Result
Click the left mouse button	relocate the cursor
Click and drag the left mouse button	select an area
Shift-click the left mouse button	extend selection
Double-click the left mouse button	select a word
Double-click and drag the left mouse button	select a group of words
Ctrl-click the left mouse button	move insertion cursor without changing the selection
Click the left mouse button on a previous ModelSim or VSIM prompt	copy and paste previous command string to current prompt
Click the middle mouse button	paste selection to the clipboard
Click and drag the middle mouse button	scroll the window

Table E-3. Keyboard Shortcuts

Keystrokes - UNIX and Windows	Result
Left Arrow Right Arrow	move cursor left or right one character

Table E-3. Keyboard Shortcuts (cont.)

Keystrokes - UNIX and Windows	Result
Ctrl + Left Arrow Ctrl + Right Arrow	move cursor left or right one word
Shift + Any Arrow	extend text selection
Ctrl + Shift + Left Arrow Ctrl + Shift + Right Arrow	extend text selection by one word
Up Arrow Down Arrow	Transcript window: scroll through command history Source window: move cursor one line up or down
Ctrl + Up Arrow Ctrl + Down Arrow	Transcript window: moves cursor to first or last line Source window: moves cursor up or down one paragraph
Ctrl + Home	move cursor to the beginning of the text
Ctrl + End	move cursor to the end of the text
Backspace Ctrl + h (UNIX only)	delete character to the left
Delete Ctrl + d (UNIX only)	delete character to the right
Esc (Windows only)	cancel
Alt	activate or inactivate menu bar mode
Alt-F4	close active window
Home Ctrl + a	move cursor to the beginning of the line
Ctrl + Shift + a	select all contents of active window
Ctrl + b	move cursor left
Ctrl + d	delete character to the right
End Ctrl + e	move cursor to the end of the line
Ctrl + f (UNIX) Right Arrow (Windows)	move cursor right one character
Ctrl + k	delete to the end of line
Ctrl + n	move cursor one line down (Source window only under Windows)
Ctrl + o (UNIX only)	insert a new line character at the cursor
Ctrl + p	move cursor one line up (Source window only under Windows)

Table E-3. Keyboard Shortcuts (cont.)

Keystrokes - UNIX and Windows	Result
Ctrl + s (UNIX) Ctrl + f (Windows)	find
Ctrl + t	reverse the order of the two characters on either side of the cursor
Ctrl + u	delete line
Page Down Ctrl + v (UNIX only)	move cursor down one screen
Ctrl + x	cut the selection
Ctrl + s Ctrl + x (UNIX Only)	save
Ctrl + v	paste the selection
Ctrl + a (Windows Only)	select the entire contents of the widget
Ctrl + \	clear any selection in the widget
Ctrl + - (UNIX) Ctrl + / (UNIX) Ctrl + z (Windows)	undoes previous edits in the Source window
Meta + < (UNIX only)	move cursor to the beginning of the file
Meta + > (UNIX only)	move cursor to the end of the file
Page Up Meta + v (UNIX only)	move cursor up one screen
Ctrl + c	copy selection
F3	Performs a Find Next action in the Source window.
F4 Shift+F4	Change focus to next pane in main window Change focus to previous pane in main window
F5 Shift+F5	Toggle between expanding and restoring size of pane to fit the entire main window Toggle on/off the pane headers.
F8	search for the most recent command that matches the characters typed (Main window only)
F9	run simulation
F10	continue simulation
F11 (Windows only)	single-step
F12 (Windows only)	step-over

The Main window allows insertions or pastes only after the prompt; therefore, you don't need to set the cursor when copying strings to the command line.

List Window Keyboard Shortcuts

Using the following keys when the mouse cursor is within the List window will cause the indicated actions:

Table E-4. List Window Keyboard Shortcuts

Key - UNIX and Windows	Action
Left Arrow	scroll listing left (selects and highlights the item to the left of the currently selected item)
Right Arrow	scroll listing right (selects and highlights the item to the right of the currently selected item)
Up Arrow	scroll listing up
Down Arrow	scroll listing down
Page Up Ctrl + Up Arrow	scroll listing up by page
Page Down Ctrl + Down Arrow	scroll listing down by page
Tab	searches forward (down) to the next transition on the selected signal
Shift + Tab	searches backward (up) to the previous transition on the selected signal
Shift + Left Arrow Shift + Right Arrow	extends selection left/right
Ctrl + f (Windows) Ctrl + s (UNIX)	opens the Find dialog box to find the specified item label within the list display

Wave Window Mouse and Keyboard Shortcuts

The following mouse actions and keystrokes can be used in the Wave window.

Table E-5. Wave Window Mouse Shortcuts




Mouse action ¹	Result
Ctrl + Click left mouse button and drag 	zoom area (in)

Table E-5. Wave Window Mouse Shortcuts

Mouse action ¹	Result
Ctrl + Click left mouse button and drag 	zoom out
Ctrl + Click left mouse button and drag 	zoom fit
Click left mouse button and drag	moves closest cursor
Ctrl + Click left mouse button on a scroll bar arrow	scrolls window to very top or bottom (vertical scroll) or far left or right (horizontal scroll)
Click middle mouse button in scroll bar (UNIX only)	scrolls window to position of click

1. If you choose **Wave > Mouse Mode > Zoom Mode**, you do not need to press the Ctrl key.

Table E-6. Wave Window Keyboard Shortcuts

Keystroke	Action
s	bring into view and center the currently active cursor
i Shift + i +	zoom in (mouse pointer must be over the cursor or waveform panes)
o Shift + o -	zoom out (mouse pointer must be over the cursor or waveform panes)
f Shift + f	zoom full (mouse pointer must be over the cursor or waveform panes)
l Shift + l	zoom last (mouse pointer must be over the cursor or waveform panes)
r Shift + r	zoom range (mouse pointer must be over the cursor or waveform panes)
m	zooms all open Wave windows to the zoom range of the active window.
Up Arrow Down Arrow	scrolls entire window up or down one line, when mouse pointer is over waveform pane scrolls highlight up or down one line, when mouse pointer is over pathname or values pane

Table E-6. Wave Window Keyboard Shortcuts

Keystroke	Action
Left Arrow	scroll pathname, values, or waveform pane left
Right Arrow	scroll pathname, values, or waveform pane right
Page Up	scroll waveform pane up by a page
Page Down	scroll waveform pane down by a page
Tab	search forward (right) to the next transition on the selected signal - finds the next edge
Shift + Tab	search backward (left) to the previous transition on the selected signal - finds the previous edge
Ctrl+G	automatically create a group for the selected signals by region with the name Group<n>. If you use this shortcut on signals for which there is already a "Group<n>" they will be placed in that region's group rather than creating a new one.
Ctrl + F (Windows) Ctrl + S (UNIX)	open the find dialog box; searches within the specified field in the pathname pane for text strings
Ctrl + Left Arrow Ctrl + Right Arrow	scroll pathname, values, or waveform pane left or right by a page

Appendix F

Setting GUI Preferences

The ModelSim GUI is programmed using Tcl/Tk. It is highly customizable. You can control everything from window size, position, and color to the text of window prompts, default output filenames, and so forth. You can even add buttons and menus that run user-programmable Tcl code.

Most user GUI preferences are stored as Tcl variables in the *.modelsim* file on Unix/Linux platforms or the Registry on Windows platforms. The variable values save automatically when you exit ModelSim. Some of the variables are modified by actions you take with menus or windows (for example, resizing a window changes its geometry variable). Or, you can edit the variables directly either from the ModelSim> prompt or the Preferences dialog.

Customizing the Simulator GUI Layout

You can customize the layout of panes, windows, toolbars, and so forth.) This section discusses layouts and how they are used in ModelSim.

Layouts and Modes of Operation

ModelSim ships with four default layouts that correspond to three modes of operation.

Table F-1. Predefined GUI Layouts

Layout	Mode
NoDesign	a design is not yet loaded
Simulate	a design is loaded
Coverage	a design is loaded with code coverage enabled
VMgmt	an option to use when working with Verification Management

As you load and unload designs, ModelSim switches between the layouts.

Custom Layouts

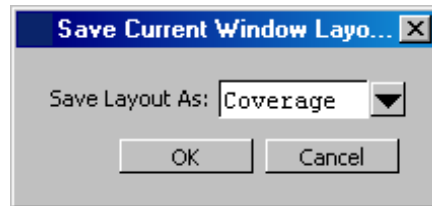
You can create custom layouts or modify the four default layouts.

Creating Custom Layouts

To create a custom layout or modify one of the default layouts, follow these steps:

1. Rearrange the GUI as you see fit.
2. Select **Layout > Save Layout As**.

Figure F-1. Save Current Window Layout Dialog Box



3. Specify a new name or use an existing name to overwrite that layout.
4. Click OK.

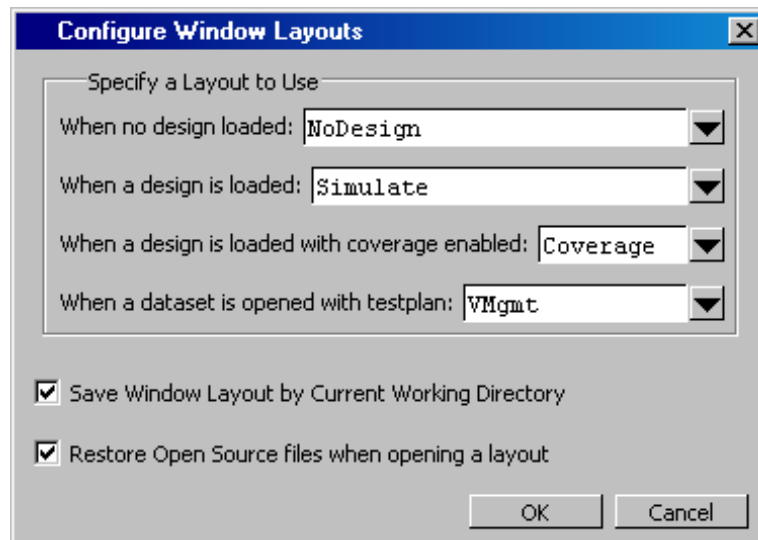
The layout is saved to the *.modelsim* file (or Registry on Windows).

Assigning Layouts to Modes

You can assign which layout appears in each mode (no design loaded, design loaded, design loaded with coverage). Follow these steps:

1. Create your custom layouts as described above.
2. Select **Layout > Configure**.

Example F-1. Configure Window Layouts Dialog Box



3. Select a layout for each mode.
4. Click OK.

The layout assignment is saved to the *.modelsim* file (Registry on Windows).

Automatic Saving of Layouts

By default any changes you make to a layout are saved automatically for the current design when you exit the tool or when you change modes. For example, if you load a design with code coverage, rearrange some windows, and then quit the simulation, the changes are saved and associated with that current working directory.

Resetting Layouts to Their Defaults

You can reset the layouts for the three modes to their original defaults. Select **Layout > Reset**. This command does not delete custom layouts.

Simulator GUI Preferences

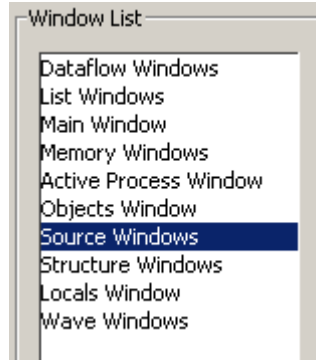
Simulator GUI preferences are stored by default either in the *.modelsim* file in your HOME directory on UNIX/Linux platforms or the Registry on Windows platforms.

Setting Preference Variables from the GUI

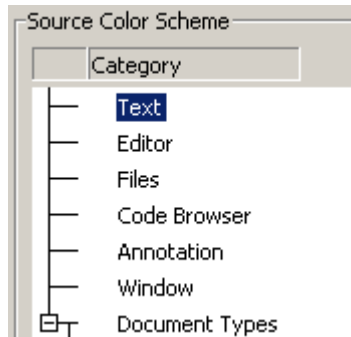
To edit a variable value from the GUI, select **Tools > Edit Preferences**.

The dialog organizes preferences into two tab groups: By Window and By Name. The By Window tab primarily allows you to change colors and fonts for various GUI objects. For example, if you want to change the color of the text in the Source window, do the following:

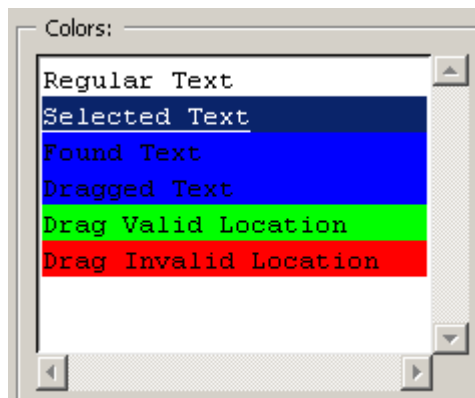
1. Select "Source Windows" from the Window List column.



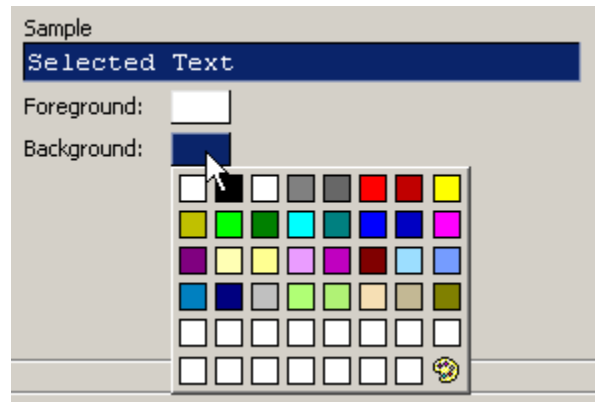
2. Select "Text" from the Source Color Scheme column.



3. Click the type of text you want to change (Regular Text, Selected Text, Found Text, and so forth) from the Colors area.



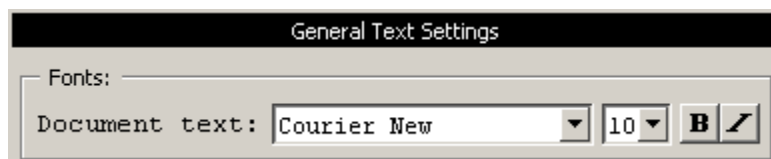
- Click the “Foreground” or “Background” color block.



- Select a color from the palette.

To change the font type and/or size of the window selected in the Windows List column, use the Fonts section of the By Window tab that appears under “General Text Settings” (Figure F-2).

Figure F-2. Change Text Fonts for Selected Windows



You can also make global font changes to all GUI windows with the Fonts section of the By Window tab (Figure F-3).

Figure F-3. Making Global Font Changes

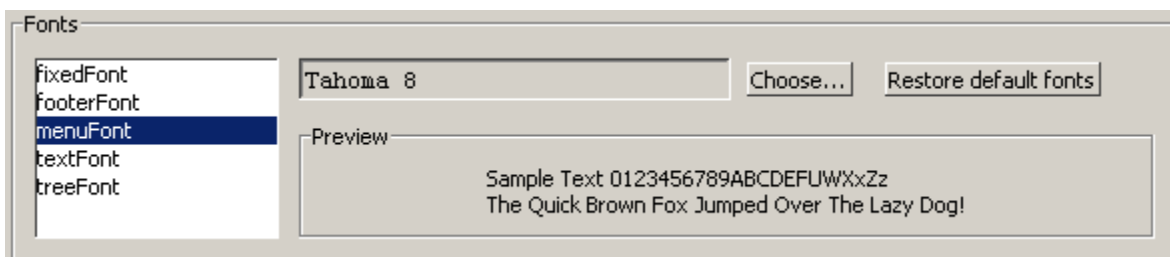


Table F-2. Global Fonts

Global Font Name	Description
fixedFont	for all text in Source window and Notepad display, and in all text entry fields or boxes
footerFont	for all footer text that appears in footer of Main window and all undocked windows

Table F-2. Global Fonts

Global Font Name	Description
menuFont	for all menu text
textFont	for Transcript window text and text in list boxes
treeFont	for all text that appears in any window that displays a hierarchical tree

The By Name tab lists every Tcl variable in a tree structure. The procedure for changing a Tcl variable is:

1. Expand the tree.
2. Highlight a variable.
3. Click **Change Value** to edit the current value.

Clicking **OK** or **Apply** at the bottom of the Preferences dialog changes the variable, and the change is saved when you exit ModelSim.

Setting Preference Variables from the Command Line

Use the Tcl [set Command Syntax](#) to customize preference variables from the Main window command line. For example:

```
set <variable name> <variable value>
```

Saving GUI Preferences

GUI preferences are saved automatically when you exit the tool.

If you prefer to store GUI preferences elsewhere, set the `MODELSIM_PREFERENCES` environment variable to designate where these preferences are stored. Setting this variable causes ModelSim to use a specified path and file instead of the default location. Here are some additional points to keep in mind about this variable setting:

- The file does not need to exist before setting the variable as ModelSim will initialize it.
- If the file is read-only, ModelSim will not update or otherwise modify the file.
- This variable may contain a relative pathname, in which case the file is relative to the working directory at the time the tool is started.

The modelsim.tcl File

Previous versions saved user GUI preferences into a *modelsim.tcl* file. Current versions will still read in a *modelsim.tcl* file if it exists. ModelSim searches for the file as follows:

- use `MODELSIM_TCL` environment variable if it exists (if `MODELSIM_TCL` is a list of files, each file is loaded in the order that it appears in the list); else
- use `./modelsim.tcl`; else
- use `$(HOME)/modelsim.tcl` if it exists

Note that in versions 6.1 and later, ModelSim will save to the `.modelsim` file any variables it reads in from a `modelsim.tcl` file (except for `user_hook` variables). The values from the `modelsim.tcl` file will override like variables in the `.modelsim` file.

User_hook Variables

`User_hook` variables allow you to add buttons and menus to the GUI. `User_hook` variables can only be stored in a `modelsim.tcl` file. They are not stored in `.modelsim`. If you need to use `user_hook` variables, you must create a `modelsim.tcl` file to store them.

Appendix G

System Initialization

ModelSim goes through numerous steps as it initializes the system during startup. It accesses various files and environment variables to determine library mappings, configure the GUI, check licensing, and so forth.

Files Accessed During Startup

The table below describes the files that are read during startup. They are listed in the order in which they are accessed.

Table G-1. Files Accessed During Startup

File	Purpose
<i>modelsim.ini</i>	contains initial tool settings; see modelsim.ini Variables for specific details on the <i>modelsim.ini</i> file
location map file	used by ModelSim tools to find source files based on easily reallocated "soft" paths; default file name is <i>mgc_location_map</i>
<i>pref.tcl</i>	contains defaults for fonts, colors, prompts, window positions, and other simulator window characteristics
.modelsim (UNIX) or Windows registry	contains last working directory, project file, printer defaults, and other user-customized GUI characteristics
<i>modelsim.tcl</i>	contains user-customized settings for fonts, colors, prompts, other GUI characteristics; maintained for backwards compatibility with older versions (see The modelsim.tcl File)
<i><project_name>.mpf</i>	if available, loads last project file which is specified in the registry (Windows) or $\$(HOME)/.modelsim$ (UNIX); see What are Projects? for details on project settings

Initialization Sequence

The following list describes in detail ModelSim's initialization sequence. The sequence includes a number of conditional structures, the results of which are determined by the existence of certain files and the current settings of environment variables.

In the steps below, names in uppercase denote environment variables (except `MTI_LIB_DIR` which is a Tcl variable). Instances of `$(NAME)` denote paths that are determined by an environment variable (except `$(MTI_LIB_DIR)` which is determined by a Tcl variable).

1. Determines the path to the executable directory (`./modeltech/<platform>`). Sets `MODEL_TECH` to this path, *unless* `MODEL_TECH_OVERRIDE` exists, in which case `MODEL_TECH` is set to the same value as `MODEL_TECH_OVERRIDE`.

Environment Variables used: [MODEL_TECH](#), [MODEL_TECH_OVERRIDE](#)

2. Finds the `modelsim.ini` file by evaluating the following conditions:
 - use `$(MODELSIM)` (which specifies the directory location and name of a `modelsim.ini` file) if it exists; else
 - use `$(MGC_WD)/modelsim.ini`; else
 - use `./modelsim.ini`; else
 - use `$(MODEL_TECH)/modelsim.ini`; else
 - use `$(MODEL_TECH)/../modelsim.ini`; else
 - use `$(MGC_HOME)/lib/modelsim.ini`; else
 - set path to `./modelsim.ini` even though the file doesn't exist

Environment Variables used: [MODELSIM](#), [MGC_WD](#), [MGC_HOME](#)

You can determine which `modelsim.ini` file was used by executing the [where](#) command.

3. Finds the location map file by evaluating the following conditions:
 - use `MGC_LOCATION_MAP` if it exists (if this variable is set to "no_map", ModelSim skips initialization of the location map); else
 - use `mgc_location_map` if it exists; else
 - use `$(HOME)/mgc/mgc_location_map`; else
 - use `$(HOME)/mgc_location_map`; else
 - use `$(MGC_HOME)/etc/mgc_location_map`; else
 - use `$(MGC_HOME)/shared/etc/mgc_location_map`; else
 - use `$(MODEL_TECH)/mgc_location_map`; else
 - use `$(MODEL_TECH)/../mgc_location_map`; else
 - use no map

Environment Variables used: [MGC_LOCATION_MAP](#), [HOME](#), [MGC_HOME](#), [MODEL_TECH](#)

4. Reads various variables from the [vsim] section of the *modelsim.ini* file. See [modelsim.ini Variables](#) for more details.
5. Parses any command line arguments that were included when you started ModelSim and reports any problems.
6. Defines the following environment variables:
 - use MODEL_TECH_TCL if it exists; else
 - set MODEL_TECH_TCL=\$(MODEL_TECH)/../tcl
 - set TCL_LIBRARY=\$(MODEL_TECH_TCL)/tcl8.4
 - set TK_LIBRARY=\$(MODEL_TECH_TCL)/tk8.4
 - set ITCL_LIBRARY=\$(MODEL_TECH_TCL)/itcl3.0
 - set ITK_LIBRARY=\$(MODEL_TECH_TCL)/itk3.0
 - set VSIM_LIBRARY=\$(MODEL_TECH_TCL)/vsim

Environment Variables used: [MODEL_TECH_TCL](#), [TCL_LIBRARY](#), [TK_LIBRARY](#), [MODEL_TECH](#), [ITCL_LIBRARY](#), [ITK_LIBRARY](#), [VSIM_LIBRARY](#)

7. Initializes the simulator's Tcl interpreter.
8. Checks for a valid license (a license is not checked out unless specified by a *modelsim.ini* setting or command line option).
9. The next four steps relate to initializing the graphical user interface.
10. Sets Tcl variable MTI_LIB_DIR=\$(MODEL_TECH_TCL)

Environment Variables used: [MTI_LIB_DIR](#), [MODEL_TECH_TCL](#)
11. Loads \$(MTI_LIB_DIR)/vsim/pref.tcl.

Environment Variables used: [MTI_LIB_DIR](#)
12. Loads GUI preferences, project file, and so forth, from the registry (Windows) or \$(HOME)/.modelsim (UNIX).

Environment Variables used: [HOME](#)
13. Searches for the *modelsim.tcl* file by evaluating the following conditions:
 - use MODELSIM_TCL environment variable if it exists (if MODELSIM_TCL is a list of files, each file is loaded in the order that it appears in the list); else
 - use ./modelsim.tcl; else
 - use \$(HOME)/modelsim.tcl if it exists

Environment Variables used: [HOME](#), [MODEL_TECH_TCL](#)

That completes the initialization sequence. Also note the following about the *modelsim.ini* file:

- When you change the working directory within ModelSim, the tool reads the [library], [vcom], and [vlog] sections of the local *modelsim.ini* file. When you make changes in the compiler or simulator options dialog or use the **vmap** command, the tool updates the appropriate sections of the file.
- The *pref.tcl* file references the default .ini file via the [GetPrivateProfileString] Tcl command. The .ini file that is read will be the default file defined at the time *pref.tcl* is loaded.

Environment Variables

Environment Variable Expansion

The shell commands **vcom**, **vlog**, **vsim**, and **vmap**, no longer expand environment variables in filename arguments and options. Instead, variables should be expanded by the shell beforehand, in the usual manner. The -f switch that most of these commands support now performs environment variable expansion throughout the file.

Environment variable expansion is still performed in the following places:

- Pathname and other values in the *modelsim.ini* file
- Strings used as file pathnames in VHDL and Verilog
- VHDL Foreign attributes
- The **PLIOBJS** environment variable may contain a path that has an environment variable.
- Verilog `\uselib` file and dir directives
- Anywhere in the contents of a -f file

The recommended method for using flexible pathnames is to make use of the MGC Location Map system (see [Using Location Mapping](#)). When this is used, then pathnames stored in libraries and project files (.mpf) will be converted to logical pathnames.

If a file or path name contains the dollar sign character (\$), and must be used in one of the places listed above that accepts environment variables, then the explicit dollar sign must be escaped by using a double dollar sign (\$\$).

Setting Environment Variables

Before compiling or simulating, several environment variables may be set to provide the functions described below. You set the variables as follows:

- Windows — through the System control panel, refer to “[Creating Environment Variables in Windows](#)” for more information.
- Linux/UNIX — typically through the *.login* script.

The LM_LICENSE_FILE variable is required; all others are optional.

DOPATH

The toolset uses the DOPATH environment variable to search for DO files (macros). DOPATH consists of a colon-separated (semi-colon for Windows) list of paths to directories. You can override this environment variable with the DOPATH Tcl preference variable.

The DOPATH environment variable isn’t accessible when you invoke vsim from a UNIX shell or from a Windows command prompt. It is accessible once ModelSim or vsim is invoked. If you need to invoke from a shell or command line and use the DOPATH environment variable, use the following syntax:

```
vsim -do "do <dofile_name>" <design_unit>
```

EDITOR

The EDITOR environment variable specifies the editor to invoke with the [edit](#) command

HOME

The toolset uses the HOME environment variable to look for an optional graphical preference file and optional location map file. Refer to [modelsim.ini Variables](#) for additional information.

HOME_0IN

The HOME_0IN environment variable identifies the location of the 0-In executables directory. Refer to the 0-In documentation for more information.

ITCL_LIBRARY

Identifies the pathname of the [incr]Tcl library; set by ModelSim to the same path as MODEL_TECH_TCL; must point to libraries supplied by Mentor Graphics.

ITK_LIBRARY

Identifies the pathname of the [incr]Tk library; set by ModelSim to the same pathname as MODEL_TECH_TCL; must point to libraries supplied by Mentor Graphics.

LD_LIBRARY_PATH

A UNIX shell environment variable setting the search directories for shared libraries. It instructs the OS where to search for the shared libraries for FLI/PLI/VPI/DPI. This variable is used for both 32-bit and 64-bit shared libraries on Solaris/Linux systems.

LD_LIBRARY_PATH_32

A UNIX shell environment variable setting the search directories for shared libraries. It instructs the OS where to search for the shared libraries for FLI/PLI/VPI/DPI. This variable is used only for 32-bit shared libraries on Solaris/Linux systems.

LD_LIBRARY_PATH_64

A UNIX shell environment variable setting the search directories for shared libraries. It instructs the OS where to search for the shared libraries for FLI/PLI/VPI/DPI. This variable is used only for 64-bit shared libraries on Solaris/Linux systems.

LM_LICENSE_FILE

The toolset's file manager uses the LM_LICENSE_FILE environment variable to find the location of the license file. The argument may be a colon-separated (semi-colon for Windows) set of paths, including paths to other vendor license files. The environment variable is required.

MGC_AMS_HOME

Specifies whether vcom adds the declaration of REAL_VECTOR to the STANDARD package. This is useful for designers using VHDL-AMS to test digital parts of their model.

MGC_HOME

Identifies the pathname of the MGC product suite.

MGC_LOCATION_MAP

The toolset uses the MGC_LOCATION_MAP environment variable to find source files based on easily reallocated "soft" paths.

MGC_WD

Identifies the Mentor Graphics working directory. This variable is used in the initialization sequence.

MODEL_TECH

Do not set this variable. The toolset automatically sets the MODEL_TECH environment variable to the directory in which the binary executable resides.

MODEL_TECH_OVERRIDE

Provides an alternative directory path for the binary executables. Upon initialization, the product sets MODEL_TECH to this path, if set.

MODEL_TECH_TCL

Specifies the directory location of Tcl libraries for Tcl/Tk and vsim, and may also be used to specify a startup DO file. This variable defaults to `<installDIR>/tcl`, however you may set it to an alternate path.

MODELSIM

The toolset uses the MODELSIM environment variable to find the `modelsim.ini` file. The argument consists of a path including the file name.

An alternative use of this variable is to set it to the path of a project file (`<Project_Root_Dir>/<Project_Name>.mpf`). This allows you to use project settings with command line tools. However, if you do this, the `.mpf` file will replace `modelsim.ini` as the initialization file for all tools.

MODELSIM_PREFERENCES

The MODELSIM_PREFERENCES environment variable specifies the location to store user interface preferences. Setting this variable with the path of a file instructs the toolset to use this file instead of the default location (your HOME directory in UNIX or in the registry in Windows). The file does not need to exist beforehand, the toolset will initialize it. Also, if this file is read-only, the toolset will not update or otherwise modify the file. This variable may contain a relative pathname – in which case the file will be relative to the working directory at the time ModelSim is started.

MODELSIM_TCL

identifies the pathname to a user preference file (for example, `C:\questasim\modelsim.tcl`); can be a list of file pathnames, separated by semicolons (Windows) or colons (UNIX); note that user preferences are now stored in the `.modelsim` file (Unix) or registry (Windows); QuestaSim will still read this environment variable but it will then save all the settings to the `.modelsim` file when you exit ModelSim.

MTI_COSIM_TRACE

The MTI_COSIM_TRACE environment variable creates an `mti_trace_cosim` file containing debugging information about FLI/PLI/VPI function calls. You should set this variable to any value before invoking the simulator.

MTI_LIB_DIR

Identifies the path to all Tcl libraries installed with ModelSim.

MTI_TF_LIMIT

The MTI_TF_LIMIT environment variable limits the size of the VSOUT temp file (generated by the toolset's kernel). Set the argument of this variable to the size of k-bytes

The environment variable TMPDIR controls the location of this file, while STDOUT controls the name. The default setting is 10, and a value of 0 specifies that there is no limit. This variable does *not* control the size of the transcript file.

MTI_RELEASE_ON_SUSPEND

The MTI_RELEASE_ON_SUSPEND environment variable allows you to turn off or modify the delay for the functionality of releasing all licenses when operation is suspended. The default setting is 10 (in seconds), which means that if you do not set this variable your licenses will be released 10 seconds after your run is suspended. If you set this environment variable with an argument of 0 (zero) ModelSim will not release the licenses after being suspended. You can change the default length of time (number of seconds) by setting this environment variable to an integer greater than 0 (zero).

MTI_USELIB_DIR

The MTI_USELIB_DIR environment variable specifies the directory into which object libraries are compiled when using the **-compile_uselibs** argument to the [vlog](#) command

MTI_VCO_MODE

The MTI_VCO_MODE environment variable determines which version of the toolset to use on platforms that support both 32- and 64-bit versions when the executables are invoked from the *modeltech/bin* directory by a Unix shell command (using full path specification or PATH search_). Acceptable values are either "32" or "64" (do not include quotes). If you do not set this variable, the preference is given to the highest performance installed version.

MTI_VOPT_FLOW

The environment variable MTI_VOPT_FLOW determines whether vopt is used as part of the vsim command. This variable is overridden by vsim switches -vopt and -novopt, but it overrides the VoptFlow setting in modelsim.ini.

Setting MTI_VOPT_FLOW to 0 means do not use vopt (-novopt). Setting it to any other value means use vopt (-vopt).

NOMMAP

When set to 1, the NOMMAP environment variable disables memory mapping in the toolset. You should only use this variable when running on Linux 7.1 because it will decrease the speed with which ModelSim reads files.

PLIOBJS

The toolset uses the PLIOBJS environment variable to search for PLI object files for loading. The argument consists of a space-separated list of file or path names

STDOUT

The argument to the STDOUT environment variable specifies a filename to which the simulator saves the VSOUT temp file information. Typically this information is deleted when the simulator exits. The location for this file is set with the TMPDIR variable, which allows you to find and delete the file in the event of a crash, because an unnamed VSOUT file is not deleted after a crash.

TCL_LIBRARY

Identifies the pathname of the Tcl library; set by ModelSim to the same pathname as MODEL_Tech_TCL; must point to libraries supplied by Mentor Graphics.

TK_LIBRARY

Identifies the pathname of the Tk library; set by ModelSim to the same pathname as MODEL_Tech_TCL; must point to libraries supplied by Mentor Graphics.

TMP

(Windows environments) The TMP environment variable specifies the path to a tempnam() generated file (VSOUT) containing all stdout from the simulation kernel.

TMPDIR

(UNIX environments) The TMPDIR environment variable specifies the path to a tempnam() generated file (VSOUT) containing all stdout from the simulation kernel.

VSIM_LIBRARY

Identifies the pathname of the Tcl files that are used by ModelSim; set by ModelSim to the same pathname as MODEL_Tech_TCL; must point to libraries supplied by Mentor Graphics.

Creating Environment Variables in Windows

In addition to the predefined variables shown above, you can define your own environment variables. This example shows a user-defined library path variable that can be referenced by the **vmap** command to add library mapping to the *modelsim.ini* file.

1. From your desktop, right-click your **My Computer** icon and select **Properties**
2. In the System Properties dialog box, select the Advanced tab

3. Click Environment Variables
4. In the Environment Variables dialog box and User variables for <user> pane, select New:
5. In the New User Variable dialog box, add the new variable with this data

```
Variable name: MY_PATH  
Variable value: \temp\work
```

6. OK (New User Variable, Environment Variable, and System Properties dialog boxes)

Library Mapping with Environment Variables

Once the **MY_PATH** variable is set, you can use it with the **vmap** command to add library mappings to the current *modelsim.ini* file.

Table G-2. Add Library Mappings to modelsim.ini File

Prompt Type	Command	Result added to <i>modelsim.ini</i>
DOS prompt	<code>vmap MY_VITAL %MY_PATH%</code>	<code>MY_VITAL = c:\temp\work</code>
ModelSim or vsim prompt	<code>vmap MY_VITAL \\$MY_PATH¹</code>	<code>MY_VITAL = \$MY_PATH</code>

1. The dollar sign (\$) character is Tcl syntax that indicates a variable. The backslash (\) character is an escape character that prevents the variable from being evaluated during the execution of **vmap**.

You can easily add additional hierarchy to the path. For example,

```
vmap MORE_VITAL %MY_PATH%\more_path\and_more_path  
vmap MORE_VITAL \$MY_PATH\more_path\and_more_path
```

Referencing Environment Variables

There are two ways to reference environment variables within ModelSim. Environment variables are allowed in a **FILE** variable being opened in VHDL. For example,

```
use std.textio.all;  
entity test is end;  
architecture only of test is  
begin  
  process  
    FILE in_file : text is in "$ENV_VAR_NAME";  
  begin  
    wait;  
  end process;  
end;
```

Environment variables may also be referenced from the ModelSim command line or in macros using the Tcl **env** array mechanism:

```
echo "$env(ENV_VAR_NAME)"
```

Note

Environment variable expansion *does not* occur in files that are referenced via the **-f** argument to **vcom**, **vlog**, or **vsim**.

Removing Temp Files (VSOUT)

The *VSOUT* temp file is the communication mechanism between the simulator kernel and the Graphical User Interface. In normal circumstances the file is deleted when the simulator exits. If ModelSim crashes, however, the temp file must be deleted manually. Specifying the location of the temp file with **TMPDIR** (above) will help you locate and remove the file.

Appendix H

Logic Modeling Hardware Models

A hardware model allows simulation of a device using the actual silicon installed as a hardware model in one of Logic Modeling's hardware modeling systems. The hardware modeling system is a network resource with a procedural interface that is accessed by the simulator.

Note



Please refer to Logic Modeling documentation from Synopsys for details on using the hardware modeler. This appendix only describes the specifics of using hardware models with ModelSim.

VHDL Hardware Model Interface

The simulator interfaces to a hardware model through a foreign architecture. The foreign architecture contains a foreign attribute string that associates a specific hardware model with the architecture. On elaboration of the foreign architecture, the simulator automatically loads the hardware modeler software and establishes communication with the specific hardware model.

The simulator locates the hardware modeler interface software based on entries in the *modelsim.ini* initialization file. The simulator and the **hm_entity** tool (for creating foreign architectures) both depend on these entries being set correctly.

These entries are found under the [lmc] section of the default *modelsim.ini* file located in the ModelSim installation directory. The default settings are as follows:

```
[lmc]
; The simulator's interface to Logic Modeling's hardware modeler SFI software
libhm = $MODEL_TECH/libhm.sl
; The simulator's interface to Logic Modeling's hardware modeler SFI software
;   (Windows NT)
; libhm = $MODEL_TECH/libhm.dll
; Logic Modeling's hardware modeler SFI software (IBM RISC System/6000)
; libsfi = <sfi_dir>/lib/rs6000/libsfi.a
; Logic Modeling's hardware modeler SFI software (Sun4 Solaris)
; libsfi = <sfi_dir>/lib/sun4.solaris/libsfi.so
; Logic Modeling's hardware modeler SFI software (Window NT)
; libsfi = <sfi_dir>/lib/pcnt/lm_sfi.dll
; Logic Modeling's hardware modeler SFI software (Linux)
; libsfi = <sfi_dir>/lib/linux/libsfi.so
```

The simulator automatically loads both the **libhm** and **libsfi** libraries when it elaborates a hardware model foreign architecture.

- **libhm** — This variable points to the tool's dynamic link library that interfaces the foreign architecture to the hardware modeler software.

By default, **libhm** points to the *libhm.sl* supplied in the installation directory indicated by the MODEL_TECH environment variable. The tool automatically sets the MODEL_TECH environment variable to the appropriate directory containing the executables and binaries for the current operating system. If you are running the Windows operating system, then you must comment out the default **libhm** entry (precede the line with the ";" character) and uncomment the **libhm** entry for the Windows operating system.

- **libsfi** — This variable points to the Logic Modeling dynamic link library software that accesses the hardware modeler.

Uncomment the appropriate **libsfi** setting for your operating system, and replace **<sfidir>** with the path to the hardware modeler software installation directory.

In addition, you must set the **LM_LIB** and **LM_DIR** environment variables as described in Logic Modeling documentation from Synopsys.

Creating Foreign Architectures with `hm_entity`

The **hm_entity** tool automatically creates entities and foreign architectures for hardware models.

Syntax

```
hm_entity [-xe] [-xa] [-c] [-93] [-modelsimini <ini_filepath>] <shell software filename>
```

Arguments

- **-xe** — Do not generate entity declarations.
- **-xa** — Do not generate architecture bodies.
- **-c** — Generate component declarations.
- **-93** — Use extended identifiers where needed.
- **-modelsimini <ini_filepath>** — Load an alternate initialization file that replaces the current initialization file. Overrides the file path specified in the MODELSIM environment variable. Specify either an absolute or relative path the initialization file. On Windows systems the path separator should be a forward slash (/).
- **<shell software filename>** — Hardware model shell software filename (see Logic Modeling documentation from Synopsys for details on shell software files)

Usage Flow

1. Create the entity and foreign architecture using the `hm_entity` tool.

By default, **hm_entity** writes the entity and foreign architecture to stdout, but you can redirect it to a file with the following syntax:

% hm_entity LMTEST.MDL > lmtest.vhd

2. Compile the entity and foreign architecture into a library named *lmc*.

For example, the following commands compile the entity and foreign architecture:

% vlib lmc

% vcom -work lmc lmtest.vhd

3. Generate a component declaration.

You will need to generate a component declaration so that you can instantiate the hardware model in your VHDL design. If you have multiple hardware models, you may want to add all of their component declarations to a package so that you can easily reference them in your design. The following command writes the component declaration to stdout for the **LMTEST** hardware model.

% hm_entity -c -xe -xa LMTEST.MDL

4. Place the component declaration into your design.

Paste the resulting component declaration into the appropriate place in your design or into a package.

Example Output

The following is an example of the entity and foreign architecture created by **hm_entity** for the **CY7C285** hardware model:

```
library ieee;
use ieee.std_logic_1164.all;

entity cy7c285 is
  generic ( DelayRange : STRING := "Max" );
  port ( A0 : in std_logic;
        A1 : in std_logic;
        A2 : in std_logic;
        A3 : in std_logic;
        A4 : in std_logic;
        A5 : in std_logic;
        A6 : in std_logic;
        A7 : in std_logic;
        A8 : in std_logic;
        A9 : in std_logic;
        A10 : in std_logic;
        A11 : in std_logic;
        A12 : in std_logic;
        A13 : in std_logic;
        A14 : in std_logic;
        A15 : in std_logic;
        CS : in std_logic;
        O0 : out std_logic;
        O1 : out std_logic;
        O2 : out std_logic;
        O3 : out std_logic;
```

```
    O4 : out std_logic;
    O5 : out std_logic;
    O6 : out std_logic;
    O7 : out std_logic;
    W  : inout std_logic );
end;
architecture Hardware of cy7c285 is
    attribute FOREIGN : STRING;
    attribute FOREIGN of Hardware : architecture is
        "hm_init $MODEL_TECH/libhm.sl ; CY7C285.MDL";
begin
end Hardware;
```

- Entity Details

- The entity name is the hardware model name (you can manually change this name if you like).
- The port names are the same as the hardware model port names (*these names must not be changed*). If the hardware model port name is not a valid VHDL identifier, then **hm_entity** issues an error message. If **hm_entity** is invoked with the **-93** option, then the identifier is converted to an extended identifier, and the resulting entity must also be compiled with the **-93** option. Another option is to create a pin-name mapping file. Consult the Logic Modeling documentation from Synopsys for details.
- The port types are **std_logic**. This data type supports the full range of hardware model logic states.
- The *DelayRange* generic selects minimum, typical, or maximum delay values. Valid values are "min", "typ", or "max" (the strings are not case-sensitive). The default is "max".

- Architecture Details

- The first part of the foreign attribute string (hm_init) is the same for all hardware models.
- The second part (*\$MODEL_TECH/libhm.sl*) is taken from the **libhm** entry in the initialization file, *modelsim.ini*.
- The third part (CY7C285.MDL) is the shell software filename. This name correlates the architecture with the hardware model at elaboration.

Hardware Model Vector Ports

The entities generated by **hm_entity** only contain single-bit ports, never vectored ports. However, for ease of use in component instantiations, you may want to create a custom component declaration and component specification that groups ports into vectors. You can also rename and reorder the ports in the component declaration. You can also reorder the ports in the entity declaration, but you can not rename them!

The following is an example component declaration and specification that groups the address and data ports of the CY7C285 hardware model:

```
component cy7c285
  generic ( DelayRange : STRING := "Max" );
  port ( A : in std_logic_vector (15 downto 0);
        CS : in std_logic;
        O : out std_logic_vector (7 downto 0);
        WAIT_PORT : inout std_logic );
end component;
for all: cy7c285
  use entity work.cy7c285
  port map (A0 => A(0),
            A1 => A(1),
            A2 => A(2),
            A3 => A(3),
            A4 => A(4),
            A5 => A(5),
            A6 => A(6),
            A7 => A(7),
            A8 => A(8),
            A9 => A(9),
            A10 => A(10),
            A11 => A(11),
            A12 => A(12),
            A13 => A(13),
            A14 => A(14),
            A15 => A(15),
            CS => CS,
            O0 => O(0),
            O1 => O(1),
            O2 => O(2),
            O3 => O(3),
            O4 => O(4),
            O5 => O(5),
            O6 => O(6),
            O7 => O(7),
            WAIT_PORT => W );
```

Hardware Model Commands

The following simulator commands are available for hardware models. Refer to the Logic Modeling documentation from Synopsys for details on these operations.

- Enable/disable test vector logging for the specified hardware model.

```
lm_vectors on|off <instance_name> [<filename>]
```

- Enable/disable timing measurement for the specified hardware model.

```
lm_measure_timing on|off <instance_name> [<filename>]
```

- Enable/disable timing checks for the specified hardware model.

```
lm_timing_checks on|off <instance_name>
```

- Enable/disable pattern looping for the specified hardware model.

```
lm_loop_patterns on|off <instance_name>
```

- Enable/disable unknown propagation for the specified hardware model.

```
lm_unknowns on|off <instance_name>
```

Appendix I

Logic Modeling SmartModels

You can use the Logic Modeling SWIFT-based SmartModel library with ModelSim. The SmartModel library is a collection of behavioral models supplied in binary form with a procedural interface that is accessed by the simulator.

You must obtain SmartModel library from Logic Modeling along with the documentation that describes how to use it. This appendix only describes the specifics of using the library with ModelSim.

Note



A 32-bit SmartModel will not run with a 64-bit version of the simulator. When trying to load the operating system specific 32-bit library into the 64-bit executable, the pointer sizes will be incorrect.

VHDL SmartModel Interface

ModelSim VHDL interfaces to a SmartModel through a foreign architecture. The foreign architecture contains a foreign attribute string that associates a specific SmartModel with the architecture. On elaboration of the foreign architecture, the simulator automatically loads the SmartModel library software and establishes communication with the specific SmartModel.

To enable the SmartModel interface you must do the following:

- Set the **LMC_HOME** environment variable to the root of the SmartModel library installation directory. Consult Logic Modeling's documentation for details.
- Uncomment the appropriate **libswift** entry in the *modelsim.ini* file for your operating system.
- If you are running the Windows operating system, you must also comment out the default **libsm** entry (precede the line with the ";" character) and uncomment the **libsm** entry for the Windows operating system.

The **libswift** and **libsm** entries are found under the [lmc] section of the default *modelsim.ini* file located in the ModelSim installation directory. The default settings are as follows:

```
[lmc]
; The simulator's interface to Logic Modeling's SmartModel SWIFT software
libsm = $MODEL_TECH/libsm.sl
; The simulator's interface to Logic Modeling's SmartModel SWIFT software
; (Windows NT)
; libsm = $MODEL_TECH/libsm.dll
; Logic Modeling's SmartModel SWIFT software (IBM RISC System/6000)
; libswift = $LMC_HOME/lib/ibmrs.lib/swift.o
; Logic Modeling's SmartModel SWIFT software (Sun4 Solaris)
; libswift = $LMC_HOME/lib/sun4Solaris.lib/libswift.so
; Logic Modeling's SmartModel SWIFT software (Windows NT)
; libswift = $LMC_HOME/lib/pcnt.lib/libswift.dll
; Logic Modeling's SmartModel SWIFT software (Linux)
; libswift = $LMC_HOME/lib/x86_linux.lib/libswift.so
```

The simulator automatically loads both the **libsm** and **libswift** libraries when it elaborates a SmartModel foreign architecture.

- **libsm** — This variable points to the tool's dynamic link library that interfaces the foreign architecture to the SmartModel software.

By default, the **libsm** entry points to the *libsm.sl* supplied in the ModelSim installation directory indicated by the **MODEL_TECH** environment variable. ModelSim automatically sets the **MODEL_TECH** environment variable to the appropriate directory containing the executables and binaries for the current operating system.

- **libswift** — This variable points to the Logic Modeling dynamic link library software that accesses the SmartModels.

Creating Foreign Architectures with `sm_entity`

The `sm_entity` tool automatically creates entities and foreign architectures for SmartModels.

Syntax

```
sm_entity [-] [-xe] [-xa] [-c] [-all] [-v] [-93] [-modelsimini <ini_filepath>]
[<SmartModelName>...]
```

Arguments

- - — Read SmartModel names from standard input.
- -xe — Do not generate entity declarations.
- -xa — Do not generate architecture bodies.
- -c — Generate component declarations.
- -all — Select all models installed in the SmartModel library.
- -v — Display progress messages.
- -93 — Use extended identifiers where needed.

- `-modelsimini <ini_filepath>` — Load an alternate initialization file that replaces the current initialization file. Overrides the file path specified in the `MODELSIM` environment variable. Specify either an absolute or relative path the initialization file. On Windows systems the path separator should be a forward slash (/).
- `<SmartModelName>` — Name of a SmartModel (see the SmartModel library documentation for details on SmartModel names).

Usage Flow

1. Create the entity and foreign architecture using the `sm_entity` tool.

By default, the `sm_entity` tool writes an entity and foreign architecture to stdout, but you can redirect it to a file with the following syntax

```
% sm_entity -all > sml.vhd
```

2. Compile the entity and foreign architecture into a library named `lmc`.

For example, the following commands compile the entity and foreign architecture:

```
% vlib lmc
```

```
% vcom -work lmc sml.vhd
```

3. Generate a component declaration

You will need to generate a component declaration for the SmartModels so that you can instantiate the SmartModels in your VHDL design. Add these component declarations to a package named `sml` (for example), and compile the package into the `lmc` library:

```
% sm_entity -all -c -xe -xa > smlcomp.vhd
```

4. Create a package of SmartModel component declarations

Edit the resulting `smlcomp.vhd` file to turn it into a package as follows:

```
library ieee;  
use ieee.std_logic_1164.all;  
package sml is  
    <component declarations go here>  
end sml;
```

5. Compile the package into the `lmc` library:

```
% vcom -work lmc smlcomp.vhd
```

6. Reference the SmartModels in your design.

Add the following `library` and `use` clauses to your code:

```
library lmc;  
use lmc.sml.all;
```

Example Output

The following is an example of an entity and foreign architecture created by **sm_entity** for the cy7c285 SmartModel.

```
library ieee;
use ieee.std_logic_1164.all;

entity cy7c285 is
  generic (TimingVersion : STRING := "CY7C285-65";
    DelayRange : STRING := "Max";
    MemoryFile : STRING := "memory" );
  port ( A0 : in std_logic;
    A1 : in std_logic;
    A2 : in std_logic;
    A3 : in std_logic;
    A4 : in std_logic;
    A5 : in std_logic;
    A6 : in std_logic;
    A7 : in std_logic;
    A8 : in std_logic;
    A9 : in std_logic;
    A10 : in std_logic;
    A11 : in std_logic;
    A12 : in std_logic;
    A13 : in std_logic;
    A14 : in std_logic;
    A15 : in std_logic;
    CS : in std_logic;
    O0 : out std_logic;
    O1 : out std_logic;
    O2 : out std_logic;
    O3 : out std_logic;
    O4 : out std_logic;
    O5 : out std_logic;
    O6 : out std_logic;
    O7 : out std_logic;
    WAIT_PORT : inout std_logic );
end;
architecture SmartModel of cy7c285 is
  attribute FOREIGN : STRING;
  attribute FOREIGN of SmartModel : architecture is
    "sm_init $MODEL_TECH/libsm.sl ; cy7c285";
begin
end SmartModel;
```

- Entity Details

- The entity name is the SmartModel name (you can manually change this name if you like).
- The port names are the same as the SmartModel port names (*these names must not be changed*). If the SmartModel port name is not a valid VHDL identifier, then **sm_entity** automatically converts it to a valid name. If **sm_entity** is invoked with the **-93** option, then the identifier is converted to an extended identifier, and the resulting entity must also be compiled with the **-93** option. If the **-93** option had been

specified in the example above, then *WAIT* would have been converted to `\WAIT\`. Note that in this example the port *WAIT* was converted to *WAIT_PORT* because **wait** is a VHDL reserved word.

- The port types are **std_logic**. This data type supports the full range of SmartModel logic states.
- The *DelayRange*, *TimingVersion*, and *MemoryFile* generics represent the SmartModel attributes of the same name. Consult your SmartModel library documentation for a description of these attributes (and others). **Sm_entity** creates a generic for each attribute of the particular SmartModel. The default generic value is the default attribute value that the SmartModel has supplied to **sm_entity**.
- Architecture Details
 - The first part of the foreign attribute string (`sm_init`) is the same for all SmartModels.
 - The second part (`$MODEL_Tech/libsm.sl`) is taken from the **libsm** entry in the initialization file, `modelsim.ini`.
 - The third part (`cy7c285`) is the SmartModel name. This name correlates the architecture with the SmartModel at elaboration.

SmartModel Vector Ports

The entities generated by **sm_entity** only contain single-bit ports, never vectored ports. This is necessary because ModelSim correlates entity ports with the SmartModel SWIFT interface by name. However, for ease of use in component instantiations, you may want to create a custom component declaration and component specification that groups ports into vectors. You can also rename and reorder the ports in the component declaration. You can also reorder the ports in the entity declaration, but you can't rename them!

The following is an example component declaration and specification that groups the address and data ports of the CY7C285 SmartModel:

```
component cy7c285
  generic ( TimingVersion : STRING := "CY7C285-65";
           DelayRange : STRING := "Max";
           MemoryFile : STRING := "memory" );
  port ( A : in std_logic_vector (15 downto 0);
        CS : in std_logic;
        O : out std_logic_vector (7 downto 0);
        WAIT_PORT : inout std_logic );
end component;

for all: cy7c285
  use entity work.cy7c285
  port map (A0 => A(0),
           A1 => A(1),
           A2 => A(2),
```

```
A3 => A(3),  
A4 => A(4),  
A5 => A(5),  
A6 => A(6),  
A7 => A(7),  
A8 => A(8),  
A9 => A(9),  
A10 => A(10),  
A11 => A(11),  
A12 => A(12),  
A13 => A(13),  
A14 => A(14),  
A15 => A(15),  
CS => CS,  
O0 => O(0),  
O1 => O(1),  
O2 => O(2),  
O3 => O(3),  
O4 => O(4),  
O5 => O(5),  
O6 => O(6),  
O7 => O(7),  
WAIT_PORT => WAIT_PORT );
```

Command Channel

The command channel is a SmartModel feature that lets you invoke SmartModel specific commands. These commands are documented in the SmartModel library documentation from Synopsys. ModelSim provides access to the Command Channel from the command line. The form of a SmartModel command is:

lmc {<instance_name> | -all} "<SmartModel command>"

- **instance_name** — is either a full hierarchical name or a relative name of a SmartModel instance. A relative name is relative to the current environment setting (see [environment](#) command). For example, to turn timing checks off for SmartModel */top/u1*:

lmc /top/u1 "SetConstraints Off"

- **-all** — applies the command to all SmartModel instances. For example, to turn timing checks off for all SmartModel instances:

lmc -all "SetConstraints Off"

There are also some SmartModel commands that apply globally to the current simulation session rather than to models. The form of a SmartModel session command is:

lmcsession "<SmartModel session command>"

SmartModel Windows

Some models in the SmartModel library provide access to internal registers with a feature called SmartModel Windows. Refer to Logic Modeling's SmartModel library documentation for details on this feature. The simulator interface to this feature is described below.

Window names that are not valid VHDL or Verilog identifiers are converted to VHDL extended identifiers. For example, with a window named `z1I10.GSR.OR`, the tool treats the name as `\z1I10.GSR.OR\` (for all commands including `lmcwin`, `add wave`, and `examine`). You must then use that name in all commands. For example,

```
add wave /top/swift_model/\z1I10.GSR.OR\
```

Extended identifiers are case sensitive.

ReportStatus

The **ReportStatus** command displays model information, including the names of window registers. For example,

```
lmc /top/u1 ReportStatus
```

SmartModel Windows description:

```
WA "Read-Only (Read Only)"  
WB "1-bit"  
WC "64-bit"
```

This model contains window registers named *wa*, *wb*, and *wc*. These names can be used in subsequent window (**lmcwin**) commands.

SmartModel lmcwin Commands

Each of the following commands requires a window instance argument that identifies a specific model instance and window name. For example, `/top/u1/wa` refers to window *wa* in model instance `/top/u1`.

- `lmcwin read` — displays the current value of a window.

```
lmcwin read <window_instance> [-<radix>]
```

The optional radix argument is **-binary**, **-decimal**, or **-hexadecimal** (these names can be abbreviated). The default is to display the value using the **std_logic** characters. For example, the following command displays the 64-bit window *wc* in hexadecimal:

```
lmcwin read /top/u1/wc -h
```

- `lmcwin write` — writes a value into a window.

```
lmcwin write <window_instance> <value>
```

The format of the value argument is the same as used in other simulator commands that take value arguments. For example, to write 1 to window *wb*, and all 1's to window *wc*:

```
lmcwin write /top/u1/wb 1  
lmcwin write /top/u1/wc X"FFFFFFFFFFFFFFFF"
```

- **lmcwin enable** — enables continuous monitoring of a window.

```
lmcwin enable <window_instance>
```

The specified window is added to the model instance as a signal (with the same name as the window) of type **std_logic** or **std_logic_vector**. This signal's values can then be referenced in simulator commands that read signal values, such as the [add list](#) command shown below. The window signal is continuously updated to reflect the value in the model. For example, to list window *wa*:

```
lmcwin enable /top/u1/wa  
add list /top/u1/wa
```

- **lmcwin disable** — disables continuous monitoring of a window.

```
lmcwin disable <window_instance>
```

The window signal is not deleted, but it no longer is updated when the model's window register changes value. For example, to disable continuous monitoring of window *wa*:

```
lmcwin disable /top/u1/wa
```

- **lmcwin release** — disables the effect of a previous **lmcwin write** command on a window net.

```
lmcwin release <window_instance>
```

Some windows are actually nets, and the **lmcwin write** command behaves more like a continuous force on the net.

Memory Arrays

A memory model usually makes the entire register array available as a window. In this case, the window commands operate only on a single element at a time. The element is selected as an array reference in the window instance specification. For example, to read element 5 from the window memory *mem*:

```
lmcwin read /top/u2/mem(5)
```

Omitting the element specification defaults to element 0. Also, continuous monitoring is limited to a single array element. The associated window signal is updated with the most recently enabled element for continuous monitoring.

Verilog SmartModel Interface

The SWIFT SmartModel library, beginning with release r40b, provides an optional library of Verilog modules and a PLI application that communicates between a simulator's PLI and the SWIFT simulator interface. The Logic Modeling documentation refers to this as the Logic Models to Verilog (LMTV) interface. To install this option, you must select the simulator type "Verilog" when you run Logic Modeling's SmartInstall program.

Linking the LMTV Interface to the Simulator

Synopsys provides a dynamically loadable library that links ModelSim to the LMTV interface.

Refer to Logic Modeling's SmartModel library documentation for details on this feature.

— Symbols —

- , 462
- #, comment character, 836
- \$disable_signal_spy, 759
- \$enable_signal_spy, 761
- \$finish
 - behavior, customizing, 897
- \$sdf_annotate system task, 805
- \$unit scope, visibility in SV declarations, 293
- +acc option, design object visibility, 219
- .ini control variables
 - AssertFile, 866
 - AssertionDebug, 866, 869
 - AssertionFailAction, 866
 - AssertionFailEnable, 867
 - AssertionFailLimit, 867
 - AssertionFailLocalVarLog, 867
 - AssertionFailLog, 868
 - AssertionPassEnable, 868
 - AssertionPassLimit, 868
 - AssertionPassLog, 868
 - BreakOnAssertion, 869
 - CheckPlusargs, 870
 - CheckpointCompressMode, 870
 - CommandHistory, 871
 - ConcurrentFileLimit, 871
 - CoverCountAll, 872
 - CoverExcludeDefault, 873
 - DefaultForceKind, 876
 - DefaultRadix, 877
 - DefaultRestartOptions, 878
 - DelayFileOpen, 878
 - DumpportsCollapse, 880
 - ErrorFile, 881
 - GenerateFormat, 883
 - GenerousIdentifierParsing, 884
 - GlobalSharedObjectList, 884
 - IgnoreError, 885
 - IgnoreFailure, 885
 - IgnoreNote, 886
 - IgnoreWarning, 887
 - IterationLimit, 887
 - License, 888
 - MessageFormat, 889
 - MessageFormatBreak, 890
 - MessageFormatBreakLine, 890
 - MessageFormatError, 890
 - MessageFormatFail, 891
 - MessageFormatFatal, 891
 - MessageFormatNote, 891
 - MessageFormatWarning, 892
 - NoAutoSDFCompile, 893
 - NumericStdNoWarnings, 896
 - PathSeparator, 898
 - Resolution, 902
 - RunLength, 902
 - ScTimeUnit, 905
 - ShowUnassociatedScNameWarning, 909
 - ShowUndebuggableScTypeWarning, 909
 - Startup, 910
 - StdArithNoWarnings, 911
 - ToggleCountLimit, 913
 - ToggleFixedSizeArray, 914
 - ToggleMaxFixedSizeArray, 914
 - ToggleMaxIntValues, 914
 - ToggleMaxRealValues, 915
 - ToggleNoIntegers, 915
 - TogglePackedAsVec, 916
 - ToggleVlogEnumBits, 916
 - ToggleVlogIntegers, 916
 - ToggleVlogReal, 917
 - ToggleWidthLimit, 917
 - TranscriptFile, 917
 - UCDBFilename, 918
 - UnbufferedOutput, 918
 - UserTimeUnit, 919
 - Veriuser, 920
 - VoptAutoSDFCompile, 921
 - VoptFlow, 921
 - WarnConstantChange, 922

WaveSignalNameWidth, 923
 WLFCacheSize, 923
 WLFCollapseMode, 923
 WLFCompress, 924
 WLFDeleteOnQuit, 924
 WLFFilename, 925
 WLFIndex, 925
 WLFOptimize, 925
 WLFSaveAllRegions, 926
 WLFSimCacheSize, 926
 WLFSizeLimit, 927
 WLFTimeLimit, 927
 ZeroIn, 928
 ZeroInOptions, 928
 .ini VHDL compiler control variables
 ShowConstantImmediateAsserts, 908
 .modelsim file
 in initialization sequence, 1003
 purpose, 1001
 .so, shared object file
 loading PLI/VPI/DPI C applications, 960
 loading PLI/VPI/DPI C++ applications,
 965

— Numerics —

0-In tools
 setting environment variable, 1005
 1076, IEEE Std, 52
 differences between versions, 257
 1364, IEEE Std, 53, 285, 343
 1364-2005
 IEEE std, 183, 810
 2-state toggle coverage, 651
 3-state toggle coverage, 651
 64-bit libraries, 250
 64-bit platforms
 choosing over 32-bit, 1008
 64-bit time
 now variable, 842
 Tcl time commands, 844
 64-bit vsim, using with 32-bit FLI apps, 980

— A —

+acc option, design object visibility, 219
 ACC routines, 977
 accelerated packages, 248

AcceptLowerCasePragmasOnly .ini file
 variable, 865
 access
 hierarchical objects, 757
 limitations in mixed designs, 403
 Active Processes pane, 92
 see also windows, Active Processes pane
 aggregates, SystemC, 374
 Algorithm
 negative timing constraint, 316
 AmsStandard .ini file variable, 865
 analog sidebar, 176
 annotating differences, wave compare, 610
 api_version in error message, 397
 architecture simulator state variable, 841
 archives
 described, 242
 argc simulator state variable, 841
 arguments
 passing to a DO file, 849
 arguments, accessing command-line, 392
 arithmetic package warnings, disabling, 931
 array of sc_signal<T>, 374
 AssertFile .ini file variable, 866
 AssertionDebug .ini file variable, 866, 869
 AssertionFailAction .ini file variable, 866
 AssertionFailEnable .ini file variable, 867
 AssertionFailLimit .ini file variable, 867
 AssertionFailLocalVarLog .ini file variable,
 867
 AssertionFailLog .ini file variable, 868
 AssertionPassEnable .ini file variable, 868
 AssertionPassLimit .ini file variable, 868
 AssertionPassLog .ini file variable, 868
 assertions
 binding, 403
 file and line number, 889
 message display, 862
 messages
 turning off, 930
 setting format of messages, 889
 warnings, locating, 889
 attribute
 definition of, 488
 auto exclusion

- fsm transitions, 656
 - auto find bp command, 723
 - auto step mode, C Debug, 723
 - automatic saving of UCDB, 698
- B —
- bad magic number error message, 531
 - base (radix)
 - List window, 582
 - Wave window, 574
 - batch-mode simulations, 51
 - bind
 - hierarchical references, 405
 - restrictions, 404
 - port mapping, 406
 - to VHDL enumerated types, 406
 - what can be bound, 404
 - bind construct
 - limitations for SystemC, 348, 412
 - SystemC binding
 - to Verilog/SV design unit, 348
 - SystemVerilog, 403
 - bind statement
 - in compilation unit scope, 410
 - syntax, 404
 - BindAtCompile .ini file variable, 869
 - binding, VHDL, default, 260
 - bitwise format, 609
 - blocking assignments, 308
 - bookmarks
 - Source window, 150
 - Wave window, 565
 - bound block
 - hierarchical references, 405
 - break
 - stop simulation run, 76, 84
 - BreakOnAssertion .ini file variable, 869
 - Breakpoint
 - SystemC constructor/destructor, 371
 - Breakpoints
 - command execution, 150
 - conditional, 150
 - deleting, 147
 - edit, 148
 - load, 150
 - saving/restoring, 599
 - set with GUI, 147
 - breakpoints
 - C code, 719
 - deleting, 599
 - edit, 596, 599
 - setting automatically in C code, 723
 - Source window, viewing in, 133
 - unavailable with vopt, 211
 - Breakpontos
 - save, 150
 - .bsm file, 626
 - bubble diagram
 - using the mouse, 112, 113
 - buffered/unbuffered output, 918
 - busses
 - RTL-level, reconstructing, 540
 - user-defined, 589
 - buswise format, 609
- C —
- C applications
 - compiling and linking, 960
 - debugging, 717
 - C Debug, 717
 - auto find bp, 723
 - auto step mode, 723
 - debugging functions during elaboration, 726
 - debugging functions when exiting, 729
 - function entry points, finding, 723
 - initialization mode, 726
 - registered function calls, identifying, 723
 - running from a DO file, 719
 - Stop on quit mode, 729
 - C++ applications
 - compiling and linking, 965
 - Call Stack pane, 100
 - cancelling scheduled events, performance, 284
 - capacity analysis, 747
 - case sensitivity
 - named port associations, 442
 - causality, tracing in Dataflow window, 621
 - cdbg_wait_for_starting command, 719
 - cell libraries, 324
 - change command
 - modifying local variables, 326

- chasing X, [622](#)
- check_synthesis argument
 - warning message, [941](#)
- CheckPlusargs .ini file variable, [870](#)
- checkpoint/restore
 - checkpointing a running simulation, [481](#)
 - foreign C code and heap memory, [481](#)
- CheckpointCompressMode .ini file variable, [870](#)
- CheckSynthesis .ini file variable, [871](#)
- cin support, SystemC, [391](#)
- Class objects
 - view in Wave window, [586](#)
- class of sc_signal<T>, [374](#)
- cleanup
 - SystemC state-based code, [366](#)
- clean-up of SystemC state-based code, [366](#)
- CLI commands for debugging transactions, [521](#)
- clock change, sampling signals at, [594](#)
- clock cycles
 - display in timeline, [572](#)
- clocked comparison, [606](#)
- Clocking block inout display, [181](#)
- Code Coverage, [159](#)
 - \$coverage_save system function, [329](#)
 - condition coverage, [636](#)
 - Current Exclusions pane, [108](#)
 - enabling with vsim, [639](#)
 - excluding lines/files, [657](#)
 - exclusion filter files
 - used in multiple simulation runs, [668](#)
 - expression coverage, [636](#), [648](#)
 - FSM coverage, [636](#)
 - Instance Coverage pane, [115](#)
 - Main window coverage data, [641](#)
 - missed branches, [127](#)
 - missed coverage, [126](#)
 - pragma exclusions, [657](#), [666](#)
 - reports, [669](#)
 - Source window data, [138](#)
 - source window details, [107](#)
 - toggle coverage, [636](#)
 - toggle coverage in Signals window, [651](#)
 - toggle details, [107](#)
- code coverage
 - and optimization, [674](#)
 - branch coverage, [636](#)
 - condition coverage, [648](#)
 - design is not fully covered, [674](#)
 - Focused Expression Coverage (FEC), [647](#)
 - see also Coverage
 - statement coverage, [636](#)
- code profiling, [733](#)
- collapsing ports, and coverage reporting, [671](#)
- collapsing time and delta steps, [538](#)
- Color
 - radix
 - example, [65](#)
- colorization, in Source window, [151](#)
- Combine Selected Signals dialog box, [117](#)
- combining signals, busses, [589](#)
- CommandHistory .ini file variable, [871](#)
- command-line arguments, accessing, [392](#)
- command-line mode, [50](#)
- commands
 - event watching in DO file, [848](#)
 - system, [840](#)
 - vcd2wlf, [827](#)
 - VSIM Tcl commands, [844](#)
- comment character
 - Tcl and DO files, [836](#)
- Commonly Used modelsim.ini Variables, [929](#)
- compare
 - add signals, [604](#)
 - adding regions, [604](#)
 - by signal, [604](#)
 - clocked, [606](#)
 - difference markers, [609](#)
 - displayed in list window, [611](#)
 - icons, [610](#)
 - options, [607](#)
 - pathnames, [608](#)
 - reference dataset, [603](#)
 - reference region, [604](#)
 - tab, [603](#)
 - test dataset, [603](#)
 - timing differences, [609](#)
 - tolerance, [606](#)
 - values, [610](#)

- wave window display, 608
- compare by region, 604
- compare commands, 602
- compare signal, virtual
 - restrictions, 589
- compare simulations, 529
- compilation
 - multi-file issues (SystemVerilog), 293
 - SDF files, 803
- compilation unit scope, 293
- Compile
 - VHDL, 254
- compile
 - SystemC
 - reducing non-debug compile time, 350
- compile order
 - auto generate, 229
 - changing, 228
 - SystemVerilog packages, 290
- Compiler Control Variable
 - SystemC
 - CppPath, 876
 - SccomLogfile, 903
 - SccomVerbose, 903
 - ScvPhaseRelationName, 905
 - UseScv, 919
- Compiler Control Variables
 - Verilog
 - AcceptLowerCasePragmasOnly, 865
 - CoverCells, 872
 - GenerateLoopIterationMax, 883
 - GenerateRecursionDepthMax, 884
 - Hazard, 885
 - LibrarySearchPath, 888
 - MultiFileCompilationUnit, 893
 - Protect, 901
 - Quiet, 901
 - Show_BadOptionWarning, 905
 - Show_Lint, 906
 - SparseMemThreshold, 910
 - UpCase, 918
 - vlog95compat, 921
 - VHDL
 - AmsStandard, 865
 - BindAtCompile, 869
 - CheckSynthesis, 871
 - CoverageFEC, 873
 - CoverageShortCircuit, 875
 - CoverageSub, 872
 - Explicit, 881
 - IgnoreVitalErrors, 886
 - NoCaseStaticError, 893
 - NoDebug, 894
 - NoIndexCheck, 894
 - NoOthersStaticError, 894
 - NoRangeCheck, 895
 - NoVital, 895
 - NoVitalCheck, 896
 - Optimize_1164, 898
 - PedanticErrors, 898
 - RequireConfigForAllDefaultBinding, 901
 - ScalarOpts, 903
 - Show_source, 906
 - Show_VitalChecksWarning, 906
 - Show_Warning1, 907
 - Show_Warning2, 907
 - Show_Warning3, 907
 - Show_Warning4, 907
 - Show_Warning5, 908
 - VHDL93, 920
- compiler directives, 336
 - IEEE Std 1364-2000, 337
 - XL compatible compiler directives, 339
- compiling
 - overview, 48
 - changing order in the GUI, 228
 - gensrc errors during, 397
 - grouping files, 229
 - order, changing in projects, 228
 - properties, in projects, 237
 - range checking in VHDL, 255
 - SystemC, 348
 - converting sc_main(), 383
 - exporting top level module, 349
 - for source level debug, 350
 - invoking sccom, 349
 - linking the compiled source, 363
 - modifying source code, 383
 - replacing sc_start(), 383

- using socom vs. raw C++ compiler, 351
- Verilog, 287
 - incremental compilation, 289
 - XL 'uselib compiler directive, 295
 - XL compatible options, 295
- VHDL, 253
- VITAL packages, 270
- compiling C code, gcc, 962
- component declaration
 - generating SystemC from Verilog or VHDL, 466
 - generating VHDL from Verilog, 439
 - vgencomp for SystemC, 466
 - vgencomp for VHDL, 439
- component, default binding rules, 260
- Compressing files
 - VCD tasks, 824
- ConcurrentFileLimit .ini file variable, 871
- configuration
 - Verilog, support, 449
- configuration simulator state variable, 841
- configurations
 - instantiation in mixed designs, 438
 - Verilog, 298
- connectivity, exploring, 618
- Constants
 - VHDL, 443
- Constraint algorithm
 - negative timing checks, 316
- construction parameters, SystemC, 393
- Constructor
 - breakpoint, 371
- Contains, 60, 62, 63
- context menus
 - Library tab, 244
- control function, SystemC, 413
- control_foreign_signal() function, 403
- Convergence
 - delay solution, 316
- convert real to time, 274
- convert time to real, 273
- converting to a module, 383
- coverage
 - auto exclusions
 - fsm transitions, 656
 - data, automatic saving of, 698
 - enable FSMs, 682
 - fsm exclusions, 665
 - fsm states, 681
 - fsm transitions, 681
 - setting default mode, 672
 - UCDB, 695
- Coverage Details window, 106
- coverage exclusion pragmas
 - fsm, 666
- coverage numbers, mismatching, 140
- coverage reports, 669
 - default mode, 672
 - HML format, 673
 - reporting all signals, 671
 - xml format, 673
- coverage toggle_ignore pragma, 664
- \$coverage_save system function, 329
- CoverageFEC .ini file variable, 873
- CoverageShortCircuit .ini file variable, 875
- CoverageSub .ini file variable, 872
- CoverCells .ini file variable, 872
- CoverCountAll .ini file variable, 872
- CoverExcludeDefault .ini file variable, 873
- CoverMaxFECRows .ini file variable, 873
- CoverMaxUDPRows .ini file variable, 874
- CoverOpt .ini file variable, 874
- covreport.xml, 673
- CppPath .ini file variable, 876
- create debug database, 617
- Creating do file, 66, 585, 599
- current exclusions
 - pragmas, 657
 - fsm, 666
- Current Exclusions pane, 108
- cursor linking, 178
- cursors
 - adding, deleting, locking, naming, 550
 - link to Dataflow window, 629
 - linking, 552
 - measuring time with, 548
 - trace events with, 621
 - Wave window, 548
- Customize GUI
 - fonts, 997

- customizing
 - via preference variables, 995
- D —
- deltas
 - explained, 261
- daemon
 - JobSpy, 780
- dashed signal lines, 176
- database
 - post-sim debug, 617
- Dataflow
 - post-sim debug database
 - create, 617
 - post-sim debug flow, 616
- Dataflow window, 109, 615
 - extended mode, 615
 - pan, 632
 - zoom, 632
 - see also* windows, Dataflow window
- dataflow.bsm file, 626
- Dataset Browser, 535
- Dataset Snapshot, 537
- datasets, 529
 - managing, 535
 - opening, 533
 - prevent dataset prefix display, 537
 - reference, 603
 - test, 603
 - view structure, 534
 - visibility, 535
- debug database
 - create, 617
- debug flow
 - post-simulation, 616
- debuggable SystemC objects, 368
- debugging
 - C code, 717
 - null value, 311
 - SIGSEGV, 311
 - SystemC channels and variables, 378
- debugging the design, overview, 49
- default binding
 - BindAtCompile .ini file variable, 869
 - disabling, 261
- default binding rules, 260
- default coverage mode, setting, 672
- Default editor, changing, 1005
- default SystemC parameter values, overriding, 393
- DefaultForceKind .ini file variable, 876
- DefaultRadix .ini file variable, 877
- DefaultRestartOptions .ini file variable, 878
- DefaultRestartOptions variable, 931
- delay
 - delta delays, 261
 - modes for Verilog models, 324
- Delay solution convergence, 316
- DelayFileOpen .ini file variable, 878
- deleting library contents, 243
- delta collapsing, 538
- delta simulator state variable, 841
- Delta time
 - recording
 - for expanded time viewing, 555
- deltas
 - in List window, 592
 - referencing simulator iteration
 - as a simulator state variable, 841
- dependent design units, 254
- descriptions of HDL items, 150
- design library
 - creating, 243
 - logical name, assigning, 245
 - mapping search rules, 246
 - resource type, 241
 - VHDL design units, 253
 - working type, 241
- design object icons, described, 59
- design object visibility, +acc, 219
- design optimization with vopt, 209
- design portability and SystemC, 350
- design units, 241
- Destructor
 - breakpoint, 371
- DEVICE
 - matching to specify path delays, 808
- dialogs
 - Runtime Options, 860
- Direct Programming Interface, 947
- directories

- moving libraries, [246](#)
- disable_signal_spy, [759](#)
- Display mode
 - expanded time, [559](#)
- display preferences
 - Wave window, [571](#)
- displaymsgmode .ini file variable, [879](#)
- distributed delay mode, [325](#)
- dividers
 - Wave window, [575](#)
- DLL files, loading, [960](#), [965](#)
- DO files (macros)
 - error handling, [852](#)
 - executing at startup, [910](#), [1007](#)
 - parameters, passing to, [849](#)
 - Tcl source command, [852](#)
- DOPATH environment variable, [1005](#)
- DPI
 - and qverilog command, [956](#)
 - export TFs, [940](#)
 - missing DPI import function, [956](#)
 - registering applications, [952](#)
 - use flow, [953](#)
- DPI access routines, [979](#)
- DPI export TFs, [940](#)
- DPI/VPI/PLI, [947](#)
- drivers
 - Dataflow Window, [619](#)
 - show in Dataflow window, [595](#)
 - Wave window, [595](#)
- dumpports tasks, VCD files, [822](#)
- DumpportsCollapse .ini file variable, [880](#)
- dynamic module array
 - SystemC, [375](#)

— E —

- edit
 - breakpoints, [148](#), [596](#), [599](#)
- Editing
 - in notepad windows, [986](#)
 - in the Main window, [986](#)
 - in the Source window, [986](#)
- Editing the modelsim.ini file, [860](#)
- EDITOR environment variable, [1005](#)
- editor, default, changing, [1005](#)
- elab_defer_fli argument, [485](#)

- elaboration file
 - creating, [483](#)
 - loading, [484](#)
 - modifying stimulus, [484](#)
 - simulating with PLI or FLI models, [485](#)
- embedded wave viewer, [620](#)
- empty port name warning, [940](#)
- enable_signal_spy, [761](#)
- Encoding
 - methods, [200](#)
- encrypt
 - IP code
 - public keys, [205](#)
 - undefined macros, [184](#)
 - vendor-defined macros, [186](#)
 - IP source code, [183](#)
 - usage models, [183](#)
 - protect pragmas, [183](#)
 - vencrypt utility, [183](#)
 - vencrypt command
 - header file, [185](#)
 - vlog +protect, [189](#)
- encrypting IP code
 - vencrypt utility, [183](#)
- Encryption
 - asymmetric, [200](#)
 - creating envelope, [201](#)
 - default asymmetric method for Questa, [201](#)
 - default symmetric method for Questa, [200](#)
 - for multiple simulators
 - Encryption
 - portable, [198](#)
 - methods, [200](#)
 - raw, [201](#)
 - usage models for VHDL, [192](#)
 - using Mentor Graphics public key, [205](#)
 - vlog +protect, [187](#)
- encryption
 - 'protect compiler directive, [189](#), [337](#)
 - securing pre-compiled libraries, [199](#)
- Encryption and Encoding methods, [200](#)
- end_of_construction() function, [392](#)
- end_of_simulation() function, [392](#)
- ENDFILE function, [267](#)
- ENDLINE function, [267](#)

- 'endprotect compiler directive, 189, 337
- entities
 - default binding rules, 260
- entity simulator state variable, 841
- environment variables, 1004
 - expansion, 1004
 - referencing from command line, 1010
 - referencing with VHDL FILE variable, 1010
 - setting, 1004
 - setting in Windows, 1009
 - TranscriptFile, specifying location of, 917
 - used in Solaris linking for FLI, 961, 966
 - used in Solaris linking for
 - PLI/VPI/DPI/FLI, 1005
 - using with location mapping, 933
 - variable substitution using Tcl, 840
- error
 - can't locate C compiler, 940
- error .ini file variable, 880
- ErrorFile .ini file variable, 881
- errors
 - "api_version" in, 397
 - bad magic number, 531
 - DPI missing import function, 956
 - getting more information, 936
 - libswift entry not found, 943
 - multiple definition, 398
 - out-of-line function, 398
 - severity level, changing, 936
 - SystemC loading, 396
 - SystemVerilog, missing declaration, 893
 - Tcl_init error, 941
 - void function, 398
 - VSIM license lost, 943
- escaped identifiers, 322, 442
 - Tcl considerations, 323
- EVCD files
 - exporting, 797
 - importing, 798
- event order
 - in optimized designs, 222
 - in Verilog simulation, 306
- event queues, 306
- Event time
 - recording
 - for expanded time viewing, 555
- event watching commands, placement of, 848
- events, tracing, 621
- exclusion filter files
 - excluding udp truth table rows, 661
 - used in multiple simulation runs, 668
- exclusions
 - lines and files, 657
 - Z values, 645
- exit codes, 938
- exiting tool on sc_stop or \$finish, 897
- exiting tool, customizing, 897
- expand
 - environment variables, 1004
- expand net, 618
- Expanded Time
 - customizing Wave window, 559
 - expanding/collapsing sim time, 561
 - with commands, 561
 - with menu selections, 561
 - with toolbar buttons, 561
 - in Wave and List, 554
 - recording, 555
 - delta time, 555
 - even time, 555
 - selecting display mode, 559
 - with command, 561
 - with menus, 560
 - with toolbar buttons, 560
 - switching time mode, 561
 - terminology, 554
 - viewing in List window, 562
 - viewing in Wave window, 556
- Explicit .ini file variable, 881
- export TFs, in DPI, 940
- Exporting SystemC modules
 - to Verilog, 455
- exporting SystemC modules
 - to VHDL, 466
- exporting top SystemC module, 349
- Expression Builder, 568
 - configuring a List trigger with, 593
 - saving expressions to Tcl variable, 570
- extended identifiers

- in mixed designs, [438](#), [466](#)
- Extended system tasks
 - Verilog, [335](#)
- F —
- F8 function key, [988](#)
- Fatal .ini file variable, [881](#)
- Fatal error
 - SIGSEGV, [312](#)
- FIFOs, viewing SystemC, [375](#)
- File compression
 - VCD tasks, [824](#)
- file compression
 - SDF files, [801](#)
- file I/O
 - TextIO package, [264](#)
- file-line breakpoints, [147](#)
 - edit, [148](#), [599](#)
- files
 - .modelsim, [1001](#)
- Files window, [159](#)
- files, grouping for compile, [229](#)
- Filter, [62](#)
- Filtering
 - Contains field, [60](#), [63](#)
- filtering
 - signals in Objects window, [128](#)
- filters
 - for Code Coverage
 - used in multiple simulation runs, [668](#)
- Find, [60](#)
 - stop, [566](#)
- find
 - inline search bar, [151](#), [164](#)
- Finite State Machines, [677](#)
 - coverage exclusions, [665](#)
 - enable coverage, [682](#)
 - enable recognition, [682](#)
 - recognition reporting, [688](#), [689](#)
 - state coverage, [681](#)
 - transition coverage, [681](#)
 - unsupported design styles, [678](#)
- fixed-point types, in SystemC
 - compiling for support, [390](#)
 - construction parameters for, [393](#)
- FLI, [259](#)
 - debugging, [717](#)
- folders, in projects, [235](#)
- Fonts
 - make global changes, [997](#)
- fonts
 - scaling, [59](#)
- force command
 - defaults, [931](#)
- foreign language interface, [259](#)
- foreign model loading
 - SmartModels, [1019](#)
- foreign module declaration
 - Verilog example, [450](#)
 - VHDL example, [460](#)
- foreign module declaration, SystemC, [449](#)
- Format
 - saving/restoring, [66](#), [585](#)
- format file, [584](#)
 - Wave window, [584](#)
- FPGA libraries, importing, [250](#)
- FSM
 - coverage exclusions, [666](#)
 - view current state, [685](#)
- fsm transitions
 - auto exclusions, [656](#)
- FsmResetTrans .ini file variable, [882](#)
- FsmSingle .ini file variable, [882](#)
- FsmXAssign .ini file variable, [883](#)
- Function call, debugging, [100](#)
- function calls, identifying with C Debug, [723](#)
- functions
 - SystemC
 - control, [413](#)
 - observe, [413](#)
 - unsupported, [390](#)
 - virtual, [541](#)
- G —
- g C++ compiler option, [369](#)
- g++, alternate installations, [350](#)
- gdb debugger, [717](#)
- generate statements, Veilog, [299](#)
- GenerateFormat .ini file variable, [883](#)
- GenerateLoopIterationMax .ini file variable, [883](#)

- GenerateRecursionDepthMax .ini variable, 884
- generic support
 - flow for VHDL instantiating SC, 467
 - SC instantiating VHDL, 460
- generics
 - passing to sc_foreign_module (VHDL), 460
 - SystemC instantiating VHDL, 460
 - VHDL, 421
- generics, integer
 - passing as template arguments, 462
- generics, integer and non-integer
 - passing as constructor arguments, 461
- GenerousIdentifierParsing .ini file variable, 884
- get_resolution() VHDL function, 271
- Global GUI changes
 - fonts, 997
- global visibility
 - PLI/FLI shared objects, 970
- GLOBALPATHPULSE
 - matching to specify path delays, 808
- GlobalSharedObjectsList .ini file variable, 884
- Glob-style, 62
- graphic interface, 543, 615
 - UNIX support, 52
- Grid Engine
 - JobSpy integration, 787
- grouping files for compile, 229
- grouping objects, Monitor window, 173
- groups
 - in wave window, 578
- GUI preferences
 - fonts, 997
- GUI_expression_format
 - GUI expression builder, 568
- H —
- hardware model interface, 1013
- Hazard .ini file variable, 885
- hazards
 - limitations on detection, 310
- Hierarchical access
 - mixed-language, 403
- Hierarchical references, 402
 - bind, 405
 - SystemC/mixed-HDL designs, 413
 - SystemVerilog, 413
- hierarchy
 - driving signals in, 763
 - forcing signals in, 272, 771
 - referencing signals in, 272, 767
 - releasing signals in, 273, 775
- highlighting, in Source window, 151
- highlights
 - in Source window, 137
- history
 - of commands
 - shortcuts for reuse, 985
- hm_entity, 1014
- HOLD
 - matching to Verilog, 808
- HOME environment variable, 1005
- HOME_0IN environment variable, 1005
- HTML format
 - coverage reports, 673
- Hypertext link, 133
- | —
- I/O
 - TextIO package, 264
- icons
 - shapes and meanings, 59
- identifiers
 - escaped, 322, 442
- ieee .ini file variable, 885
- IEEE libraries, 248
- IEEE Std 1076, 52
 - differences between versions, 257
- IEEE Std 1364, 53, 285, 343
- IEEE Std 1364-2005, 183, 810
- IgnoreError .ini file variable, 885
- IgnoreFailure .ini file variable, 885
- IgnoreNote .ini file variable, 886
- IgnoreVitalErrors .ini file variable, 886
- IgnoreWarning .ini file variable, 887
- importing EVCD files, waveform editor, 798
- importing FPGA libraries, 250
- incremental compilation
 - automatic, 291
 - manual, 291

- with Verilog, [289](#)
- index checking, [255](#)
- \$init_signal_driver, [763](#)
- init_signal_driver, [763](#)
- \$init_signal_spy, [767](#)
- init_signal_spy, [272](#), [767](#)
- init_usertfs function, [728](#), [949](#)
- initialization of SystemC state-based code, [366](#)
- initialization sequence, [1001](#)
- inline search bar, [151](#), [164](#)
- inlining
 - VHDL subprograms, [255](#)
- input ports
 - matching to INTERCONNECT, [807](#)
 - matching to PORT, [807](#)
- instantiation in mixed-language design
 - Verilog from VHDL, [438](#)
 - VHDL from Verilog, [441](#)
- instantiation in SystemC-Verilog design
 - SystemC from Verilog, [455](#)
 - Verilog from SystemC, [448](#)
- instantiation in SystemC-VHDL design
 - VHDL from SystemC, [458](#)
- instantiation in VHDL-SystemC design
 - SystemC from VHDL, [465](#)
- INTERCONNECT
 - matching to input ports, [807](#)
- interconnect delays, [812](#)
- IOPATH
 - matching to specify path delays, [807](#)
- IP code
 - encrypt, [183](#)
 - public keys, [205](#)
 - undefined macros, [184](#)
 - vendor-defined macros, [186](#)
 - encryption usage models, [183](#), [192](#)
 - using protect pragmas, [183](#)
 - vencrypt usage models, [183](#)
- iteration_limit, infinite zero-delay loops, [263](#)
- IterationLimit .ini file variable, [887](#)

— J —

- JobSpy
 - daemon, [780](#)

— K —

- keyboard shortcuts
 - List window, [989](#)
 - Main window, [986](#)
 - Source window, [986](#)
 - Wave window, [989](#)
- keywords
 - SystemVerilog, [288](#)

— L —

- L work, [293](#)
- language templates, [144](#)
- language versions, VHDL, [257](#)
- libraries
 - 64-bit and 32-bit in same library, [250](#)
 - creating, [243](#)
 - design libraries, creating, [243](#)
 - design library types, [241](#)
 - design units, [241](#)
 - group use, setting up, [246](#)
 - IEEE, [248](#)
 - importing FPGA libraries, [250](#)
 - mapping
 - from the command line, [245](#)
 - from the GUI, [245](#)
 - hierarchically, [929](#)
 - search rules, [246](#)
 - modelsim_lib, [271](#)
 - moving, [246](#)
 - multiple libraries with common modules, [293](#)
 - naming, [245](#)
 - others clause, [246](#)
 - predefined, [248](#)
 - refreshing library images, [249](#)
 - resource libraries, [241](#)
 - std library, [248](#)
 - Synopsys, [248](#)
 - Verilog, [292](#), [419](#), [830](#)
 - VHDL library clause, [247](#)
 - working libraries, [241](#)
 - working vs resource, [47](#)
 - working with contents of, [243](#)
- library map file, Verilog configurations, [298](#)
- library mapping, overview, [47](#)

- library maps, Verilog 2001, [298](#)
- library simulator state variable, [841](#)
- library, definition, [46](#)
- LibrarySearchPath .ini file variable, [888](#)
- libsm, [1019](#)
- libswift, [1019](#)
 - entry not found error, [943](#)
- License .ini file variable, [888](#)
- licensing
 - License variable in .ini file, [888](#)
- limit toggle coverage, [654](#)
- Limiting WLF file, [532](#)
- link cursors, [178](#), [552](#)
- linking SystemC source, [363](#)
- List pane
 - see also* pane, List pane
- List window, [116](#), [546](#)
 - expanded time viewing, [562](#)
 - setting triggers, [593](#)
 - waveform comparison, [611](#)
 - see also* windows, List window
- LM_LICENSE_FILE environment variable, [1006](#)
- Load
 - breakpoints, [150](#)
- loading the design, overview, [48](#)
- local variables
 - modifying with change command, [326](#)
- Locals window, [120](#)
 - see also* windows, Locals window
- location maps, referencing source files, [933](#)
- locations maps
 - specifying source files with, [933](#)
- lock message, [941](#)
- locking cursors, [550](#)
- log file
 - overview, [529](#)
 - see also* WLF files
- Logic Modeling
 - SmartModel
 - command channel, [1024](#)
 - SmartModel Windows
 - lmcwin commands, [1025](#)
 - memory arrays, [1026](#)
- long simulations
 - saving at intervals, [537](#)
- LSF
 - JobSpy integration, [787](#)
- M —
- MacroNestingLevel simulator state variable, [841](#)
- macros (DO files), [848](#)
 - creating from a saved transcript, [163](#)
 - depth of nesting, simulator state variable, [841](#)
 - error handling, [852](#)
 - parameters
 - as a simulator state variable (n), [841](#)
 - passing, [849](#)
 - total number passed, [841](#)
 - startup macros, [930](#)
- Main window, [66](#)
 - see also* windows, Main window
- malloc()
 - checkpointing foreign C code, [481](#)
- mapping
 - data types, [416](#)
 - libraries
 - from the command line, [245](#)
 - hierarchically, [929](#)
 - symbols
 - Dataflow window, [626](#)
 - SystemC in mixed designs, [436](#)
 - SystemC to Verilog, [431](#)
 - SystemC to VHDL, [437](#)
 - Verilog states in mixed designs, [419](#)
 - Verilog states in SystemC designs, [430](#)
 - Verilog to SytemC, port and data types, [430](#)
 - Verilog to VHDL data types, [416](#)
 - VHDL to SystemC, [422](#)
 - VHDL to Verilog data types, [420](#)
- mapping libraries, library mapping, [245](#)
- mapping signals, waveform editor, [798](#)
- math_complex package, [248](#)
- math_real package, [248](#)
- MaxReportRhsCrossProducts .ini file variable, [889](#)
- mc_scan_plusargs()
 - using with an elaboration file, [485](#)
- memories

- displaying the contents of, [122](#)
- navigation, [125](#)
- selecting memory instances, [125](#)
- sparse memory modeling, [340](#)
- viewing contents, [125](#)
- memory
 - capacity analysis, [747](#)
 - modeling in VHDL, [274](#)
- memory allocation
 - checkpointing foreign C code, [481](#)
- memory allocation profiler, [734](#)
- memory leak, cancelling scheduled events, [284](#)
- memory leaks and transaction handles, [509](#)
- memory tab
 - memories you can view, [123](#)
- Memory window, [122](#)
- merge
 - test-associated, [706](#)
- merging
 - results from multiple simulation runs, [668](#)
- message system, [935](#)
- Message Viewer Display Options dialog box, [169](#)
- Message Viewer tab, [165](#)
- MessageFormat .ini file variable, [889](#)
- MessageFormatBreak .ini file variable, [890](#)
- MessageFormatBreakLine .ini file variable, [890](#)
- MessageFormatError .ini file variable, [890](#)
- MessageFormatFail .ini file variable, [891](#)
- MessageFormatFatal .ini file variable, [891](#)
- MessageFormatNote .ini file variable, [891](#)
- MessageFormatWarning .ini file variable, [892](#)
- Messages, [165](#)
- messages, [935](#)
 - bad magic number, [531](#)
 - empty port name warning, [940](#)
 - exit codes, [938](#)
 - getting more information, [936](#)
 - lock message, [941](#)
 - long description, [936](#)
 - metavalue detected, [941](#)
 - redirecting, [917](#)
 - sensitivity list warning, [941](#)
 - suppressing warnings from arithmetic packages, [931](#)
 - Tcl_init error, [941](#)
 - too few port connections, [942](#)
 - turning off assertion messages, [930](#)
 - VSIM license lost, [943](#)
 - warning, suppressing, [936](#)
- metavalue detected warning, [941](#)
- MFCU, [294](#)
- MGC_LOCATION_MAP env variable, [933](#)
- MGC_LOCATION_MAP variable, [1006](#)
- MinGW gcc, [962](#), [966](#)
- mismatching coverage numbers, [140](#)
- missed coverage
 - branches, [127](#)
- Missed Coverage pane, [126](#)
- missing DPI import function, [956](#)
- Mixed-language
 - hierarchical references, [402](#)
- mixed-language simulation, [401](#)
 - access limitations, [403](#)
- mode, setting default coverage, [672](#)
- MODEL_Tech environment variable, [1006](#)
- MODEL_Tech_Tcl environment variable, [1007](#)
- modeling memory in VHDL, [274](#)
- MODELSIM environment variable, [1007](#)
- modelsim.ini
 - found by the tool, [1002](#)
 - default to VHDL93, [931](#)
 - delay file opening with, [932](#)
 - editing,, [860](#)
 - environment variables in, [929](#)
 - force command default, setting, [931](#)
 - hierarchical library mapping, [929](#)
 - opening VHDL files, [932](#)
 - restart command defaults, setting, [931](#)
 - transcript file created from, [930](#)
 - turning off arithmetic package warnings, [931](#)
 - turning off assertion messages, [930](#)
- modelsim.tcl, [998](#)
- modelsim_lib, [271](#)
- modelsim_lib .ini file variable, [892](#)

MODELSIM_PREFERENCES variable, 998, 1007

modes of operation, 50

Modified field, Project tab, 233

modify

- breakpoints, 148, 596, 599

modifying local variables, 326

modules

- handling multiple, common names, 293
- with unnamed ports, 440

Monitor window

- grouping/ungrouping objects, 173

mouse shortcuts

- Main window, 986
- Source window, 986
- Wave window, 989

.mpf file, 223

- loading from the command line, 240
- order of access during startup, 1001

msgmode .ini file variable, 892

msgmode variable, 165

mti_cosim_trace environment variable, 1007

mti_inhibit_inline attribute, 255

MTI_SYSTEMC macro, 350

MTI_TF_LIMIT environment variable, 1008

MTI_VCO_MODE environment variable, 1008

MTI_VOPT_FLOW, 1008

multi file compilation unit (MFCU), 294

multi-file compilation issues, SystemVerilog, 293

MultiFileCompilationUnit .ini file variable, 893

Multiple simulations, 529

— N —

n simulator state variable, 841

Name field

- Project tab, 232

name visibility in Verilog generates, 299

names, modules with the same, 293

naming optimized designs, 210

Negative timing

- algorithm for calculating delays, 313
- check limits, 313
- constraint algorithm, 316

- constraints, 314
- delay solution convergence, 316
- syntax for \$recrem, 315
- syntax for \$setuphold, 313
- using delayed inputs for checks, 321

Negative timing checks, 313

nets

- Dataflow window, displaying in, 109, 615
- values of
 - displaying in Objects window, 127
 - saving as binary log file, 529
- waveforms, viewing, 174

new function

- initialize SV object handle, 311

Nlview widget Symlib format, 627

NoAutoSDFCompile .ini file variable, 893

NoCaseStaticError .ini file variable, 893

NOCHANGE

- matching to Verilog, 810

NoDebug .ini file variable, 894

NoIndexCheck .ini file variable, 894

NOMMAP environment variable, 1008

non-blocking assignments, 308

NoOthersStaticError .ini file variable, 894

NoRangeCheck .ini file variable, 895

note .ini file variable, 895

Notepad windows, text editing, 986

- notrigger argument, 594

NoVital .ini file variable, 895

NoVitalCheck .ini file variable, 896

Now simulator state variable, 841

now simulator state variable, 842

null value

- debugging, 311

numeric_bit package, 248

numeric_std package, 248

- disabling warning messages, 931

NumericStdNoWarnings .ini file variable, 896

— O —

object

- defined, 52

Object handle

- initialize with new function, 311

objects

- virtual, 539

Objects window, [127](#)
 objects, viewable SystemC, [368](#)
 observe function, SystemC, [413](#)
 observe_foreign_signal() function, [403](#)
 OnFinish .ini file variable, [897](#)
 OnFinishPendingAssert .ini file variable, [897](#)
 operating systems supported, *See Installation Guide*
 Optimization Configurations, [235](#)
 optimizations
 design object visibility, [219](#)
 event order issues, [222](#)
 timing checks, [222](#)
 Verilog designs, [209](#)
 VHDL subprogram inlining, [255](#)
 Optimize_1164 .ini file variable, [898](#)
 optimized designs
 naming, [210](#)
 optimized designs, unnamed, [212](#)
 order of events
 in optimized designs, [222](#)
 ordering files for compile, [228](#)
 organizing projects with folders, [235](#)
 OSCI simulator, differences with vsim, [389](#)
 Others clause
 libraries, [246](#)
 overview, simulation tasks, [44](#)

— P —

packages
 standard, [248](#)
 textio, [248](#)
 util, [271](#)
 VITAL 1995, [269](#)
 VITAL 2000, [269](#)
 page setup
 Dataflow window, [631](#)
 Wave window, [586](#)
 pan, Dataflow window, [632](#)
 parallel transaction
 definition of, [489](#)
 parameter support
 SC instantiating Verilog, [450](#)
 SystemC instantiating Verilog, [450](#)
 Verilog instantiating SC, [456](#)
 Verilog instantiating SystemC, [456](#)

parameters
 making optional, [850](#)
 passing from Verilog to SC, [456](#)
 passing to sc_foreign_module (Verilog), [451](#)
 using with macros, [849](#)
 parameters (Verilog to SC)
 passing as constructor arguments, [451](#)
 passing integer as template arguments, [452](#)
 path delay mode, [325](#)
 path delays, matching to DEVICE statements, [808](#)
 path delays, matching to
 GLOBALPATHPULSE statements, [808](#)
 path delays, matching to IOPATH statements, [807](#)
 path delays, matching to PATHPULSE statements, [808](#)
 pathnames
 comparisons, [608](#)
 hiding in Wave window, [572](#)
 PATHPULSE
 matching to specify path delays, [808](#)
 PathSeparator .ini file variable, [898](#)
 PedanticErrors .ini file variable, [898](#)
 performance
 cancelling scheduled events, [284](#)
 improving for Verilog simulations, [209](#)
 PERIOD
 matching to Verilog, [810](#)
 phase transaction
 definition of, [489](#)
 platforms
 choosing 32- versus 64-bit, [1008](#)
 platforms supported, *See Installation Guide*
 PLI
 design object visibility and auto +acc, [219](#)
 loading shared objects with global symbol visibility, [970](#)
 specifying which apps to load, [950](#)
 Veriuser entry, [950](#)
 PLI/VPI, [342](#)
 debugging, [717](#)
 tracing, [980](#)

- PLI/VPI/DPI, [947](#)
 - registering DPIapplications, [952](#)
 - specifying the DPI file to load, [970](#)
- PliCompatDefault .ini file variable, [899](#)
- PLIOBJS environment variable, [950](#), [1009](#)
- plusargs
 - changing behavior of, [870](#)
- PORT
 - matching to input ports, [807](#)
- port collapsing, toggle coverage, [671](#)
- Port driver data, capturing, [827](#)
- ports, unnamed, in mixed designs, [440](#)
- ports, VHDL and Verilog, [418](#)
- Postscript
 - saving a waveform in, [585](#)
 - saving the Dataflow display in, [629](#)
- post-sim debug flow, [616](#)
- pragmas, [657](#)
 - protecting IP code, [183](#)
- precision
 - in timescale directive, [303](#)
 - simulator resolution, [303](#)
- precision, simulator resolution, [412](#)
- PrefCoverage(DefaultCoverageMode), [672](#)
- PrefCoverage(pref_InitFilterFrom), [662](#)
- preference variables
 - .ini files, located in, [865](#)
 - editing, [995](#)
 - saving, [995](#)
- preferences
 - saving, [995](#)
 - Wave window display, [571](#)
- PrefMemory(ExpandPackedMem) variable, [125](#)
- primitives, symbols in Dataflow window, [626](#)
- printing
 - Dataflow window display, [629](#)
 - waveforms in the Wave window, [585](#)
- printing simulation stats, [900](#)
- PrintSimStats .ini file variable, [900](#)
- PrintSVPackageLoadingAttribute .ini file variable, [900](#)
- profile report command, [745](#)
- Profiler, [733](#)
 - %parent fields, [739](#)
 - clear profile data, [736](#)
 - enabling memory profiling, [734](#)
 - enabling statistical sampling, [736](#)
 - getting started, [734](#)
 - handling large files, [735](#)
 - Hierarchical View, [739](#)
 - interpreting data, [737](#)
 - memory allocation, [734](#)
 - memory allocation profiling, [736](#)
 - profile report command, [745](#)
 - Profile Report dialog, [746](#)
 - Ranked View, [738](#)
 - report option, [745](#)
 - results, viewing, [737](#)
 - statistical sampling, [734](#)
 - Structural View, [740](#)
 - viewing profile details, [741](#)
- Programming Language Interface, [342](#), [947](#)
- project tab
 - sorting, [233](#)
- project window
 - information in, [232](#)
- projects, [223](#)
 - accessing from the command line, [240](#)
 - adding files to, [226](#)
 - benefits, [223](#)
 - close, [232](#)
 - compile order, [228](#)
 - changing, [228](#)
 - compiler properties in, [237](#)
 - compiling files, [227](#)
 - creating, [225](#)
 - creating simulation configurations, [233](#)
 - folders in, [235](#)
 - grouping files in, [229](#)
 - loading a design, [230](#)
 - MODELSIM environment variable, [1007](#)
 - open and existing, [232](#)
 - overview, [223](#)
- protect
 - source code, [183](#)
- Protect .ini file variable, [901](#)
- 'protect compiler directive, [189](#), [337](#)
- protect pragmas
 - encrypting IP code, [183](#)

- protected types, [276](#)
- Public encryption key, [205](#)
- Public encryption keys, [205](#)
- Q —
- quick reference
 - table of simulation tasks, [44](#)
- Quiet .ini file variable, [901](#)
- qverilog command
 - DPI support, [956](#)
- R —
- race condition, problems with event order, [306](#)
- Radix
 - change in Watch pane, [171](#)
 - color
 - example, [65](#)
- radix
 - List window, [582](#)
 - SystemVerilog types, [175](#), [575](#)
 - user-defined, [63](#)
 - definition body, [64](#)
 - Wave window, [574](#)
- Radix define command
 - setting radix color, [65](#)
- range checking, [255](#)
- Raw encryption, [201](#)
- readers and drivers, [618](#)
- real type, converting to time, [274](#)
- rebuilding supplied libraries, [248](#)
- Recall breakpoints, [599](#)
- reconstruct RTL-level design busses, [540](#)
- Recording
 - expanded time, [555](#)
- RECOVERY
 - matching to Verilog, [809](#)
- RECREM
 - matching to Verilog, [809](#)
- redirecting messages, TranscriptFile, [917](#)
- reference region, [604](#)
- refreshing library images, [249](#)
- regions
 - virtual, [542](#)
- registered function calls, [723](#)
- registers
 - values of
 - displaying in Objects window, [127](#)
 - saving as binary log file, [529](#)
 - waveforms, viewing, [174](#)
- regular-expression, [63](#)
- REMOVAL
 - matching to Verilog, [809](#)
- reporting
 - code coverage, [669](#)
- reports
 - fsm recognition, [688](#), [689](#)
- RequireConfigForAllDefaultBinding .ini file variable, [901](#)
- resolution
 - in SystemC simulation, [364](#)
 - mixed designs, [412](#)
 - returning as a real, [271](#)
 - verilog simulation, [303](#)
 - VHDL simulation, [260](#)
- Resolution .ini file variable, [902](#)
- resolution simulator state variable, [842](#)
- resource libraries
 - specifying, [247](#)
- restart command
 - defaults, [931](#)
- Restore
 - breakpoints, [599](#)
- Restoring
 - window format, [66](#), [585](#)
- results, saving simulations, [529](#)
- return to VSIM prompt on sc_stop or \$finish, [897](#)
- RTL-level design busses
 - reconstructing, [540](#)
- RunLength .ini file variable, [902](#)
- Runtime Options Dialog, [860](#)
- S —
- Save
 - breakpoints, [150](#)
- saveLines preference variable, [163](#)
- Saving
 - window format, [66](#), [585](#)
- saving
 - simulation options in a project, [233](#)
 - waveforms, [529](#)
- sc_argc() function, [392](#)

- sc_argv() function, 392
- sc_clock() functions, moving, 383
- sc_cycle() function, 390
- sc_fifo, 375
- sc_fix and sc_ufix, 393
- sc_fixed and sc_ufixed, 393
- sc_foreign_module, 459
- sc_foreign_module (Verilog)
 - and parameters, 451
- sc_foreign_module (VHDL)
 - and generics, 460
- sc_main(), 383
- sc_main() function, 347
- sc_main() function, converting, 383
- SC_MODULE_EXPORT macro, 349
- sc_signal() functions, moving, 383
- sc_signed and sc_unsigned, 393
- sc_start() function, 390
- sc_start() function, replacing in SystemC, 389
- sc_start(), replacing, 383
- sc_stop()
 - behavior of, 393
 - behavior, customizing, 897
- ScalarOpts .ini file variable, 903
- scaling fonts, 59
- sccom
 - using sccom vs. raw C++ compiler, 351
- sccom -link command, 363, 467
- SccomLogfile .ini file variable, 903
- SccomVerbose .ini file variable, 903
- scgenmod, using, 449, 459
- ScMainFinishOnQuit .ini file variable, 904
- ScMainStackSize .ini file variable, 904
- ScTimeUnit .ini file variable, 905
- ScvPhaseRelationName .ini variable, 904, 905
- SDF
 - compiled SDF, 803
 - disabling timing checks, 813
 - errors and warnings, 803
 - instance specification, 802
 - interconnect delays, 812
 - mixed VHDL and Verilog designs, 812
 - specification with the GUI, 802
 - troubleshooting, 814
 - Verilog
 - \$sdf_annotate system task, 806
 - optional conditions, 811
 - optional edge specifications, 810
 - rounded timing values, 812
 - SDF to Verilog construct matching, 807
 - VHDL
 - resolving errors, 805
 - SDF to VHDL generic matching, 804
- SDF annotate
 - \$sdf_annotate system task, 805
- SDF annotation
 - matching single timing check, 814
- SDF DEVICE
 - matching to Verilog constructs, 808
- SDF GLOBALPATHPULSE
 - matching to Verilog constructs, 808
- SDF HOLD
 - matching to Verilog constructs, 808
- SDF INTERCONNECT
 - matching to Verilog constructs, 807
- SDF IOPATH
 - matching to Verilog constructs, 807
- SDF NOCHANGE
 - matching to Verilog constructs, 810
- SDF PATHPULSE
 - matching to Verilog constructs, 808
- SDF PERIOD
 - matching to Verilog constructs, 810
- SDF PORT
 - matching to Verilog constructs, 807
- SDF RECOVERY
 - matching to Verilog constructs, 809
- SDF RECREM
 - matching to Verilog constructs, 809
- SDF REMOVAL
 - matching to Verilog constructs, 809
- SDF SETUPHOLD
 - matching to Verilog constructs, 809
- SDF SKEW
 - matching to Verilog constructs, 809
- SDF WIDTH
 - matching to Verilog constructs, 810
- \$sdf_done, 333
- Search
 - stop, 566

- search
 - inline search bar
 - Source window, [151](#)
 - Transcript, [164](#)
- Search bar, [60](#)
- searching
 - Expression Builder, [568](#)
 - Verilog libraries, [292](#), [442](#)
- sensitivity list warning, [941](#)
- SETUP
 - matching to Verilog, [808](#)
- SETUPHOLD
 - matching to Verilog, [809](#)
- severity, changing level for errors, [936](#)
- SFCU, [294](#)
- Share
 - user-defined types, [443](#)
- shared library
 - building in SystemC, [363](#)
- shared objects
 - loading FLI applications
 - see FLI Reference manual
 - loading PLI/VPI/DPI C applications, [960](#)
 - loading PLI/VPI/DPI C++ applications, [965](#)
 - loading with global symbol visibility, [970](#)
- Shortcuts
 - text editing, [986](#)
- shortcuts
 - command history, [985](#)
 - command line caveat, [985](#)
 - List window, [989](#)
 - Main window, [986](#)
 - Source window, [986](#)
 - Wave window, [989](#)
- show drivers
 - Dataflow window, [619](#)
 - Wave window, [595](#)
- Show_BadOptionWarning .ini file variable, [905](#)
- Show_Lint .ini file variable, [906](#)
- Show_source .ini file variable, [906](#)
- Show_VitalChecksWarning .ini file variable, [906](#)
- Show_Warning1 .ini file variable, [907](#)
- Show_Warning2 .ini file variable, [907](#)
- Show_Warning3 .ini file variable, [907](#)
- Show_Warning4 .ini file variable, [907](#)
- Show_Warning5 .ini file variable, [908](#)
- ShowConstantImmediateAsserts .ini file variable, [908](#)
- ShowFunctions .ini file variable, [908](#)
- ShowUnassociatedScNameWarning .ini file variable, [909](#)
- ShowUndebuggableScTypeWarning .ini file variable, [909](#)
- ShutdownFile .ini file variable, [909](#)
- Signal
 - create virtual, [590](#)
- signal breakpoints
 - edit, [596](#)
- signal groups
 - in wave window, [578](#)
- signal interaction
 - Verilog and SystemC, [422](#)
- Signal Segmentation Violations
 - debugging, [311](#)
- Signal Spy, [272](#), [767](#)
 - disable, [759](#)
 - enable, [761](#)
- \$signal_force, [771](#)
- signal_force, [272](#), [771](#)
- \$signal_release, [775](#)
- signal_release, [273](#), [775](#)
- signals
 - combining into a user-defined bus, [589](#)
 - dashed, [176](#)
 - Dataflow window, displaying in, [109](#), [615](#)
 - driving in the hierarchy, [763](#)
 - filtering in the Objects window, [128](#)
 - hierarchy
 - driving in, [763](#)
 - referencing in, [272](#), [767](#)
 - releasing anywhere in, [775](#)
 - releasing in, [273](#), [775](#)
 - sampling at a clock change, [594](#)
 - transitions, searching for, [564](#)
 - types, selecting which to view, [128](#)
 - values of
 - displaying in Objects window, [127](#)

- forcing anywhere in the hierarchy, [272](#), [771](#)
 - saving as binary log file, [529](#)
 - virtual, [540](#)
 - waveforms, viewing, [174](#)
- SignalSpyPathSeparator .ini file variable, [910](#)
- SIGSEGV
 - fatal error message, [312](#)
- SIGSEGV error, [311](#)
- simulating
 - batch mode, [50](#)
 - command-line mode, [50](#)
 - comparing simulations, [529](#)
 - default run length, [862](#)
 - iteration limit, [862](#)
 - mixed language designs
 - compilers, [402](#)
 - libraries, [402](#)
 - resolution limit in, [412](#)
 - mixed Verilog and SystemC designs
 - channel and port type mapping, [423](#)
 - Verilog port direction, [429](#)
 - Verilog state mapping, [430](#)
 - mixed Verilog and VHDL designs
 - Verilog parameters, [418](#)
 - Verilog state mapping, [419](#)
 - VHDL and Verilog ports, [418](#)
 - VHDL generics, [421](#)
 - mixed VHDL and SystemC designs
 - SystemC state mapping, [436](#)
 - VHDL port direction, [436](#)
 - VHDL port type mapping, [432](#)
 - VHDL sc_signal data type mapping, [433](#)
- saving dataflow display as a Postscript file, [629](#)
- saving options in a project, [233](#)
- saving simulations, [529](#)
- saving waveform as a Postscript file, [585](#)
- SystemC, [345](#), [363](#)
 - usage flow for SystemC only, [347](#)
- Verilog, [302](#)
 - delay modes, [324](#)
 - hazard detection, [310](#)
 - optimizing performance, [209](#)
 - resolution limit, [303](#)
 - XL compatible simulator options, [322](#)
- VHDL, [256](#)
- viewing results in List pane, [116](#)
- viewing results in List window, [546](#)
- VITAL packages, [270](#)
- simulating the design, overview, [49](#)
- simulation
 - basic steps for, [46](#)
- Simulation Configuration
 - creating, [233](#)
- simulation task overview, [44](#)
- simulations
 - event order in, [306](#)
 - saving results, [529](#)
 - saving results at intervals, [537](#)
- simulator resolution
 - mixed designs, [412](#)
 - returning as a real, [271](#)
 - SystemC, [364](#)
 - Verilog, [303](#)
 - VHDL, [260](#)
- simulator state variables, [841](#)
- simulator, difference from OSCI, [389](#)
- single file compilation unit (SFCU), [294](#)
- sizetf callback function, [974](#)
- SKEW
 - matching to Verilog, [809](#)
- sm_entity, [1020](#)
- SmartModels
 - creating foreign architectures with
 - sm_entity, [1020](#)
 - invoking SmartModel specific commands, [1024](#)
 - linking to, [1019](#)
 - lmcwin commands, [1025](#)
 - memory arrays, [1026](#)
 - Verilog interface, [1027](#)
 - VHDL interface, [1019](#)
- so, shared object file
 - loading PLI/VPI/DPI C applications, [960](#)
 - loading PLI/VPI/DPI C++ applications, [965](#)
- Source
 - textual dataflow, [143](#)

- Source annotation
 - Annotation, 141
- source annotation, 141
- source code mismatches
 - bypassing warning, 703
- source code pragmas, 657, 666
- source code, security, 189, 199, 337
- source files
 - Debug, 141
- source files, referencing with location maps, 933
- source files, specifying with location maps, 933
- source highlighting, customizing, 151
- source libraries
 - arguments supporting, 295
- Source window, 132
 - clear highlights, 137
 - code coverage data, 138
 - colorization, 151
 - inline search bar, 151
 - tab stops in, 151
 - see also* windows, Source window
- source-level debug
 - SystemC, enabling, 369
- sparse memory modeling, 340
- SparseMemThreshold .ini file variable, 910
- specify path delays
 - matching to DEVICE construct, 808
 - matching to GLOBALPATHPULSE construct, 808
 - matching to IOPATH statements, 807
 - matching to PATHPULSE construct, 808
- Standard Developer's Kit User Manual, 54
- standards supported, 52
- start_of_simulation() function, 392
- Startup
 - macro in the modelsim.ini file, 910
- startup
 - files accessed during, 1001
 - macros, 930
 - startup macro in command-line mode, 50
 - using a startup file, 930
- Startup .ini file variable, 910
- State machines
 - view current state, 685
- state variables, 841
- statistical sampling profiler, 734
- status bar
 - Main window, 71
- Status field
 - Project tab, 232
- std .ini file variable, 911
- std_arith package
 - disabling warning messages, 931
- std_developerskit .ini file variable, 911
- std_logic_arith package, 248
- std_logic_signed package, 248
- std_logic_textio, 248
- std_logic_unsigned package, 248
- StdArithNoWarnings .ini file variable, 911
- STDOUT environment variable, 1009
- steps for simulation, overview, 46
- stimulus
 - modifying for elaboration file, 484
- Stop wave drawing, 566
- struct of sc_signal<T>, 374
- structure, 474
- subprogram inlining, 255
- subprogram write is ambiguous error, fixing, 265
- substreams
 - definition of, 489
- suppress .ini file variable, 912
- suspended thread, 722
- sv_std .ini file variable, 912
- SVFileExtensions .ini file variable, 912
- Svlog .ini file variable, 913
- symbol mapping
 - Dataflow window, 626
- symbolic link to design libraries (UNIX), 246
- Symmetric encryption
 - Encryption
 - symmetric, 200
- Synopsis hardware modeler, 1013
- synopsys .ini file variable, 913
- Synopsys libraries, 248
- syntax highlighting, 151
- synthesis
 - rule compliance checking, 871, 872
- system calls

- VCD, [822](#)
 - Verilog, [325](#)
 - system commands, [840](#)
 - system tasks
 - proprietary, [329](#)
 - VCD, [822](#)
 - Verilog, [325](#)
 - Verilog-XL compatible, [333](#)
 - SystemC
 - aggregates of signals/ports, [374](#)
 - calling member import functions in SC scope, [471](#)
 - cin support, [391](#)
 - compiling for source level debug, [350](#)
 - compiling optimized code, [349](#)
 - component declaration for instantiation, [466](#)
 - construction parameters, [393](#)
 - constructor/destructor breakpoints, [371](#)
 - control function, [413](#)
 - converting sc_main(), [383](#)
 - converting sc_main() to a module, [383](#)
 - debugging of channels and variables, [378](#)
 - declaring/calling member import functions in SV, [470](#)
 - dynamic module array, [375](#)
 - exporting sc_main, example, [384](#)
 - exporting top level module, [349](#)
 - fixed-point types, [393](#)
 - foreign module declaration, [449](#)
 - generic support, instantiating VHDL, [460](#)
 - hierarchical references in mixed designs, [413](#)
 - instantiation criteria in Verilog design, [455](#)
 - instantiation criteria in VHDL design, [465](#)
 - linking the compiled source, [363](#)
 - maintaining design portability, [350](#)
 - mapping states in mixed designs, [436](#)
 - VHDL, [437](#)
 - memories, viewing, [376](#)
 - mixed designs with Verilog, [401](#)
 - mixed designs with VHDL, [401](#)
 - observe function, [413](#)
 - parameter support, Verilog instances, [450](#)
 - prim channel aggregates, [374](#)
 - reducing non-debug compile time, [350](#)
 - replacing sc_start(), [383](#)
 - sc_clock(), moving to SC_CTOR, [383](#)
 - sc_fifo, [375](#)
 - sc_signal(), moving to SC_CTOR, [383](#)
 - signals, viewing global and static, [374](#)
 - simulating, [363](#)
 - source code, modifying for vsim, [383](#)
 - stack space for threads, [395](#)
 - state-based code, initializing and cleanup, [366](#)
 - troubleshooting, [395](#)
 - unsupported functions, [390](#)
 - user defined signals and ports, viewable, [368](#)
 - viewable objects, [368](#)
 - viewable types, [367](#)
 - viewable/debuggable objects, [368](#)
 - viewing FIFOs, [375](#)
 - virtual functions, [366](#)
 - SystemC binding
 - to Verilog/SV design unit, [348](#), [403](#)
 - SystemC modules
 - exporting for use in Verilog, [455](#)
 - exporting for use in VHDL, [466](#)
 - SystemVerilog
 - hierarchical references, [413](#)
 - keyword considerations, [288](#)
 - multi-file compilation, [293](#)
 - object handle
 - initialize with new function, [311](#)
 - supported implementation details, [53](#)
 - SystemVerilog bind
 - limitations for SystemC, [348](#), [412](#)
 - SystemVerilog classes
 - view in Wave window, [586](#)
 - SystemVerilog DPI
 - specifying the DPI file to load, [970](#)
 - SystemVerilog types
 - radix, [175](#), [575](#)
- T —
- tab stops
 - Source window, [151](#)
 - Tcl, ?? to [846](#)
 - command separator, [839](#)

- command substitution, 838
- command syntax, 834
- evaluation order, 839
- history shortcuts, 985
- preference variables, 995
- relational expression evaluation, 839
- time commands, 844
- variable
 - substitution, 840
 - VSIM Tcl commands, 844
 - with escaped identifiers, 323
- Tcl_init error message, 941
- temp files, VSOUT, 1011
- template arguments
 - passing integer parameters as, 452
- terminology
 - for expanded time, 554
- test-associated merge, 706
- testbench, accessing internal objects from, 757
- Text
 - filtering, 62
- text and command syntax, 53
- Text editing, 986
- TEXTIO
 - buffer, flushing, 268
- TextIO package
 - alternative I/O files, 267
 - containing hexadecimal numbers, 266
 - dangling pointers, 267
 - ENDFILE function, 267
 - ENDLINE function, 267
 - file declaration, 264
 - implementation issues, 265
 - providing stimulus, 268
 - standard input, 265
 - standard output, 265
 - WRITE procedure, 265
 - WRITE_STRING procedure, 266
- textual dataflow
 - in the Source window, 143
- TF routines, 979
- TFMPC
 - explanation, 942
- thread
 - debugging, 722
- time
 - measuring in Wave window, 548
 - resolution in SystemC, 364
 - time resolution as a simulator state variable, 842
- time collapsing, 538
- Time mode switching
 - expanded time, 561
- time resolution
 - in mixed designs, 412
 - in Verilog, 303
 - in VHDL, 260
- time type
 - converting to real, 273
- time unit
 - in SystemC, 364
- timeline
 - display clock cycles, 572
- timescale directive warning
 - investigating, 303
- timing
 - differences shown by comparison, 609
 - disabling checks, 813
 - in optimized designs, 222
- Timing checks
 - delay solution convergence, 316
 - negative
 - constraint algorithm, 316
 - constraints, 314
 - syntax for \$recrem, 315
 - syntax for \$setuphold, 313
 - using delayed inputs for checks, 321
 - negative check limits, 313
- TMPDIR environment variable, 1009
- to_real VHDL function, 273
- to_time VHDL function, 274
- toggle coverage, 651
 - 3-state, 651
 - count limit, 913
 - excluding bus bits, 664
 - excluding enum signals, 665
 - limiting, 654
 - max VHDL integer values, 914
 - port collapsing, 671
 - reporting, duplication of elements, 671

- reporting, ordering of nodes, [671](#)
 - Verilog/SV supported data types, [652](#)
 - viewing in Signals window, [651](#)
 - ToggleCountLimit .ini file variable, [913](#)
 - ToggleFixedSizeArray .ini file variable, [914](#)
 - ToggleMaxFixedSizeArray .ini file variable, [914](#)
 - ToggleMaxIntValues .ini file variable, [914](#)
 - ToggleMaxRealValues .ini file variable, [915](#)
 - ToggleNoIntegers .ini file variable, [915](#)
 - TogglePackedAsVec .ini file variable, [916](#)
 - ToggleVlogEnumBits .ini file variable, [916](#)
 - ToggleVlogIntegers .ini file variable, [916](#)
 - ToggleVlogReal .ini file variable, [917](#)
 - ToggleWidthLimit .ini file variable, [917](#)
 - tolerance
 - leading edge, [606](#)
 - trailing edge, [606](#)
 - too few port connections, explanation, [942](#)
 - tool structure, [43](#)
 - Toolbar
 - filter, [62](#)
 - toolbar
 - Main window, [74](#)
 - tracing
 - events, [621](#)
 - source of unknown, [622](#)
 - transaction
 - definition of, [488](#)
 - transaction handles and memory leaks, [509](#)
 - transactions
 - CLI commands for debugging, [521](#)
 - parallel, [489](#)
 - phase, [489](#)
 - Transcript
 - inline search bar, [164](#)
 - transcript
 - disable file creation, [164](#), [930](#)
 - file name, specified in modelsim.ini, [930](#)
 - saving, [163](#)
 - using as a DO file, [163](#)
 - Transcript window
 - changing buffer size, [163](#)
 - changing line count, [163](#)
 - TranscriptFile .ini file variable, [917](#)
 - triggers, in the List window, [593](#)
 - triggers, in the List window, setting, [591](#)
 - troubleshooting
 - DPI, missing import funtion, [956](#)
 - SystemC, [395](#)
 - unexplained behaviors, SystemC, [395](#)
 - TSSSI
 - in VCD files, [827](#)
 - type
 - converting real to time, [274](#)
 - converting time to real, [273](#)
 - Type field, Project tab, [232](#)
 - Types
 - sharing user-defined, [443](#)
 - types
 - virtual, [542](#)
 - types, fixed-point in SystemC, [390](#)
 - types, viewable SystemC, [367](#)
- U —
- UCDB, [695](#)
 - automatic saving of, [698](#)
 - UCDBFilename .ini file variable, [918](#)
 - UDP, [287](#), [289](#), [292](#), [293](#), [300](#), [302](#), [324](#)
 - UnbufferedOutput .ini file variable, [918](#)
 - undefined symbol, error, [396](#)
 - unexplained behavior during simulation, [395](#)
 - unexplained simulation behavior, [395](#)
 - ungrouping
 - in wave window, [580](#)
 - ungrouping objects, Monitor window, [173](#)
 - unit delay mode, [325](#)
 - unknowns, tracing, [622](#)
 - unnamed designs, [212](#)
 - unnamed ports, in mixed designs, [440](#)
 - unsupported functions in SystemC, [390](#)
 - UpCase .ini file variable, [918](#)
 - usage models
 - encrypting IP code, [183](#)
 - vencrypt utility, [183](#)
 - use clause, specifying a library, [248](#)
 - use flow
 - Code Coverage, [636](#)
 - DPI, [953](#)
 - SystemC-only designs, [347](#)
 - user-defined bus, [539](#), [589](#)

user-defined primitive (UDP), [287](#), [289](#), [292](#),
[293](#), [300](#), [302](#), [324](#)

user-defined radix, [63](#)
definition body, [64](#)

User-defined types
sharing, [443](#)

UserTimeUnit .ini file variable, [919](#)

UseScv .ini file variable, [919](#)

util package, [271](#)

— V —

values

of HDL items, [150](#)

variables

editing, [860](#)

environment, [1004](#)

expanding environment variables, [1004](#)

LM_LICENSE_FILE, [1006](#)

modelsim.ini, [865](#)

reading from the .ini file, [843](#)

setting environment variables, [1004](#)

simulator state variables

iteration number, [841](#)

name of entity or module as a variable,
[841](#)

resolution, [841](#)

simulation time, [841](#)

values of

displaying in Objects window, [127](#)

saving as binary log file, [529](#)

VCD files

capturing port driver data, [827](#)

case sensitivity, [818](#)

creating, [817](#)

dumpports tasks, [822](#)

exporting created waveforms, [797](#)

from VHDL source to VCD output, [824](#)

stimulus, using as, [819](#)

supported TSSI states, [827](#)

translate into WLF, [827](#)

VCD system tasks, [822](#)

vcd2wlf command, [827](#)

vencrypt command

header file, [185](#)

Verilog

ACC routines, [977](#)

capturing port driver data with -dumpports,
[827](#)

cell libraries, [324](#)

compiler directives, [336](#)

compiling and linking PLI C applications,
[960](#)

compiling and linking PLI C++
applications, [965](#)

compiling design units, [287](#)

compiling with XL 'uselib compiler
directive, [295](#)

component declaration, [439](#)

configuration support, [449](#)

configurations, [298](#)

DPI access routines, [979](#)

event order in simulation, [306](#)

extended system tasks, [335](#)

generate statements, [299](#)

instantiation criteria in mixed-language
design, [438](#)

instantiation criteria in SystemC design,
[448](#)

instantiation of VHDL design units, [441](#)

language templates, [144](#)

library usage, [292](#)

mapping states in mixed designs, [419](#)

mapping states in SystemC designs, [430](#)

mixed designs with SystemC, [401](#)

mixed designs with VHDL, [401](#)

parameter support, instantiating SystemC,
[456](#)

parameters, [418](#)

port direction, [429](#)

resource libraries, [247](#)

sdf_annotate system task, [805](#)

simulating, [302](#)

delay modes, [324](#)

XL compatible options, [322](#)

simulation hazard detection, [310](#)

simulation resolution limit, [303](#)

SmartModel interface, [1027](#)

source code viewing, [132](#)

standards, [52](#)

system tasks, [325](#)

TF routines, [979](#)

- to SystemC, channel and port type mapping, [423](#)
- XL compatible compiler options, [295](#)
- XL compatible routines, [980](#)
- XL compatible system tasks, [333](#)
- verilog .ini file variable, [919](#)
- Verilog 2001
 - disabling support, [921](#)
- Verilog PLI/VP/DPII
 - registering VPI applications, [951](#)
- Verilog PLI/VPI
 - 64-bit support in the PLI, [980](#)
 - debugging PLI/VPI code, [981](#)
- Verilog PLI/VPI/DPI
 - compiling and linking PLI/VPI C++ applications, [965](#)
 - compiling and linking PLI/VPI/CPI C applications, [960](#)
 - PLI callback reason argument, [973](#)
 - PLI support for VHDL objects, [976](#)
 - registering PLI applications, [949](#)
 - specifying the PLI/VPI file to load, [969](#)
- Verilog/SV supported data types
 - for toggle coverage, [652](#)
- Verilog-XL
 - compatibility with, [285](#)
- Veriuser .ini file variable, [920](#), [950](#)
- Veriuser, specifying PLI applications, [950](#)
- veriuser.c file, [975](#)
- VHDL
 - .ini compiler control variables
 - ShowConstantImmediateAsserts, [908](#)
 - compile, [254](#)
 - compiling design units, [253](#)
 - conditions and expressions, automatic conversion of H and L., [875](#)
 - constants, [443](#)
 - creating a design library, [253](#)
 - delay file opening, [932](#)
 - dependency checking, [254](#)
 - encryption, [192](#)
 - file opening delay, [932](#)
 - foreign language interface, [259](#)
 - hardware model interface, [1013](#)
 - instantiation criteria in SystemC design, [458](#)
 - instantiation from Verilog, [441](#)
 - instantiation of Verilog, [416](#)
 - language templates, [144](#)
 - language versions, [257](#)
 - library clause, [247](#)
 - mixed designs with SystemC, [401](#)
 - mixed designs with Verilog, [401](#)
 - object support in PLI, [976](#)
 - optimizations
 - inlining, [255](#)
 - port direction, [436](#)
 - port type mapping, [432](#)
 - resource libraries, [247](#)
 - sc_signal data type mapping, [433](#)
 - simulating, [256](#)
 - SmartModel interface, [1019](#)
 - source code viewing, [132](#)
 - standards, [52](#)
 - timing check disabling, [256](#)
 - VITAL package, [248](#)
- VHDL binding
 - to Verilog/SV design unit, [403](#)
- VHDL utilities, [271](#), [272](#), [767](#)
 - get_resolution(), [271](#)
 - to_real(), [273](#)
 - to_time(), [274](#)
- VHDL-1987, compilation problems, [257](#)
- VHDL-1993
 - enabling support for, [920](#)
- VHDL-2002
 - enabling support for, [920](#)
- VHDL93 .ini file variable, [920](#)
- viewing, [165](#)
 - library contents, [243](#)
 - waveforms, [529](#)
- viewing FIFOs, [375](#)
- virtual compare signal, restrictions, [589](#)
- virtual functions in SystemC, [366](#)
- virtual hide command, [540](#)
- virtual objects, [539](#)
 - virtual functions, [541](#)
 - virtual regions, [542](#)
 - virtual signals, [540](#)

- virtual types, [542](#)
- virtual region command, [542](#)
- virtual regions
 - reconstruct RTL hierarchy, [542](#)
- virtual save command, [541](#)
- Virtual signal
 - create, [590](#)
- virtual signal command, [540](#)
- virtual signals
 - reconstruct RTL-level design busses, [540](#)
 - reconstruct the original RTL hierarchy, [540](#)
 - virtual hide command, [540](#)
- visibility
 - column in structure tab, [535](#)
 - design object and +acc, [219](#)
 - design object and vopt, [209](#)
 - of declarations in \$unit, [293](#)
- VITAL
 - compiling and simulating with accelerated VITAL packages, [270](#)
 - compliance warnings, [270](#)
 - disabling optimizations for debugging, [270](#)
 - specification and source code, [268](#)
 - VITAL packages, [269](#)
- vital2000 .ini file variable, [920](#)
- vl_logic, [829](#)
- vlog command
 - +protect argument, [187](#), [189](#)
- vlog95compat .ini file variable, [921](#)
- Vopt
 - suppress warning messages, [937](#)
- vopt
 - and breakpoints, [211](#)
- vopt command, [209](#)
- VoptAutoSDFCompile .ini file variable, [921](#)
- VoptFlow .ini file variable, [921](#)
- VPI, registering applications, [951](#)
- VPI/PLI, [342](#)
- VPI/PLI/DPI, [947](#)
 - compiling and linking C applications, [960](#)
 - compiling and linking C++ applications, [965](#)
- VSIM license lost, [943](#)
- VSIM prompt, returning to, [897](#)
- vsim, differences with OSCI simulator, [389](#)

VSOUT temp file, [1011](#)

— W —

- WarnConstantChange .ini file variable, [922](#)
- warning #6820, [703](#)
- warning .ini file variable, [922](#)
- warnings
 - disabling at time 0, [931](#)
 - empty port name, [940](#)
 - exit codes, [938](#)
 - getting more information, [936](#)
 - messages, long description, [936](#)
 - metavalue detected, [941](#)
 - severity level, changing, [936](#)
 - suppressing VCOM warning messages, [936](#)
 - suppressing VLOG warning messages, [937](#)
 - suppressing VOPT warning messages, [937](#)
 - suppressing VSIM warning messages, [938](#)
 - Tcl initialization error 2, [941](#)
 - too few port connections, [942](#)
 - turning off warnings from arithmetic packages, [931](#)
 - waiting for lock, [941](#)
- Wave drawing
 - stop, [566](#)
- wave groups, [578](#)
 - add items to existing, [581](#)
 - creating, [579](#)
 - deleting, [580](#)
 - drag from Wave to List, [581](#)
 - drag from Wave to Transcript, [581](#)
 - removing items from existing, [581](#)
 - ungrouping, [580](#)
- Wave Log Format (WLF) file, [529](#)
- wave log format (WLF) file
 - see also* WLF files
- wave viewer, Dataflow window, [620](#)
- Wave window, [174](#), [544](#)
 - compare waveforms, [608](#)
 - cursor linking, [552](#)
 - customizing for expanded time, [559](#)
 - expanded time viewing, [554](#), [556](#)
 - in the Dataflow window, [620](#)
 - saving layout, [584](#)
 - timeline

- display clock cycles, [572](#)
 - values column, [610](#)
 - view SV class objects, [586](#)
 - see also* windows, Wave window
- wave window
 - dashed signal lines, [176](#)
- Waveform Compare
 - adding clocks, [605](#)
 - adding regions, [604](#)
 - adding signals, [604](#)
 - annotating differences, [610](#)
 - clocked comparison, [606](#)
 - compare by region, [604](#)
 - compare by signal, [604](#)
 - compare options, [607](#)
 - compare tab, [603](#)
 - comparison commands, [602](#)
 - comparison method, [605](#)
 - differences in text format, [611](#)
 - flattened designs, [612](#)
 - hierarchical designs, [612](#)
 - icons, [610](#)
 - initiating with GUI, [602](#)
 - introduction, [600](#)
 - leading edge tolerance, [606](#)
 - list window display, [611](#)
 - mixed-language support, [600](#)
 - pathnames, [608](#)
 - reference dataset, [603](#)
 - reference region, [604](#)
 - saving and reloading, [612](#)
 - setup options, [601](#)
 - signals with different names, [602](#)
 - test dataset, [603](#)
 - timing differences, [609](#)
 - trailing edge tolerance, [606](#)
 - using comparison wizard, [601](#)
 - using the GUI, [602](#)
 - values column, [610](#)
 - wave window display, [608](#)
- Waveform Comparison
 - created waveforms, using with, [798](#)
 - difference markers, [609](#)
- waveform editor
 - creating waveforms, [791](#)
 - editing waveforms, [793](#)
 - mapping signals, [798](#)
 - saving stimulus files, [796](#)
 - simulating, [796](#)
 - Waveform Compare, using with, [798](#)
- waveform logfile
 - overview, [529](#)
 - see also* WLF files
- waveforms, [529](#)
 - optimize viewing of, [925](#)
 - viewing, [174](#)
- WaveSignalNameWidth .ini file variable, [923](#)
- WIDTH
 - matching to Verilog, [810](#)
- Window format
 - saving/restoring, [66](#), [585](#)
- windows
 - Active Processes pane, [92](#)
 - Dataflow window, [109](#), [615](#)
 - zooming, [632](#)
 - List window, [116](#), [546](#)
 - display properties of, [582](#)
 - formatting HDL items, [582](#)
 - saving data to a file, [586](#)
 - setting triggers, [591](#), [593](#)
 - Locals window, [120](#)
 - Main window, [66](#)
 - status bar, [71](#)
 - text editing, [986](#)
 - time and delta display, [71](#)
 - toolbar, [74](#)
 - Memory window, [122](#)
 - Objects window, [127](#)
 - Signals window
 - VHDL and Verilog items viewed in, [127](#)
 - Source window, [132](#)
 - text editing, [986](#)
 - viewing HDL source code, [132](#)
 - Variables window
 - VHDL and Verilog items viewed in, [120](#)
 - Wave window, [174](#), [544](#)
 - adding HDL items to, [546](#)
 - cursor measurements, [548](#)

- display preferences, [571](#)
 - display range (zoom), changing, [564](#)
 - format file, saving, [584](#)
 - path elements, changing, [923](#)
 - time cursors, [548](#)
 - zooming, [564](#)
 - WLF file
 - limiting, [532](#)
 - WLF file parameters
 - cache size, [532](#)
 - collapse mode, [532](#)
 - compression, [532](#)
 - delete on quit, [532](#)
 - filename, [531](#)
 - optimization, [532](#)
 - overview, [531](#)
 - size limit, [531](#)
 - time limit, [531](#)
 - WLF files
 - collapsing events, [538](#)
 - indexing during simulation, [925](#)
 - optimizing waveform viewing, [925](#)
 - saving, [530](#)
 - saving at intervals, [537](#)
 - WLFCacheSize .ini file variable, [923](#)
 - WLFCollapseMode .ini file variable, [923](#)
 - WLFCompress .ini variable, [924](#)
 - WLFDeleteOnQuit .ini variable, [924](#)
 - WLFFilename .ini file variable, [925](#)
 - WLFIndex .ini file variable, [925](#)
 - WLFOptimize .ini file variable, [925](#)
 - WLFSaveAllRegions .ini file variable, [926](#)
 - WLFSimCacheSize .ini variable, [926](#)
 - WLFSizeLimit .ini variable, [927](#)
 - WLFTimeLimit .ini variable, [927](#)
 - WLFUseThreads .ini file variable, [928](#)
 - work library, [242](#)
 - creating, [243](#)
 - write format restart, [66](#), [585](#), [599](#)
 - WRITE procedure, problems with, [265](#)
- X —
- X
- tracing unknowns, [622](#)
- xml format
- coverage reports, [673](#)

- Z —
- Z values, automatically excluded, [645](#)
 - zero delay elements, [261](#)
 - zero delay mode, [325](#)
 - zero-delay loop, infinite, [263](#)
 - zero-delay oscillation, [263](#)
 - zero-delay race condition, [306](#)
 - ZeroIn .ini variable, [928](#)
 - ZeroInOptions .ini variable, [928](#)
 - zoom
 - Dataflow window, [632](#)
 - saving range with bookmarks, [565](#)

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 16. **REVIEW OF LICENSE USAGE.** Customer will monitor the access to and use of Software. With prior written notice and during Customer's normal business hours, Mentor Graphics may engage an internationally recognized accounting firm to review Customer's software monitoring system and records deemed relevant by the internationally recognized accounting firm to confirm Customer's compliance with the terms of this Agreement or U.S. or other local export laws. Such review may include FLEXIm or FLEXnet (or successor product) report log files that Customer shall capture and provide at Mentor Graphics' request. Customer shall make records available in electronic format and shall fully cooperate with data gathering to support the license review. Mentor Graphics shall bear the expense of any such review unless a material non-compliance is revealed. Mentor Graphics shall treat as confidential information all information gained as a result of any request or review and shall only use or disclose such information as required by law or to enforce its rights under this Agreement. The provisions of this section shall survive the termination of this Agreement.
 17. **CONTROLLING LAW, JURISDICTION AND DISPUTE RESOLUTION.** The owners of the Mentor Graphics intellectual property rights licensed under this Agreement are located in Ireland and the United States. To promote consistency around the world, disputes shall be resolved as follows: This Agreement shall be governed by and construed under the laws of the State of Oregon, USA, if Customer is located in North or South America, and the laws of Ireland if Customer is located outside of North or South America. All disputes arising out of or in relation to this Agreement shall be submitted to the exclusive jurisdiction of Portland, Oregon when the laws of Oregon apply, or Dublin, Ireland when the laws of Ireland apply. Notwithstanding the foregoing, all disputes in Asia (except for Japan) arising out of or in relation to this Agreement shall be resolved by arbitration in Singapore before a single arbitrator to be appointed by the Chairman of the Singapore International Arbitration Centre ("SIAC") to be conducted in the English language, in accordance with the Arbitration Rules of the SIAC in effect at the time of the dispute, which rules are deemed to be incorporated by reference in this section. This section shall not restrict Mentor Graphics' right to bring an action against Customer in the jurisdiction where Customer's place of business is located. The United Nations Convention on Contracts for the International Sale of Goods does not apply to this Agreement.
 18. **SEVERABILITY.** If any provision of this Agreement is held by a court of competent jurisdiction to be void, invalid, unenforceable or illegal, such provision shall be severed from this Agreement and the remaining provisions will remain in full force and effect.
 19. **MISCELLANEOUS.** This Agreement contains the parties' entire understanding relating to its subject matter and supersedes all prior or contemporaneous agreements, including but not limited to any purchase order terms and conditions. Some Software may contain code distributed under a third party license agreement that may provide additional rights to Customer. Please see the applicable Software documentation for details. This Agreement may only be modified in writing by authorized representatives of the parties. All notices required or authorized under this Agreement must be in writing and shall be sent to the person who signs this Agreement, at the address specified below. Waiver of terms or excuse of breach must be in writing and shall not constitute subsequent consent, waiver or excuse.