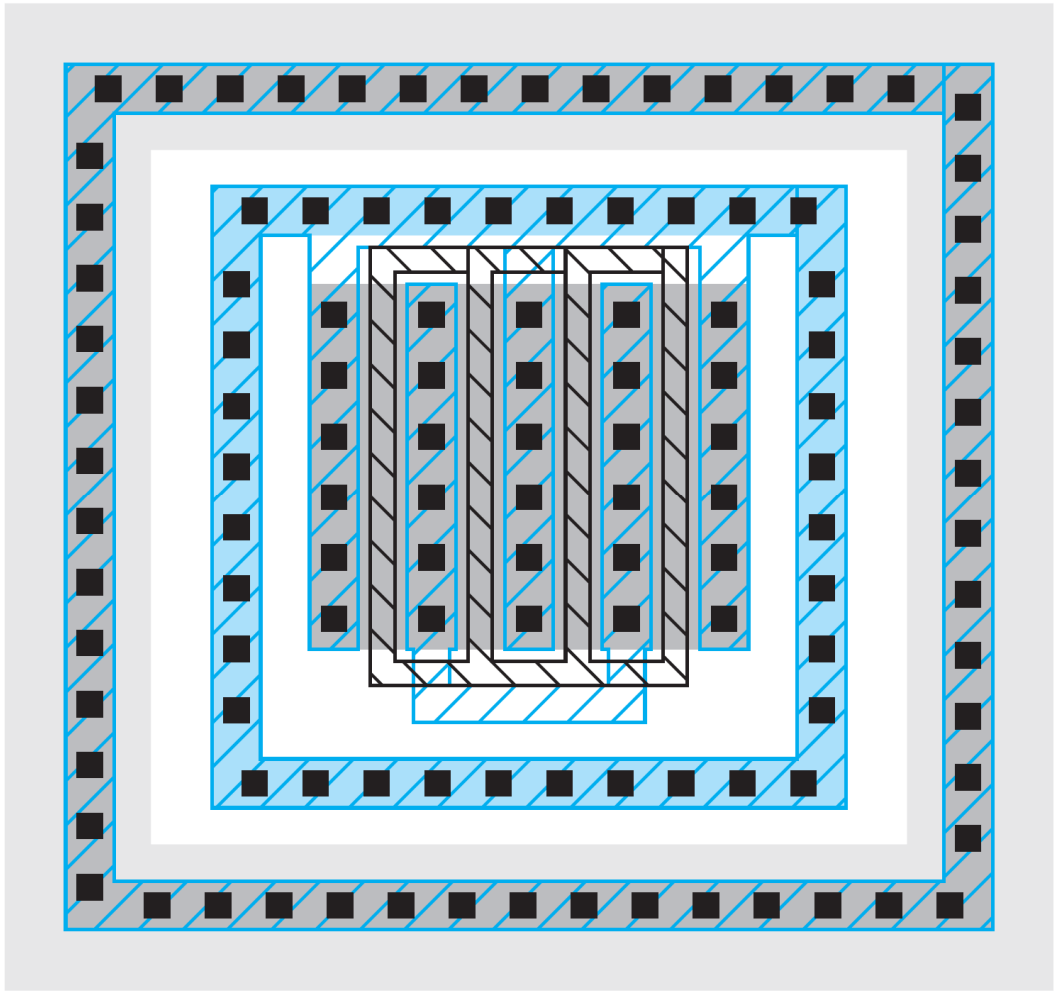

FIGURE 13.45 Double guard rings around folded nMOS output transistor

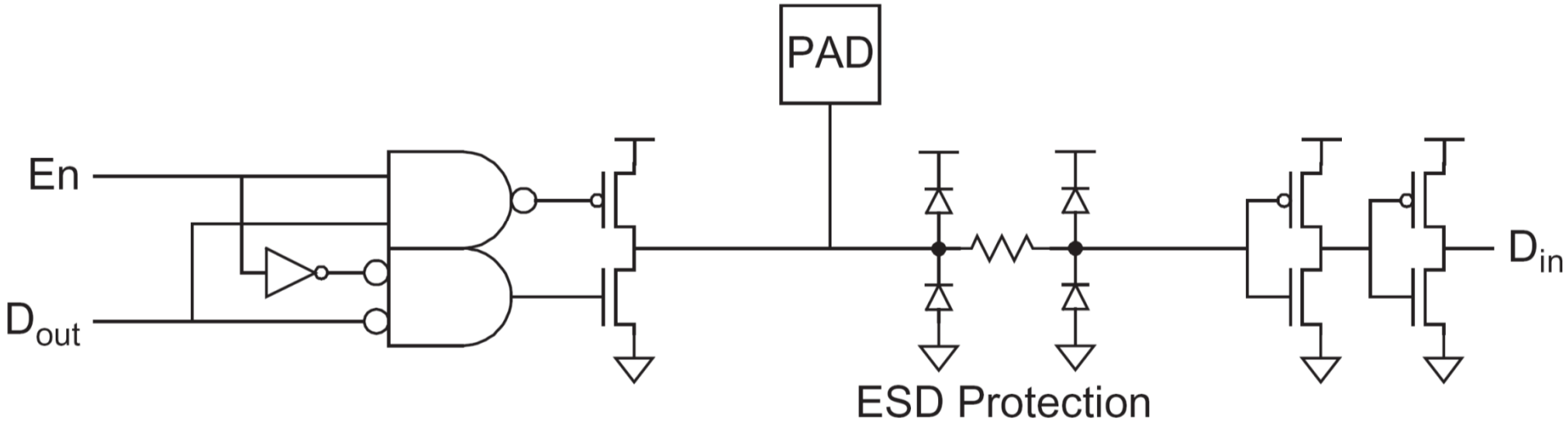

FIGURE 13.47 Bidirectional pad circuitry

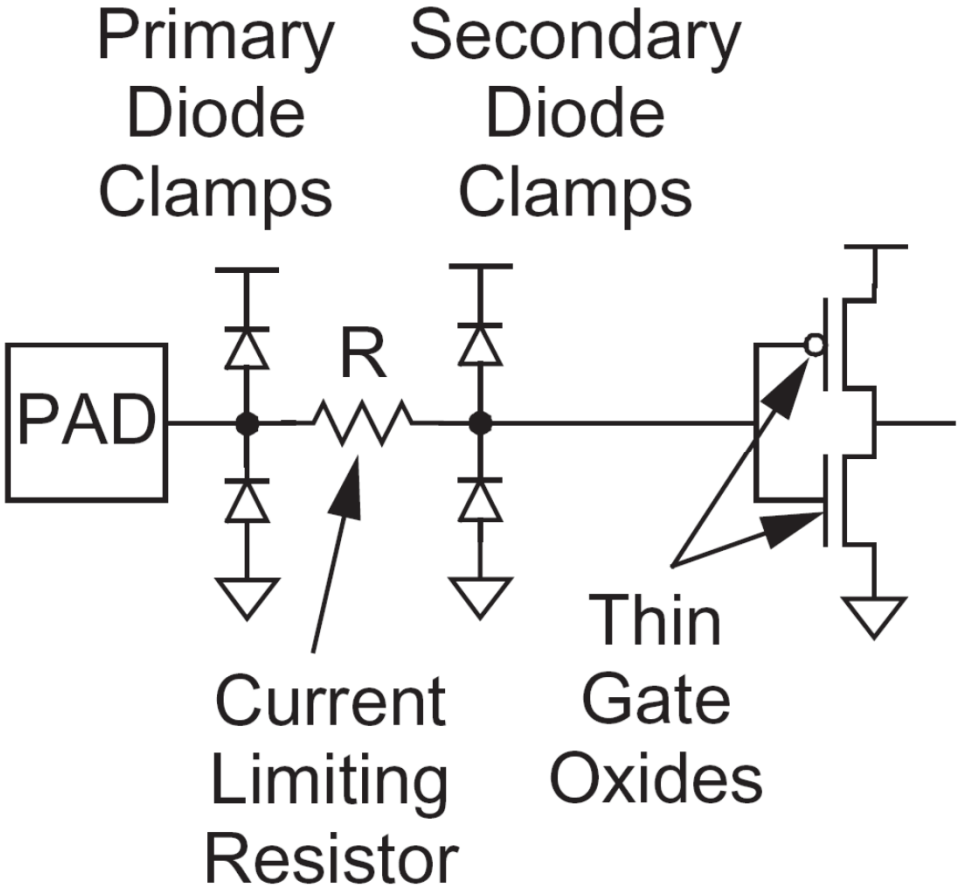

FIGURE 13.49 Input protection circuitry

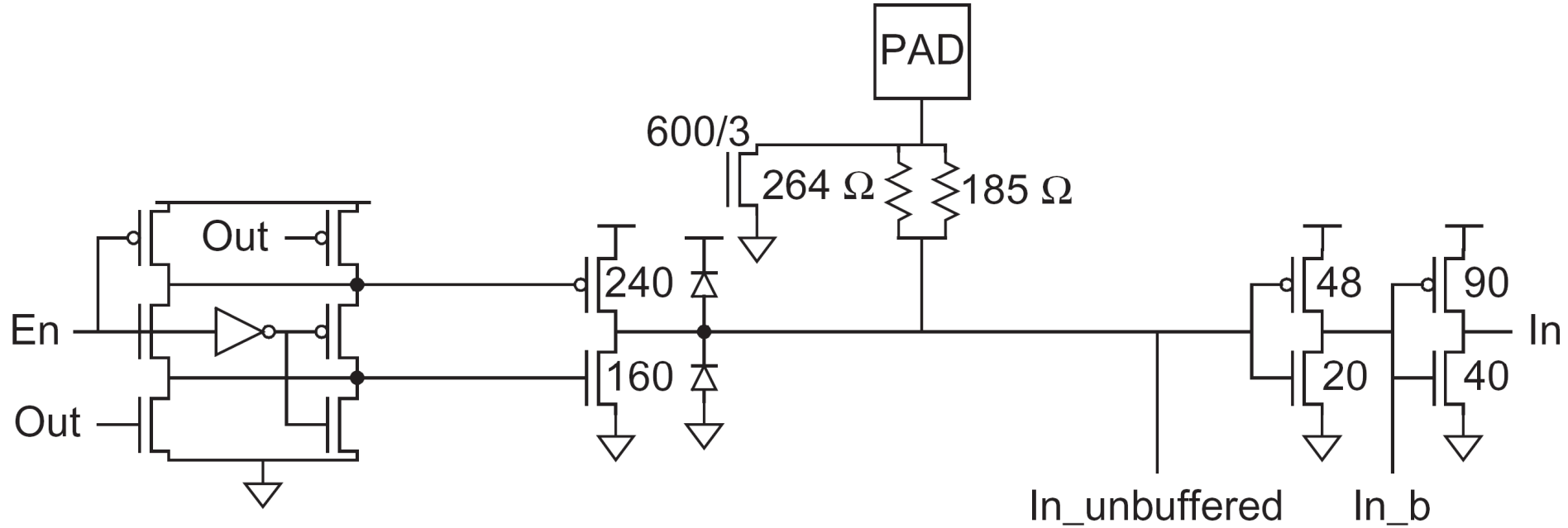

FIGURE 13.52 MOSIS bidirectional pad schematic