RapidChip™ family of Foundation Slices

OVERVIEW

LSI Logic's RapidChip Semiconductor Platform redefines the custom logic market by offering designers a new alternative to the existing design options of standard-cell ASICs, FPGAs, and ASSPs. RapidChip was developed using the years of experience LSI Logic has in ASIC design methodology and manufacturing. The RapidChip platform offers a unique blend of performance and flexibility, while dramatically reducing the design and manufacturing timescales associated with high-performance custom design.

The seven RapidChip foundation slices are aimed at particular applications as the platforms for custom design. The slices contain pre-diffused memory and high-performance system building blocks from the LSI Logics CoreWare® library, along with customizable logic. Additional application-specific CoreWare elements are also provided for mapping into the slices. Customization is accomplished by mapping this CoreWare IP along with the designers' logic to the slice using the metal layers.

RC1800 Foundation Slices

RC1800 Slice Name	RC1810	RC1820	RC1830	RC1840	RC1845	RC1850	RC1860
Customer Usable Gates (M)	0.5	1.0	1.3	1.5	1.8	2.2	2.5
9-Kbit 2-Port RAMs	8	8	6	12	12	12	16
9-Kbit Dual-Port RAMs	2	4	4	8	8	8	12
36-Kbit 2-Port RAMs	6	8	12	16	16	20	24
144-Kbit Single-Port RAMs	2	4	3	5	6	8	2
Total RAM bits (M)	0.6	1.0	0.9	1.6	1.6	2.0	1.3
ARM926 8K/8K Caches	0	0	0	1	1	1	0
GigaBlaze SerDes@3.1875Gbit/Sec	4	4	4	8	0	8	12
DDR PHY bits	0	0	40	40	0	80	0
600 MHz to 1250 MHz PLLs 100 MHz to 500 MHz PLLs	1 3	1 3	1 3	1 3	1 3	1 3	1 3
Base Configurable I/O	304	422	428	486	638	514	546
Configurable I/O with DDR			346	404		432	
Pins (1mm pitch) Flip Chip Package Body Size	544 27mm	736 31mm	788 31mm	960 35mm	960 35mm	1157 40mm	1157 40mm

FEATURES

- Deep Sub-Micron Technology Platforms
  - Family of seven slices
  - Embedded Diffused IP
  - Up to 2.5M Usable Gates
  - Up to 2Mbit Diffused RAM
  - Up to 638 Metal Configurable I/Os
  - Offered in 0.18 micron G12R
- Tools and Methodology
  - Optimized for Time-To-Market
  - Predictable, Single-Pass Design Closure
  - Slice Specific Verification Environment including Transactors and Monitors
- Design Productivity Tools
  - Memory Generator
  - I/O Configurator
  - Clock Factories
- Pre-diffused Proven CoreWare IP
  - GigaBlaze®: 1 to 3.1875 Gb/s Gbit Ethernet, XAUI FibreChannel, Serial ATA InfiniBand, RapidIO
  - Processors: ARM®,
- Advanced Proven CoreWare IP
  - XGXS
  - Microprocessor Core and AMBA Peripherals
  - DDR, RLDRAM Controllers
  - Ethernet MAC 10/100/1G/10G
  - FibreChannel and SCSI Controllers
  - USB host and function
  - PCI Controllers

LSI LOGIC®

RapidChip™ Foundation Slices

- Memories
  - High Density Single/Multi-Port SRAM
  - Register files
  - ROM

BENEFIT

- Combines the best features of Standard Cell ASIC and FPGA:
  - High Performance
  - High Density
  - Low Development Cost
  - Rich IP Coreware Library
  - Fast Time-to-Marktet
  - Reduced Risk
  - Increased Predictability
  - Customizable Benefits

DESIGN FLOW AND PRODUCTIVITY

The time-to-market promise of RapidChip is delivered through the unique advantages of a new design methodology and tool set. This methodology relies on three key elements to provide its accelerated and deterministic flow - a set of automated tools and shells, strict design rules and guidelines, and the inherent predictability of designing with a customizable logic structure. By eliminating lengthy timing closure loops, the RapidChip methodology boosts productivity and enables fast, deterministic throughput from final netlist to prototypes.

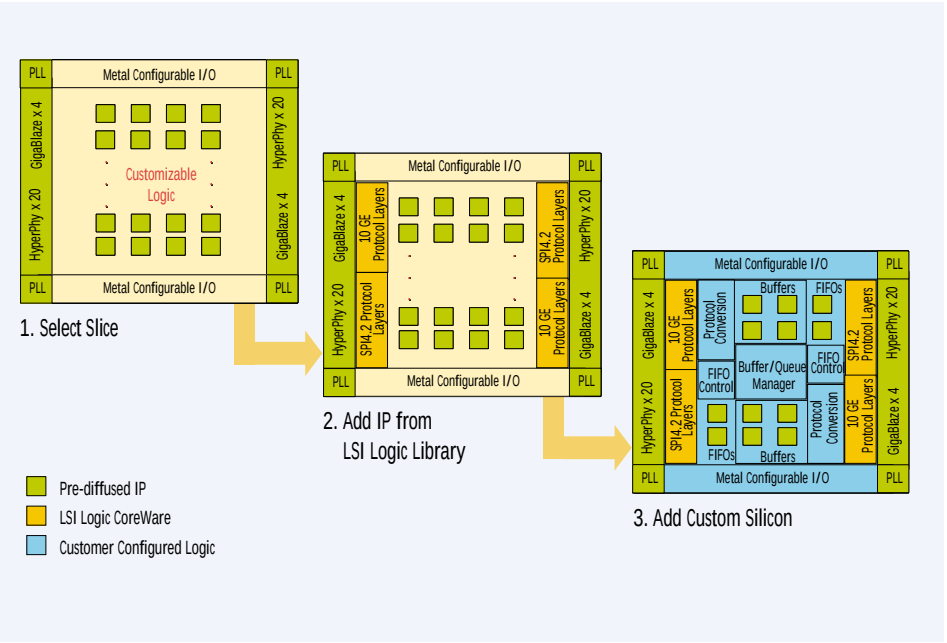

Figure 2: Three steps to Custom Silicon

A number of views or shells of the selected slice and additional IP are provided to accelerate every phase of the design process. Shells are provided for RTL design, Verification, Static Timing Analysis, Synthesis and Test. As an example, a designer's custom logic is connected to well-defined interfaces within the RTL Shell for the particular RapidChip slice being used, resulting in a simple integration process. Designers also benefit from consistent hierarchy management inherent to the RTL design capabilities within RapidChip methodology.

The verification shell provides an advanced starting point for the functional verification phase of designing a custom device. This ready-made environment includes reference models for all cores, transactors, monitors and protocol checkers.

LOGIC INTEGRATION

With RapidChip, designers have access to the latest deep sub-micron process technologies without the compromises of Programmable Logic Devices. RapidChip's customizable metal architecture allows for the implementation of up to two and one-half million usable logic gates.

Memory requirements are realized with high-density, pre-diffused cells or by utilizing portions of the customizable logic. Automated tools make implementation choice transparent to the user. Other dedicated tools for generating clock networks, bus structures and test logic – automate error prone tasks ensuring critical functions are created correct-by-construction.

EMBEDDED MEMORY BLOCKS

Single-port, 2-port and dual-port, high-density, high performance RAM blocks are diffused into each RapidChip slice, defining a memory space that can be configured to meet a particular application. Blocks can be customized and combined to create larger memories. Controllers can be built in the transistor fabric to create multi-port memory structures. Key features that can be configured include: combination of up to four independent memory blocks, configuration of up to four read/write ports, word length up to 128 bits and error management overhead up to two bits/byte.

GIGABLAZE® MULTI-GIGABIT TRANSCEIVER

A major time-saving feature of the RapidChip family of slices is derived from the diffused GigaBlaze® serializer/deserializer (SerDes) technology. These high-performance building blocks represent a fifth-generation product with the proven capability to enable such standards-compliant interfaces as 1 and 10Gbit Ethernet, Fibre Channel, Serial ATA, Serial Attached SCSI, PCI Express and more.

CONFIGURABLE I/O

High performance I/O is one of the key benefits of a RapidChip slice. Dedicated I/Os are diffused in the slice where industry standards dictate performance and power reasons provide justification.

Because designers require flexibility all slices have configurable I/Os, of which all can address the most commonly used signally stands, such as LVTTL, LVDS, HSTL, SSTL, etc. Designers can specify the standard as well as voltage levels, drive strengths and pin locations.

DELIVERING ON THE PROMISE OF DESIGN RE-USE

RapidChip makes advanced CoreWare IP blocks from LSI Logic available in three forms: hard, firm, and soft.

Hard Cores - High speed transceivers such as HyperPHY® and GigaBlaze®, and CPUs – are pre-placed using silicon-optimized technology.

Firm Cores - Implemented in the customizable logic region, relocatable with fixed timing.

Soft Cores - Provided as synthesizeable RTL, implemented in the customizable logic region.

I/O cells with metal configurable Vdd and driver characteristics simplify the design process.

RapidChip™ Foundation Slices

Configurable I/O

I/O Signaling Standard	Type	Vdd Voltage	Drive Strength
CMOS/LVTTL[1]	Bidirect	3.3V	12 ma, 8 ma, 4 ma, 2 ma
CMOS/LVTTL[1]	Bidirect	2.5V	12 ma, 8 ma, 4 ma, 2 ma
CMOS/LVTTL[1]	Bidirect	1.8V	12 ma, 8 ma, 4 ma, 2 ma
SSTL-2	Bidirect	2.5V	Class-I, Class-II
HSTL Single-Ended	Bidirect	1.5V	Class-I, Class-II, Class-III
LVDS Differential Input	Input		
LVDS Differential Output	Output		
LVPECL	Input	3.3V	
PCI-66	Bidirect	3.3V	
Impedance Match (50 ohm)	Bidirect	3.3V	

[1] Available with pull-ups and pull-downs.

FLIP CHIP PACKAGING

Each foundation slice has a carefully chosen package to ensure all electrical and mechanical design requirements are met based on worst-case conditions. The design and construction of each package provides a highly stable electrical environment and excellent thermal characteristics for the most demanding applications. Each package also meets the requirements for very high-speed I/Os. The number of I/Os, the die size and the power consumption of a particular slice determine which packages can be used.

With multiple independent power domains, all packages are optimized to reduce VDD/VSS path inductance, signal I/O path inductance and signal-to-signal crosstalk. 100% differential pair routing for I/Os with a Z_0 of 50-55 ohms provides a “no compromises” environment for operating multiple high performance Serdes at the maximum data rates of 3.1875 Gb/s.

Optimal power plane segmentation maximizes I/O utilization

Power splits match physical size of DDR and SerDes blocks

Clock and PLL locations optimized to enhance performance and facilitate ESD protection

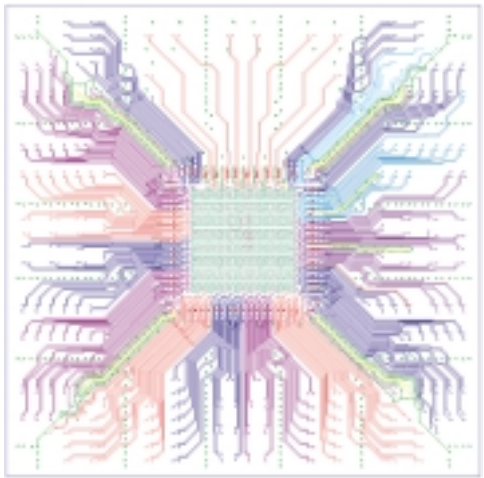

Figure 3: Slice Optimised Packaging

For more information please call:

LSI Logic Corporation
North American Headquarters
Milpitas, CA
Tel: 866 574 5741

LSI Logic Europe Ltd.
European Headquarters
United Kingdom
Tel: 44 1344 426544
Fax: 44 1344 481039

LSI Logic KK Headquarters
Tokyo, Japan
Tel: 81 3 5463 7821
Fax: 81 3 5463 7820

LSI Logic Hong Kong
Tsuenwan, Hong Kong
Tel: 852-2405-8600
Fax: 852-2412-7820

LSI Logic web site
www.lsilogic.com

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