Ion-Implanted Complementary MOS Transistors in Low-Voltage Circuits

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Abstract—**Simple but reasonably accurate equations are derived, which describe MOS transistor operation in the weak inversion region near turn-on. These equations are used to find the transfer characteristics of complementary MOS (CMOS) inverters. The smallest supply voltage at which these circuits will function is approximately $8kT/q$. A boron ion implantation is used for adjusting MOST turn-on voltage for low-voltage circuits.**

Introduction

RECENTLY, techniques have been developed for fabricating complementary MOS transistors with low turn-on voltages, enabling them to be used in circuits with supply voltages less than 1.35 V [1]–[3]. MOS transistors in low-voltage digital circuits are, by necessity, operating near their turn-on or threshold voltage. Unfortunately, in the vicinity of turn-on, the assumptions commonly used in deriving device characteristic equations are inaccurate [4]. In Section I of this paper, new MOS transistor characteristic equations are derived, which are simple but reasonably accurate in the weak inversion region near turn on, as well as elsewhere.

In Section II these equations are used to find the transfer characteristic of a low-voltage complementary MOS inverter and the minimum supply voltage at which the inverter will function is determined. This limit is important since it serves to define the minimum power-speed product that can be achieved with CMOS digital circuits.

In Section III a technique of adjusting MOST turn-on voltage by ion implantation is described. A theory of the turn-on voltage change as a function of the implantation parameters is developed and a brief description of the MOST fabrication procedure is included. By using ion implantation in conjunction with standard aluminum-gate MOS processing, low-voltage complementary integrated circuits with excellent performance characteristics can be achieved.

I. Device Equations Including Weak Inversion Effects

An n-channel MOS transistor [Fig. 1(a)] is analyzed. As illustrated in Fig. 1(b), ψ_s is the total band bending and ϕ_f is the potential difference between the intrinsic level (midband gap) and the Fermi level. The potential difference between the electron quasi-Fermi level and the bulk Fermi level is ϕ_c, which is nonzero because there is a transverse electron current flowing (i.e., a drain-source voltage is applied).

Integrating Poisson's equation, the total charge in the semiconductor is given approximately [4] by

$$Q_s = -\sqrt{2q\epsilon_s N_A(\psi_s + kT/q)}\,\exp\left[q(\psi_s - \phi_c - 2\,|\phi_f|)/kT\right]. \tag{1}$$

This gives the total semiconductor charge per unit area $Q_s = Q_n + Q_B$ as a function of ψ_s and ϕ_c. Two distinct cases of this equation can be identified. These are 1) a weak inversion case where the inversion layer charge per unit area Q_n is much less than the depletion region charge per unit area Q_B and 2) a strong inversion case where Q_n is much greater than Q_B. Making approximations appropriate in each of these cases, the following formulas, giving Q_n as a function of the gate voltage V_G and the electron quasi-Fermi level ϕ_c are derived in the Appendix.

1) Weak Inversion:

$$-Q_n = C_0\left(n\frac{kT}{q}\right)\exp\left(\frac{q}{nkT}\left[V_G - V_T(\phi_c) - n\frac{kT}{q}\right]\right), \tag{2a}$$

valid when $V_G \leq V_T(\phi_c) + n(kT/q)$.

2) Strong Inversion:

$$-Q_n = C_0[V_G - V_T(\phi_c)], \tag{2b}$$

valid when $V_G \geq V_T(\phi_c) + n(kT/q)$. C_0 is the oxide capacitance per unit area.

$$V_T(\phi_c) = V_{FB} + 2\,|\phi_f| + \phi_c + \frac{1}{C_0}\sqrt{2q\epsilon_s N_A(2\,|\phi_f| + \phi_c)}, \tag{3}$$

is the threshold voltage referenced to the substrate. V_{FB} is the flat-band voltage [5].

N_A is the substrate doping density and ϵ_s is the semiconductor dielectric constant.

$$n = \frac{C_d + C_{fs} + C_0}{C_0} \tag{4}$$

$$C_d \triangleq \frac{\partial}{\partial \psi_s}(Q_B)\Big|_{\psi_s = 2|\phi_f| + \phi_c},$$

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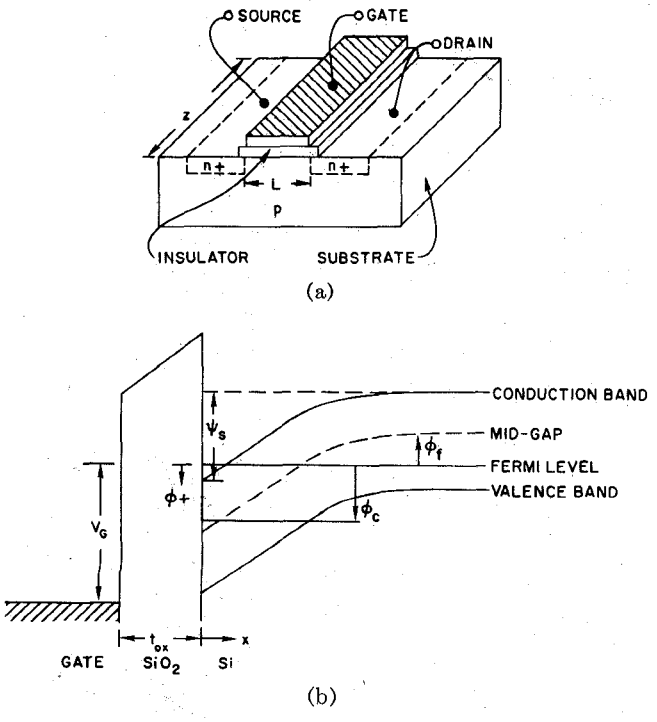

Fig. 1. (a) Physical structure of n-channel MOST. (b) Band diagram of n-channel MOST.

and

$$Q_B = \sqrt{2q\epsilon_s N_A(\psi_s)},$$

so that

$$C_d = \frac{\sqrt{2q\epsilon_s N_A}}{2\sqrt{2\,|\phi_f| + \phi_c}}. \tag{5}$$

and $C_{fs} = qN_{fs}$, where N_{fs} is the fast surface state density per electronvolt evaluated at $\psi_s = \phi_c + 2|\phi_f|$.

A simple physical explanation of (2a) is presented here in lieu of the complete derivation given in the Appendix. If the gate voltage is varied by a small amount ΔV_G there will be a small change in surface potential, $\Delta\psi_s$. $\Delta\psi_s$ may be found with the aid of the equivalent circuit shown in Fig. 2. C_e is the capacitance of the mobile electrons, or $(\partial Q_n/\partial\phi_s)$. When the surface is strongly inverted C_e is much larger than C_o, C_d, and C_{fs} so that ψ_s is essentially constant. However, when the surface is weakly inverted C_e is small compared to C_d and C_{fs}. The equivalent circuit then yields $\Delta\psi_s = (1/n)\Delta V_G$. In weak inversion Q_n varies as a constant $\times$ exp $[q(\psi_s - \phi_c)kT]$. From this, it is apparent that $Q_n \sim$ exp $[qV_G/nkT - q\phi_c/kT]$. The remaining terms in (2a) are found by considerations presented in the Appendix.

It can be easily shown [5] that when a MOST is operated in the linear region (small drain voltage) the drain-to-source conductance g_D is given by [5],

$$g_D = \frac{Z}{L}\,\mu_n\,|Q_n(\phi_c = 0)|. \tag{6}$$

Plots of the measured versus theoretical linear region g_D

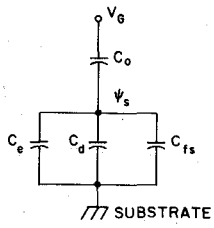

Fig. 2. Model circuit of MOS structure.

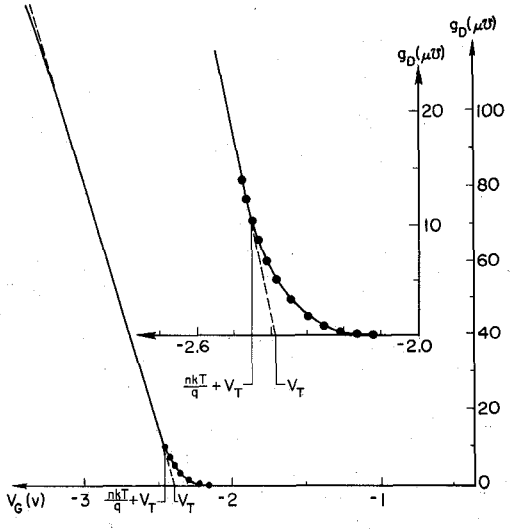

Fig. 3. Channel conductance g_D versus gate voltage V_G for device 1. ——experiment; ···· theory.

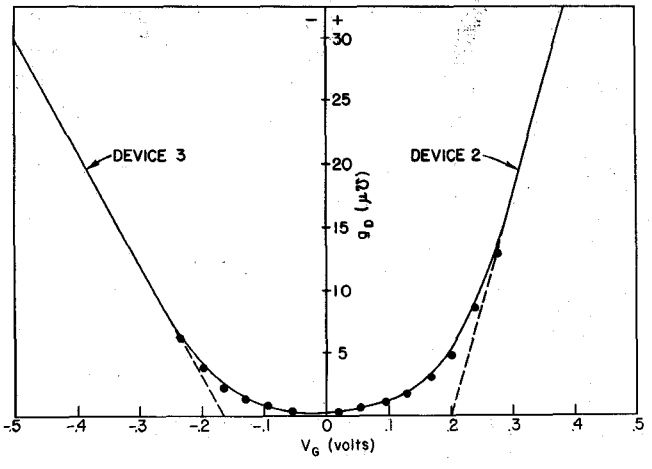

Fig. 4. Channel conductance g_D versus gate voltage V_G for devices 2 and 3. ——experiment; ···· theory.

for three devices are shown in Figs. 3 and 4. Table I contains pertinent data about the devices.

The drain current-voltage characteristics of a MOST are now found using the following relation for the drain current I_D [4]

$$I_D = (Z/L)\mu_n \int_0^{V_D} |Q_n(\phi_c)|\, d\phi_c. \tag{7}$$

Here Z is the channel width, L, the channel length, μ_n, the effective electron surface mobility, and V_D, the drain-to-source voltage. The two relations for Q_n, (2a), and (2b), when inserted in (7) generate three distinct modes

TABLE I

Devices	Device Constants	Calculated from Plot
Device 1	$N_D = 1 \times 10^{15}$ cm^{-3} $t_{0x} = 1000$ Å $m = 1 + \frac{C_d}{C_0} = 1.46$	$V_T = 2.39$ V $n = 3.08$ $N_{fs} = 3.8 \times 10^{11}$ cm^{-2} eV^{-1} $K = 153\ \mu$A/V^2 $= \frac{Z}{L}\mu C_0$
Device 2	$N_A = 1.6 \times 10^{16}$ cm^{-3} $t_{0x} = 1000$ Å $m = 2.05$	$V_T = 0.20$ V $n = 2.80$ $N_{fs} = 1.6 \times 10^{11}$ cm^{-2} eV^{-1} $K = 180\ \mu$A/V^2
Device 5	$N_D = 1 \times 10^{15}$ $t_{0x} = 10000$ Å $m = 1.46$	$V_T = -.165$ V $n = 2.70$ $N_{fs} = 2.7 \times 10^{11}$ cm^{-2} eV^{-1} $K = 90\ \mu$A/V^2

of operation for the MOST. The characteristic equations for each mode are presented below.

A. Strong Inversion Only

In this case the gate voltage is large enough to strongly invert the entire channel. Equation (2b) applies to the integration (7). The defining criteria for this region are

$$V_G \geq V_T(0) + n(kT/q)$$

and

$$V_G \geq V_T(V_D) + n(kT/q),$$

where the argument of V_T gives the value of ϕ_c at which (3) is evaluated. Solving the preceding inequality for V_D* gives $V_D \leq V_D$* where

$$V_D^* = V_G - \left(V_T + n\frac{kT}{q}\right) + V_B\left[1 + \frac{V_B}{4|\phi_f|} - \sqrt{\left(1 + \frac{V_B}{4|\phi_f|}\right)^2 + \frac{V_G - [V_T + n(kT/q)]}{2|\phi_f|}}\right]. \quad (8)$$

Here V_B is defined as $|Q_b(\psi_s = 2|\phi_f|)|/C_0$ and $V_T = V_T(0)$. Using (2a), (7) becomes

$$I_D = (Z/L)\mu_n C_0\left\{(V_G - V_{FB} - 2|\phi_f|)V_D - \frac{V_D^2}{2} - V_B\frac{4|\phi_f|}{3}\left[\left(1 + \frac{V_D}{2|\phi_f|}\right)^{3/2} - 1\right]\right\} \quad (9a)$$

valid when $V_D \leq V_D$* and $V_G \geq V_T + n(kT/q)$. Equations (9a), (9b) can be simplified by assuming that $V_D \ll 2|\phi_f|$ yielding

$$I_D \cong \frac{Z}{L}\mu_n C_0\left[(V_G - V_T)V_D - \frac{V_D^2}{2}\right], \quad (9b)$$

valid when $V_D \leq (V_G - (V_T + n(kT/q))/m$, where $m = (C_0 + C_d)/C_0$.

B. Mixed Strong and Weak Inversion

In this case, the gate voltage is large enough to strongly invert the channel near the source but the drain voltage is also large enough to cause weak inversion near the drain. In other words, the device is operating near saturation. The criteria are $V_G \geq V_T(0) + n(kT/q)$ and $V_G \leq V_T(V_D) + n(kT/q)$. This yields $V_D \geq V_D$*. In this case (2b) applies to that part of the integration where $0 \leq \phi_c \leq V_D$* and (2a) applies when V_D* $\leq \phi_c \leq V_D$. The major contribution of (1) to the integration is for V_D* $\leq \phi_c \leq V_D$* $+ n(kT/q)$ because the integrand decreases exponentially in ϕ_c. The bulk charge term in $V_T(\phi_c)$, (3), will vary only slightly in this range and thus it is reasonable to expand about $\phi_c = V_D$*. This gives $V_T(\phi_c) = V_T(V_D$*$) + m(\phi_c - V_D$*$)$ where $m = (C_0 + C_d)/C_0$. Equation (7) becomes upon integrating and noting that $V_G = V_T(V_D$*$) + n(kT/q)$,

$$I_D = \frac{Z}{L}\mu_n C_0\left\{(V_G - V_{FB} - 2|\phi_f|)V_D^* - \frac{V_D^{*2}}{2} - V_B\frac{4|\phi_f|}{3}\left[\left(1 + \frac{V_D^*}{2|\phi_f|}\right)^{3/2} - 1\right] + \frac{1}{m}\left(n\frac{kT}{q}\right)^2\left(1 - \exp\left[\frac{-mq}{nkt}(V_D - V_D^*)\right]\right)\right\}, \quad (10)$$

valid when $V_D \geq V_D$* and $V_G \geq V_T + n(kT/q)$.

The C_d term in n is evaluated at $\phi_c = V_D$*.

C. Weak Inversion Only

In this case the gate voltage is not large enough to strongly invert the channel at any point. The criterion is $V_G \leq V_T + n(kT/q)$.

Integrating as before

$$I_D = \frac{Z}{L}\mu_n C_0\frac{1}{m}\left(n\frac{kT}{q}\right)^2\exp\left[\frac{q}{nkT}\left(V_G - V_T - n\frac{kT}{q}\right)\right]\cdot\left\{1 - \exp\left[\frac{-mq}{nkT}V_D\right]\right\}, \quad (11)$$

valid when $V_G \leq V_T + n(kT/q)$. The C_d term in n is evaluated at $\phi_c = V_D$*.

Equations (9a), (9b), (10), and (11) characterize the dc behavior of the MOST. The noticeable effects of the weak inversion region are 1) exponential dependence of I_D on V_G and V_D when $V_G \leq V_T + n(kT/q)$ and 2) exponential transition into saturation instead of the classical parabolic form.

The drain characteristics of the device whose Q_n versus V_G relation is shown in Fig. 3 were measured and plotted in Fig. 5. On the same graph, both the classical theory (dashed line) and the theory including weak inversion effects (solid line) are shown. Good agreement is obtained between the experimental data and the predictions of the weak inversion theory.

Figs. 6 and 7 show the experimental and theoretical drain characteristics of a low-threshold voltage complementary pair whose Q_n versus V_G relations are shown in Fig. 4. Only the weak inversion region is plotted. The

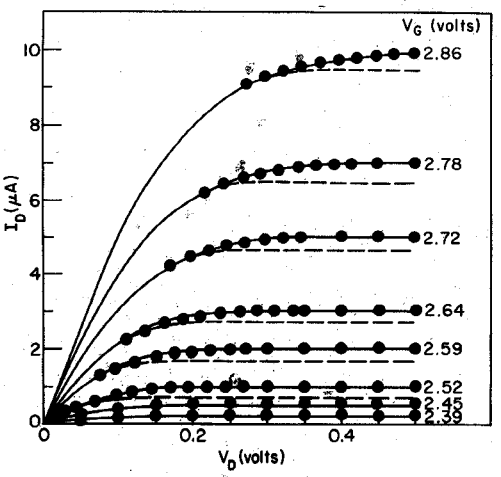

Fig. 5. Drain characteristics for device 1. ——experiment; ----classical theory (9a); ···· theory including weak inversion effects (10a) and (11a).

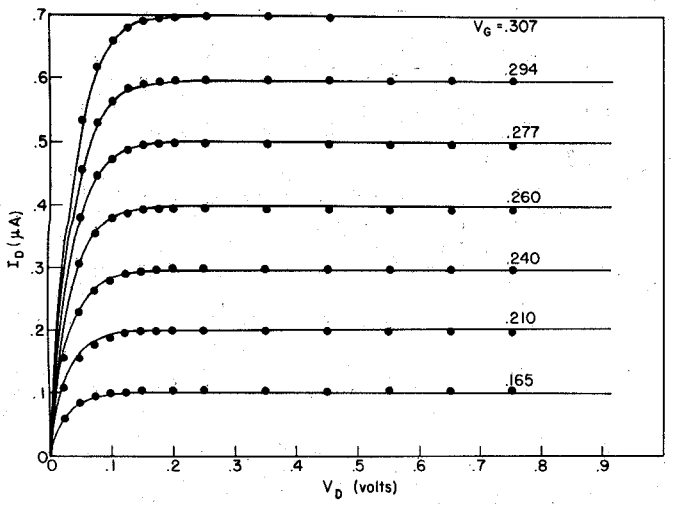

Fig. 6. Drain characteristics for device 2 in weak inversion region. ——experiment; ···· theory (11a).

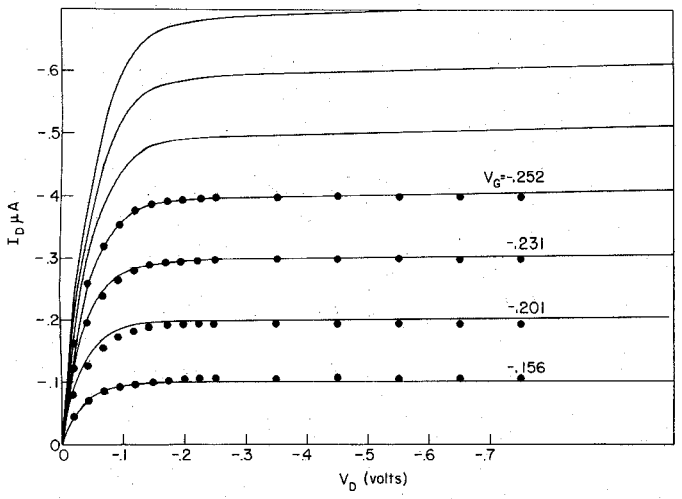

Fig. 7. Drain characteristics for device 3. ——experiment; ···· theory (11a).

values of V_T, n, and $K = (Z/L)\mu C_o$ used in the calculations for Figs. 5, 6, and 7 were taken from Table I. Again, good agreement is obtained for both the n-channel and p-channel devices.

II. Low-Voltage Complementary Inverters

Complementary MOS logic circuits offer distinct advantages in power consumption compared to single-ended circuits. However, to obtain the greatest power savings and lowest power-speed product they should be operated at the lowest practical supply voltage [6]. Realizing that MOS transistors do not turn off as abruptly as the classical equations (9a) and (9b) indicate, but are weakly inverted at gate voltages below V_T, it is desirable to find the minimum supply voltage V_s at which complementary circuits will operate. To this end, the transfer characteristic of a complementary inverter is now determined.

The inverter circuit being analyzed is shown in Fig. 8. The following notations are used. V_{Tp} and V_{Tn} are the magnitude of the thresholds of the n- and p-channel devices, respectively. $K_n = (Z/L)\mu_n C_o$ is the gain constant of the n-channel device and K_p similarly for the p-channel device m_n and n_n, as defined in Section I, refer to the values of m and n for the n-channel device. For the p-channel device m_p replaces m_n and n_p replaces n_n. It is assumed that both transistors are in the weak-inversion-only region. This will be the case if $V_s - V_{Tp} - n_p(kT/q) \leq V_{in} \leq V_{Tn} + n_n(kT/q)$.

Equating the drain current, as found by (11) for both devices, yields

$$\begin{aligned} I_D &= K_n\left(n_n \frac{kT}{q}\right)^2 \frac{1}{m_n} \\ &\quad \cdot \exp\left[q\left(V_{in} - V_{Tn} - n_n \frac{kT}{q}\right) \Big/ n_n kT\right] \\ &\quad \cdot (1 - \exp\left[-m_n q V_0 / n_n kT\right]) \\ &= K_p\left(n_p \frac{kT}{q}\right)^2 \frac{1}{m_p} \\ &\quad \cdot \exp\left[q\left(V_s - V_{in} - V_{Tp} - n_p \frac{kT}{q}\right) \Big/ n_p kT\right] \\ &\quad \cdot (1 - \exp\left[-m_p q(V_s - V_0)/n_p kT\right]). \end{aligned}$$

Solving for V_{in} gives

$$\begin{aligned} V_{in} &= \frac{kT}{q}\left(\frac{n_n n_p}{n_n + n_p}\right) \ln\left(\frac{K_p}{K_n}\frac{n_p^2 m_n}{n_n^2 m_p}\right) \\ &\quad + \frac{n_n}{n_n + n_p} V_s + \frac{n_n n_p}{n_n + n_p}\left(\frac{V_{Tn}}{n_n} - \frac{V_{Tp}}{n_p}\right) \\ &\quad + \frac{kT}{q}\left(\frac{n_n n_p}{n_n + n_p}\right) \ln\left(\frac{1 - \exp\left[-m_p q(V_s - V_0)/n_p kT\right]}{1 - \exp\left[-m_n q V_0 / n_n kT\right]}\right). \end{aligned} \tag{12}$$

The measured transfer characteristic for the complementary pair (devices 2 and 3) for various power supply voltages is shown in Fig. 9. Equation (12), using the

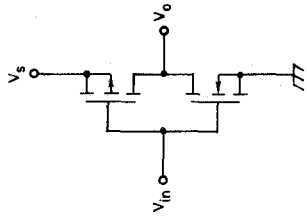

Fig. 8. CMOS inverter circuit.

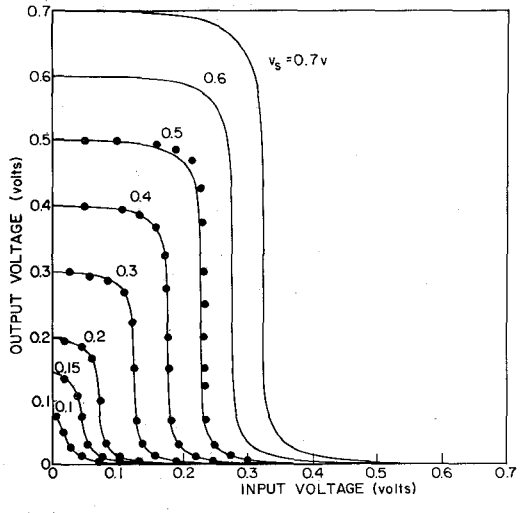

Fig. 9. CMOS inverter transfer characteristics. ——experiment; ···· theory (12a).

device constants from Table I, is also plotted in Fig. 9. It is interesting to note that there is no hysteresis in the transfer characteristic, even when $V_s < |V_{Tn}| + |V_{Tp}|$.

A simple expression for the inverter gain may be found by assuming $m_n = m_p = m$ and $n_n = n_p = n$. Differentiating (12) with respect to V_o gives the reciprocal of the inverter gain. The maximum gain is found to occur at $V_o = V_s/2$ and is given by

$$A_v = \frac{1}{m}\left(\exp\left[\frac{mqV_s}{2nkT}\right] - 1\right). \tag{13}$$

It is seen that V_s must be at least 3–4 nkT/mq for the inverter to have sufficient gain for use in a digital circuit. Thus

$$V_{s,\min} \approx 4\frac{nkT}{mq}. \tag{14}$$

If $N_{fs} = 0$ then $n/m = 1$ and the inverter displays the maximum nonlinearity obtainable in semiconductor material [7]. Transistors fabricated using conventional clean oxide techniques including a low temperature anneal in forming gas will have n/m in the neighborhood of 2 (see Table I), giving a minimum usable supply of about $8kT/q$ or 0.2 V at 27°C. Standard fabrication techniques yield a spread in turn-on voltages on the order of 0.2 V so a practical supply voltage could never be quite as low as 0.2 V. However, regardless of improvements in control of threshold during fabrication, the supply voltage can never be less than that given by (14). It is interesting to note that reduced operating temperatures permit lower supply voltages [7].

III. Adjusting MOST Turn-on Voltage by Ion Implantation

In the preceding discussion of low-voltage complementary MOS circuits, it has been assumed that the transistor turn-on voltage could always be adjusted to the desired value, approximately half the supply voltage [8]. Using conventional aluminum gate processing this is possible with n-channel devices. Unfortunately, aluminum gate p-channel devices will always have turn-on voltages of −2 V or less. This section discusses a technique for ion-implanting boron [9] through the gate oxide to form a shallow p-layer in the channel region of a p-channel device. This technique decreases the magnitude of the turn-on voltage from its initial value. As a result, devices whose original thresholds were in the neighborhood of −2–3 V can have their thresholds shifted as close to zero as desired. Device 3, whose transfer and drain characteristics are shown in Figs. 4 and 6, was fabricated by this method, resulting in $V_{TP} = -0.17$ V.

It will be assumed that the implanted boron concentration N_A (at the semiconductor surface), is greater than the n-type substrate doping density N_D creating a p-type surface layer. A depletion region will exist at the p-n junction extending a distance 1_p from the junction toward the surface where from [4]

$$1_p = \frac{N_D}{N_A}\left[\frac{2\epsilon(|\phi_{fp}| + |\phi_{fn}|)}{q}\frac{N_A}{(N_A - N_D)N_D}\right]^{1/2}, \tag{15}$$

assuming that the boron density is uniformly distributed from the surface to a depth W. The total implanted dose per unit area in the silicon is $N_I = N_A W$.

For boron doses of interest N_A will be much greater than N_D. In this case (15) becomes

$$1_p = \frac{W}{qN_1}\sqrt{2qN_D\epsilon_s(|\phi_{fn}| + |\phi_{fp}|)}. \tag{16}$$

Since $|\phi_{fn}| \approx |\phi_{fp}|$, (16) can be approximated by

$$1_p \simeq W\frac{Q_B(\psi_s = 2|\phi_f|)}{qN_I}. \tag{17}$$

Equation (17) reevals that if N_I is greater than $Q_B(\psi_s = 2|\phi_f|)/q$, the junction depletion region will not extend to the semiconductor surface. Q_B/q is about 10^{11} cm^{-2} for the typical n-type substrate resistivity of 5 Ω-cm. From considerations below, it is seen that if N_I is less than 10^{11} cm^{-2} the shift in turn-on voltage is less than 0.5 V. In practice a larger shift in turn-on voltage is usually desired causing 1_p to be less than W. The possibility then exists for an undepleted region of mobile holes to exist near the semiconductor surface. This situation is illustrated in Fig. 10(a). Increasing the gate voltage from the value at flat band creates a surface depletion region in the p-layer. At some voltage the surface depletion region will extend to the junction depletion region removing all mobile holes from the channel region

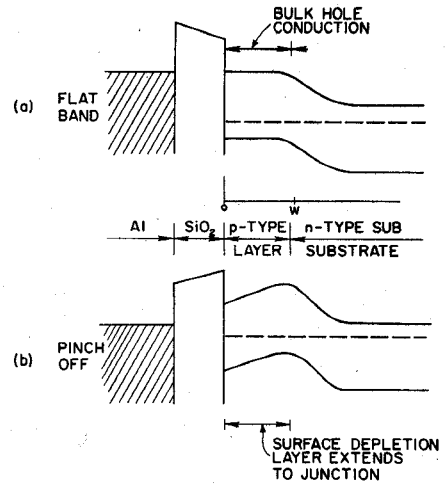

Fig. 10. Band structure for a boron-implanted p-channel MOS transistor.

as illustrated in Fig. 10(b). This is the turn-on voltage for the device.

At this point, calculating the turn-on after implantation V_{TI} is straightforward. The depth of the surface depletion layer 1_s is

$$1_s = \sqrt{\frac{2\epsilon_s \psi_t}{qN_A}}, \tag{18}$$

where ψ_t is the surface depletion region band bending in the p-layer. At turn-on $1_s + 1_p = W$ so that

$$\sqrt{\frac{2\epsilon_s \psi_t}{qN_A}} + \frac{Q_B W}{qN_I} = W. \tag{19}$$

Solving (19) for ψ_t gives

$$\psi_t = \frac{qN_I W(1 - Q_B/qN_I)^2}{2\epsilon_s}. \tag{20}$$

The gate voltage at turn-on, including charge from both the surface and junction depletion regions, is thus

$$V_{TI} = \Phi_{MS} - \frac{Q_{SS}}{C_0} - (|\phi_{fn}| + |\phi_{fp}|) + \psi_t + \frac{qN_I}{C_0} - \frac{Q_B}{C_0}. \tag{21}$$

Φ_{MS} is the metal-semiconductor work function for the n-type substrate. The turn-on voltage prior to implantation is

$$V_T = \Phi_{MS} - \frac{Q_{SS}}{C_0} - 2|\phi_{fn}| - \frac{Q_B}{C_0}. \tag{22}$$

The shift in turn on ΔV_T is thus

$$\Delta V_T = V_{TI} - V_T = (|\phi_{fp}| - |\phi_{fn}|) + \frac{qN_I}{C_0} + \frac{qN_I W(1 - Q_B/qN_I)^2}{2\epsilon_s}. \tag{23}$$

$(|\phi_{fp}| - |\phi_{fn}|)$ can usually be neglected.

The last term in (23) is the surface band bending and must be less than $2|\phi_{fp}|$ or the surface would become n-type, prohibiting further band bending. If the surface becomes n-type before the surface depletion region extends deep enough to entirely deplete the p-layer the device cannot be turned off. Since ψ_t must be less than $2|\phi_{fp}|$ for complete turn-off to be possible, (20) gives

$$2|\phi_{fp}| \leq \psi_t = \frac{qN_I W}{2\epsilon_s} \tag{24}$$

assuming $Q_B/qN_I \ll 1$. The maximum possible shift in threshold $\Delta V_{T\,\max}$, while having a device that can be turned off, is, using (23) and (24),

$$\Delta V_{T\,\max} = 2|\phi_{fp}| + \frac{4|\phi_{fp}|\epsilon_s}{WC_0} = 2|\phi_{fp}|\left[\frac{2\epsilon_s/W}{C_0} + 1\right] \tag{25}$$

Thinner p-layers allow larger shifts in turn-on voltage. When both the gate oxide and W are 1000 Å, $\Delta V_{T\,\max}$ is about 5.2 V.

The threshold-shifting boron implantation is done after gate oxidation. Only those ions that pass through the oxide will contribute to N_I. Computer calculations of the Lindhard, Scharff, and Schiott depth-penetration theory [10] predict that the boron will have a Gaussian concentration profile centered about a depth which depends on the implantation voltage and a standard deviation about one third this depth. At a 30-kV implantation voltage, 50 percent of the boron will penetrate a 1000-Å gate oxide, at 40 kV 80 percent will penetrate a 1000-Å gate 93 percent will penetrate. Energies in the range of 30–50 kV have been found suitable for device fabrication provided the doses are adjusted to allow for the partial penetration.

The implantation must be followed by an anneal to restore crystal damage and activate the boron. Annealing for ten minutes at 1050°C appears to give complete activation and gives good SiO_2–Si interface characteristics. Following this anneal the junction depth is about 1500 Å. If the anneal is performed at less than 900°C, the boron will not be totally active and the device properties are degraded. Device 3 received a dose of 1.1×10^{12} cm^{-2} at 30 kV and was annealed at 1050°C. The resulting shift in turn-on voltage was +2 V.

The turn-on voltages of n-channel devices can also be shifted in a positive direction by boron implantation. Of course, in this case there is no junction formed by the implantation. If the depth of the boron is much less than the surface depletion-layer depth, Q_B will not be greatly affected by the implant and the turn-on shift will be $\Delta V_T = qN_I/C_o$.

CMOS integrated circuits with a wide variety of threshold voltages can be fabricated using ion implantation to adjust threshold voltages and to provide a predeposition for doping p-type regions where the n-channel devices are located.

Conclusion

The fast surface state density N_{fs} is the most important factor in determining the performance of MOS

transistors in the weak inversion region near turn-on. At room temperature CMOS circuits can operate at supply voltages as low as 0.2 V, provided the fast surface state density is low enough. Ion implantation of boron is a convenient method of adjusting the turn-on voltage of MOS transistors, both n- and p-channel, to permit operation at low supply voltages.

Appendix

The total charge per unit area Q_s in the semiconductor is given by Sze [4]. For substrate doping levels of interest $q\psi_s/kT > 20$ when ψ_s is near threshold. Q_s is then approximated by

$$Q_s = -\sqrt{2q\epsilon_s N_A(\psi_s+(kT/q)\exp[q(\psi_s-\phi_c-2|\phi_f|)/kT])}, \tag{26}$$

where N_A is the R-type substrate-doping density and ϵ_s is the dielectric constant of the semiconductor. Assuming that the voltage developed across the surface inversion layer is much less than $2|\phi_f|$, the immobile charge in the surface depletion region Q_B is

$$Q_B = -\sqrt{2q\epsilon_s N_A\psi_s}. \tag{27}$$

This leaves $Q_n = Q_s - Q_B$ mobile electrons per unit area in the inversion layer.

$$Q_n = -[\sqrt{2q\epsilon_s N_A(\psi_s+(kT/q)\exp[q(\psi_s-\phi_c-2|\phi_f|)/kT])} - \sqrt{2q\epsilon_s N_A\psi_s}] \tag{28}$$

The gate voltage V_G is given by

$$V_G = \Phi_{MS} + \psi_s - \frac{Q_{SS}}{C_0} - \frac{Q_{fs0}}{C_0} + \frac{qN_{fs}}{C_0}(\psi_s - \phi_c - 2|\phi_f|) - \frac{Q_n}{C_0} - \frac{Q_B}{C_0}. \tag{29}$$

Φ_{MS} is the metal semiconductor work function, Q_{SS} the fixed interface charge per unit area, Q_{fso} the charge in filled fast surface states per unit area when $\psi_s = \phi_c + 2|\phi_f|$, N_{fs} the fast surface state density per electronvolt at $\psi_s = \phi_c + 2|\phi_f|$, and C_0 the oxide capacitance per unit area.

Q_n is found as a function of V_G by eliminating ψ_s from (28) and (29). This cannot be done in closed form. However, from (28) two distinct regions can be identified. A weak inversion region is defined by

$$(kT/q)\exp[q(\psi_s - \phi_c - 2|\phi_f|)/kT] \ll \psi_s,$$

(i.e., the bulk charge dominates the inversion layer charge) and a strong inversion region by $(kT/q)\exp[q(\psi_s - \phi_c - 2|\phi_f|)/kT] \gg \psi_s$. The weak inversion criterion is valid when $\psi_s \leq \phi_c + 2|\phi_f|$. For ψ_s slightly greater than $\phi_c + 2|\phi_f|$ the exponential rapidly increases and the strong inversion criterion is valid.

For the weak inversion region, Q_n is found by a first-order Taylor-series expansion of (28) in powers of $\exp[q(\psi_s - \phi_c - 2|\phi_f|)/kT]$. This gives

$$-Q_n = \frac{\sqrt{2q\epsilon_s N_A}}{2\sqrt{\psi_s}}\frac{kT}{q}\exp[q(\psi_s - \phi_c - 2|\phi_f|)/kT]. \tag{30}$$

Since there will be significant mobile charge only when ψ_s is in the vicinity of $\phi_c + 2|\phi_f|$ it is reasonable to expand the Q_B term in (29) about $\psi_s = \phi_c + 2|\phi_f|$. By the weak inversion criterion Q_n (30) is negligible compared with Q_B and (29) becomes

$$V_G = V_{FB} + \phi_c + 2|\phi_f| + \frac{\sqrt{2q\epsilon_s N_A(\phi_c + 2|\phi_f|)}}{C_0} + \left(1 + \frac{C_d}{C_0} + \frac{C_{fs}}{C_0}\right)(\psi_s - \phi_c - 2|\phi_f|)$$

or

$$\psi_s - \phi_c - 2|\phi_f| = \frac{1}{n}[V_G - V_T(\phi_c)]. \tag{31}$$

where

$$V_{FB} = \Phi_{MS} - \frac{Q_{SS}}{C_0} - \frac{Q_{fs0}}{C_0}$$

$$n = \frac{C_d + C_{fs} + C_0}{C_0}$$

and

$$V_T(\phi_c) = V_{FB} + \phi_c + 2|\phi_f| + \frac{\sqrt{2q\epsilon_s N_A(\phi_c + 2|\phi_f|)}}{C_0} \tag{32}$$

is the gate voltage when $\psi_s = \phi_c + 2|\phi_f|$. C_d and C_{fs} are given by (5).

Inserting (31) into (30) and evaluating the denominator at $\psi_s = \phi_c + 2|\phi_f|$ gives Q_n as a function of V_G in the weak inversion region.

$$-Q_n = C_d(kT/q)\exp q[V_G - V_T(\phi_c)]/nkT]. \tag{33}$$

When ψ_s is some small amount (several kT/q) greater than $\phi_c + 2|\phi_s|$ the exponential term in (28) dominates and the strong inversion criterion is satisfied. From (29) it is apparent that ψ_s varies logarithmically with V_G in the strong inversion region. As a first approximation it is assumed that ψ_s is pinned a small potential $\Delta\phi$ above $\phi_c + 2|\phi_f|$. In other words $\psi_s = 2|\phi_f| + \Delta\phi$ when the surface is strongly inverted. Equation (29) then yields, upon solving for Q_n,

$$-Q_n = C_0\left[V_G - V_T(\phi_c) - \left(1 + \frac{C_d}{C_0}\right)\Delta\phi\right]. \tag{34}$$

$\Delta\phi$ is found by assuming that the weak inversion equation (33) must be just tangent to the strong inversion equation (34). The point of tangency V_α is the dividing point above which (34) is valid and below which (33) is valid. Equating (33) and (34) and their derivatives

at V_α yields

$$\Delta\phi = \frac{1}{1 + \frac{C_d}{nC_0}} \frac{kT}{q} \left[\ln\left(\frac{nC_0}{C_d}\right) - 1 \right] \tag{35}$$

$$V_\alpha = V_T(\phi_c) + \left(1 + \frac{C_d}{C_0}\right) \Delta\phi + n(kT/q). \tag{36}$$

Equations (33)–(36) thus furnish an approximate description of the inversion layer charge in both the strong and weak inversion regions.

Usually a turn-on voltage $V'_T(\phi_c)$ is experimentally defined by extension of the linear portion (strong inversion) of the Q_n versus V_G relation to zero charge. From (34) this means that $V'_T(\phi_c) = V_T(\phi_c) + (1 + (C_d/C_0))\ \Delta\phi$. Substituting this relation for $V'_T(\phi_c)$ into (33)–(36) yields the following convenient equations

$$-Q_n = C_0\left(n\frac{kT}{q}\right) \exp\left[\frac{q}{nkT}\left(V_G - V'_T(\phi_c) - n\frac{kT}{q}\right)\right], \tag{37}$$

valid when $V_G \leq V'_T(\phi_c) + n(kT/q)$ and

$$-Q_n = C_0[V_G - V'_T(\phi_c)], \tag{38}$$

valid when $V_G \geq V'_T(\phi_c) + n(kT/q)$. Since $V'_T(\phi_c)$ differs only by a small constant from $V_T(\phi_c)$, no distinction is made between them in the text.

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Complementary Transistor–Transistor Logic (CT^2L)—An Approach to High-Speed Micropower Logic

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***Abstract*—A new approach to micropower integrated circuits has been developed and is called complementary transistor–transistor logic (CT^2L).[1] This logic combines the inherent low standby power of a complementary inverter with the high speed of the T^2L-type input. Results of the monolithic fabricated circuits are presented.**

Introduction

THE concept of using complementary (p-n-p and n-p-n) transistors in logic circuits was advanced by Baker,[2] for obtaining a maximum efficiency design. Some of the features of a circuit that uses complementary transistors at the output are the following.

1) Drive capabilities are excellent since the load is driven by a low-impedance source in both directions.

2) Both the high- and low-output voltages are clamped by the $V_{CE(sat)}$ of the transistors.

3) Fast switching speeds are inherent at low powers.

4) The circuit operates with only one power supply.

5) There is low standby power; i.e., when there is NO LOAD, the power dissipated is that of the base currents.

This paper describes the development of a new approach to micropower microelectronic digital circuits called complementary transistor–transistor logic (CT^2L). This logic combines the inherent low standby power and excellent drive capability of a complementary inverter with the high speed of the T^2L-type input. This new logic achieves high speeds (2 MHz) while maintaining very low worst case standby power (300 μW). Worst case standby power is for a "0" input and + 10 percent power-supply voltage.

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