First Encounter Workshop 1

What you will learn

- Setting up First Encounter environment
- Importing a design
- Using the Design Browser
- Learning floor planning
- Editing floor plan objects
- Running Amoeba Placement
- Running automatic clock tree synthesis
- Running Trial Route
- Viewing the design
- Extracting RC data
- Generating wire load models
- Generating simulation files
- Calculating delays and generating SDF file

Mouse and Keyboard Usage

Left Mouse Button
Click – Selects/Highlights an object.
Double Click – Opens the Object Attribute form.

Middle Mouse Button
Click-and-Drag – Pans the display.

Right Mouse Button
Click-and-Drag – Zooms in the display.

Editing a Floor Plan Object
Space Bar – Change focus on an object to be edited.

General Bind Keys

Key	Action	Description
q	Attribute	Display the object attribute form on selected object.
f	Fit Display	Zooms the display to fit the design area.
g	Group	Moves up the hierarchy on the highlighted Hinstance.
u	Ungroup	Moves down the hierarchy on the highlighted Hinstance.
v	View DB	View the attributes of highlighted object.
z	Zoom-in	Zooms in the display, 2x.
Z	Zoom-out	Zooms out the display, 2x.
Shift	Select	Allows multiple selections of objects.
Arrows	Pan	Pans the display in direction of arrow.
Delete	Ruler	Removes last ruler displayed.
Space Bar	Focus	Changes the focus of overlapping objects

Auto Query Bind Keys

Key	Action	Description
n	Focus	Changes the focus of overlapping objects.
p	Focus	Changes the focus of previous overlapping object.

Edit Special Route form Bind Keys

Key + Mouse Button	Action	Description
Shift + Left button	End	Ends the drawing mode for creating special route.
Delete	Delete	Removes last point/segment.
Arrows	Moves	Moves the current segment in direction of arrow.
w	Warp	Allows drawing pencil to move freely.

1. CHECKING AND SETTING THE ENVIRONMENT

The following are the instructions to use the 'train' example design to learn the First Encounter (FE) design tool. You need to find the installed directory to get access to the sample design. It is located in the 'gift/tutorial' directory.

Checklist:

a. Locate the Encounter install directory.
b. Create a work directory to run the sample design.

1) Set the following environment variables:

```
setenv ENCOUNTER <install_directory>
set path=($ENCOUNTER/tools.sun4v/fe/bin $path)
setenv LM_LICENSE_FILE                    \
<install_directory>/share/fe/<cdslmd_lic>
setenv DISPLAY <your_local_machine>:0.0
```

Note 1: The '`tools.sun4v`' depends on the workstation platform and `tools.sun4v` is for Solaris 6, `tools.hppa` is for HPUX 11.0, and `tools.lnx86` is for Red Hat Linux 7.2 & 7.3.

2) Copy all the contents (files and directories) from the 'fe/gift/tutorial/' directory to your work directory. Use the UNIX commands
`mkdir <directory_name>` and
`cd <directory_name>` and
`cp –r $ENCOUNTER/share/fe/gift/tutorial/* .`

2. TESTCASE INFORMATION

The testcase contains almost 60,000 instances, 188 IOs, and about 71,700 nets. The netlist format is hierarchical Verilog and the process has 3 layers of metal. It has one clock source, MCK.

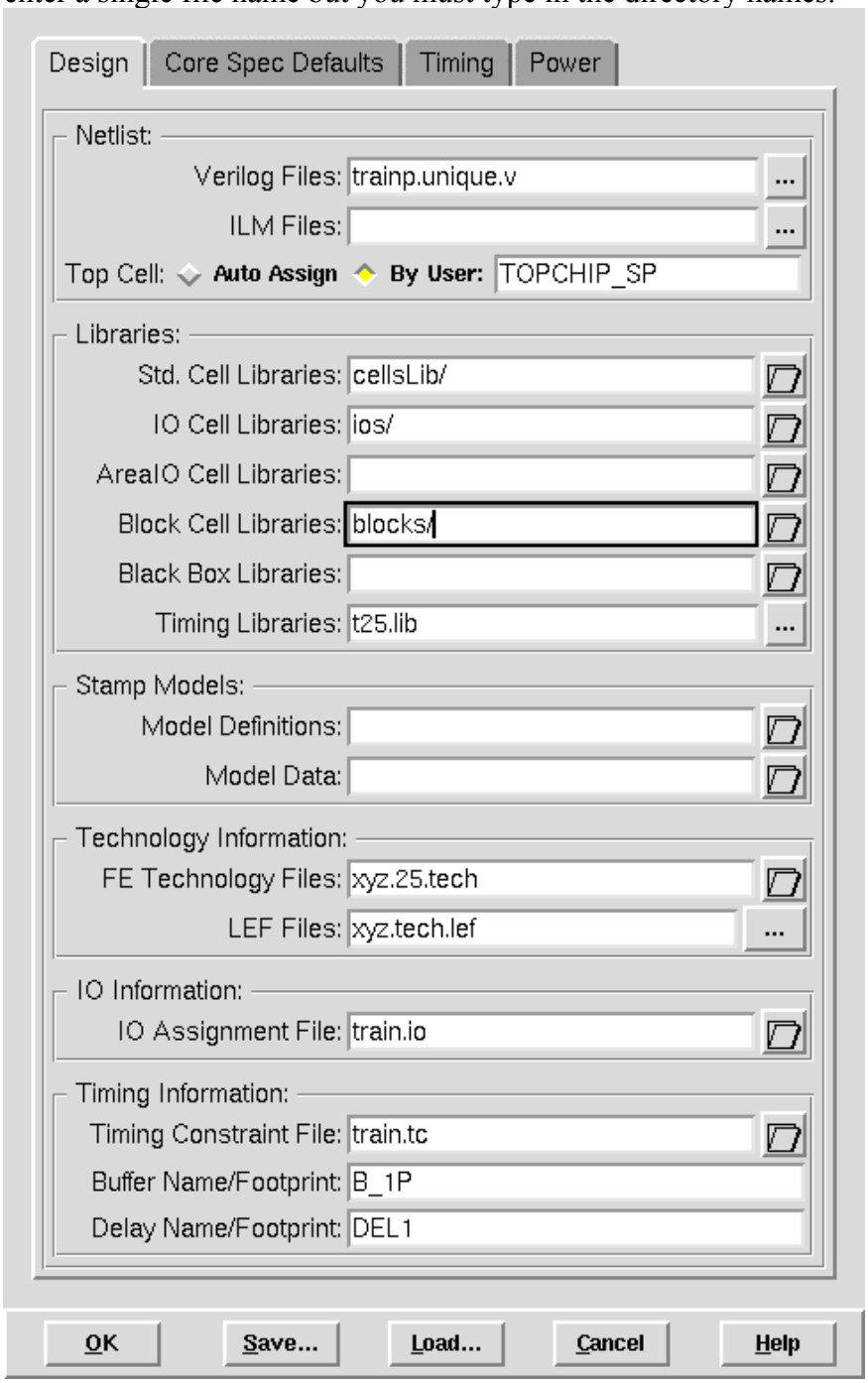
3. START A FIRST ENCOUNTER SESSION

In your work directory, type `encounter` and the First Encounter Tool displays. If not, type the UNIX command, `which encounter` to see if the path has been set properly.

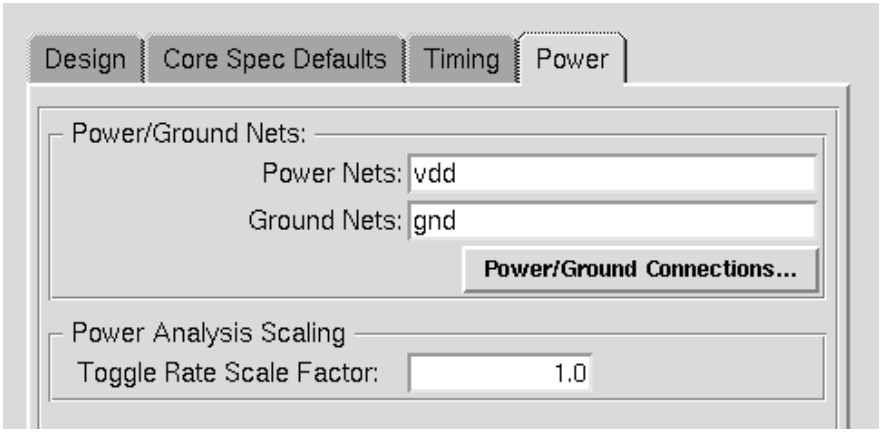
4. IMPORTING THE DESIGN

This first portion of the workshop should take you about 45 Minutes.

Design Import - Open the *Design Import* form (*Design -> Design Import…*) and complete the *Design* form as shown below. Remember that you can use the file widget to enter a single file name but you must type in the directory names.



Next, click the *Power* tab and enter `vdd` in the *Power Nets* text box and `gnd` in the *Ground Nets* text box, as shown below.



If you want, you can click the *Load* button. Select `train.conf` to set up the form's configuration to import the design and click the *Open* button to load the form.
Click on the *Core Spec Default* tab of the Design Import form just to see the default values. Click the *Ok* button to import the design.

Specifying chip size - Open the *FloorPlan -> Specify Floor Plan…*form and use the default setting for *Core Size by*: *Aspect Ratio*:. Next, under the selection of *Core Margins by*: *Core to IO Boundary,* enter `100` for *Core to Left*, *Core to Right*, *Core to Top*, and *Core to Bottom*. Click *OK* to move the IO pads 100 Microns from the outside edge of the core box and this sets the IO box. Now the die box size is set by the height of the IO pad instances.

Viewing the design - What are the pink colored objects and what are the green-grayish colored objects? Double click on several objects to see names and properties of the design objects. The pink objects are the top-level hierarchical instance module guides and the green-grayish objects are all the block (hard macro) guides. The pink guides represent the design modules of the imported netlist and note that the size of the module guides relate to the design size of each module.

Next, select module `SH17`. Now use the `u`-key (ungroup) to graphically move down the hierarchy and note that SH17 is peeled away from its location in the chip display area. Successive `u`-keys will peel another layer of hierarchy. To re-group the hierarchy, use the `g`-key (be sure one of the child modules or blocks is selected). Remember that the ungrouping and re-grouping can be done in the *Amoeba view* also. This is of course after running the Amoeba Placement program.

Note the blue flylines, which display fanout connection between each design module guide and block. Also, note the highlighted blocks (darker green and yellow outline). These blocks are child blocks of the selected module. If you click the *Net* button in the *Colors Tool* area, this will not display the blue flylines enabling you to see the child blocks easily.

Design Browser - Open the *Utility -> Design Browser…*to view the hierarchical design that was imported. Highlight `SH17`, the largest module. How many cells does it contain? Double click on `SH17` to push down into its submodules. Double click on the minus sign in front of Attribute to view SH17's properties. You can do the same to ' - Terms' to view the 376 terminals.

You can double click on the instance names and move down the hierarchy until either the primitive cell or design block is reached.

If you want to find or highlight a net name, notice the stepper button that shows *Instance*. To find a net, just enter the net name and change the stepper selection to *Net* or a <`CR`> will also work. We will do this exercise soon.

5. LEARNING FLOOR PLANNING

Slowly position the cursor over each of the *Floor Plan Tools* buttons to display what they are. Now click on the *Move* tool so you can start moving a module guide into the core design area. You use the *Reshape/resize* to reshape (with `Shift` key) or resize an object.

Now move blocks into the core area. Then create floor plan objects such as *Placement Blockages* and *Density Screens*. Now double click on several of these created objects to view their properties or use the `q`-key after highlighting the object. This form allows you to change their properties and save the changes. Change the *Area Density* value of a Density Screen object.

There are several ways you can remove the objects from your current *Floor Plan view*; 1) move them outside of the design area box, 2) use the *FloorPlan -> Clear Floor Plan…* form that has several clearing options and categories.

Designing power and ground rings around the core design area or around a block(s) can be done by using the *FloorPlan -> Power Planning -> Add Rings…* form, and the *FloorPlan -> Power Planning -> Add Stripes…* forms is used to design power and ground stripes.

First, move several blocks into the core design area, highlight them and add power/ground rings around them. You can also design power/ground stripes. If you zoom-in, you can see the vias.

You can also interactively create stripes by using the *FloorPlan -> Power Planning -> Edit Special Route* form. Also, this form is used to edit existing power/ground routes. Selecting the Pencil button allows the drawing of special route(s) and the combination of the `Shift`-key plus the *Left Mouse* button ends the drawing.

Now, pre-place a standard cell using the Design Brower. First, open the *Browser* and enter `SH11/I87/SH2/I38/I13` in the text entry box followed by a <CR>. It is a standard cell of cell type FD1. Click the *Attribute* button (text page with an arrow) to open the *Attribute* form for the instance. To pre-place this instance, 1) click the *get coord* button to pre-place the instance in the core design area and 2) select the *Preplaced* option. After clicking *Ok*, can you see the pre-placed standard cell? Double click the standard cell to see its connection flylines. Remember that you can pre-place a module, block, or standard cell using the Design Brower.

Now save your floor plan to file in '`fp`' format and the floor plan file is one of the most important files for FE.

6. LOAD-IN THE DESIGN'S FLOOR PLAN AND RUN PLACEMENT

This portion of the workshop should go faster since the computer is going to do most of the work and less experimenting. Plan on 35 Minutes for this portion.

First, clear the core design area of all floor plan objects.

Load Floor Plan - Open the *FloorPlan -> Load Floor Plan -> FP…* form. Select the file `train.fp` and click the *Open* button. Now several module guides and blocks are pre-placed and a few other objects have appeared.

Edit Two Module Guides to prepare for Clock Tree synthesis – Two module guides need to have the standard cell placement utilization reduced. First open the Design Browser to find clock net `MPCLK`. Note that the clock net is in 2 modules, `SH27` and `SH28` and the clock output pin are from block `SH28/I62/SH2/I42`. Given this information, now change the 2 modules' placement density to 70%. This is done by double-clicking each guide, `SH27` and `SH28`, and change the *Placement Density* to `70.0`.
Note that if you save the floor plan at this point, the saved floor plan file will contain these 2 module density constraints changes.

Run Amoeba Placement - Open the *Place -> Place…* form. Now, click the *Ok* button (use the default *Medium Effort*. The normal runtime is about 7 minutes.

Viewing the Design after Placement - Once the placement program is done, you can view the placed design in the *Placement* and *Amoeba* views.

Open the *FloorPlan -> Generate Floor Plan Guide…* form from the menu. Click the *Ok* button. Now you are going to view how the placement program placed all the remaining module guides and blocks that were not pre-placed during floor planning.

7. RUN CLOCK TREE SYNTHESIS

Clock Specification file - After running placement, Clock Tree Synthesis can be run but a clock specification file is needed. Look at the file `train.cts.auto`. The clock output leaf pin name is `SH28/I62/SH2/I42/MPCLK`. If you have more internal clocks, you just add its information to the specification file.

Run Clock Tree Synthesis - Open the *Clock -> Synthesis Clock Tree…* form and select the clock specification file, `train.cts.auto`. To display the clock tree, select *Display Clock Tree* form item. Click *Ok* to run synthesis. Note the multi-color instances, which represent its delay in the clock path. Also, a report is generated. To clear the display, use the *Clock -> Clear Clock Tree Display* menu item.

8. RUN TRIAL ROUTE AND SAVING THE DESIGN

Run Trial Route - Open the *Route -> Trial Route…* form. Click the *Ok* button when ready. No option is to be selected. Or instead, you can type the First Encounter (FE) command, `trialRoute`, in the SPC console window to run Trial Route.

Once trial route completes, there are two things to look for. First, a visual view of route congestion. This is done looking for the red color diamond shapes. Now zoom-in to view the congestion displayed. There are two sets of numbers. The first set (#-top/#-bottom) is for the vertical connection where #-top is the required routes and #-bottom is the available routes. The second set of numbers is for the horizontal connections. These diamond shaped congestion locators represent an average in the area.

If you want to display congestion bars, select *Hcongest* and *Vcongest* in the *Colors Tool* area. The colors for the route congestion overflow bars are:

Color Bar	Overflow
Blue	>0 – 0.999
Green	1.0 – 1.999
Yellow	2.0 – 2.999
Red	3.0 – 3.999
Magenta	4.0 – 4.999
Grey to White	>5.0

Second, view the log file or the SPC console for the congestion table produced by Trial Route. The label of the table is *Congestion distribution*:. Just before this table, look for the last line with label *Overflow*:. If both numbers in the (#% H) and (#% V) are less than 0.5%, then this design is good for any detail router. The less than 0.5% is good for

three (3) layers of metal and less than 1.0% is usually good for five (5) or more layers of metal.

Save the Design - It is a good idea at this point to save everything you have done in the First Encounter tool. Open the *Design -> Save Design..* form. Enter your own archive file name or use the default and click the *Save* button when ready. Now you can restore your work in a future First Encounter session. Note that no netlist file is saved unless the imported design was changed by First Encounter.

Viewing the Design after Trial Route – You can see connection flylines in the *Floor Plan view*, but in the *Amoeba view*, the routed interconnections can be displayed. This is done by double clicking a module or block (this also opens the Attribute form). More interestingly, this double clicking can be used in the *Placement view*. The actual routed interconnect for specific nets can be viewed. You must zoom way in to see the connections.

Use the *Design Browser* to highlight net `SH17/I350_Q`. This is done by first typing in the net name, then a <CR>. Highlight the net by click the *magnifier* button. Next, use *View -> Zoom Selected* menu item to zoom-in to this net.

You can also highlight in reverse with the *Design Browser*. First, highlight a net in the design display area, and then in the *Design Browser*, click the *Get Selected* button (button with several rectangles), and now the name of the selected object's name is displayed.

Viewing Different Objects – You can open the Color area -> *More -> Color Preference* form to see all the objects in First Encounter. The displaying of these objects can be turned off or on and the color selection can be changed to suit your convention.

9. EXTRACT RC DATA AND GENERATE WIRE LOAD MODELS

Setting Timing Models – In the timing library that was read in during design import, there are temperature, process, and voltage conditions that are modeled. Open the *Timing -> Specify Operating Condition…* form and select *Typical*.

Extract RC Data - To extract the capacitance for the design, open the *Timing -> Extract RC…* form. Since it will take time to generate and write files over the network, select formats of interests and generate the simulation files. The files are written to your work directory. Now, you can examine them.

Generate Wire Load Model - To generate the wire load models at every level of the hierarchy, open the *Timing -> Generate Wireload Model…* form. Select *Cell* or *Instance Based* and *click* the *Ok* button. There are 4 wireload files created in your work directory, 2 data files `TOPCHIP_SP.wl.hier` and `TOPCHIP_SP.wl.flat` and 2 load script files `TOPCHIP_SP.wl.hier.scr` and `TOPCHIP_SP.wl.flat.scr`.

Calculate Delay – Next, delays are calculated for the interconnect wires and include instance delays. To do this, open the *Timing -> Calculation Delay…* form. To see what delay default is used for large nets, open the *Design -> Design Import's Timing& Power Defaults* page. Select the *Ideal Clock* option if you did not run clock tree synthesis. Click *Ok* when ready. A file in SDF format is created.

10. ON-LINE HELP

Getting Help – The User's Guide is available using Acrobat Reader. Click on the *Help* button in the First Encounter tool window. Also, the *Help* button in each form will direct the Reader to the proper page of the User's Guide.

Back to lecture 2.

FOR PEOPLE WHO DO NOT PLAN TO EXCERSIZE WORKSHOP 2 WHICH FEATURES PARTITIONING A DESIGN AND RUNNING IPO, DO NOT EXIT FIRST ENCOUNTER. YOU CAN CONTINUE LATER AND RUN IPO.

Run Timing Analysis and Generate Slack Report – Open the *Timing -> Timing Analysis* form and run the default *Setup Time Analysis* by clicking *OK*. When done, view the slack report by using the *Timing -> Slack Brower…* to open the slack report file, `TOPCHIP_SP.slk.`

Running IPO – Open the *Timing -> In-Place Optimization…* form and use the form's default setting:

- Effort Level: *Medium*
- Fix Tran/Cap: *Only Critical Paths*
- Add Ports: *As Needed* and
- Route Mode: *Keep Updated.*

Now, click *Ok* to run IPO.

When IPO is done, view the slack report, `TOPCHIP_SP_ipo/TOPCHIP_SP_ipo.slk` to see how much timing improvement was made. In Workshop 2, timing closure by running IPO is achieved.