ISE 10.1 Quick Start Tutorial

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Preface

About This Tutorial

The ISE 10.1 Quick Start Tutorial is a hands-on learning tool for new users of the ISE software and for users who wish to refresh their knowledge of the software. The tutorial demonstrates basic set-up and design methods available in the PC version of the ISE software. By the end of the tutorial, you will have a greater understanding of how to implement your own design flow using the ISE 10.1 software.

Additional Resources

To find additional documentation, see the Xilinx website at:

http://www.xilinx.com/literature.

To search the Answer Database of silicon, software, and IP questions and answers, or to create a technical support WebCase, see the Xilinx website at:

http://www.xilinx.com/support.

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ISE 10.1 Quick Start Tutorial

The ISE 10.1 Quick Start Tutorial provides Xilinx PLD designers with a quick overview of the basic design process using ISE 10.1. After you have completed the tutorial, you will have an understanding of how to create, verify, and implement a design.

Note: This tutorial is designed for ISE 10.1 on Windows.

This tutorial contains the following sections:

- "Getting Started"
- "Create a New Project"
- "Create an HDL Source"
- "Design Simulation"
- "Create Timing Constraints"
- "Implement Design and Verify Constraints"
- "Reimplement Design and Verify Pin Locations"
- "Download Design to the Spartan™-3 Demo Board"

For an in-depth explanation of the ISE design tools, see the ISE In-Depth Tutorial on the Xilinx® web site at: http://www.xilinx.com/support/techsup/tutorials/

Getting Started

Software Requirements

To use this tutorial, you must install the following software:

- ISE 10.1

  For more information about installing Xilinx® software, see the *ISE Release Notes and Installation Guide* at: http://www.xilinx.com/support/software_manuals.htm.

Hardware Requirements

To use this tutorial, you must have the following hardware:

- Spartan-3 Startup Kit, containing the Spartan-3 Startup Kit Demo Board

Starting the ISE Software

To start ISE, double-click the desktop icon,

or start ISE from the Start menu by selecting:

Start → **All Programs** → **Xilinx ISE 10.1**→ **Project Navigator**

Note: Your start-up path is set during the installation process and may differ from the one above.

Accessing Help

At any time during the tutorial, you can access online help for additional information about the ISE software and related tools.

To open Help, do either of the following:

- Press **F1** to view Help for the specific tool or function that you have selected or highlighted.
- Launch the **ISE Help Contents** from the Help menu. It contains information about creating and maintaining your complete design flow in ISE.

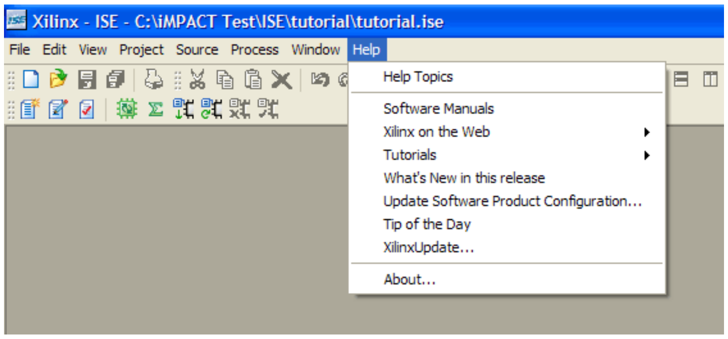


Figure 1: **ISE Help Topics**

Create a New Project

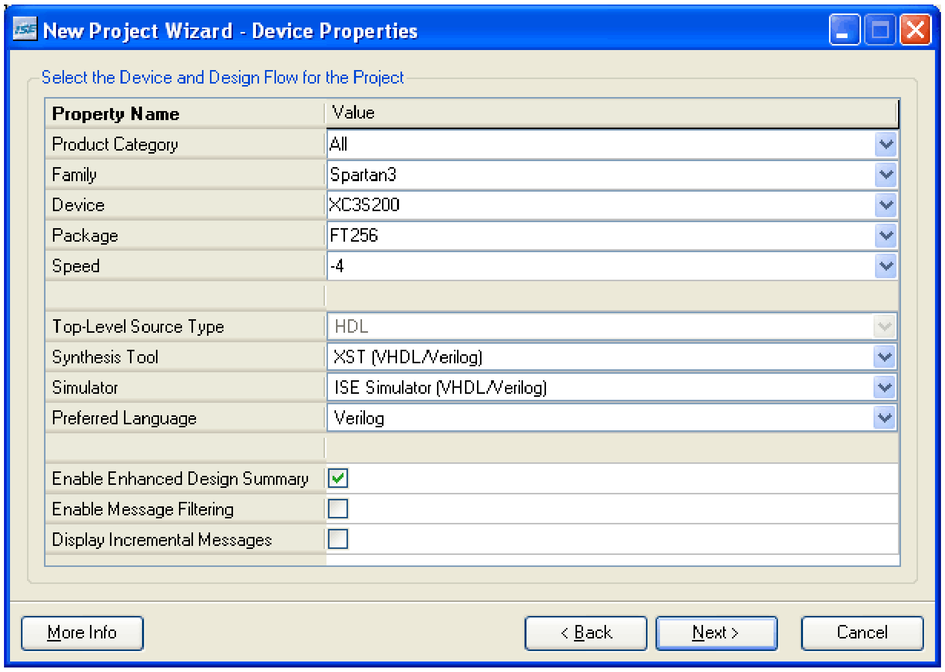
Create a new ISE project which will target the FPGA device on the Spartan-3 Startup Kit demo board.

To create a new project:

1. Select **File** > **New Project...** The New Project Wizard appears.
2. Type **tutorial** in the Project Name field.
3. Enter or browse to a location (directory path) for the new project. A tutorial subdirectory is created automatically.
4. Verify that **HDL** is selected from the Top-Level Source Type list.
5. Click **Next** to move to the device properties page.
6. Fill in the properties in the table as shown below:
   - Product Category: **All**
   - Family: **Spartan3**
   - Device: **XC3S200**
   - Package: **FT256**
   - Speed Grade: **-4**
   - Top-Level Source Type: **HDL**
   - Synthesis Tool: **XST (VHDL/Verilog)**
   - Simulator: **ISE Simulator (VHDL/Verilog)**
   - Preferred Language: **Verilog** (or **VHDL**)
   - Verify that **Enable Enhanced Design Summary** is selected.

   Leave the default values in the remaining fields.

   When the table is complete, your project properties will look like the following:


New Project Wizard - Device Properties
Select the Device and Design Flow for the Project
More Info
< Back
Next >
Cancel

Property Name	Value
Product Category	All
Family	Spartan3
Device	XC3S200
Package	FT256
Speed	-4
Top-Level Source Type	HDL
Synthesis Tool	XST (VHDL/Verilog)
Simulator	ISE Simulator (VHDL/Verilog)
Preferred Language	Verilog
Enable Enhanced Design Summary	✓
Enable Message Filtering	☐
Display Incremental Messages	☐

Figure 2: **Project Device Properties**

7. Click **Next** to proceed to the Create New Source window in the New Project Wizard. At the end of the next section, your new project will be complete.

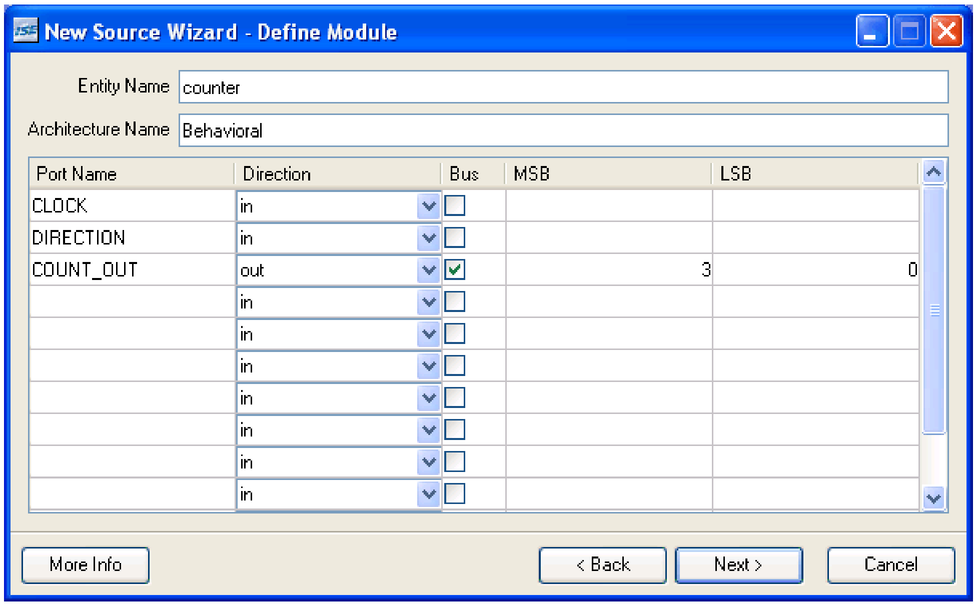
Create an HDL Source

In this section, you will create the top-level HDL file for your design. Determine the language that you wish to use for the tutorial. Then, continue either to the "Creating a VHDL Source" section below, or skip to the "Creating a Verilog Source" section.

Creating a VHDL Source

Create a VHDL source file for the project as follows:

1. Click the **New Source** button in the New Project Wizard.
2. Select **VHDL Module** as the source type.
3. Type in the file name **counter**.
4. Verify that the **Add to project** checkbox is selected.
5. Click **Next**.
6. Declare the ports for the counter design by filling in the port information as shown below:



Entity Name: counter

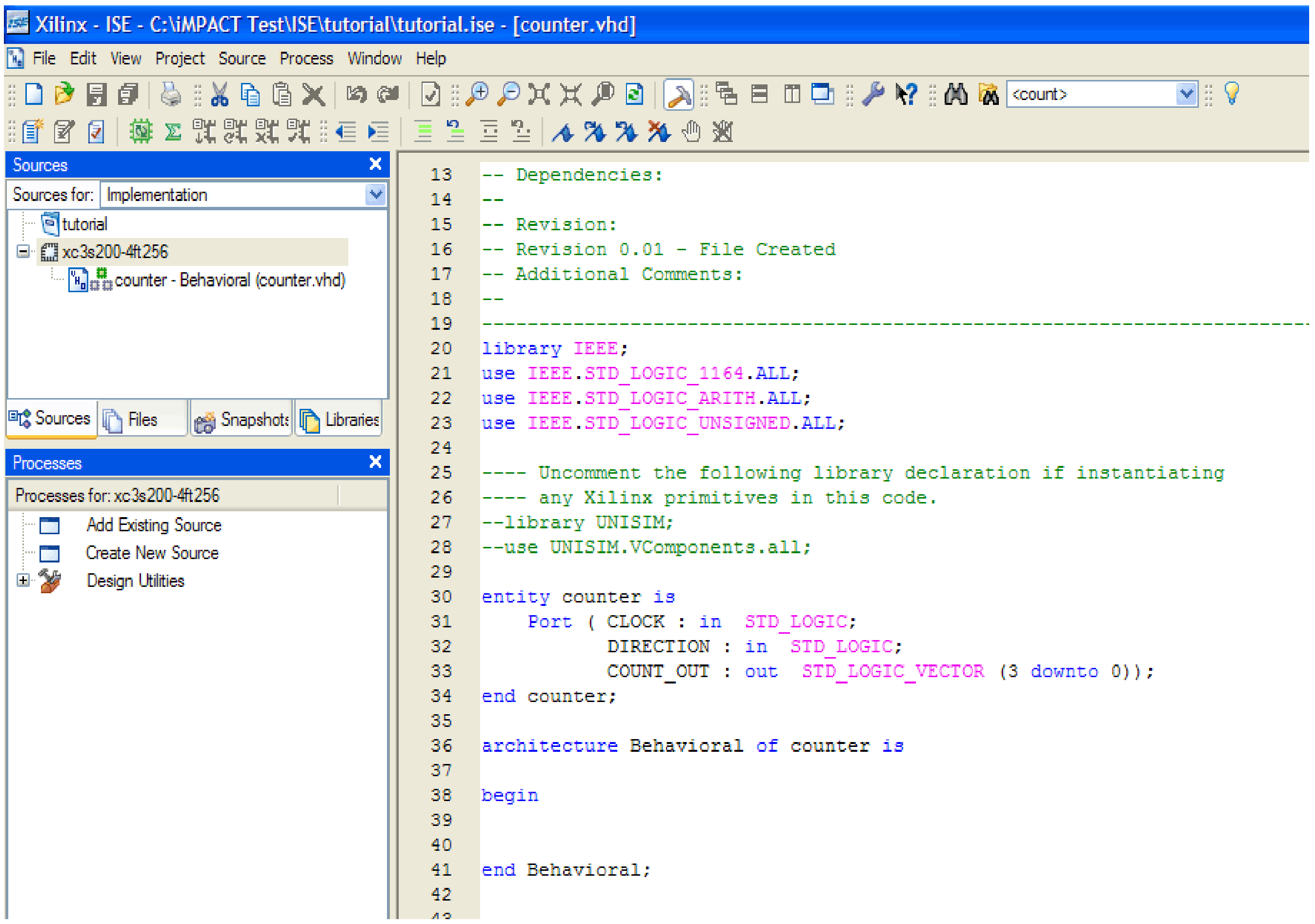
Architecture Name: Behavioral

Port Name	Direction	Bus	MSB	LSB
CLOCK	in	☐		
DIRECTION	in	☐		
COUNT_OUT	out	✓	3	0
	in	☐		
	in	☐		
	in	☐		
	in	☐		
	in	☐		
	in	☐		
	in	☐		

Figure 3: **Define Module**

7. Click **Next**, then **Finish** in the New Source Wizard - Summary dialog box to complete the new source file template.
8. Click **Next**, then **Next**, then **Finish**.

The source file containing the entity/architecture pair displays in the Workspace, and the counter displays in the Source tab, as shown below:


Xilinx - ISE - C:\iMPACT Test\ISE\tutorial\tutorial.ise - [counter.vhd]
File Edit View Project Source Process Window Help
<count>
Sources
Sources for: Implementation
tutorial
xc3s200-4ft256
counter - Behavioral (counter.vhd)
Sources Files Snapshots Libraries
Processes
Processes for: xc3s200-4ft256
Add Existing Source
Create New Source
Design Utilities

```
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

---- Uncomment the following library declaration if instantiating
---- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity counter is
    Port ( CLOCK : in  STD_LOGIC;
           DIRECTION : in  STD_LOGIC;
           COUNT_OUT : out  STD_LOGIC_VECTOR (3 downto 0));
end counter;

architecture Behavioral of counter is

begin


end Behavioral;
```

Figure 4: **New Project in ISE**

Using Language Templates (VHDL)

The next step in creating the new source is to add the behavioral description for the counter. To do this you will use a simple counter code example from the ISE Language Templates and customize it for the counter design.

1. Place the cursor just below the begin statement within the counter architecture.
2. Open the Language Templates by selecting **Edit** → **Language Templates…**

   Note: You can tile the Language Templates and the counter file by selecting **Window** → **Tile Vertically** to make them both visible.
3. Using the "**+**" symbol, browse to the following code example:

   VHDL → **Synthesis Constructs** → **Coding Examples** → **Counters** → **Binary** → **Up/Down Counters** → **Simple Counter**
4. With Simple Counter selected, select **Edit** → **Use in File**, or select the **Use Template in File** toolbar button. This step copies the template into the counter source file.

5. Close the Language Templates.

Final Editing of the VHDL Source

1. Add the following signal declaration to handle the feedback of the counter output below the architecture declaration and above the first begin statement:

   ```
   signal count_int : std_logic_vector(3 downto 0) := "0000";
   ```

2. Customize the source file for the counter design by replacing the port and signal name placeholders with the actual ones as follows:

   - replace all occurrences of `<clock>` with `CLOCK`
   - replace all occurrences of `<count_direction>` with `DIRECTION`
   - replace all occurrences of `<count>` with `count_int`

3. Add the following line below the end process; statement:

   ```
   COUNT_OUT <= count_int;
   ```

4. Save the file by selecting **File** → **Save**.

When you are finished, the counter source file will look like the following:

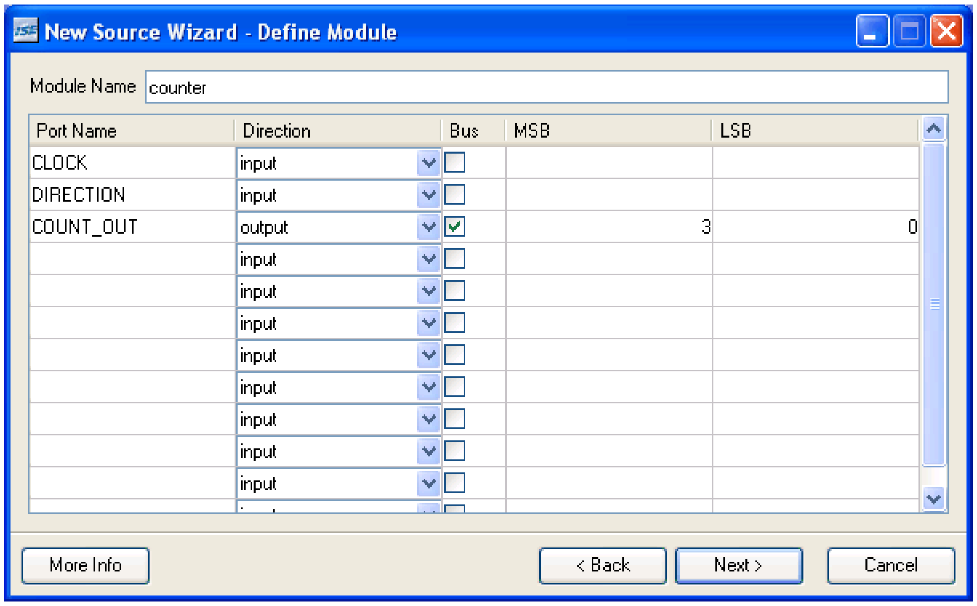
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx primitive in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity counter is
  Port ( CLOCK : in  STD_LOGIC;
    DIRECTION : in  STD_LOGIC;
    COUNT_OUT : out  STD_LOGIC_VECTOR (3 downto 0));
end counter;

architecture Behavioral of counter is
signal count_int : std_logic_vector(3 downto 0) := "0000";
begin
process (CLOCK)
begin
  if CLOCK='1' and CLOCK'event then
    if DIRECTION='1' then
      count_int <= count_int + 1;
    else
      count_int <= count_int - 1;
    end if;
  end if;
end process;
COUNT_OUT <= count_int;
end Behavioral;
```

You have now created the VHDL source for the tutorial project. Skip past the Verilog sections below, and proceed to the "Checking the Syntax of the New Counter Module"section.

Creating a Verilog Source

Create the top-level Verilog source file for the project as follows:

1. Click **New Source** in the New Project dialog box.
2. Select **Verilog Module** as the source type in the New Source dialog box.
3. Type in the file name **counter**.
4. Verify that the **Add to Project** checkbox is selected.
5. Click **Next**.
6. Declare the ports for the counter design by filling in the port information as shown below:



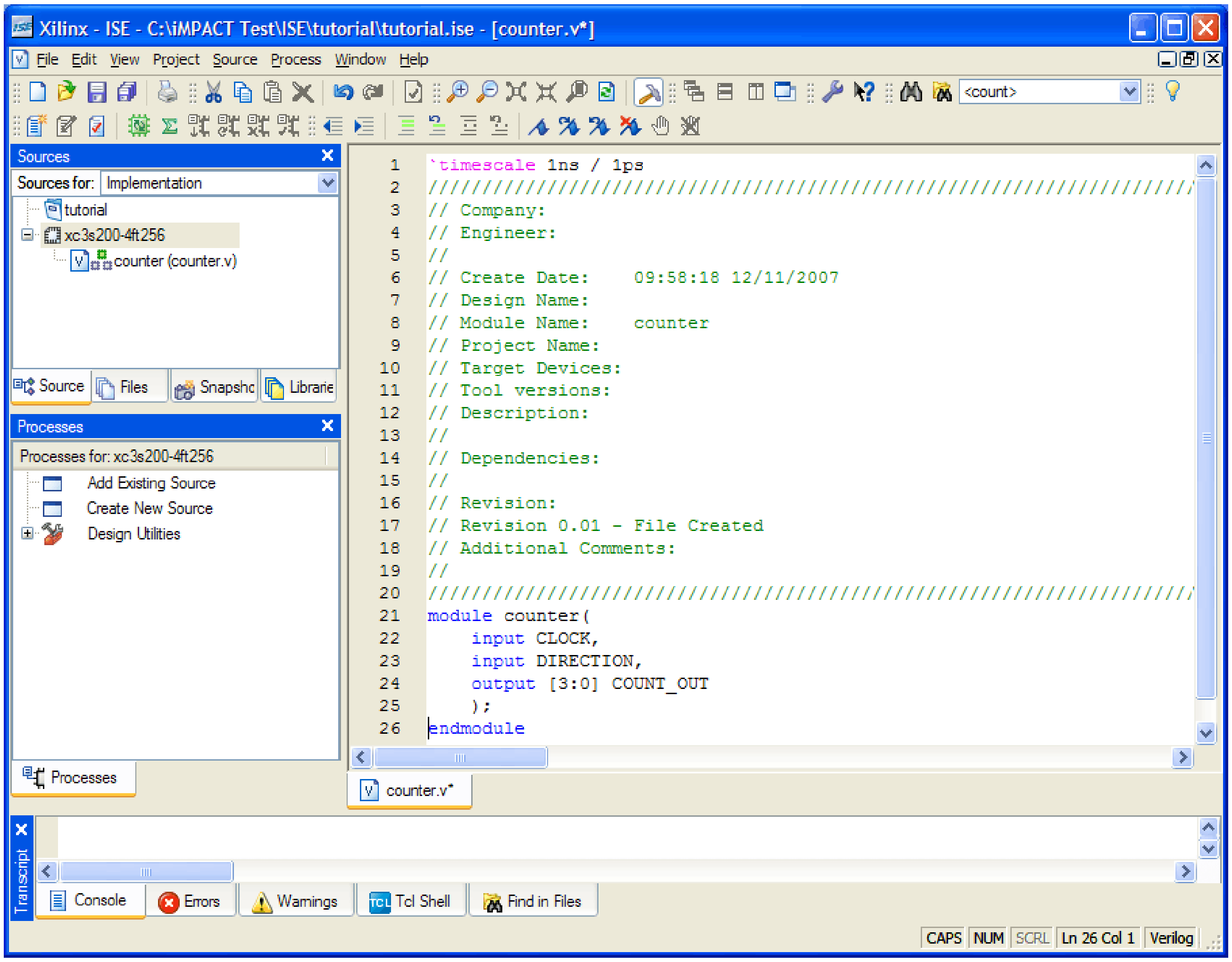
Module Name: counter

Port Name	Direction	Bus	MSB	LSB
CLOCK	input	☐		
DIRECTION	input	☐		
COUNT_OUT	output	✓	3	0
	input	☐		
	input	☐		
	input	☐		
	input	☐		
	input	☐		
	input	☐		
	input	☐		
	input	☐		

Figure 5: **Define Module**

7. Click **Next**, then **Finish** in the New Source Information dialog box to complete the new source file template.
8. Click **Next**, then **Next**, then **Finish**.

The source file containing the counter module displays in the Workspace, and the counter displays in the Sources tab, as shown below:



Xilinx - ISE - C:\iMPACT Test\ISE\tutorial\tutorial.ise - [counter.v*]
File Edit View Project Source Process Window Help
Sources
Sources for: Implementation
tutorial
xc3s200-4ft256
counter (counter.v)
Source
Files
Snapshc
Librarie
Processes
Processes for: xc3s200-4ft256
Add Existing Source
Create New Source
Design Utilities
Processes
counter.v*
Transcript
Console
Errors
Warnings
Tcl Shell
Find in Files
CAPS NUM SCRL Ln 26 Col 1 Verilog

```
`timescale 1ns / 1ps
////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date:    09:58:18 12/11/2007
// Design Name:
// Module Name:    counter
// Project Name:
// Target Devices:
// Tool versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
////////////////////////////////////////////////////////////////////////
module counter(
    input CLOCK,
    input DIRECTION,
    output [3:0] COUNT_OUT
    );
endmodule
```

Figure 6: **New Project in ISE**

Using Language Templates (Verilog)

The next step in creating the new source is to add the behavioral description for counter. Use a simple counter code example from the ISE Language Templates and customize it for the counter design.

1. Place the cursor on the line below the output [3:0] COUNT_OUT; statement.
2. Open the Language Templates by selecting **Edit** → **Language Templates…**

   Note: You can tile the Language Templates and the counter file by selecting **Window** → **Tile Vertically** to make them both visible.
3. Using the "**+**" symbol, browse to the following code example:

   Verilog → **Synthesis Constructs** → **Coding Examples** → **Counters** → **Binary** → **Up/Down Counters** → **Simple Counter**

4. With Simple Counter selected, select **Edit** → **Use in File**, or select the **Use Template in File** toolbar button. This step copies the template into the counter source file.

5. Close the Language Templates.

Final Editing of the Verilog Source

1. To declare and initialize the register that stores the counter value, modify the declaration statement in the first line of the template as follows:

   replace: `reg [<upper>:0] <reg_name>;`

   with: `reg [3:0] count_int = 0;`

2. Customize the template for the counter design by replacing the port and signal name placeholders with the actual ones as follows:

   - replace all occurrences of `<clock>` with `CLOCK`
   - replace all occurrences of `<up_down>` with `DIRECTION`
   - replace all occurrences of `<reg_name>` with `count_int`

3. Add the following line just above the endmodule statement to assign the register value to the output port:

   ```
   assign COUNT_OUT = count_int;
   ```

4. Save the file by selecting **File** → **Save**.

When you are finished, the code for the counter will look like the following:

```
module counter(CLOCK, DIRECTION, COUNT_OUT);
input CLOCK;
input DIRECTION;
output [3:0] COUNT_OUT;
);

reg [3:0] count_int = 0;
  always @(posedge CLOCK)
    if (DIRECTION)
      count_int <= count_int + 1;
    else
      count_int <= count_int - 1;

assign COUNT_OUT = count_int;
endmodule
```

You have now created the Verilog source for the tutorial project.

Checking the Syntax of the New Counter Module

When the source files are complete, check the syntax of the design to find errors and typos.

1. Verify that **Implementation** is selected from the drop-down list in the Sources window.

2. Select the **counter** design source in the Sources window to display the related processes in the Processes window.

3. Click the "**+**" next to the Synthesize-XST process to expand the process group.
4. Double-click the **Check Syntax** process.

   Note: You must correct any errors found in your source files. You can check for errors in the Console tab of the Transcript window. If you continue without valid syntax, you will not be able to simulate or synthesize your design.
5. Close the HDL file.

Design Simulation

Verifying Functionality using Behavioral Simulation

Create a test bench waveform containing input stimulus you can use to verify the functionality of the counter module. The test bench waveform is a graphical view of a test bench.

Create the test bench waveform as follows:

1. Select the **counter** HDL file in the Sources window.
2. Create a new test bench source by selecting **Project** → **New Source**.
3. In the New Source Wizard, select **Test Bench WaveForm** as the source type, and type **counter_tbw** in the File Name field.
4. Click **Next**.
5. The Associated Source page shows that you are associating the test bench waveform with the source file `counter`. Click **Next**.
6. The Summary page shows that the source will be added to the project, and it displays the source directory, type, and name. Click **Finish**.
7. You need to set the clock frequency, setup time and output delay times in the Initialize Timing dialog box before the test bench waveform editing window opens.

   The requirements for this design are the following:

   - The counter must operate correctly with an input clock frequency = 25 MHz.
   - The DIRECTION input will be valid 10 ns before the rising edge of CLOCK.
   - The output (COUNT_OUT) must be valid 10 ns after the rising edge of CLOCK.

   The design requirements correspond with the values below.

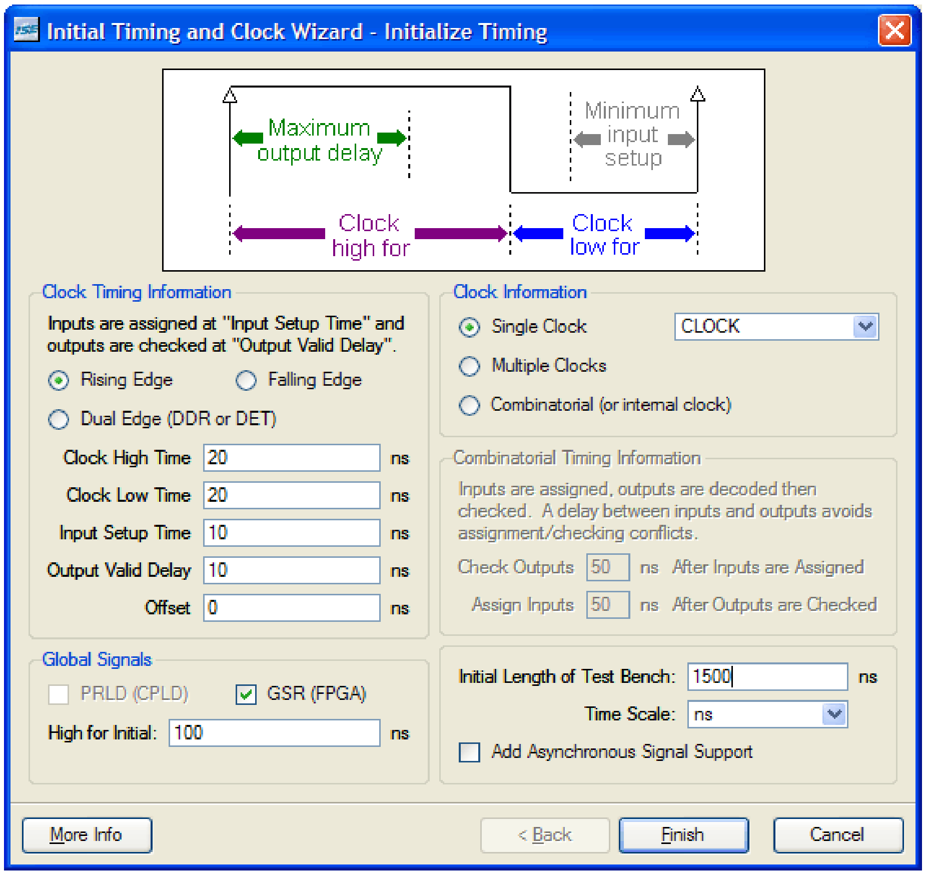
   Fill in the fields in the Initialize Timing dialog box with the following information:

   - Clock High Time: **20** ns.
   - Clock Low Time: **20** ns.
   - Input Setup Time: **10** ns.
   - Output Valid Delay: **10** ns.
   - Offset: **0** ns.
   - Global Signals: **GSR (FPGA)**

   Note: When GSR(FPGA) is enabled, 100 ns. is added to the Offset value automatically.

   - Initial Length of Test Bench: **1500** ns.

Leave the default values in the remaining fields.



Clock Timing Information

Inputs are assigned at "Input Setup Time" and outputs are checked at "Output Valid Delay".

[✓ Rising Edge] Falling Edge

Dual Edge (DDR or DET)

Clock High Time: 20 ns

Clock Low Time: 20 ns

Input Setup Time: 10 ns

Output Valid Delay: 10 ns

Offset: 0 ns

Clock Information

[✓ Single Clock] CLOCK

Multiple Clocks

Combinatorial (or internal clock)

Combinatorial Timing Information

Inputs are assigned, outputs are decoded then checked. A delay between inputs and outputs avoids assignment/checking conflicts.

Check Outputs 50 ns After Inputs are Assigned

Assign Inputs 50 ns After Outputs are Checked

Global Signals

PRLD (CPLD) [✓ GSR (FPGA)]

High for Initial: 100 ns

Initial Length of Test Bench: 1500 ns

Time Scale: ns

Add Asynchronous Signal Support

Figure 7: **Initialize Timing**

8. Click **Finish** to complete the timing initialization.
9. The blue shaded areas that precede the rising edge of the CLOCK correspond to the Input Setup Time in the Initialize Timing dialog box. Toggle the DIRECTION port to define the input stimulus for the counter design as follows:
   - Click on the blue cell at approximately the **300** ns to assert DIRECTION high so that the counter will count up.
   - Click on the blue cell at approximately the **900** ns to assert DIRECTION low so that the counter will count down.

Note: For more accurate alignment, you can use the **Zoom In** and **Zoom Out** toolbar buttons.

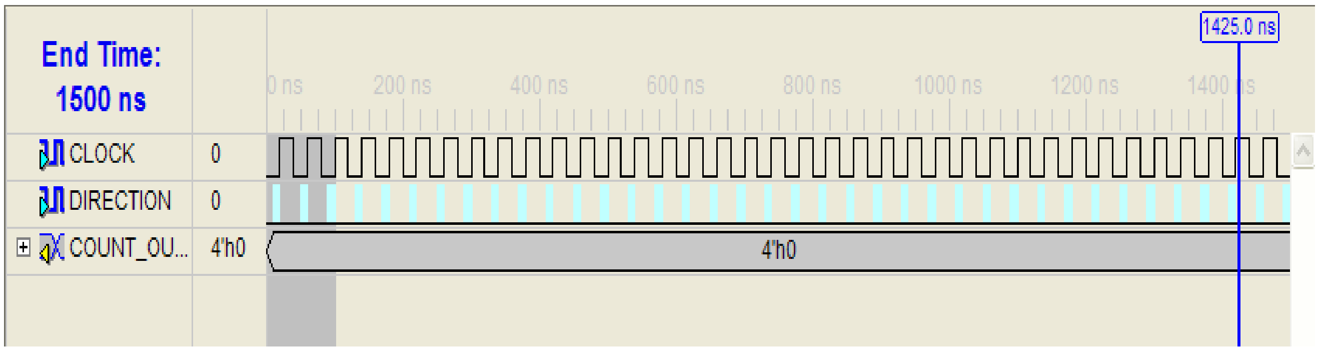


Figure 8: **Test Bench Waveform**

10. Save the waveform.
11. In the Sources window, select the **Behavioral Simulation** view to see that the test bench waveform file is automatically added to your project.

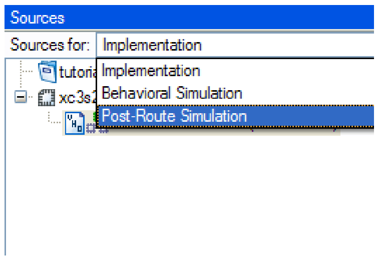


Figure 9: **Behavior Simulation Selection**

12. Close the test bench waveform.

Simulating Design Functionality

Verify that the counter design functions as you expect by performing behavior simulation as follows:

1. Verify that **Behavioral Simulation** and **counter_tbw** are selected in the Sources window.
2. In the **Processes** tab, click the “**+**” to expand the Xilinx ISE Simulator process and double-click the **Simulate Behavioral Model** process.

   The ISE Simulator opens and runs the simulation to the end of the test bench.
3. To view your simulation results, select the **Simulation** tab and zoom in on the transitions.

The simulation waveform results will look like the following:

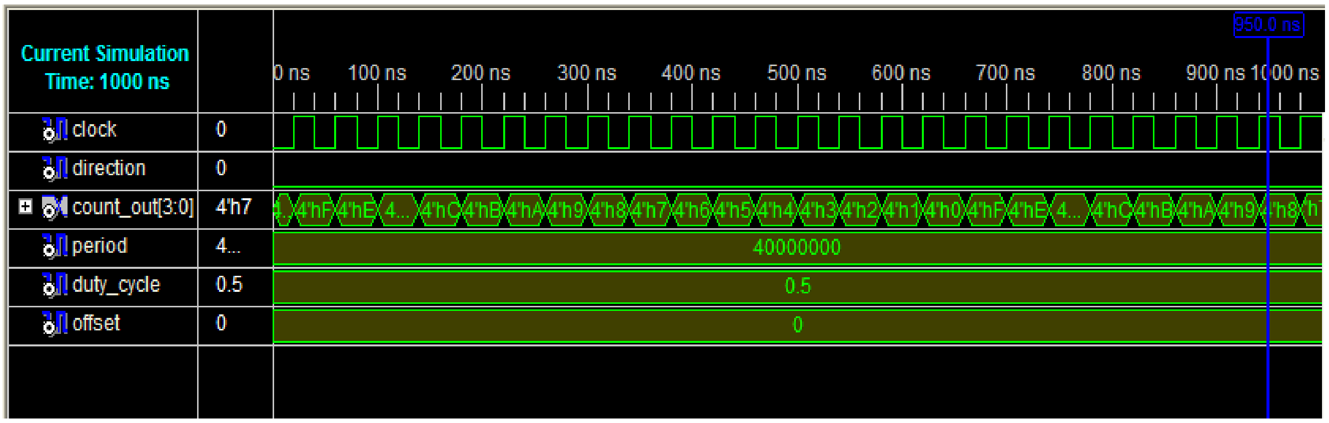

Current Simulation Time: 1000 ns
950.0 ns
0 ns
100 ns
200 ns
300 ns
400 ns
500 ns
600 ns
700 ns
800 ns
900 ns
1000 ns
clock
0
direction
0
count_out[3:0]
4'h7
4'hF 4'hE 4... 4'hC 4'hB 4'hA 4'h9 4'h8 4'h7 4'h6 4'h5 4'h4 4'h3 4'h2 4'h1 4'h0 4'hF 4'hE 4... 4'hC 4'hB 4'hA 4'h9 4'h8
period
4...
40000000
duty_cycle
0.5
0.5
offset
0
0

Figure 10: **Simulation Results**

Note: You can ignore any rows that start with **TX**.

4. Verify that the counter is counting up and down as expected.
5. Close the simulation view. If you are prompted with the following message, "You have an active simulation open. Are you sure you want to close it?", click **Yes** to continue.

You have now completed simulation of your design using the ISE Simulator.

Create Timing Constraints

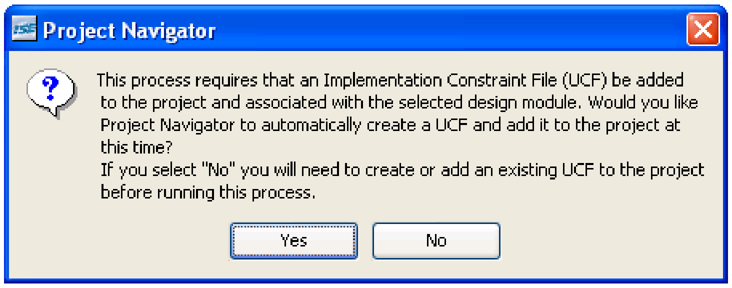
Specify the timing between the FPGA and its surrounding logic as well as the frequency the design must operate at internal to the FPGA. The timing is specified by entering constraints that guide the placement and routing of the design. It is recommended that you enter global constraints. The clock period constraint specifies the clock frequency at which your design must operate inside the FPGA. The offset constraints specify when to expect valid data at the FPGA inputs and when valid data will be available at the FPGA outputs.

Entering Timing Constraints

To constrain the design do the following:

1. Select **Implementation** from the drop-down list in the Sources window.
2. Select the **counter** HDL source file.
3. Click the "**+**" sign next to the User Constraints processes group, and double-click the **Create Timing Constraints** process.

   ISE runs the Synthesis and Translate steps and automatically creates a User Constraints File (UCF). You will be prompted with the following message:



Project Navigator

This process requires that an Implementation Constraint File (UCF) be added to the project and associated with the selected design module. Would you like Project Navigator to automatically create a UCF and add it to the project at this time?
If you select "No" you will need to create or add an existing UCF to the project before running this process.

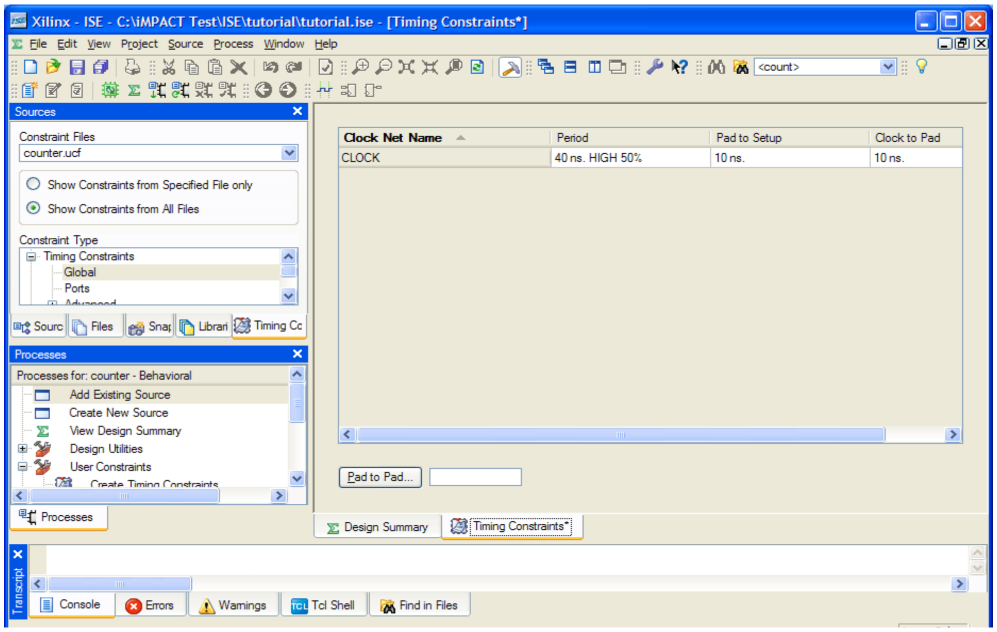
Figure 11: **Prompt to Add UCF File to Project**

4. Click **Yes** to add the UCF file to your project.

   The `counter.ucf` file is added to your project and is visible in the Sources window. The Xilinx Constraints Editor opens automatically.

   Note: You can also create a UCF file for your project by selecting **Project** → **Create New Source**.
5. In the Timing Constraints dialog, enter the following in the Period, Pad to Setup, and CLock to Pad fields:
   - **Period: 40**
   - **Pade to Setup: 10**
   - **Clock to Pad: 10**
6. Press **Enter**.

After the information has been entered, the dialog should look like what is shown below..



Xilinx - ISE - C:\iMPACT Test\ISE\tutorial\tutorial.ise - [Timing Constraints*]

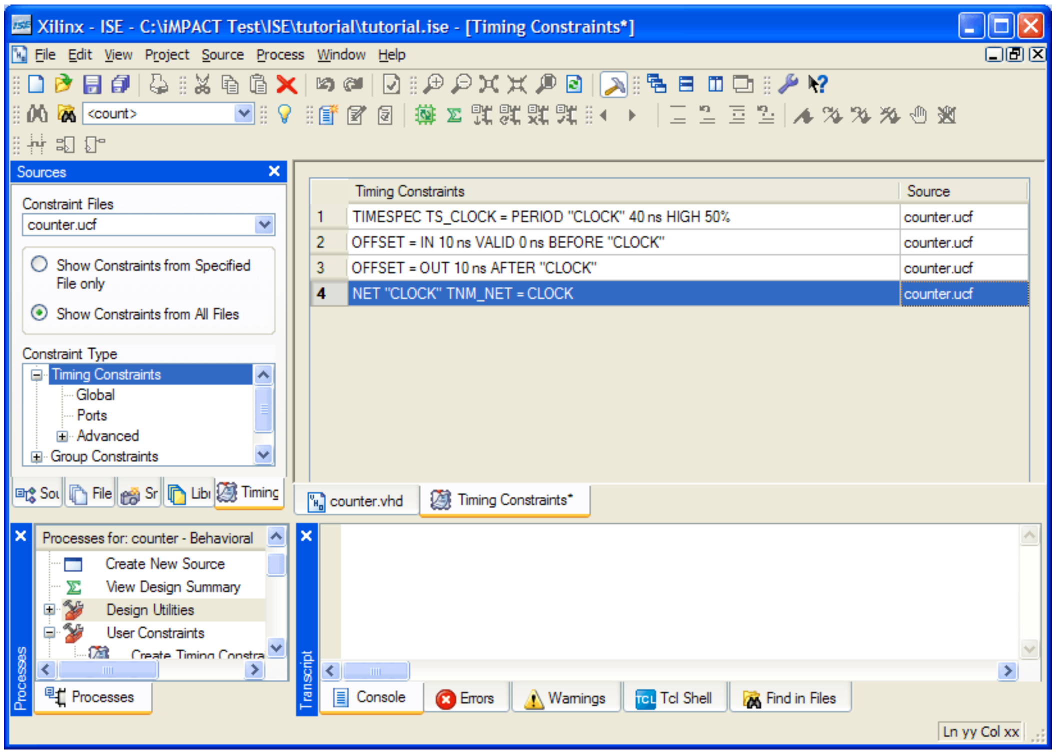
Constraint Files: counter.ucf

( ) Show Constraints from Specified File only
(●) Show Constraints from All Files

Clock Net Name	Period	Pad to Setup	Clock to Pad
CLOCK	40 ns. HIGH 50%	10 ns.	10 ns.

Figure 12: **Creating Timing Constraints**

7. Select **Timing Constraints** under Constraint Type in the Timing Constraints tab and the newly created timing constraints are displayed as follows:



Xilinx - ISE - C:\iMPACT Test\ISE\tutorial\tutorial.ise - [Timing Constraints*]

Constraint Files: counter.ucf

( ) Show Constraints from Specified File only
(●) Show Constraints from All Files

Constraint Type: Timing Constraints

	Timing Constraints	Source
1	TIMESPEC TS_CLOCK = PERIOD "CLOCK" 40 ns HIGH 50%	counter.ucf
2	OFFSET = IN 10 ns VALID 0 ns BEFORE "CLOCK"	counter.ucf
3	OFFSET = OUT 10 ns AFTER "CLOCK"	counter.ucf
4	NET "CLOCK" TNM_NET = CLOCK	counter.ucf

Figure 13: **Timing Constraints**

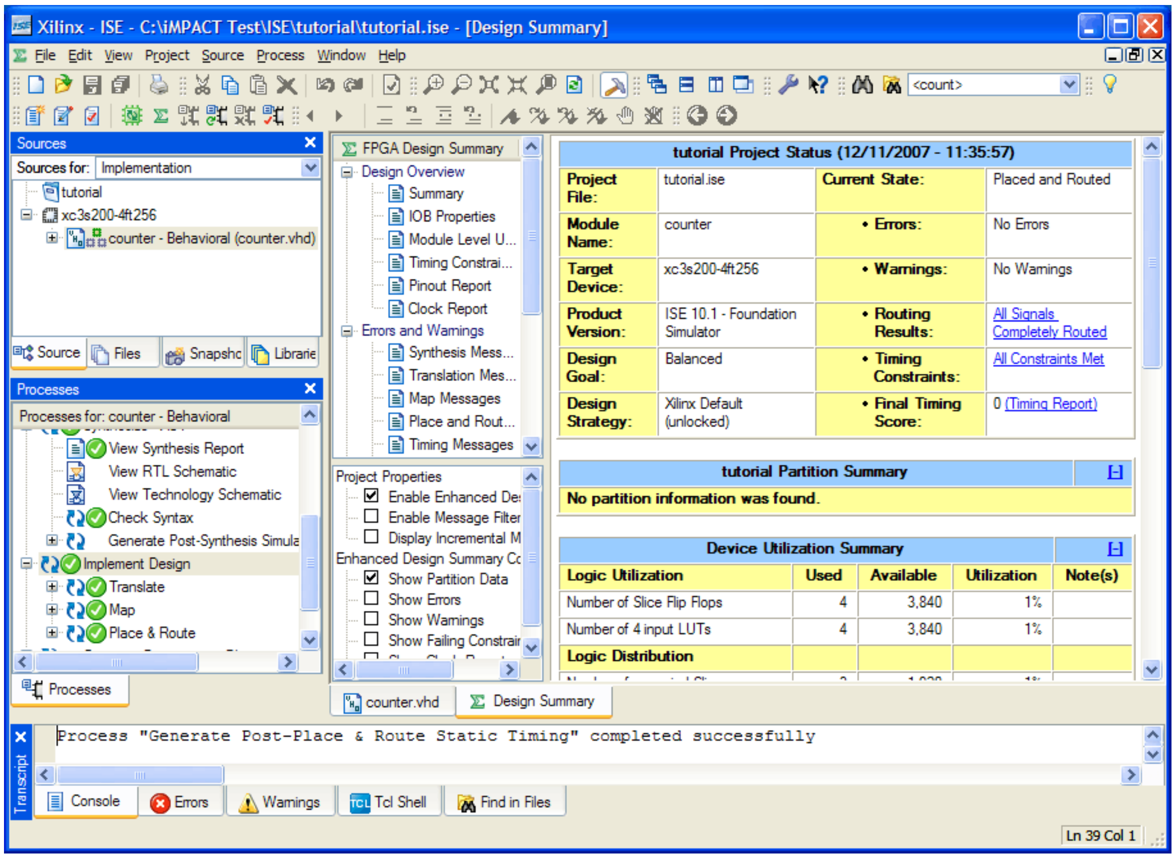
8. Save the timing constraints. If you are prompted to rerun the TRANSLATE or XST step, click **OK** to continue.
9. Close the Constraints Editor.

Implement Design and Verify Constraints

Implement the design and verify that it meets the timing constraints specified in the previous section.

Implementing the Design

1. Select the **counter** source file in the Sources window.
2. Open the Design Summary by double-clicking the **View Design Summary** process in the Processes tab.
3. Double-click the **Implement Design** process in the Processes tab.
4. Notice that after Implementation is complete, the Implementation processes have a green check mark next to them indicating that they completed successfully without Errors or Warnings.



tutorial Project Status (12/11/2007 - 11:35:57)

Project File:	tutorial.ise	**Current State:**	Placed and Routed
Module Name:	counter	• **Errors:**	No Errors
Target Device:	xc3s200-4ft256	• **Warnings:**	No Warnings
Product Version:	ISE 10.1 - Foundation Simulator	• **Routing Results:**	All Signals Completely Routed
Design Goal:	Balanced	• **Timing Constraints:**	All Constraints Met
Design Strategy:	Xilinx Default (unlocked)	• **Final Timing Score:**	0 (Timing Report)

tutorial Partition Summary

No partition information was found.

Device Utilization Summary

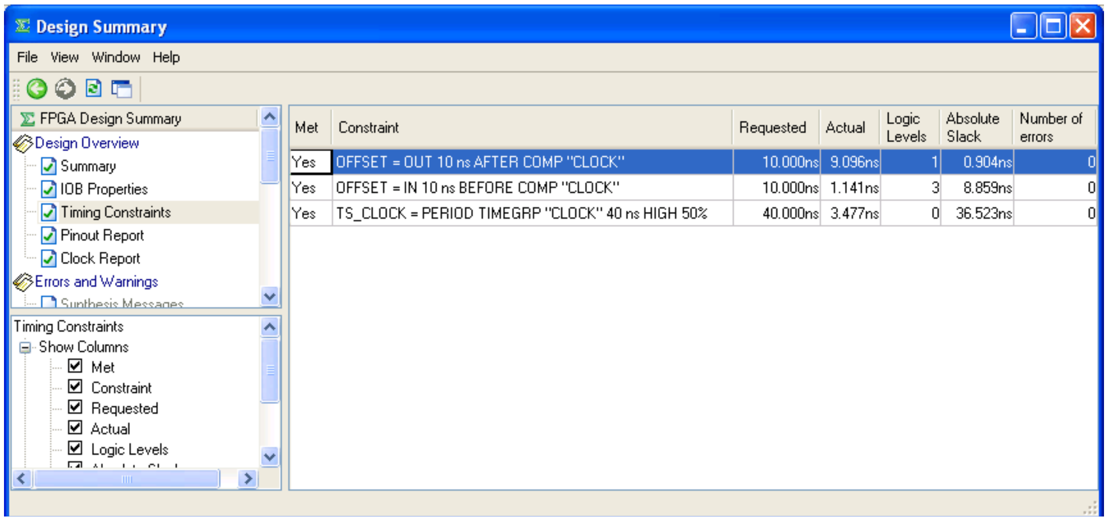
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	4	3,840	1%	
Number of 4 input LUTs	4	3,840	1%	
Logic Distribution				

```
Process "Generate Post-Place & Route Static Timing" completed successfully
```

Figure 14: **Post Implementation Design Summary**

5. Locate the **Performance Summary** table near the bottom of the Design Summary.

6. Click the **All Constraints Met** link in the Timing Constraints field to view the Timing Constraints report. Verify that the design meets the specified timing requirements.



Met	Constraint	Requested	Actual	Logic Levels	Absolute Slack	Number of errors
Yes	OFFSET = OUT 10 ns AFTER COMP "CLOCK"	10.000ns	9.096ns	1	0.904ns	0
Yes	OFFSET = IN 10 ns BEFORE COMP "CLOCK"	10.000ns	1.141ns	3	8.859ns	0
Yes	TS_CLOCK = PERIOD TIMEGRP "CLOCK" 40 ns HIGH 50%	40.000ns	3.477ns	0	36.523ns	0

Figure 15: **All Constraints Met Report**

7. Close the Design Summary.

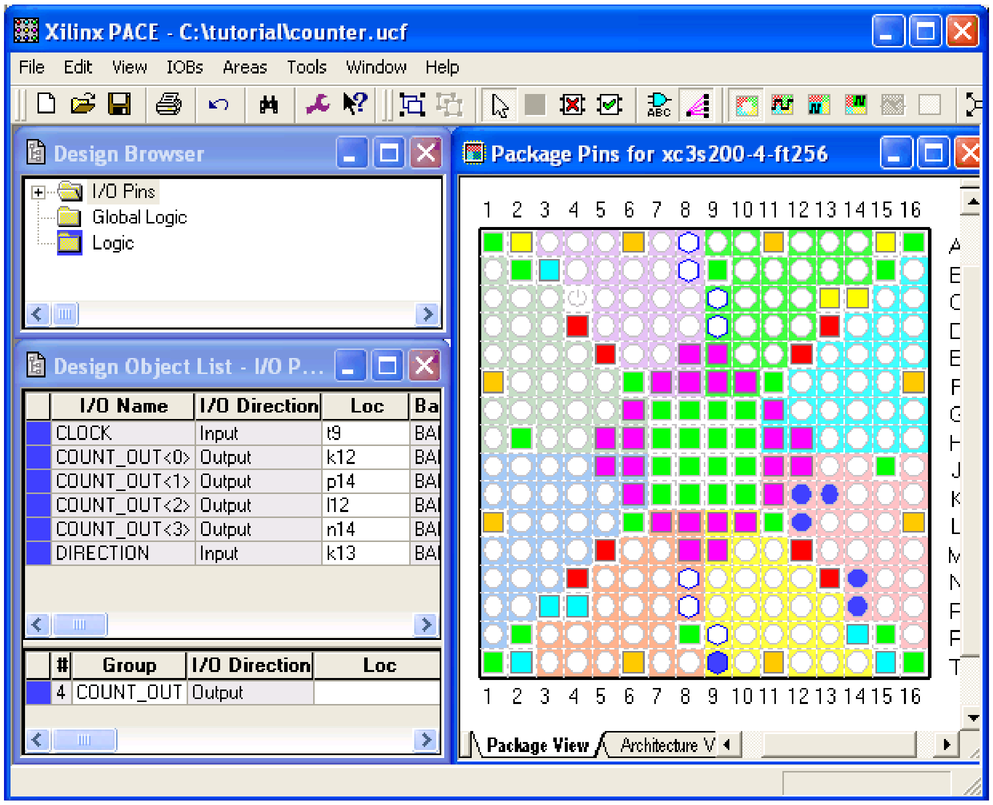
Assigning Pin Location Constraints

Specify the pin locations for the ports of the design so that they are connected correctly on the Spartan-3 Startup Kit demo board.

To constrain the design ports to package pins, do the following:

1. Verify that **counter** is selected in the Sources window.
2. Double-click the **Floorplan Area/IO/Logic - Post Synthesis** process found in the User Constraints process group. The Xilinx Pinout and Area Constraints Editor (PACE) opens.
3. Select the **Package View** tab.
4. In the Design Object List window, enter a pin location for each pin in the **Loc** column using the following information:
   - CLOCK input port connects to FPGA pin **T9** (GCK0 signal on board)
   - COUNT_OUT<0> output port connects to FPGA pin **K12** (LD0 signal on board)
   - COUNT_OUT<1> output port connects to FPGA pin **P14** (LD1 signal on board)
   - COUNT_OUT<2> output port connects to FPGA pin **L12** (LD2 signal on board)
   - COUNT_OUT<3> output port connects to FPGA pin **N14** (LD3 signal on board)
   - DIRECTION input port connects to FPGA pin **K13** (SW7 signal on board)

Notice that the assigned pin locations are shown in blue:


Xilinx PACE - C:\tutorial\counter.ucf
File Edit View IOBs Areas Tools Window Help
Design Browser
I/O Pins
Global Logic
Logic
Design Object List - I/O P...
Package Pins for xc3s200-4-ft256
Package View
Architecture V

I/O Name	I/O Direction	Loc	Ba
CLOCK	Input	t9	BAI
COUNT_OUT<0>	Output	k12	BAI
COUNT_OUT<1>	Output	p14	BAI
COUNT_OUT<2>	Output	l12	BAI
COUNT_OUT<3>	Output	n14	BAI
DIRECTION	Input	k13	BAI

#	Group	I/O Direction	Loc
4	COUNT_OUT	Output	

Figure 16: **Package Pin Locations**

5. Select **File** → **Save**. You are prompted to select the bus delimiter type based on the synthesis tool you are using. Select **XST Default <>** and click **OK**.
6. Close PACE.

Notice that the Implement Design processes have an orange question mark next to them, indicating they are out-of-date with one or more of the design files. This is because the UCF file has been modified.

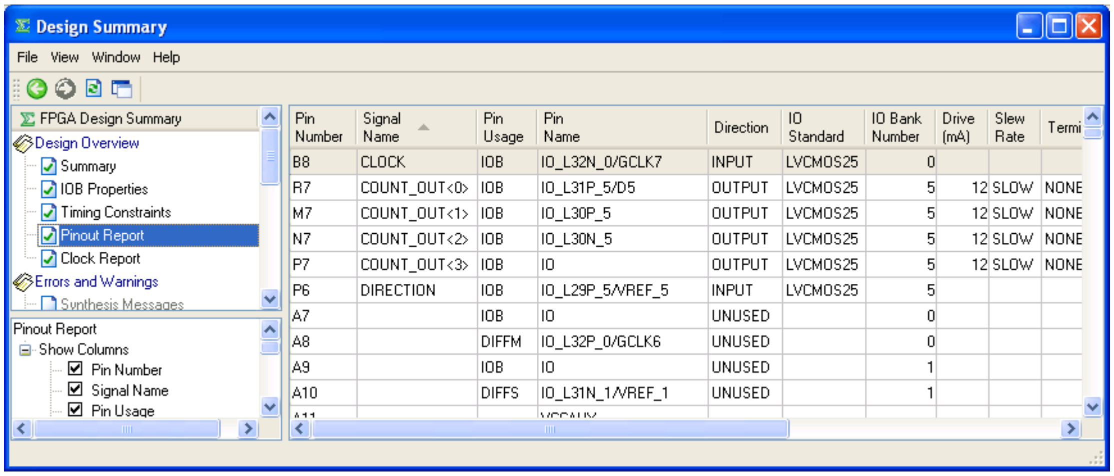
Reimplement Design and Verify Pin Locations

Reimplement the design and verify that the ports of the counter design are routed to the package pins specified in the previous section.

First, review the Pinout Report from the previous implementation by doing the following:

1. Open the Design Summary by double-clicking the **View Design Summary** process in the Processes window.

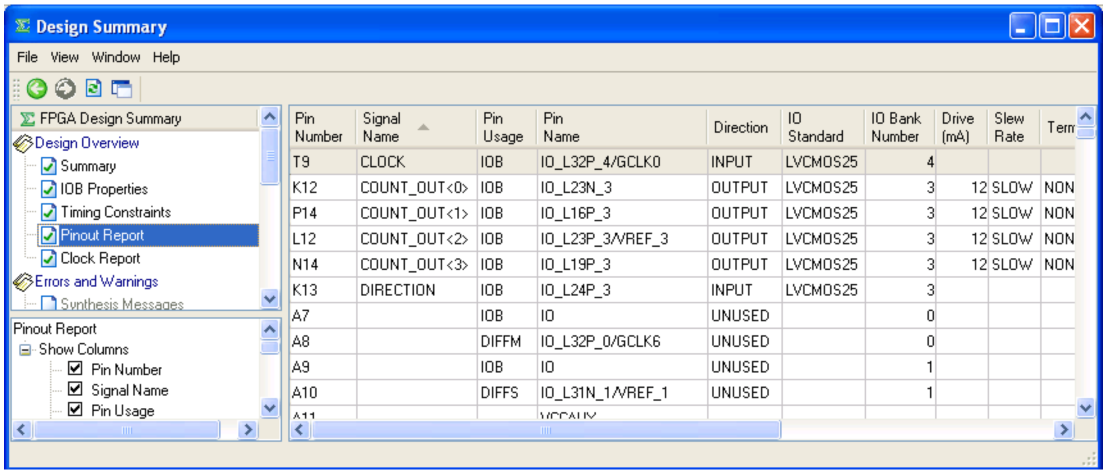
2. Select the **Pinout Report** and select the **Signal Name** column header to sort the signal names. Notice the Pin Numbers assigned to the design ports in the absence of location constraints.



Pin Number	Signal Name	Pin Usage	Pin Name	Direction	IO Standard	IO Bank Number	Drive (mA)	Slew Rate	Termi
B8	CLOCK	IOB	IO_L32N_0/GCLK7	INPUT	LVCMOS25	0			
R7	COUNT_OUT<0>	IOB	IO_L31P_5/D5	OUTPUT	LVCMOS25	5	12	SLOW	NONE
M7	COUNT_OUT<1>	IOB	IO_L30P_5	OUTPUT	LVCMOS25	5	12	SLOW	NONE
N7	COUNT_OUT<2>	IOB	IO_L30N_5	OUTPUT	LVCMOS25	5	12	SLOW	NONE
P7	COUNT_OUT<3>	IOB	IO	OUTPUT	LVCMOS25	5	12	SLOW	NONE
P6	DIRECTION	IOB	IO_L29P_5/VREF_5	INPUT	LVCMOS25	5			
A7		IOB	IO	UNUSED		0			
A8		DIFFM	IO_L32P_0/GCLK6	UNUSED		0			
A9		IOB	IO	UNUSED		1			
A10		DIFFS	IO_L31N_1/VREF_1	UNUSED		1			

Figure 17: **Package Pin Locations Prior to Pin Location Constraints**

3. Reimplement the design by double-clicking the **Implement Design** process.
4. Select the **Pinout Report** again and select the **Signal Name** column header to sort the signal names.
5. Verify that signals are now being routed to the correct package pins.



Pin Number	Signal Name	Pin Usage	Pin Name	Direction	IO Standard	IO Bank Number	Drive (mA)	Slew Rate	Term
T9	CLOCK	IOB	IO_L32P_4/GCLK0	INPUT	LVCMOS25	4			
K12	COUNT_OUT<0>	IOB	IO_L23N_3	OUTPUT	LVCMOS25	3	12	SLOW	NON
P14	COUNT_OUT<1>	IOB	IO_L16P_3	OUTPUT	LVCMOS25	3	12	SLOW	NON
L12	COUNT_OUT<2>	IOB	IO_L23P_3/VREF_3	OUTPUT	LVCMOS25	3	12	SLOW	NON
N14	COUNT_OUT<3>	IOB	IO_L19P_3	OUTPUT	LVCMOS25	3	12	SLOW	NON
K13	DIRECTION	IOB	IO_L24P_3	INPUT	LVCMOS25	3			
A7		IOB	IO	UNUSED		0			
A8		DIFFM	IO_L32P_0/GCLK6	UNUSED		0			
A9		IOB	IO	UNUSED		1			
A10		DIFFS	IO_L31N_1/VREF_1	UNUSED		1			

Figure 18: **Package Pin Locations After Pin Location Constraints**

6. Close the Design Summary.

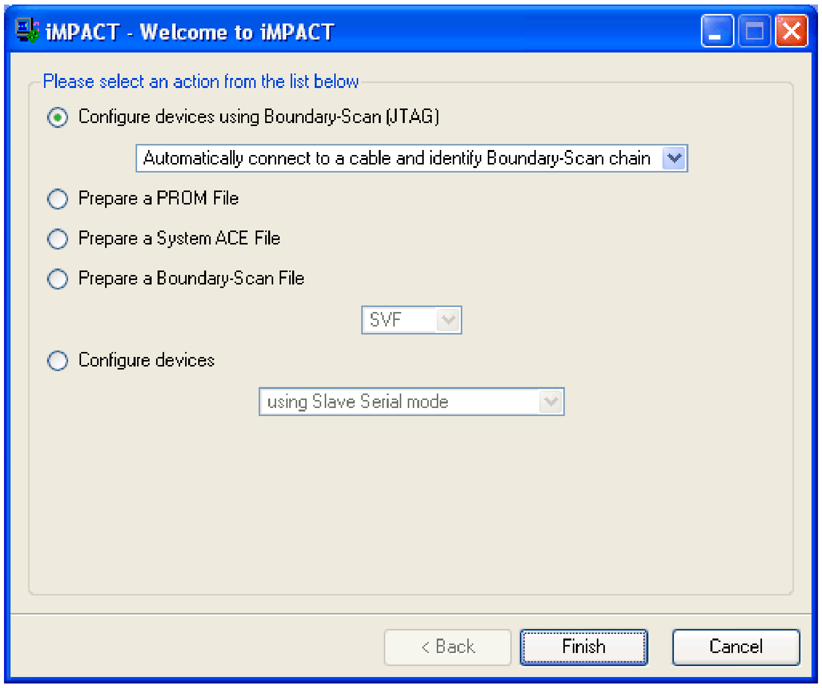
Download Design to the Spartan™-3 Demo Board

This is the last step in the design verification process. This section provides simple instructions for downloading the counter design to the Spartan-3 Starter Kit demo board.

1. Connect the 5V DC power cable to the power input on the demo board (J4).
2. Connect the download cable between the PC and demo board (J7).
3. Select **Implementation** from the drop-down list in the Sources window.

4. Select **counter** in the Sources window.
5. In the Process window, double-click the **Configure Target Device** process.
6. The Xilinx WebTalk Dialog box may open during this process. Click **Decline.**

iMPACT opens and the Configure Devices dialog box is displayed.



Please select an action from the list below

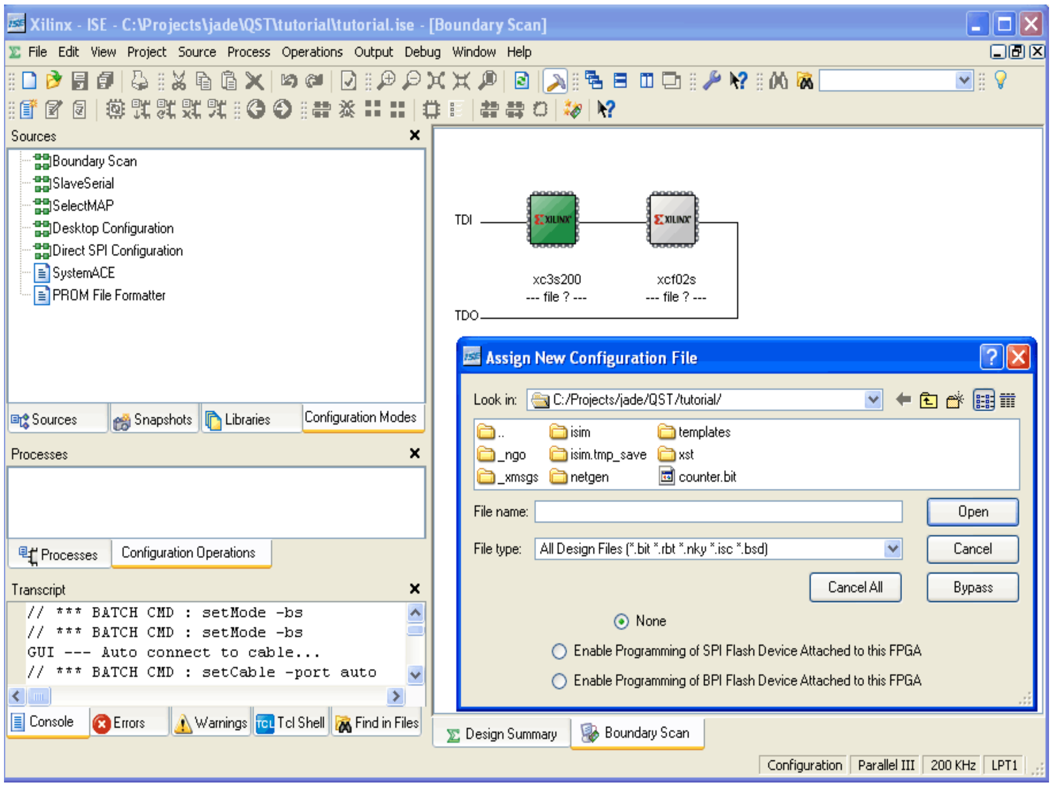
- [✓ Configure devices using Boundary-Scan (JTAG)]
  - Automatically connect to a cable and identify Boundary-Scan chain
- Prepare a PROM File
- Prepare a System ACE File
- Prepare a Boundary-Scan File
  - SVF
- Configure devices
  - using Slave Serial mode

Figure 19: **iMPACT Welcome Dialog Box**

7. In the Welcome dialog box, select **Configure devices using Boundary-Scan (JTAG)**.
8. Verify that **Automatically connect to a cable and identify Boundary-Scan chain** is selected.
9. Click **Finish**.
10. If you get a message saying that there are two devices found, click **OK** to continue.

    The devices connected to the JTAG chain on the board will be detected and displayed in the iMPACT window.

11. The **Assign New Configuration File** dialog box appears. To assign a configuration file to the xc3s200 device in the JTAG chain, select the `counter.bit` file and click **Open**.



```
// *** BATCH CMD : setMode -bs
// *** BATCH CMD : setMode -bs
GUI --- Auto connect to cable...
// *** BATCH CMD : setCable -port auto
```

Look in: C:/Projects/jade/QST/tutorial/

File type: All Design Files (*.bit *.rbt *.nky *.isc *.bsd)

[✓ None]
Enable Programming of SPI Flash Device Attached to this FPGA
Enable Programming of BPI Flash Device Attached to this FPGA

Figure 20: **Assign New Configuration File**

12. If you get a Warning message, click **OK**.
13. Select **Bypass** to skip any remaining devices.
14. Right-click on the xc3s200 device image, and select **Program...** The **Programming Properties** dialog box opens.
15. Click **OK** to program the device.

    When programming is complete, the Program Succeeded message is displayed.

    Program Succeeded

    On the board, LEDs 0, 1, 2, and 3 are lit, indicating that the counter is running.
16. Close iMPACT without saving.

You have completed the ISE Quick Start Tutorial. For an in-depth explanation of the ISE design tools, see the ISE In-Depth Tutorial on the Xilinx® web site at: http://www.xilinx.com/support/techsup/tutorials/