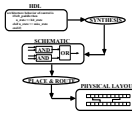
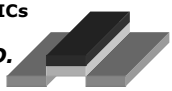
DESIGNING FPGAS & ASICS

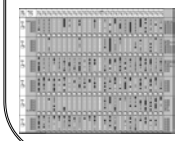


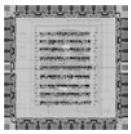
Overview of FPGAs and ASICs



Prof. Don Bouldin, Ph.D.

Electrical & Computer Engineering
University of Tennessee
TEL: (865)-974-5444
FAX: (865)-974-5483
dbouldin@tennessee.edu

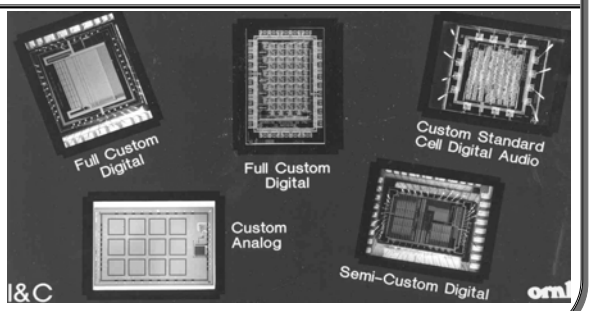




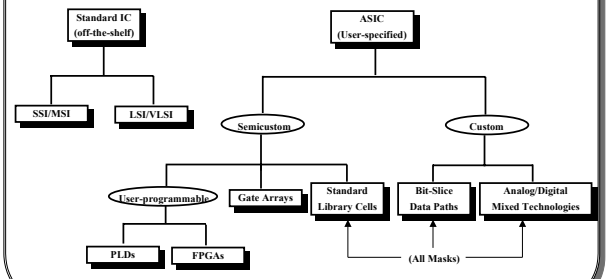
COURSE OUTLINE

- Overview of FPGAs and ASICs
- Using Synthesis
- HDL Examples
- Simulation and Testing
- Physical Place and Route
- Testing ASICs
- Component Reuse

A VARIETY OF ASICS ARE POSSIBLE

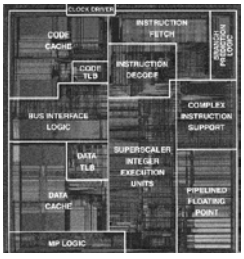


APPLICATIONS MAY USE STANDARD ICs or FPGAs/ASICs



THE COST PER GATE DECREASES AS THE DENSITY OF AN I.C. INCREASES

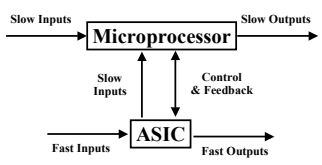
- Microprocessors and other off-the-shelf LSI/VLSI chips are the *most* cost-effective because millions of gates are available in a single chip. ($0.0001/gate; 20,000 gates/pin)
- SSI/MSI glue logic chips are the *least* cost-effective because only a few gates are available in a single chip. ($0.01/gate; 1-3 gates/pin)



PENTIUM

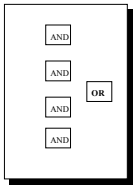
SYSTEM FUNCTIONS ARE OFTEN SPLIT BETWEEN THE CPU AND AN ASIC

- The most economical means of implementing logic functions is to use a microprocessor.
- When the microprocessor is too slow or too busy to handle some fast inputs and outputs, an ASIC can be used to implement "random" logic.



PROGRAMMABLE LOGIC DEVICES ARE BEST FOR SMALL DESIGNS WITH I/O

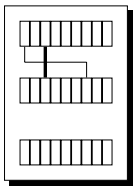
PLDs



- Vendor prefabricates multiple sets of ANDs and ORs with programmable connections
- User specifies connections to implement desired logic functions
- Replaces 200 to 8,000 gates with single package of 20-84 pins
- Electrically programmable (and erasable) by the user one at a time within minutes
- PC-based development system costs $3K

FPGAS ARE BEST FOR ADAPTABLE SITUATIONS

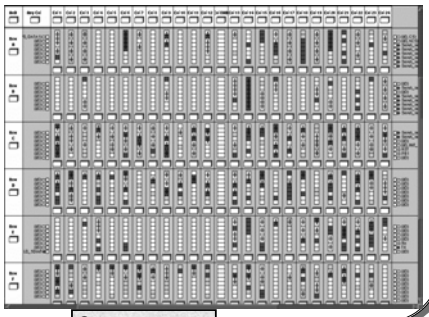
FPGAs



- Vendor prefabricates parts with rows of gates and programmable connections
- User specifies connections to implement logic functions
- Replaces 8,000 to 200,000 gates (or more)
- Electrically programmable (and erasable) by the user one at a time within minutes
- Production quantity < 200,000
- PC-based development system costs $10K

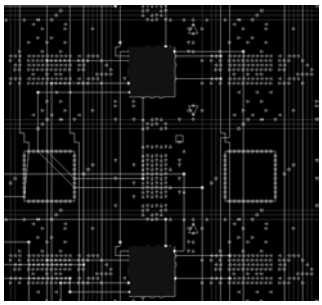
ALTERA FLEX-10K FPGA LAYOUT

Vendor prefabricates parts with rows of gates (look-up tables) and programmable connections (not shown).



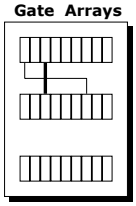
DETAILED LAYOUT OF XILINX FPGA

Programmable switches (*puddles* which have RC delay) determine which wiring segments (short, medium, long) are connected.



MGAS ARE BEST FOR HIGH-QUANTITY DESIGNS WITH CRITICAL TIME-TO-MARKET

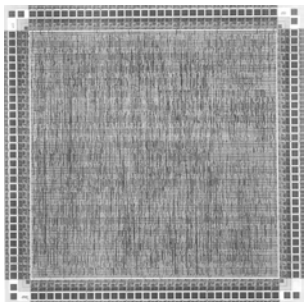
Mask Gate Arrays



- Vendor prefabricates rows of gates and stockpiles wafers
- User specifies *two* layers to implement logic functions
- Replaces 20,000 to 200,000 gates (or more)
- After place & route, masks are made for *two* layers
- Workstation-based development system costs $ 20K
- Turnaround time for prototypes is 3 weeks

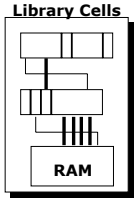
A MASK GATE ARRAY CAN BE STOCKPILED AND THEN PERSONALIZED

- The fabricator provides basic gates with space for interconnect.
- The application designer submits a logic net-list which defines the interconnect layers.



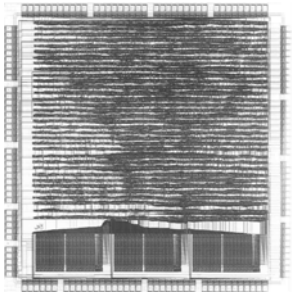
STANDARD-CELLS ARE BEST FOR HIGH-QUANTITY APPLICATIONS WITH RAM

Standard-Height Library Cells



- Vendor develops library disk files of logic functions (and internal RAM or cache).
- User selects cells and specifies *two* layers of interconnections
- After place & route, masks are made for *all* layers
- Replaces 20,000 to 2,000,000 gates (or more)
- Workstation-based development system costs $ 20K
- Turnaround time for prototypes is 8 weeks

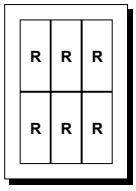
STANDARD-HEIGHT CELL CHIPS CAN ALSO USE EMBEDDED RAM



Space between rows for wiring can be varied as needed.

BIT-SLICE DATA PATHS ARE BEST FOR SPECIAL-PURPOSE PARALLEL PROCESSING

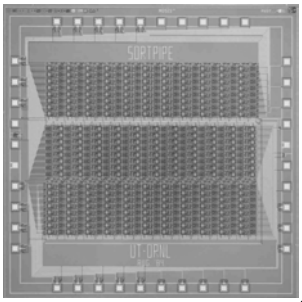
Replicated Bit-Slices



- User performs *custom* layout of bit-slices which are then replicated
- Most efficient use of silicon
- Masks are made for *all* layers
- Replaces 20,000 to 200,000 gates (or more)
- Workstation-based development system costs $ 150K
- Turnaround time for prototypes is 8 weeks

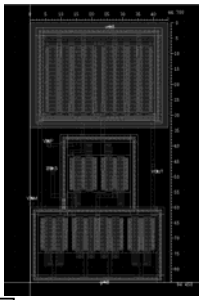
DATAPATH OR BIT-SLICE LAYOUT IS THE MOST EFFICIENT

- The basic cell has been designed with its neighbors in mind.
- One bit has been arrayed 8 times to form a byte.
- Each byte is connected to its neighbor to form a datapath or systolic array.



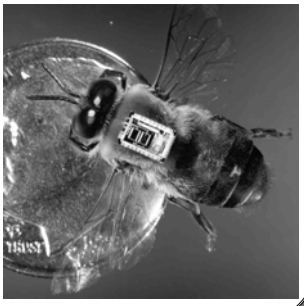
SPECIAL TECHNIQUES ARE USED FOR LAYOUT OF ANALOG CIRCUITS

- Layouts use multi-gate fingers and common-centroid symmetry to improve matching of devices.
- Poly2-Poly1 capacitors save space.
- Switched-capacitor circuits replace large resistors.
- Guard rings reduce noise.



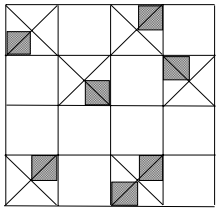
MIXED-SIGNAL ICS USE BOTH ANALOG AND DIGITAL CIRCUITS

- Solar cells provide power.
- Analog circuit detects when sufficient energy is available.
- Digital circuit provides for series of pulses.
- Infrared LEDs emit output that is detectable 1 mile away.

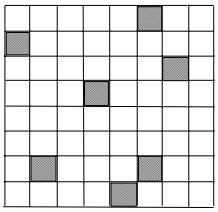


MINIMIZING AREA INCREASES BOTH THE NUMBER OF SITES AND YIELD

Sites - Bad Die = Good Die
16 - 6 = 10

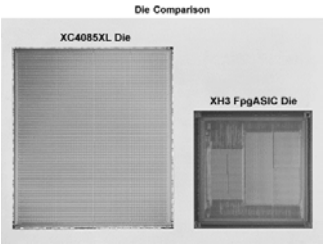


Sites - Bad Die = Good Die
64 - 7 = 57



FPGAS COST MORE AND ARE SLOWER THAN MGAS

- **FPGAs cost 2x *more* since programmable logic and interconnect switches result in larger die size.**
- **FPGAs are 2x *slower* since programmable interconnect switches have greater RC delay than metal vias.**



Convert when >200,000 copies or 2x faster speed is needed.

APPLICATIONS MAY USE STANDARD ICs or FPGAs/ASICs