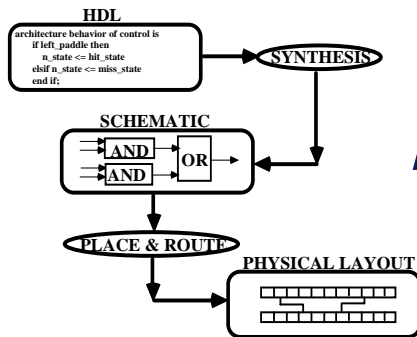


# DESIGN USING FPGAS

## ECE 551 Overview

*Prof. Don Bouldin, Ph.D.*



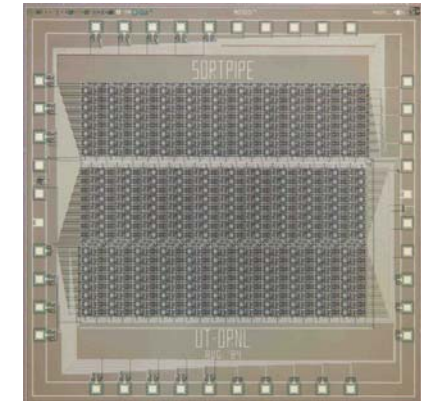
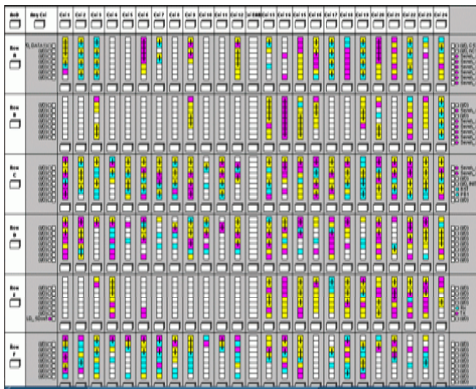
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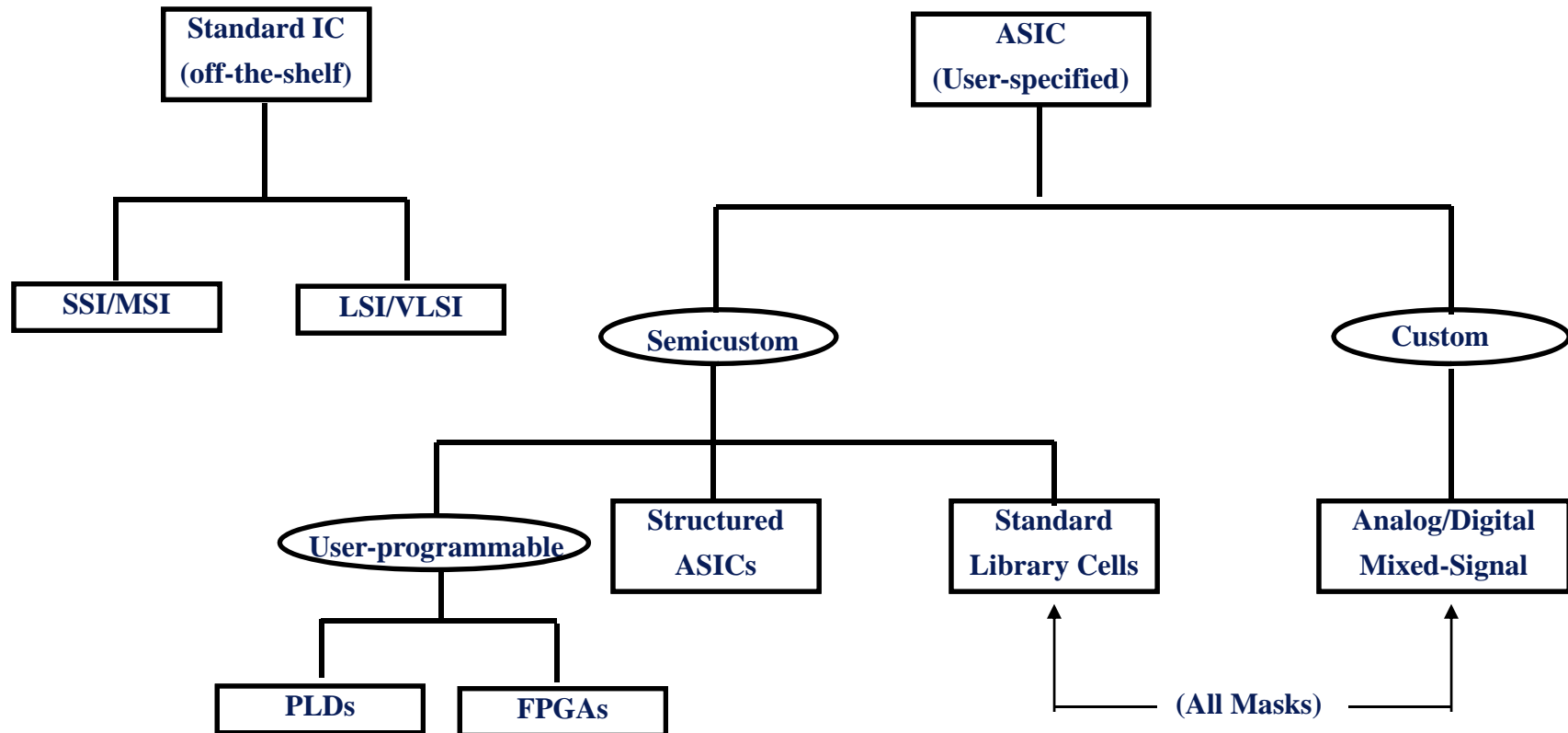


# REAL-TIME EMBEDDED SYSTEMS

- An electronic system containing a CPU without an operating system visible to the end-user.
- It interacts with peripheral devices within fixed time constraints.
- A minimum of resources are employed to perform the required tasks.
- In addition to functionality and cost, other constraints include power management, fault tolerance, quality of service, security, etc.

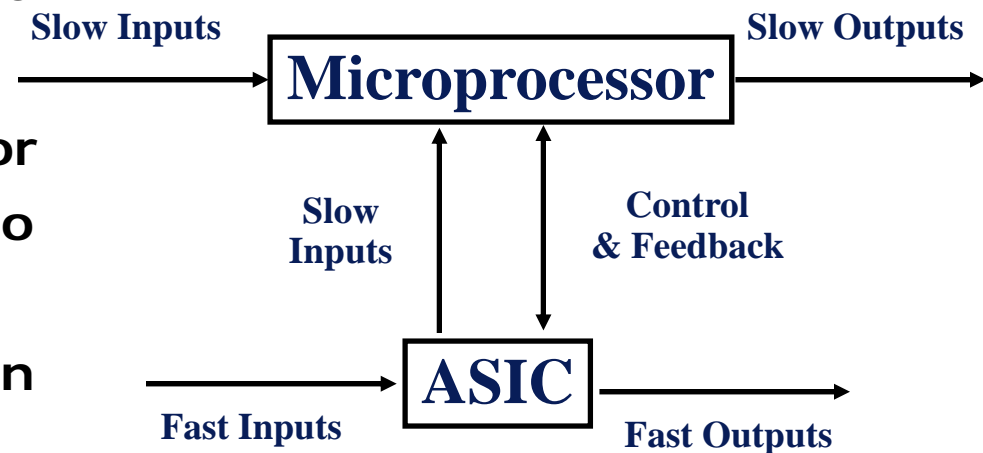


# APPLICATIONS MAY USE STANDARD ICs or FPGAs/ASICs

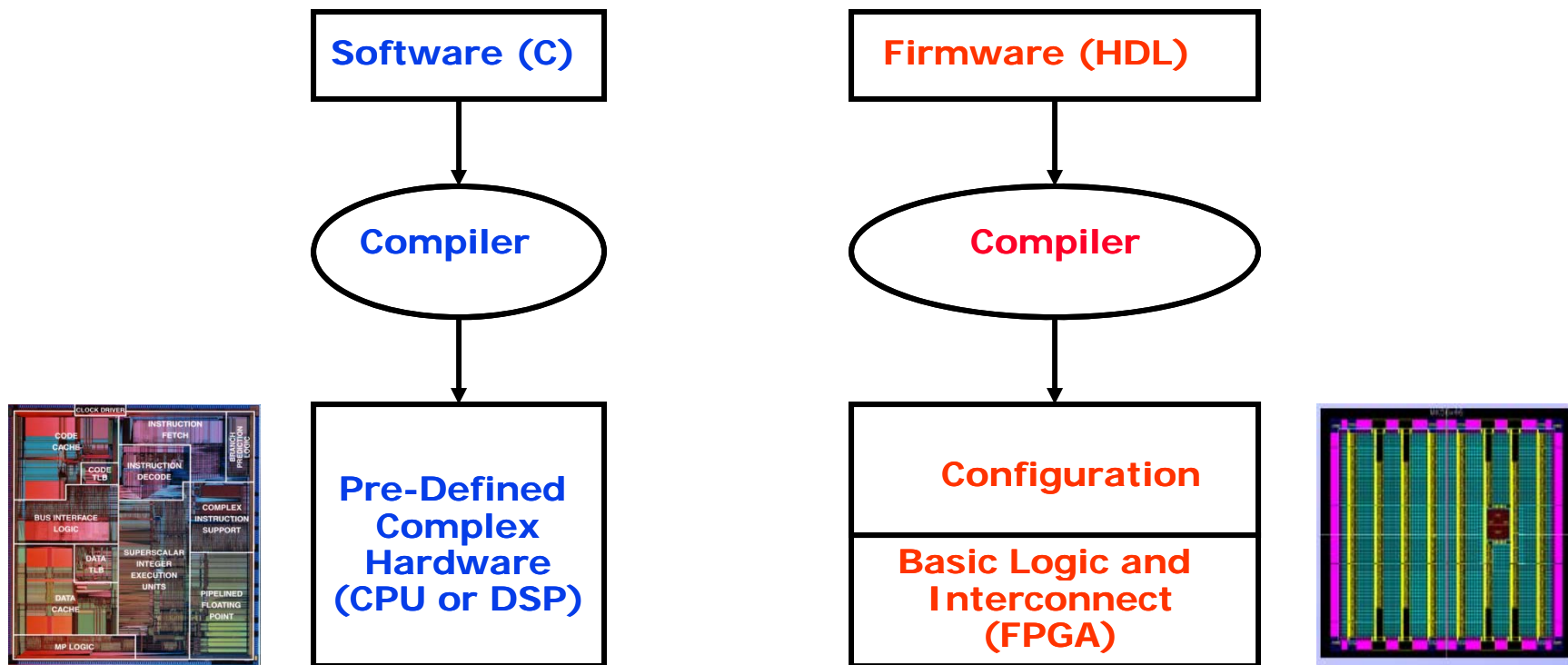


# SYSTEM FUNCTIONS ARE OFTEN SPLIT BETWEEN THE CPU AND AN ASIC

- The most economical means of implementing logic functions is to use a microprocessor.
- When the microprocessor is too slow or too busy to handle some fast inputs and outputs, an ASIC can be used to implement high-speed concurrent operations.

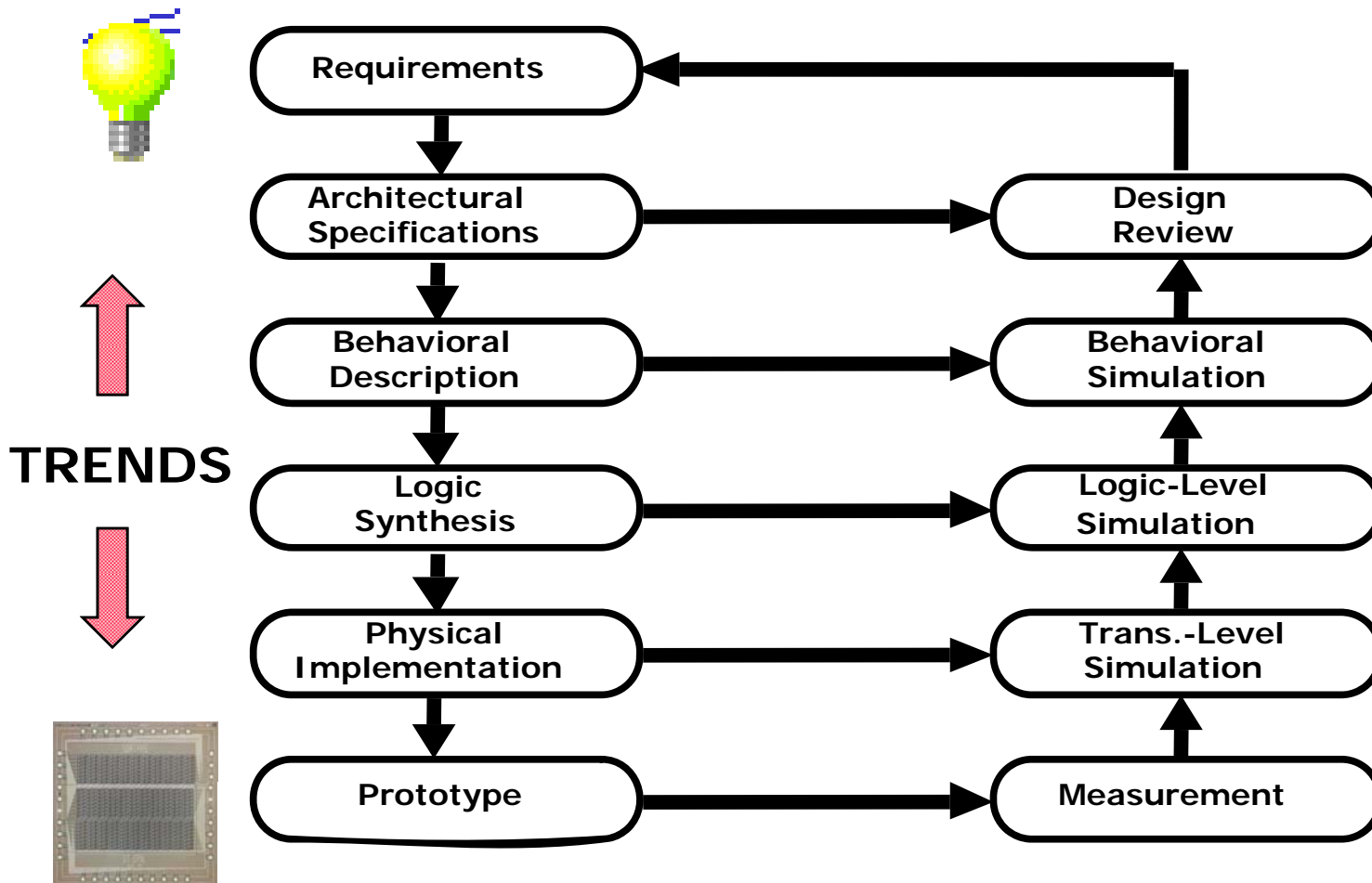


# FPGAS PROVIDE PRECISE CONTROL OF THE HARDWARE



- CPUs have a single arithmetic unit with a fixed bit size.
- FPGAs can have multiple units with flexible bit sizes.

# MICROELECTRONIC SYSTEM DESIGN CONSISTS OF ITERATIVE REFINEMENTS OF SYNTHESIS AND VERIFICATION

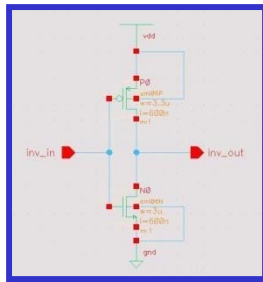


# ECE 551 & ECE 651

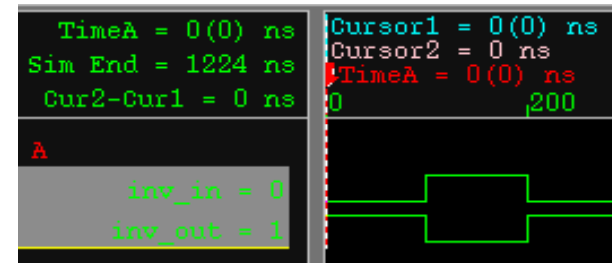
- **ECE 551 (logic level; b/w):**
  - Pairs create project using VHDL
  - Simulate pre-synthesis and post-layout
  - Demonstrate using 200K-gate Xilinx FPGA on Spartan3 Board with I/O
  - Implement on screen only using Altera FPGA
- **ECE 651 (physical level; color):**
  - Perform custom IC design (but not submit for fab)
  - Compare manual design vs. automated tools
  - Study nanometer design issues (cross-talk, power)

# CUSTOM IC DESIGN FLOW

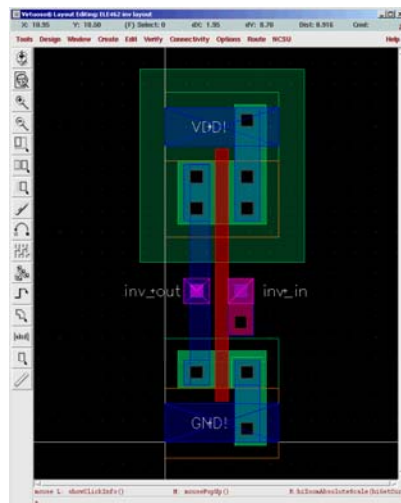
## 1--SCHEMATIC



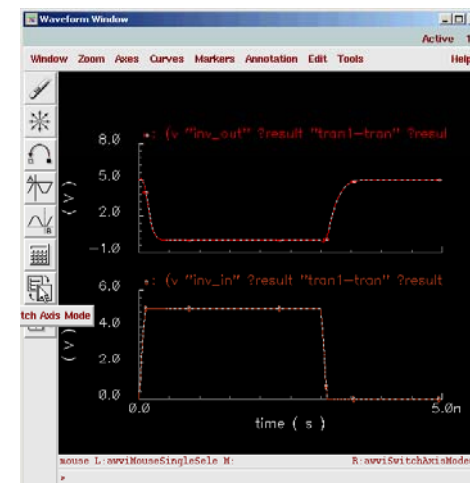
## 2--PRE-LAYOUT LOGIC SIMULATION



## 3--MANUAL LAYOUT



## 4--POST-LAYOUT TRANS. SIMULATION





# SEMI-CUSTOM DESIGN FLOW OF DIGITAL FPGAs/ASICs

## 1—HDL

CASE w IS

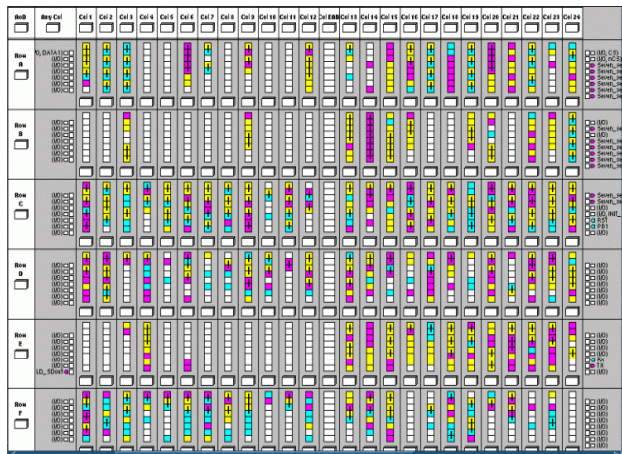
```
WHEN "00" => y <= "1000" ;  
WHEN "01" => y <= "0100" ;  
WHEN "10" => y <= "0010" ;  
WHEN OTHERS => y <= "0001" ;  
END CASE ;
```



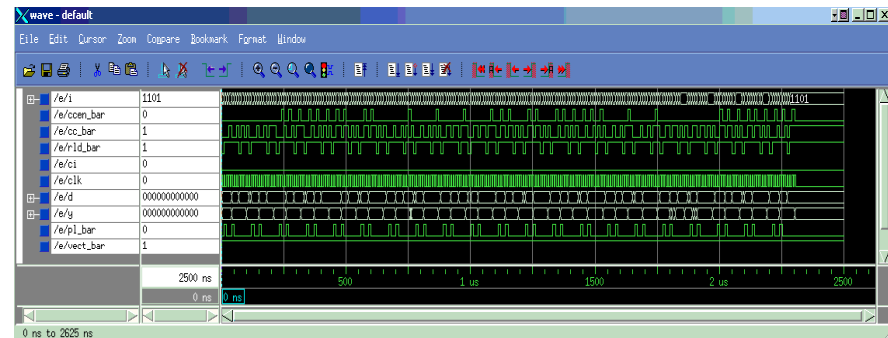
## 2--PRE-SYNTHESIS SIMULATION



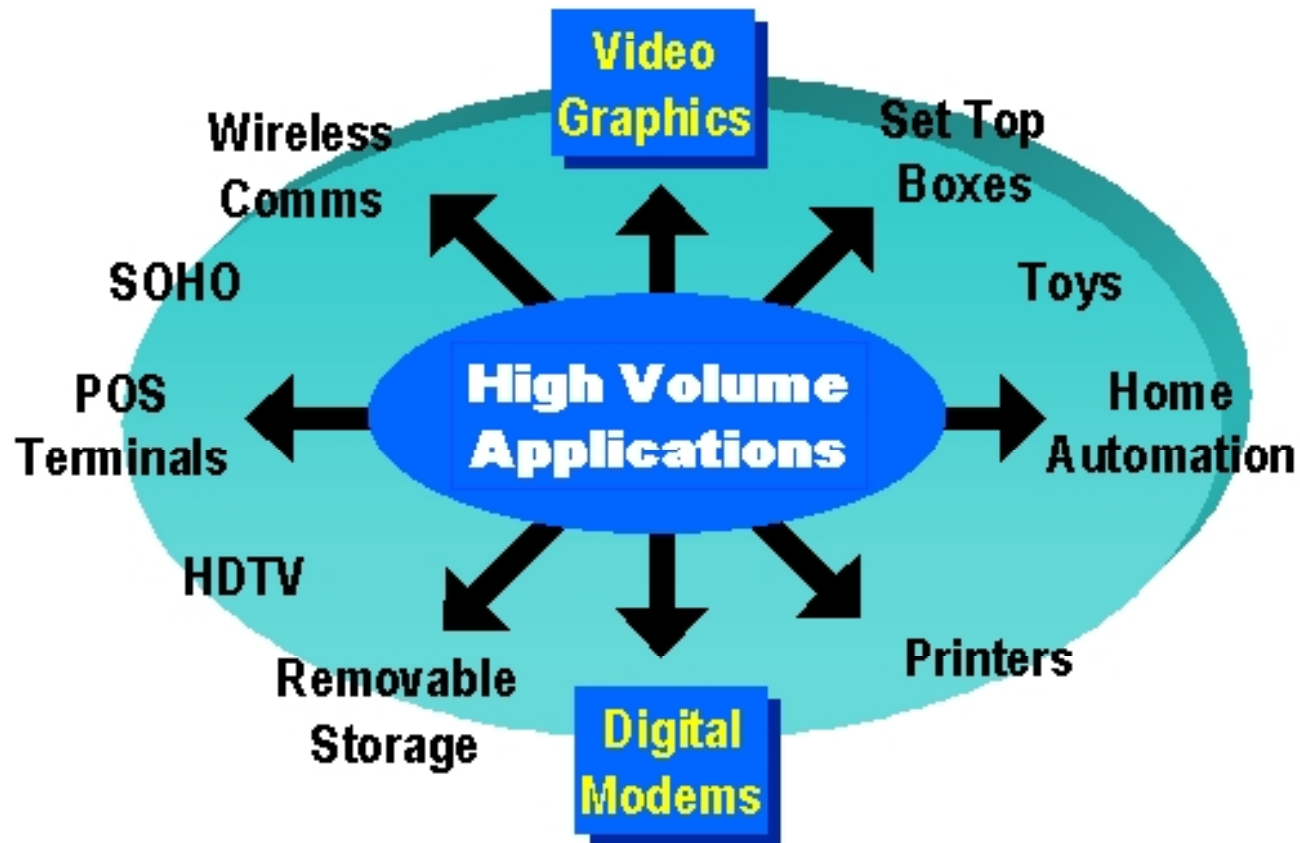
## 3—SYNTHESIS/AUTO LAYOUT



## 4--POST-LAYOUT SIMULATION



# HIGH VOLUME APPLICATIONS OF FPGAS



[www.xilinx.com](http://www.xilinx.com)

# TELECOMMUNICATIONS IS THE LARGEST MARKET FOR FPGAS

- Xilinx (XLNX) and Cisco (CSCO) stock prices have tracked together for two decades.

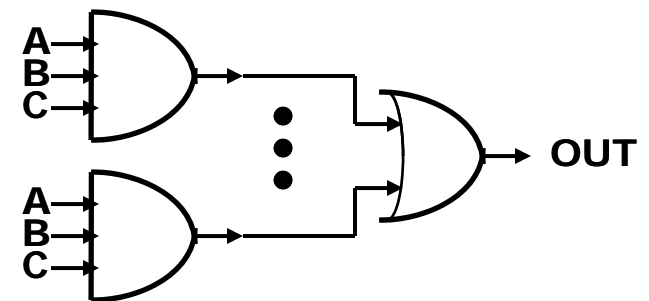


# PROGRAMMABLE LOGIC ARRAY

- Any 8-row truth table can be implemented using eight 3-input AND gates followed by a single OR gate with 8 inputs.
- An array of AND-OR tiles can be programmed to implement logic.
- In this example, only two outputs are required for row 4 and row 7:

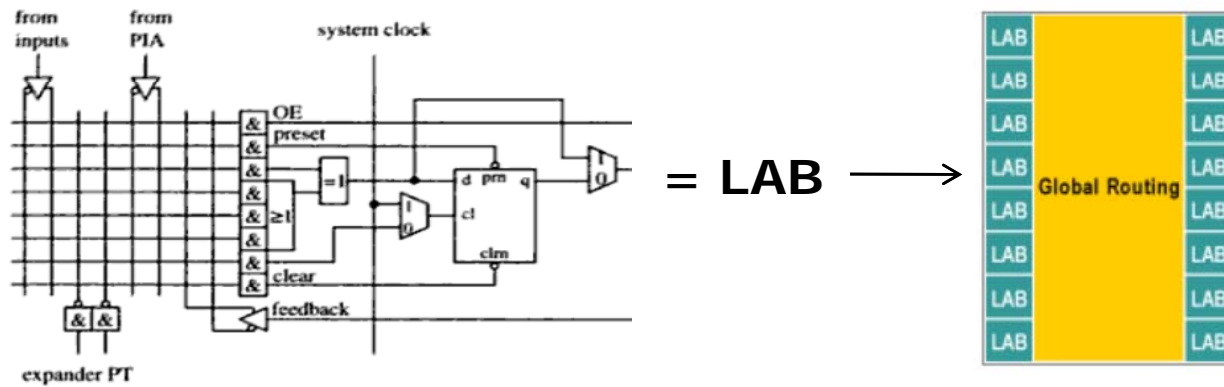
$$\text{OUT} = \overline{A}\overline{B}\overline{C} + ABC$$

<u>ROW</u>	<u>A</u>	<u>B</u>	<u>C</u>	<u>OUT</u>
0	0	0	0	0
1	0	0	1	0
2	0	1	0	0
3	0	1	1	0
4	1	0	0	1
5	1	0	1	0
6	1	1	0	0
7	1	1	1	1



# PLD AND CPLD

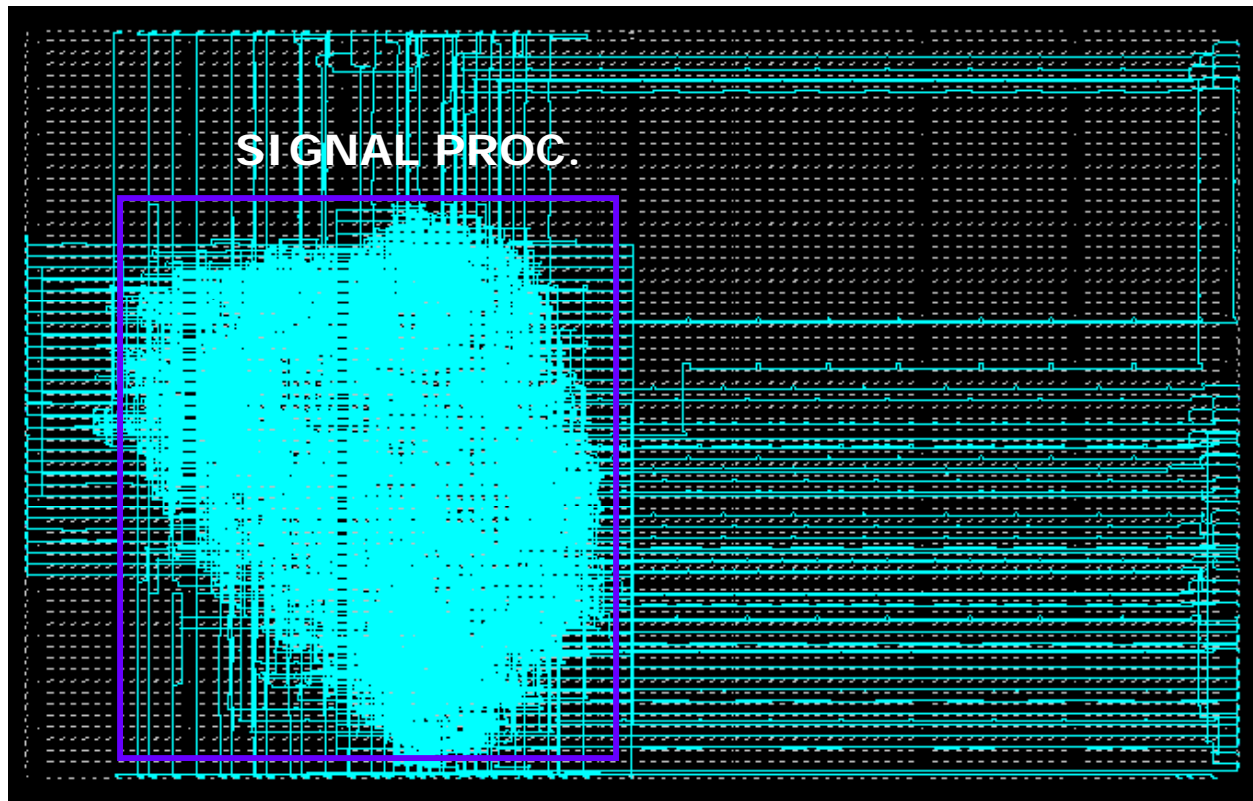
- Initially, programmable logic devices (PLDs) consisted of an array of 8 AND-OR tiles (called Logic Array Blocks or LABs by Altera) plus some additional interconnecting wires and storage elements.
- Larger components with 128 tiles (or more) became known as CPLDs or Complex PLDs. The tiles can be interconnected via a wiring matrix.



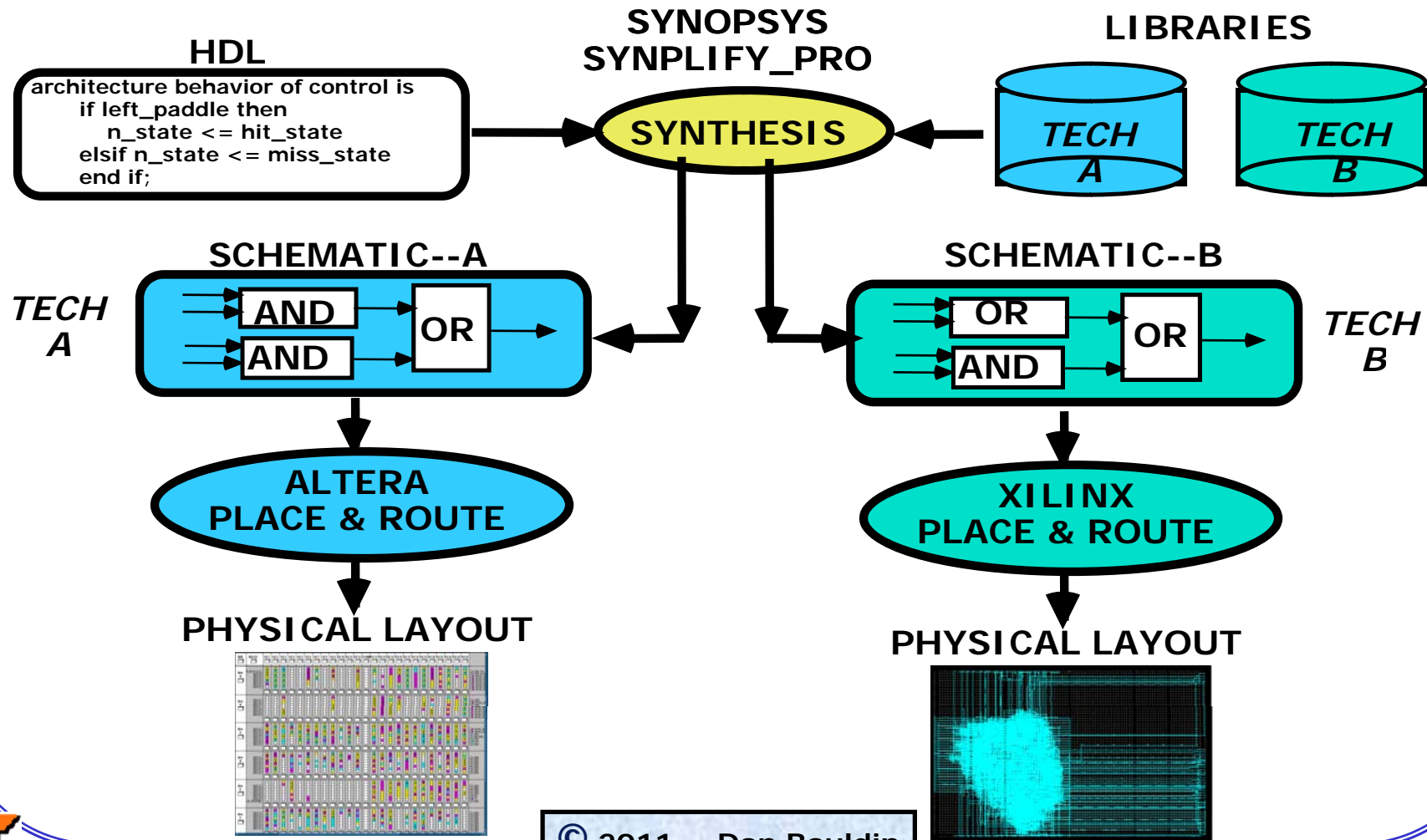
[www.altera.com](http://www.altera.com)

# RECONFIGURABLE COMPONENTS ARE ADAPTABLE

The internal logic and interconnect of a reconfigurable component (FPGA) may be specified by the user and changed at any time.



# HDL DESIGNS CAN BE TARGETED TO MULTIPLE LAYOUTS



# COURSE GOALS

This **project-oriented** course involves:

- (1) **design** of field-programmable gate arrays (FPGAs)
- (2) using synthesis and automatic placement and routing software
- (3) to implement the design using multiple technologies (Altera and Xilinx)
- (4) with local/remote access to LINUX workstations
- (5) free use of Xilinx prototyping boards
- (6) grade depending on homework, project and final exam
- (7) all presentation slides will be posted on the web:

<http://web.eecs.utk.edu/~bouldin/courses/551/overview.html>