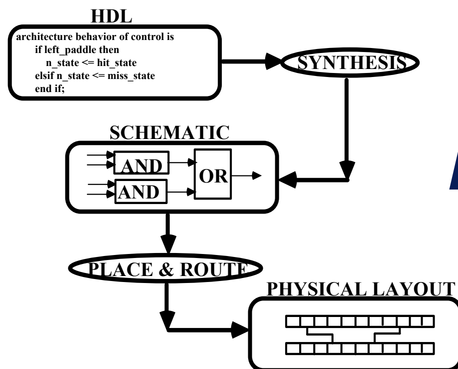
# DESIGNING FPGAS & ASICS




## Testing ASICs

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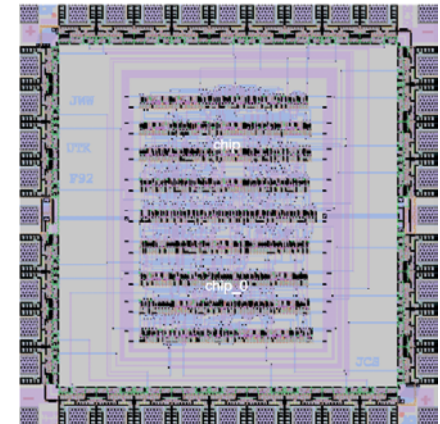

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# COURSE OUTLINE

- Overview of FPGAs and ASICs
- Using Synthesis
- HDL Examples
- Simulation and Testing
- Physical Place and Route
- Testing ASICs
- Component Reuse

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# TESTING ASICS

- Functional Tests
- Manufacturing Tests
- Fault Coverage
- Test Pattern Generation
- Internal Scan
- Boundary Scan
- Built-In Self-Test

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# FUNCTIONAL TEST STIMULI

- Functional test stimuli validate that the circuit exhibits the required behavior at the desired speed.
- It is too time-consuming to develop and to apply an exhaustive set of functional stimuli so usually the designer tests only favorite cases and expected trouble spots like overflow, etc.
- CAD tools to assist in this process generally take equations and generate 1's and 0's.

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# MANUFACTURING TEST STIMULI ARE NECESSARY BUT COSTLY

- Manufacturing has far less than 100% yield so each part must be tested to determine whether the circuit you desired was actually manufactured.
- First, known test structures are probed on the wafer to determine its acceptance.
- Then, each die on the wafer is probed and tested at d.c.
- Packaged parts are tested individually by the vendor at low speed (usually 1 MHz).
- The designer may then screen parts individually at full speed and under various environmental conditions.

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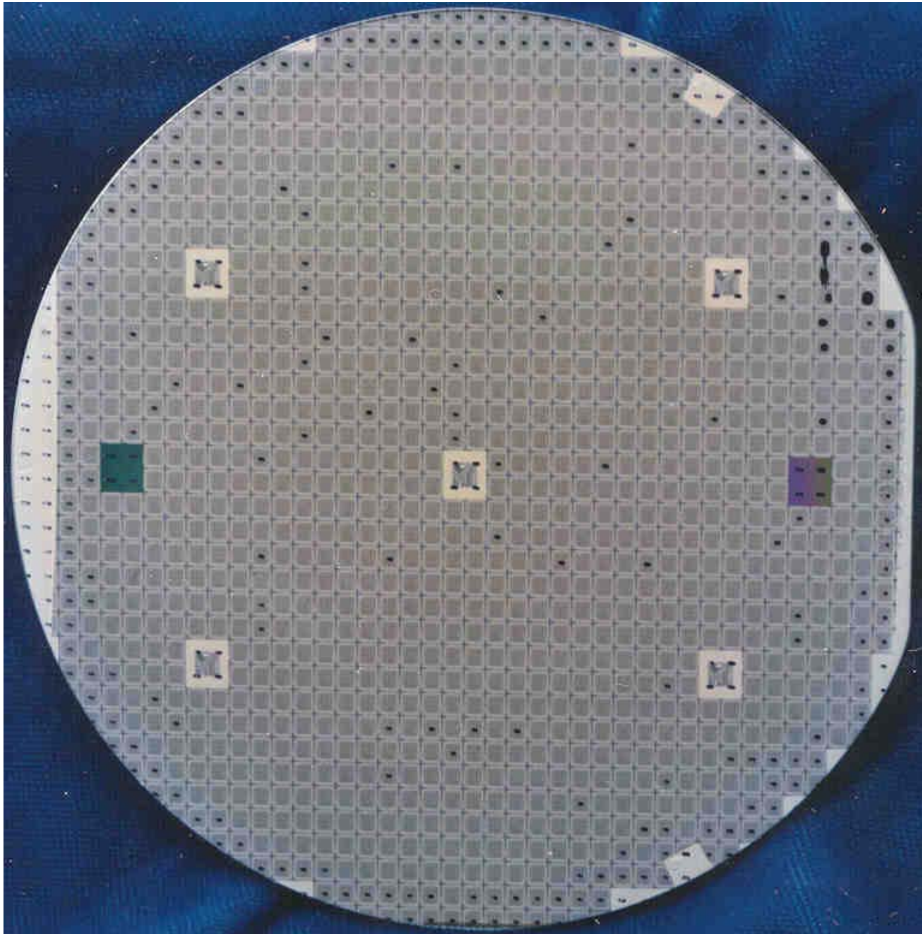
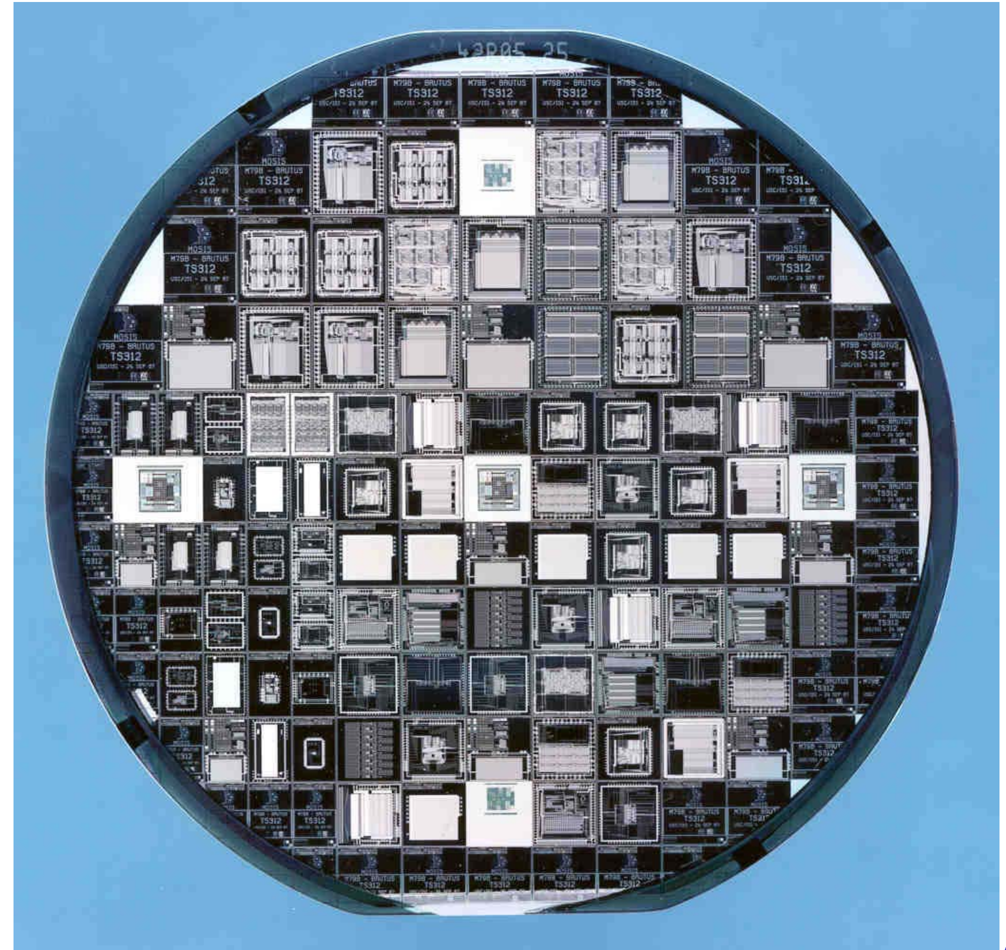
# SHARING MULTI-PROJECT MASKS AND WAFERS SAVES MONEY






MOSIS

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# MANUFACTURING TEST STIMULI AND FAULT COVERAGE

- Manufacturing test stimuli should provide sufficient coverage to achieve the desired quality.
- The more demanding the coverage, the fewer defective parts that will be shipped.
- Fault grading can be applied at the logic-level or at the MOS switch-level. Vendors encourage toggling of all logic nodes from 0 to 1 and 1 to 0 whether used or not.
- A minimum set of stimuli that can detect (not locate) faults is used for screening production parts to minimize time on the tester and its per-pin memory requirements.

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# DEFECTIVE PARTS AS A FUNCTION OF FAULT COVERAGE PERCENTAGE

| Defective Parts | Fault Coverage |
| --- | --- |
| 227 | 50.00% |
| 133 | 90.00% |
| 90 | 99.00% |
| 3 | 99.99% |

***Out of 10,000 Parts***

Table 14.24, Page 795
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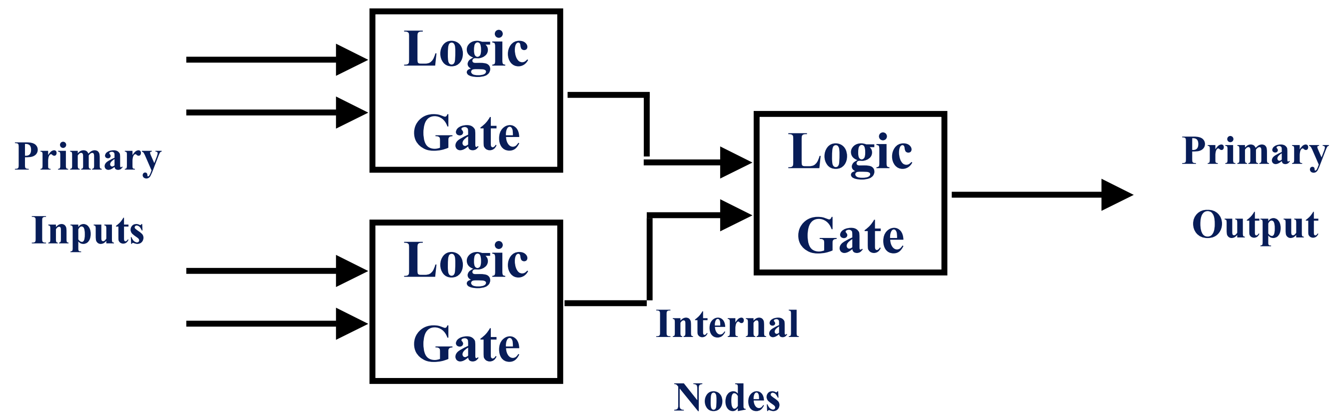
# GENERATING TEST STIMULI FOR LOGIC FAULT COVERAGE

- Stimuli must be applied to primary inputs and cause the internal nodes to toggle.  Responses must be observable from the primary outputs.
- Manufacturing test stimuli are generated before fabrication since the circuit can still be modified to enhance controllability and observability.  This is called "design for testability".

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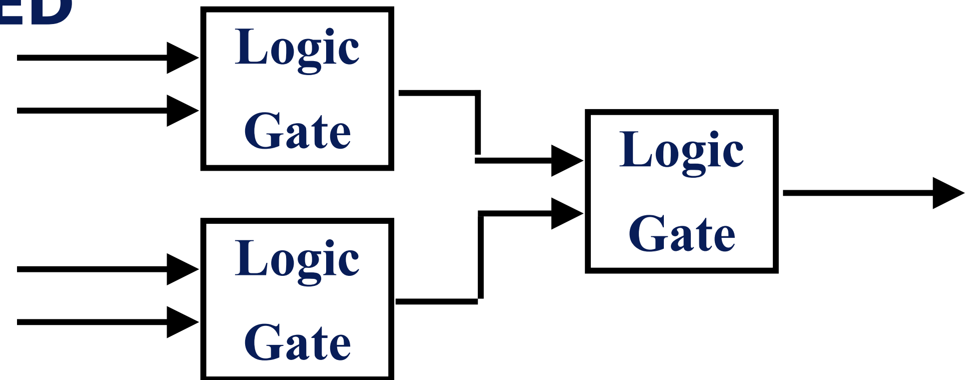
# FAULT COVERAGE IS BASED ON THE STUCK-AT MODEL

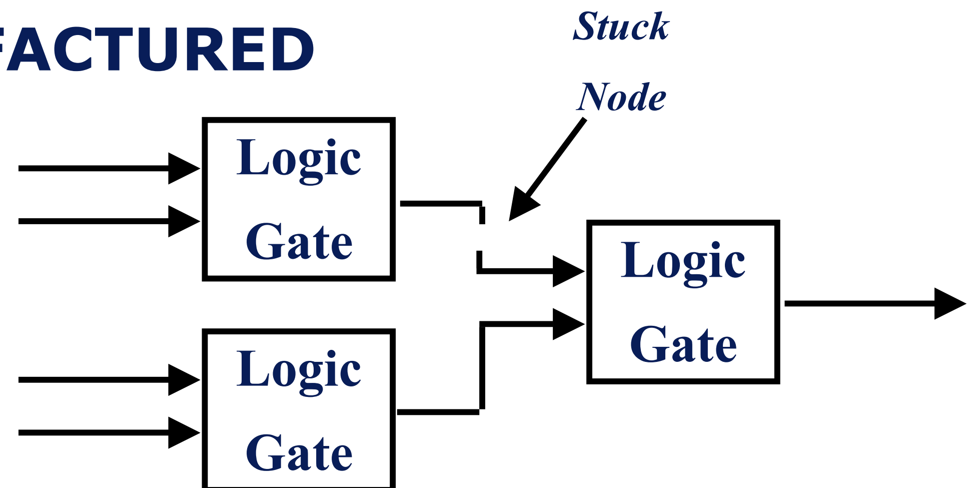
**DESIGNED**




**STUCK-AT MODEL**

- A node may be GOOD, Stuck-at-0 or Stuck-at-1.
- Only one node is considered to be at fault at any one time.

**MANUFACTURED**

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# DETECTION OF STUCK-AT FAULTS

To detect whether F1 at the output of U2 is s-a-1, apply an input of C = 0, B =1 and A=1.

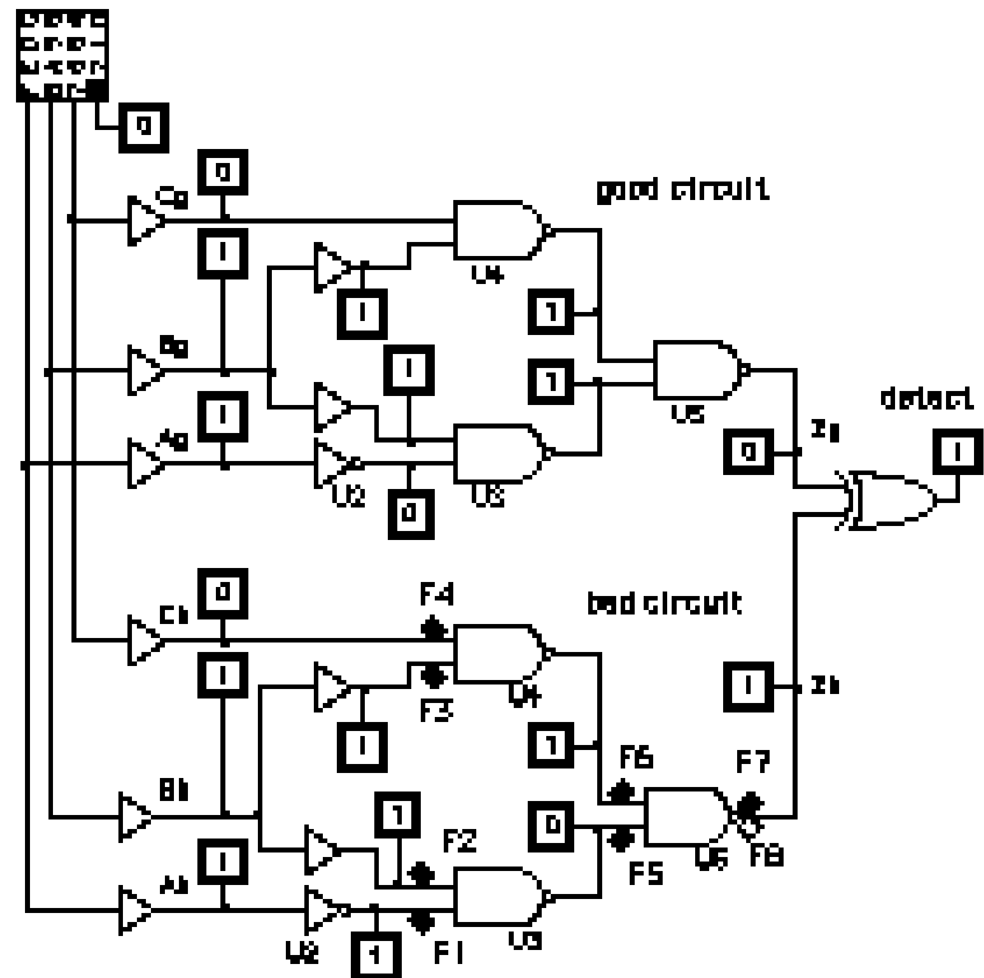


Fig. 14.16, Page 752
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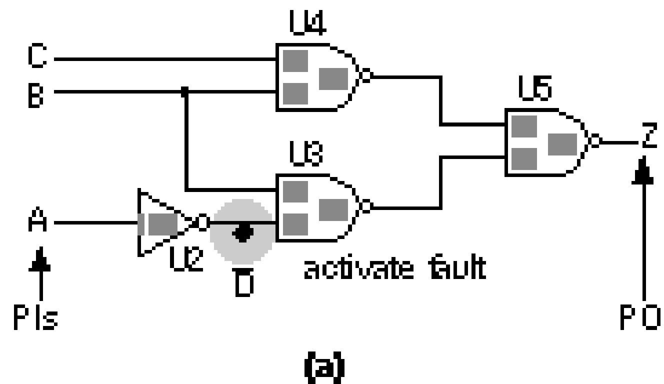
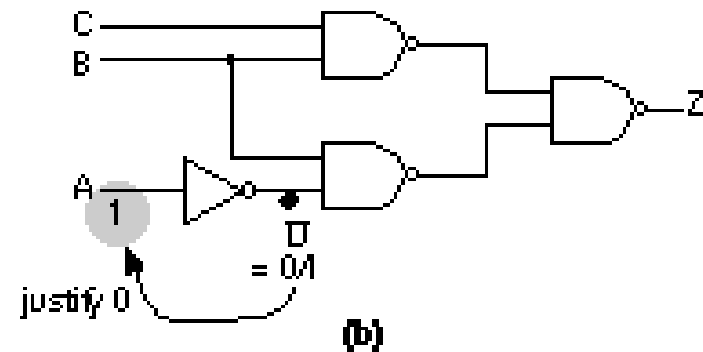
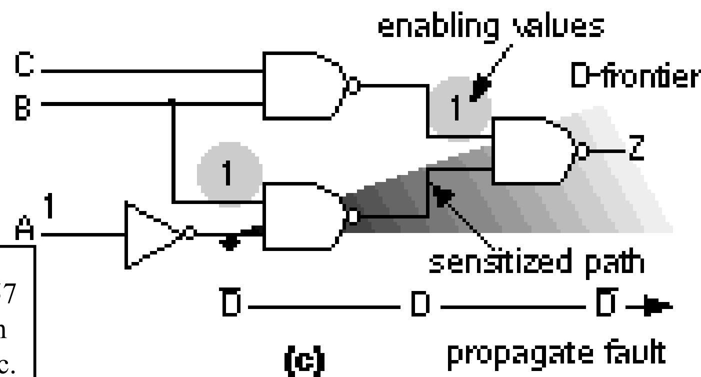
# JUSTIFICATION AND PROPAGATION FOR FAULT DETECTION



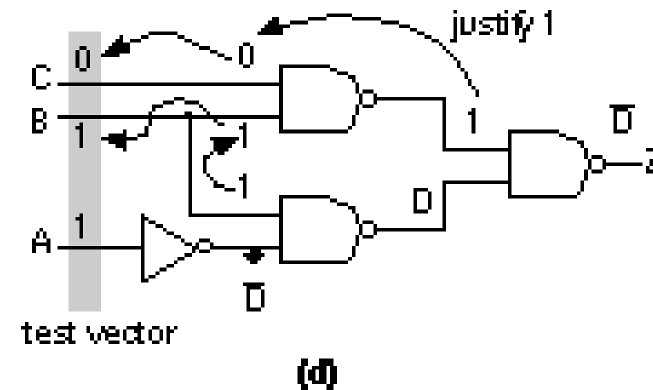




Fig. 14.18, Page 757
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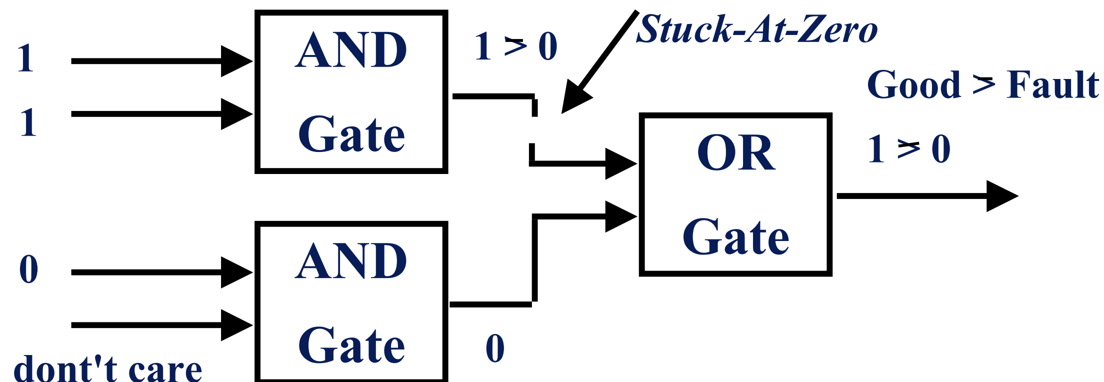
# GENERATION OF TEST STIMULI FOR STUCK-AT FAULTS

- **FUNCTIONAL--generated as a byproduct of verifying the intended operation.**
- **EXHAUSTIVE--too time-consuming for large, practical circuits but okay for small ones. Can use a counter to generate all possible 1's and 0's on the fly.**
- **RANDOM--easily generated on the fly using a linear feedback shift register.**
- **DETERMINISTIC--can be guaranteed to be generated if a test exists. However, this process may require substantial computing resources. Automatic Test Pattern Generator (ATPG) programs like Lasar, Podem and Fan are based on the D-algorithm.**

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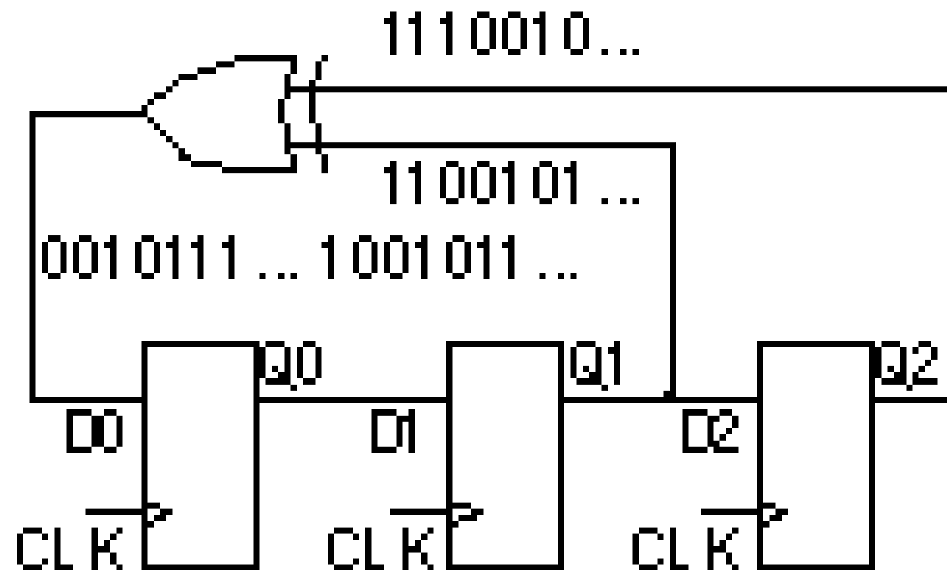
# RANDOM PATTERN GENERATION

**A Linear Feedback Shift Register (LFSR) can produce a Pseudo-Random Binary Sequence (PBRS).**

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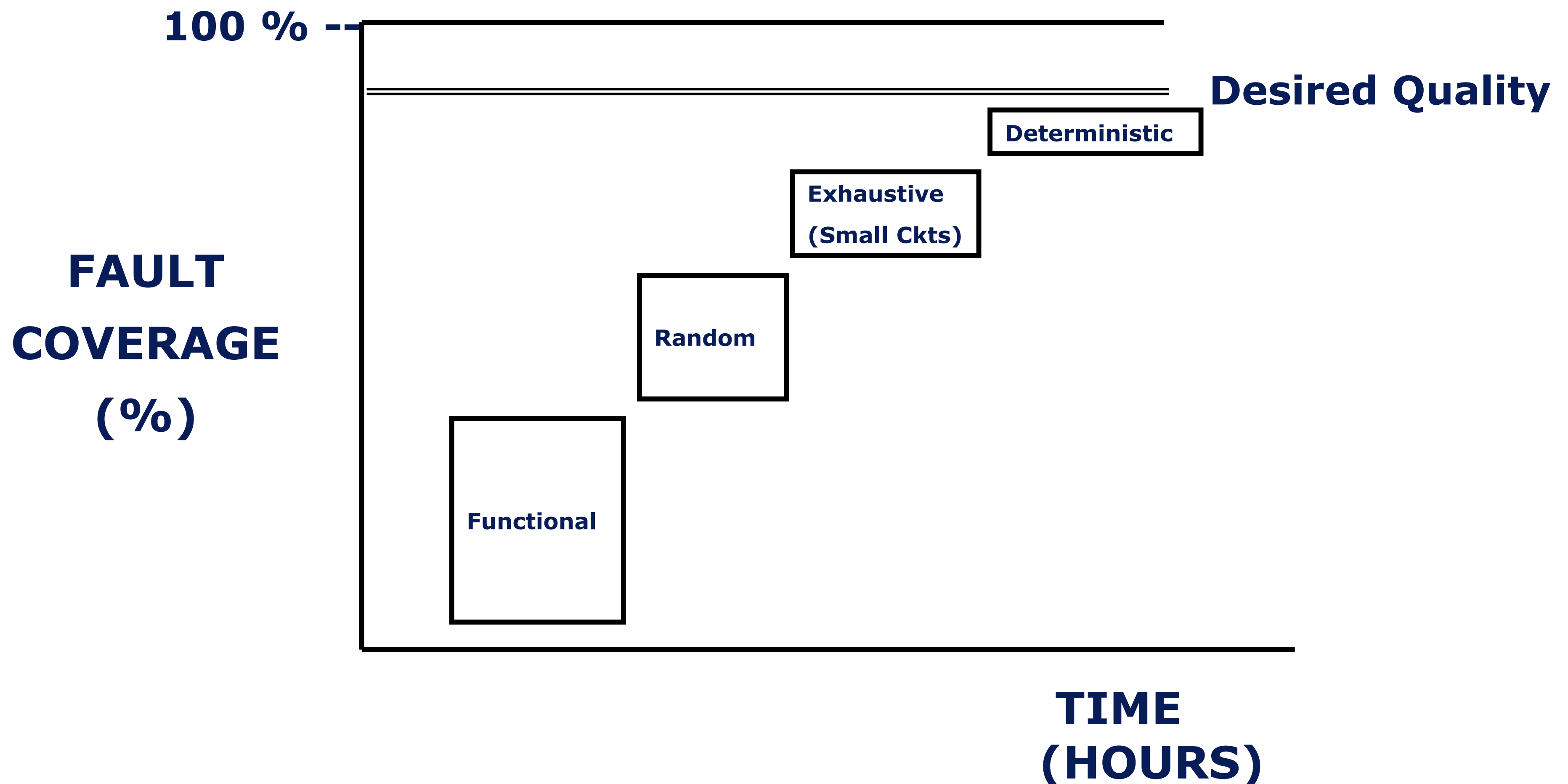
# STRATEGY FOR GENERATING TEST STIMULI

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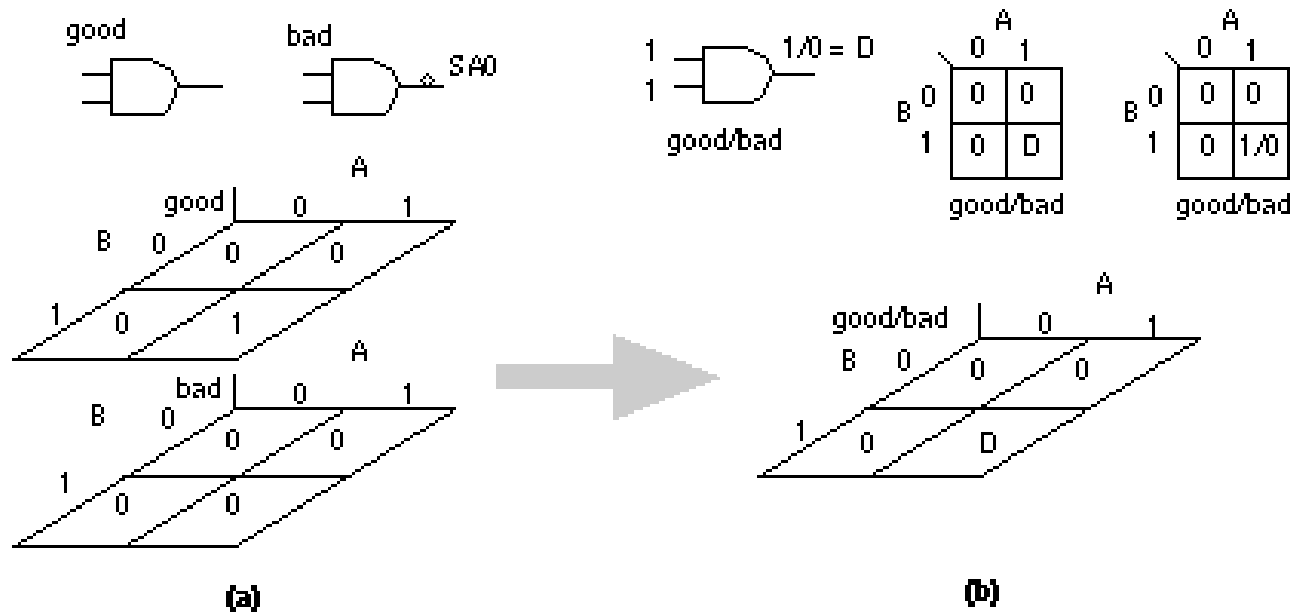
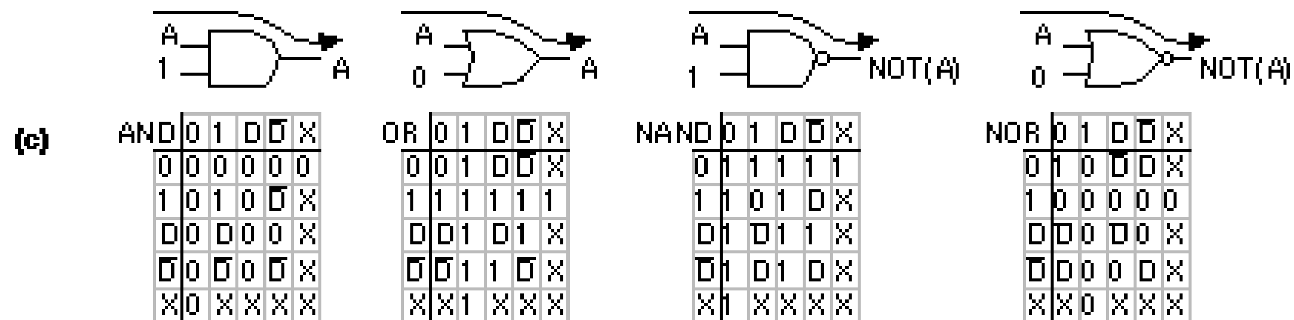
# DETERMINISTIC ALGORITHM FOR DETECTING FAULTS




| AND | 0 | 1 | D | $\overline{D}$ | X |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | $\overline{D}$ | X |
| D | 0 | D | 0 | 0 | X |
| $\overline{D}$ | 0 | $\overline{D}$ | 0 | $\overline{D}$ | X |
| X | 0 | X | X | X | X |

| OR | 0 | 1 | D | $\overline{D}$ | X |
|---|---|---|---|---|---|
| 0 | 0 | 1 | D | $\overline{D}$ | X |
| 1 | 1 | 1 | 1 | 1 | 1 |
| D | D | 1 | D | 1 | X |
| $\overline{D}$ | $\overline{D}$ | 1 | 1 | $\overline{D}$ | X |
| X | X | 1 | X | X | X |

| NAND | 0 | 1 | D | $\overline{D}$ | X |
|---|---|---|---|---|---|
| 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | D | X |
| D | 1 | $\overline{D}$ | 1 | 1 | X |
| $\overline{D}$ | 1 | D | 1 | D | X |
| X | 1 | X | X | X | X |

| NOR | 0 | 1 | D | $\overline{D}$ | X |
|---|---|---|---|---|---|
| 0 | 1 | 0 | $\overline{D}$ | D | X |
| 1 | 0 | 0 | 0 | 0 | 0 |
| D | $\overline{D}$ | 0 | $\overline{D}$ | 0 | X |
| $\overline{D}$ | D | 0 | 0 | D | X |
| X | X | 0 | X | X | X |

Fig. 14.17, Page 756
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# CONTROLLABILITY AND OBSERVABILITY FOR FAULT DETECTION

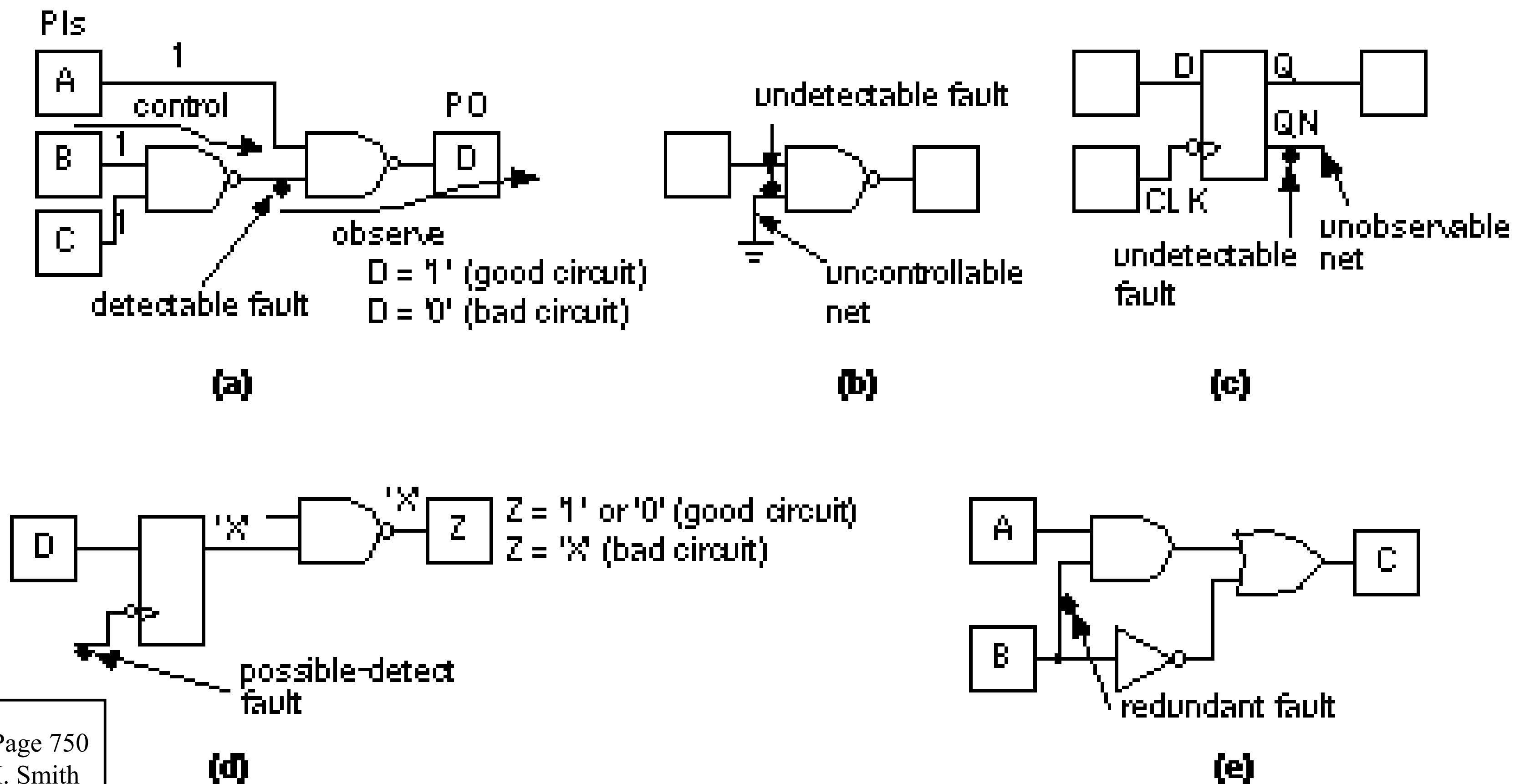


Fig. 14.15, Page 750
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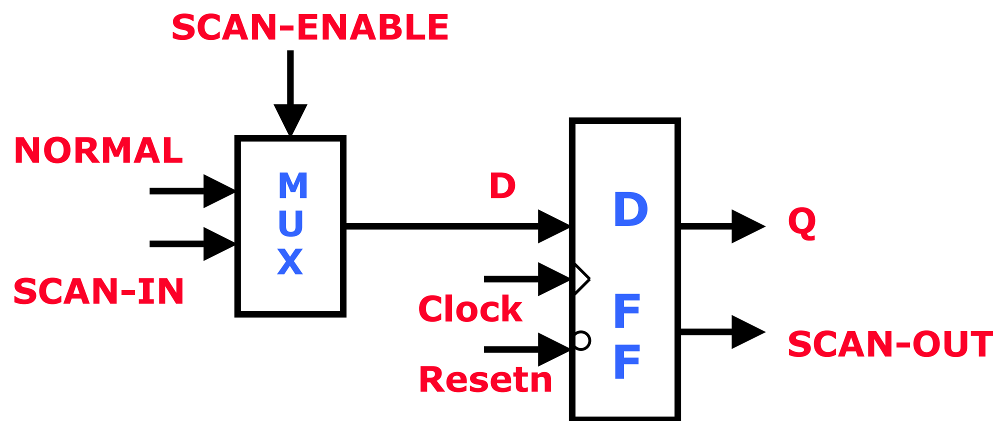
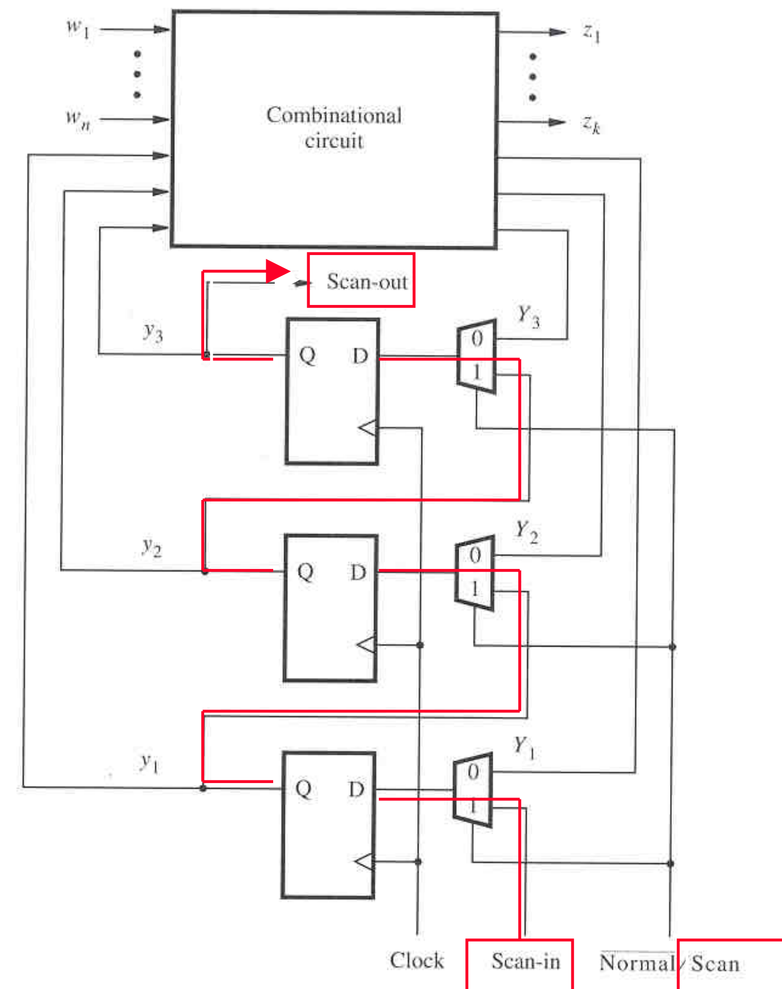
# MULTIPLEXED FLIP-FLOPS ARE USED FOR INTERNAL SCAN TESTING

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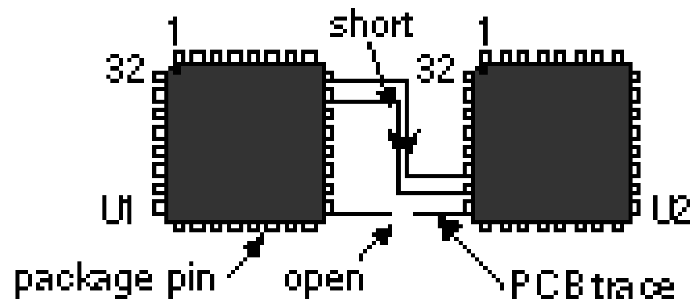
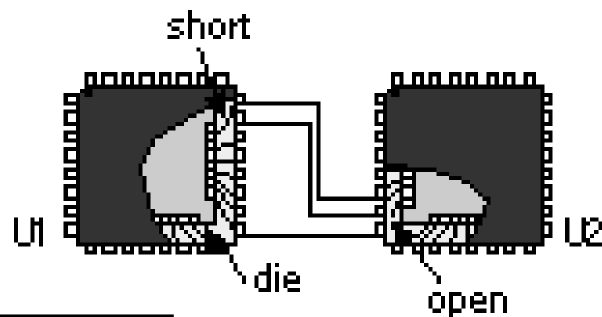
# BOUNDARY SCAN CAN DETECT BOARD FAULTS AND PIN-POINT DEFECTIVE ICS



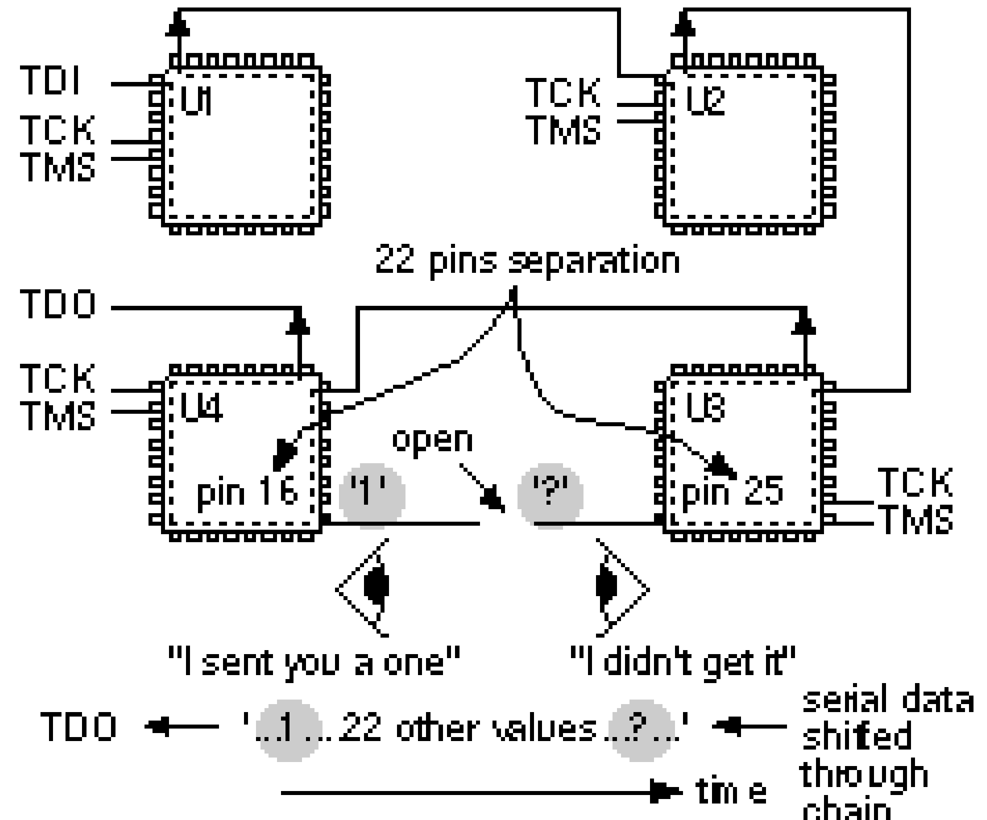




Fig. 14.1, Page 715
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# ADVANTAGES OF BOUNDARY SCAN TESTING

- Provides a standard protocol for invoking BIST in I.C.s after assembly onto P.C. boards.
- Allows I.C.s to be tested thoroughly in their complete, interconnected environment at any time during the life of the system.
- Provides standardized basis for thorough testing of all interconnect including system backplanes.
- Needs less expensive test equipment.
- Simplifies system-level diagnostic software.

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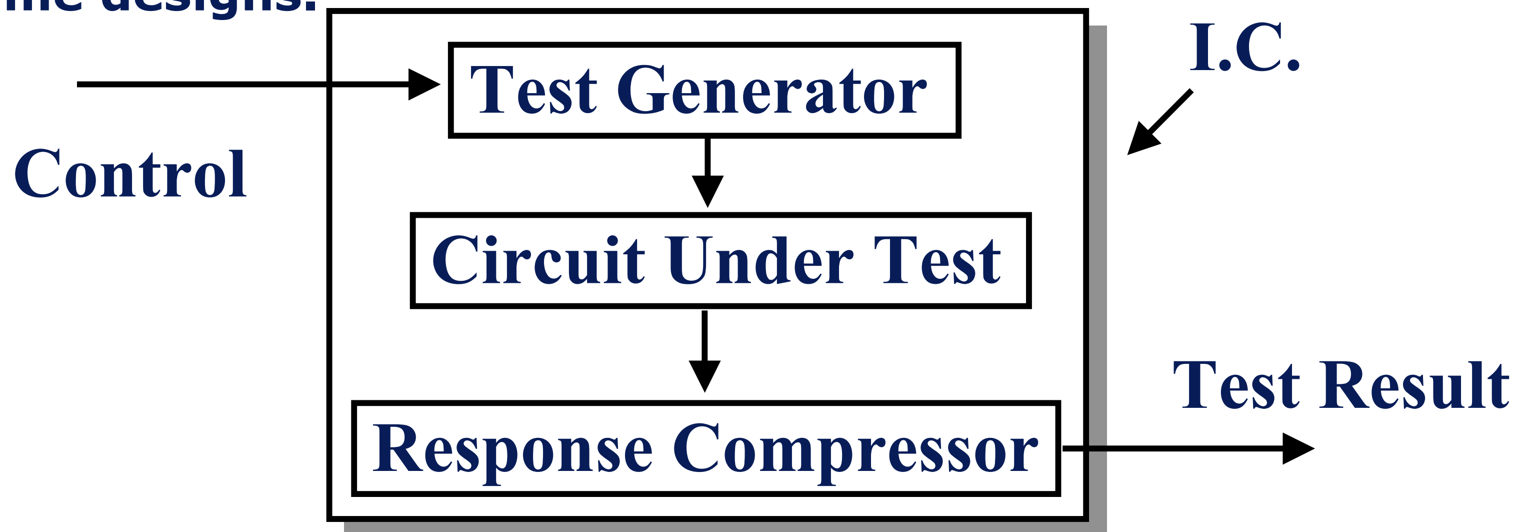
# ADVANTAGES OF BUILT-IN SELF-TEST

- Eliminates the need to generate and apply a large set of test vectors externally via the I/O pins.
- Permits testing at speed under real-world conditions.
- Improves access to internal nodes.
- Assures that test issues are addressed early in the development cycle which results in higher quality, first-time designs.

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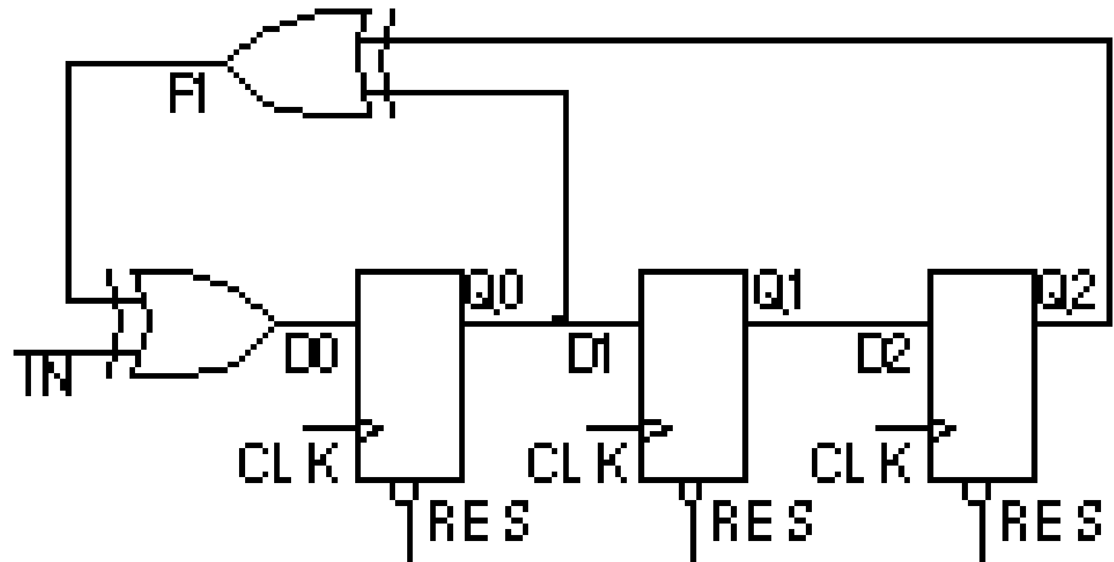
# SINGLE-INPUT SIGNATURE COMPRESSOR

**A Linear Feedback Shift Register (LFSR) can compress a serial input into a residual signature.**

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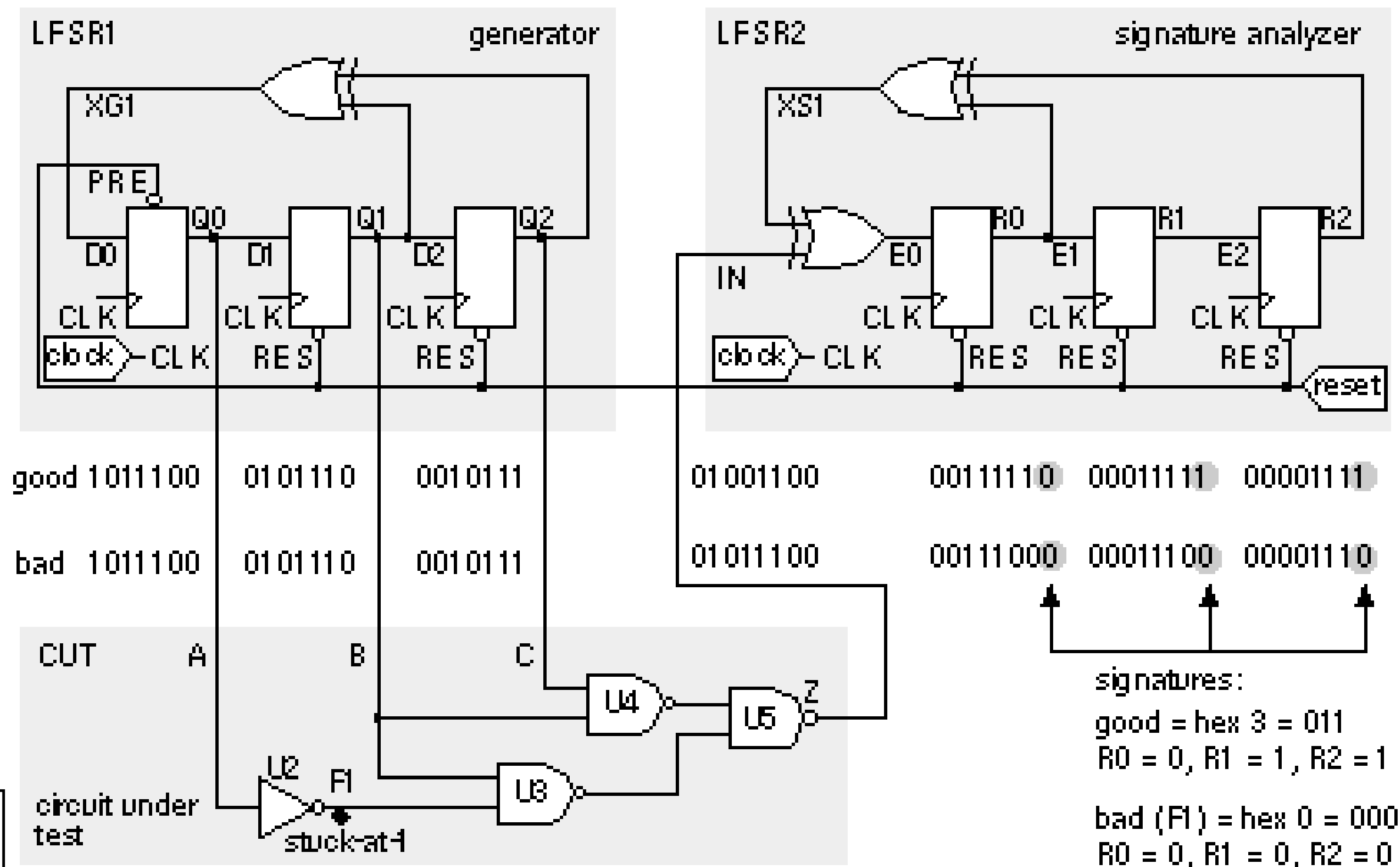
# BUILT-IN SELF-TEST (BIST)

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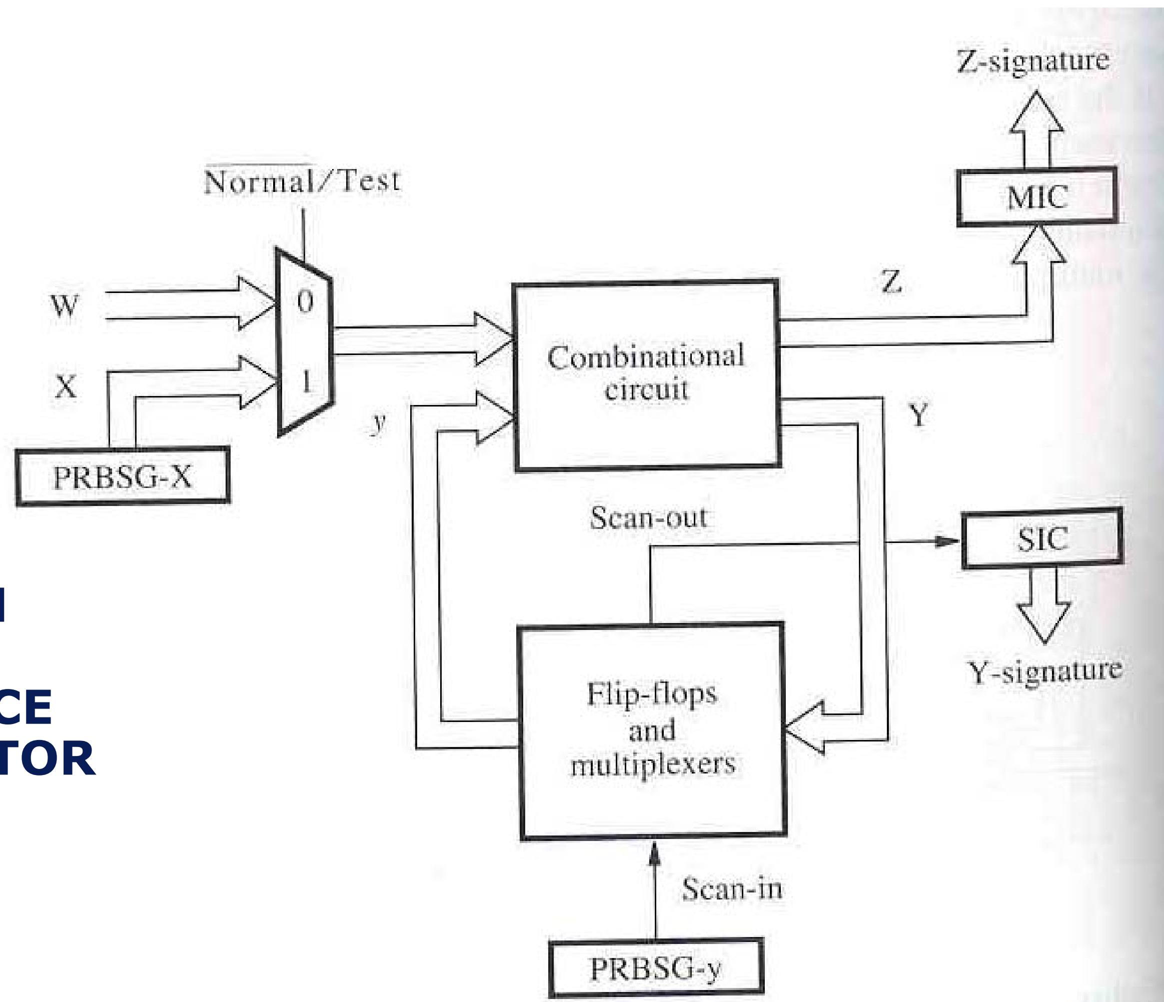
# BUILT-IN SELF-TEST (BIST)




MULTIPLE INPUT COMPRESSOR

SINGLE INPUT COMPRESSOR

PSEUDO RANDOM BINARY SEQUENCE GENERATOR

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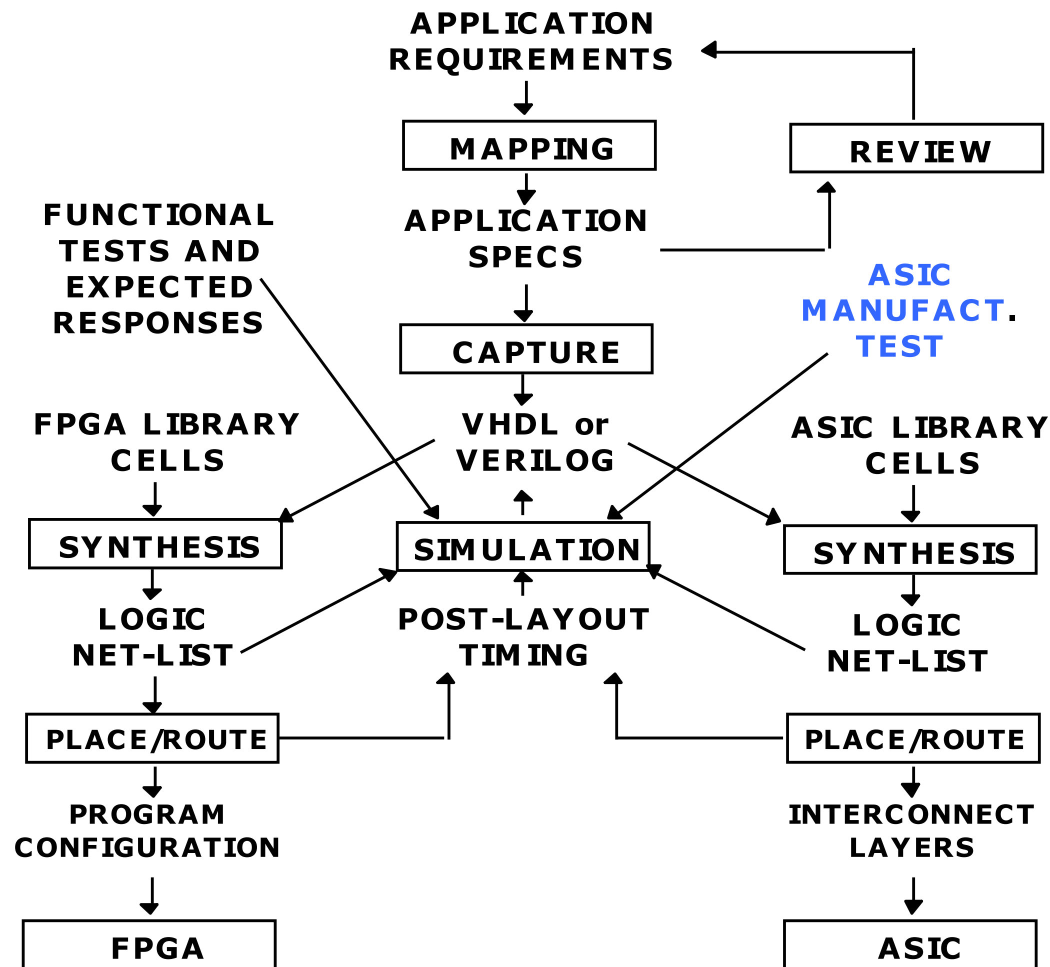
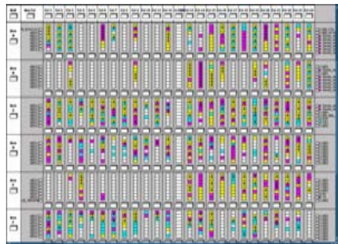
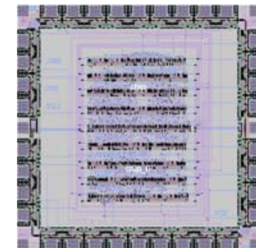
# DESIGN FLOW FOR FPGAS AND ASICS





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# COMPARISON OF PRODUCT DEVELOPMENT

| Design Stage | FPGA (weeks) | ASIC (weeks) |
|---|---|---|
| Design Specification | 1.0 | 1.0 |
| Design Entry | 1.6 | 1.6 |
| Functional Simulation | 2.4 | 4.0 |
| Test Vector Generation | 0.0 | 6.4 |
| Vendor Interface | 0.0 | 1.6 |
| Prototype Test | 1.6 | 1.6 |
| Prototype Lead Time | 0.0 | 2.0 |
| Production Lead Time | 0.0 | 6.0 |
| Total Design Cycle | 7.0 | 24.0 |

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# COMPARISON OF PRODUCT COSTS

| EXPENSE | FPGA | ASIC |
| --- | --- | --- |
| Raw unprogrammed part | 8.00 | 4.00 |
| Design/Simulation | 3.15 | 7.92 |
| Mfgr. Test Vectors | 0 | 2.88 |
| Place/Route/Masks | 0 | 2.20 |
| Final part | 11.15 | 17.00 |

**Costs in $/part assuming quantity < 200,000 copies**

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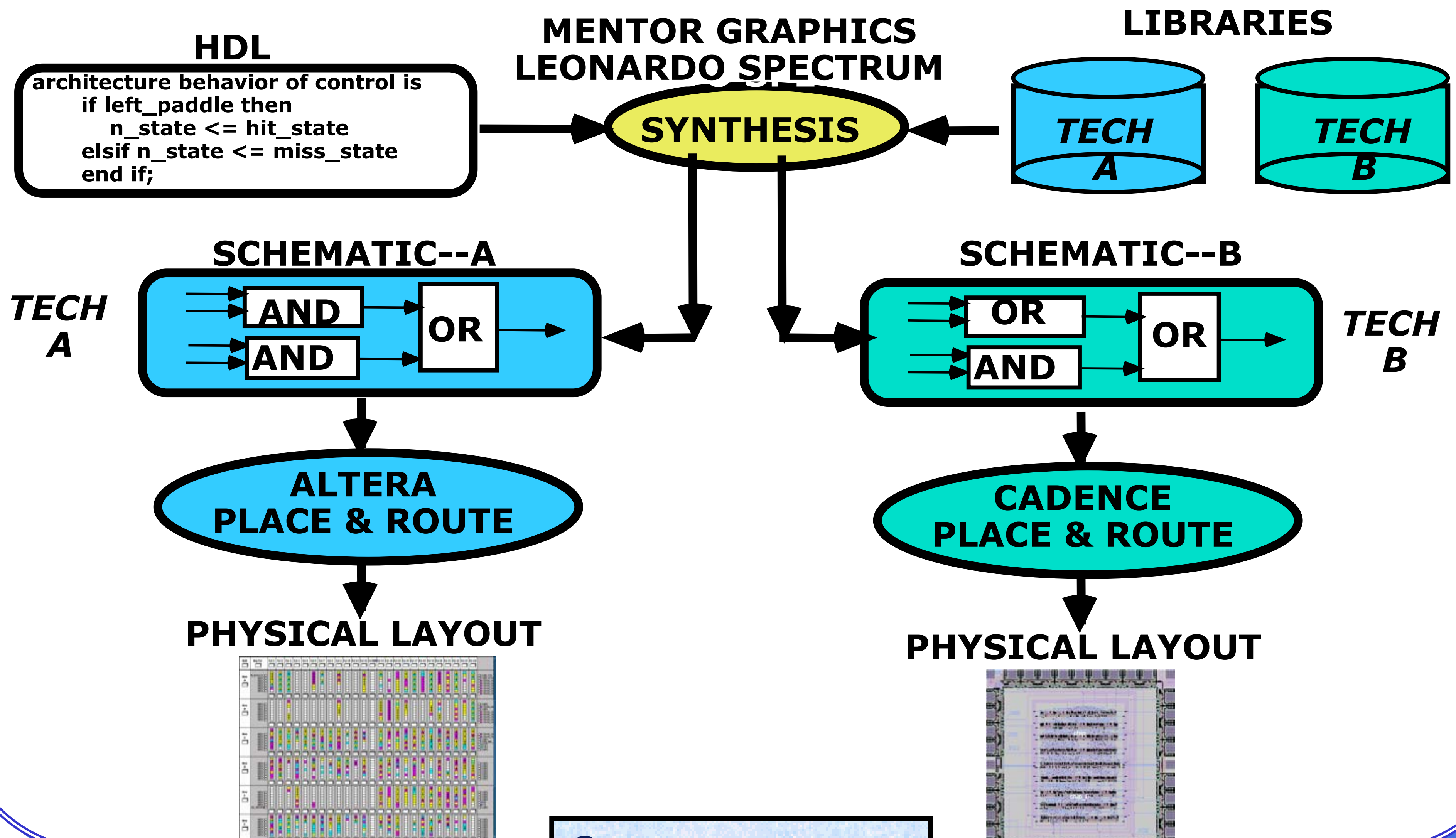
# HDL DESIGNS CAN BE TARGETED TO MULTIPLE LAYOUTS

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