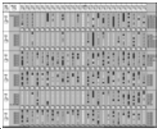
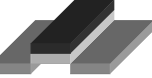
DESIGNING FPGAS & ASICS

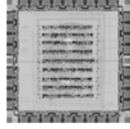


Testing ASICs



Prof. Don Bouldin, Ph.D.

Electrical & Computer Engineering
University of Tennessee
TEL: (865)-974-5444
FAX: (865)-974-5483
dbouldin@tennessee.edu



© 2003 -- Don Bouldin

COURSE OUTLINE

- Overview of FPGAs and ASICs
- Using Synthesis
- HDL Examples
- Simulation and Testing
- Physical Place and Route
- Testing ASICs
- Component Reuse

© 2003 -- Don Bouldin

TESTING ASICS

- Functional Tests
- Manufacturing Tests
- Fault Coverage
- Test Pattern Generation
- Internal Scan
- Boundary Scan
- Built-In Self-Test

© 2003 -- Don Bouldin

FUNCTIONAL TEST STIMULI

- Functional test stimuli validate that the circuit exhibits the required behavior at the desired speed.
- It is too time-consuming to develop and to apply an exhaustive set of functional stimuli so usually the designer tests only favorite cases and expected trouble spots like overflow, etc.
- CAD tools to assist in this process generally take equations and generate 1's and 0's.

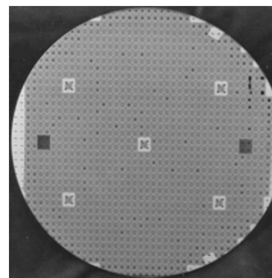
© 2003 -- Don Bouldin

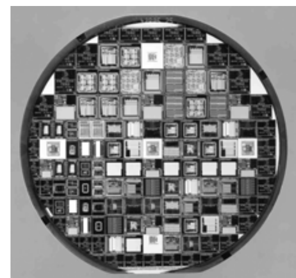
MANUFACTURING TEST STIMULI ARE NECESSARY BUT COSTLY

- Manufacturing has far less than 100% yield so each part must be tested to determine whether the circuit you desired was actually manufactured.
- First, known test structures are probed on the wafer to determine its acceptance.
- Then, each die on the wafer is probed and tested at d.c.
- Packaged parts are tested individually by the vendor at low speed (usually 1 MHz).
- The designer may then screen parts individually at full speed and under various environmental conditions.

© 2003 -- Don Bouldin

SHARING MULTI-PROJECT MASKS AND WAFERS SAVES MONEY





MOSIS

© 2003 -- Don Bouldin

MANUFACTURING TEST STIMULI AND FAULT COVERAGE

- Manufacturing test stimuli should provide sufficient coverage to achieve the desired quality.
- The more demanding the coverage, the fewer defective parts that will be shipped.
- Fault grading can be applied at the logic-level or at the MOS switch-level. Vendors encourage toggling of all logic nodes from 0 to 1 and 1 to 0 whether used or not.
- A minimum set of stimuli that can detect (not locate) faults is used for screening production parts to minimize time on the tester and its per-pin memory requirements.

© 2003 -- Don Bouldin

DEFECTIVE PARTS AS A FUNCTION OF FAULT COVERAGE PERCENTAGE

Defective Parts	Fault Coverage
227	50.00%
133	90.00%
90	99.00%
3	99.99%

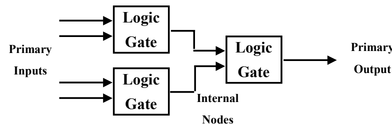
Out of 10,000 Parts

Table 14.24, Page 795
ASICs by M. Smith
© 1997 A-W-L, Inc.
Used by permission.

© 2003 -- Don Bouldin

GENERATING TEST STIMULI FOR LOGIC FAULT COVERAGE

- Stimuli must be applied to primary inputs and cause the internal nodes to toggle. Responses must be observable from the primary outputs.
- Manufacturing test stimuli are generated before fabrication since the circuit can still be modified to enhance controllability and observability. This is called "design for testability".

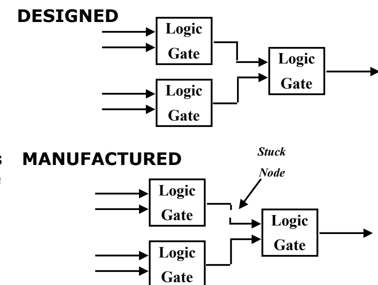


© 2003 -- Don Bouldin

FAULT COVERAGE IS BASED ON THE STUCK-AT MODEL

STUCK-AT MODEL

- A node may be GOOD, Stuck-at-0 or Stuck-at-1.
- Only one node is considered to be at fault at any one time.



© 2003 -- Don Bouldin

DETECTION OF STUCK-AT FAULTS

To detect whether F1 at the output of U2 is s-a-1, apply an input of C = 0, B =1 and A=1.

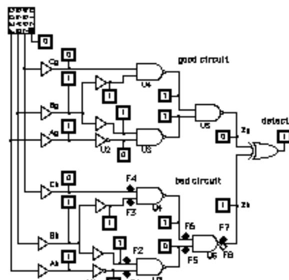


Fig. 14.16, Page 752
ASICs by M. Smith
© 1997 A-W-L, Inc.
Used by permission.

© 2003 -- Don Bouldin

JUSTIFICATION AND PROPAGATION FOR FAULT DETECTION

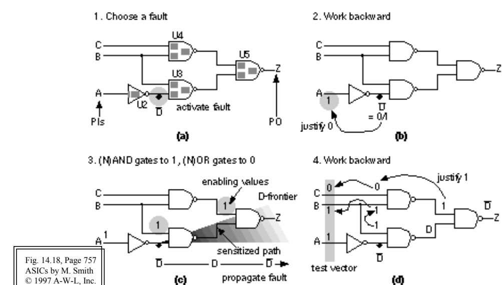
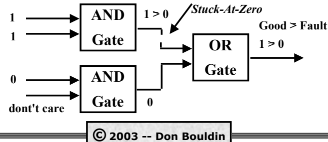


Fig. 14.18, Page 757
ASICs by M. Smith
© 1997 A-W-L, Inc.
Used by permission.

© 2003 -- Don Bouldin

GENERATION OF TEST STIMULI FOR STUCK-AT FAULTS

- **FUNCTIONAL--generated as a byproduct of verifying the intended operation.**
- **EXHAUSTIVE--too time-consuming for large, practical circuits but okay for small ones. Can use a counter to generate all possible 1's and 0's on the fly.**
- **RANDOM--easily generated on the fly using a linear feedback shift register.**
- **DETERMINISTIC--can be guaranteed to be generated if a test exists. However, this process may require substantial computing resources. Automatic Test Pattern Generator (ATPG) programs like Lasar, Podem and Fan are based on the D-algorithm.**



© 2003 -- Don Bouldin

RANDOM PATTERN GENERATION

A Linear Feedback Shift Register (LFSR) can produce a Pseudo-Random Binary Sequence (PBRS).

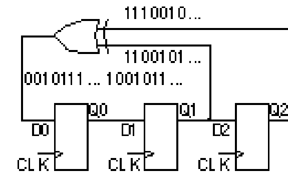
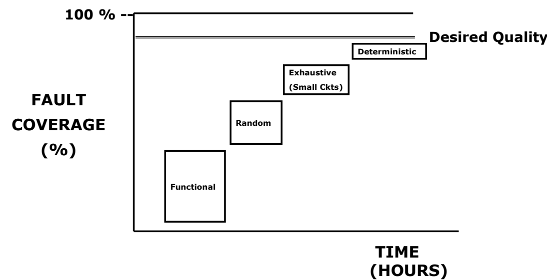


Fig. 14.23, Page 766
ASICs by M. Smith
© 1997 A-W-L, Inc.
Used by permission.

© 2003 -- Don Bouldin

STRATEGY FOR GENERATING TEST STIMULI



© 2003 -- Don Bouldin

DETERMINISTIC ALGORITHM FOR DETECTING FAULTS

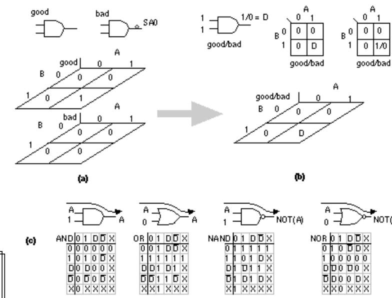


Fig. 14.17, Page 756
ASICs by M. Smith
© 1997 A-W-L, Inc.
Used by permission.

© 2003 -- Don Bouldin

CONTROLLABILITY AND OBSERVABILITY FOR FAULT DETECTION

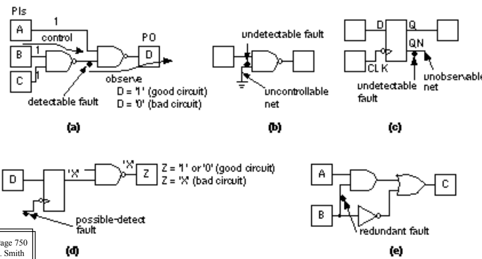


Fig. 14.15, Page 750
ASICs by M. Smith
© 1997 A-W-L, Inc.
Used by permission.

© 2003 -- Don Bouldin

MULTIPLEXED FLIP-FLOPS ARE USED FOR INTERNAL SCAN TESTING

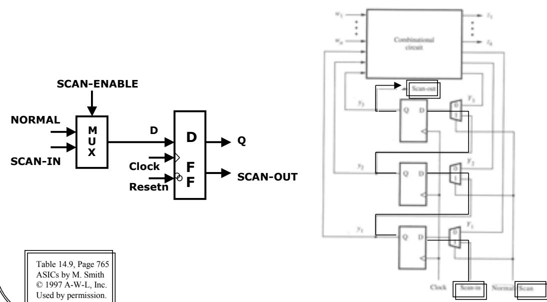


Table 14.9, Page 765
ASICs by M. Smith
© 1997 A-W-L, Inc.
Used by permission.

© 2003 -- Don Bouldin

BOUNDARY SCAN CAN DETECT BOARD FAULTS AND PIN-POINT DEFECTIVE ICS

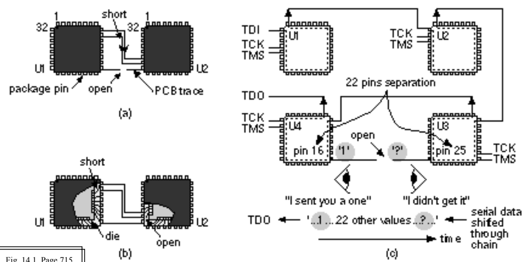


Fig. 14.1, Page 715
ASICs by M. Smith
© 1997 A-W-L, Inc.
Used by permission.

© 2003 -- Don Bouldin

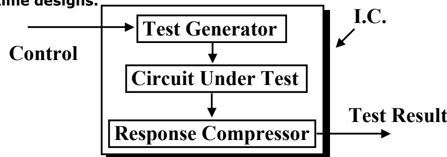
ADVANTAGES OF BOUNDARY SCAN TESTING

- **Provides a standard protocol for invoking BIST in I.C.s after assembly onto P.C. boards.**
- **Allows I.C.s to be tested thoroughly in their complete, interconnected environment at any time during the life of the system.**
- **Provides standardized basis for thorough testing of all interconnect including system backplanes.**
- **Needs less expensive test equipment.**
- **Simplifies system-level diagnostic software.**

© 2003 -- Don Bouldin

ADVANTAGES OF BUILT-IN SELF-TEST

- **Eliminates the need to generate and apply a large set of test vectors externally via the I/O pins.**
- **Permits testing at speed under real-world conditions.**
- **Improves access to internal nodes.**
- **Assures that test issues are addressed early in the development cycle which results in higher quality, first-time designs.**



© 2003 -- Don Bouldin

SINGLE-INPUT SIGNATURE COMPRESSOR

A Linear Feedback Shift Register (LFSR) can compress a serial input into a residual signature.

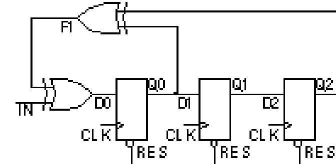


Fig. 14.24, Page 767
ASICs by M. Smith
© 1997 A-W-L, Inc.
Used by permission.

© 2003 -- Don Bouldin

BUILT-IN SELF-TEST (BIST)

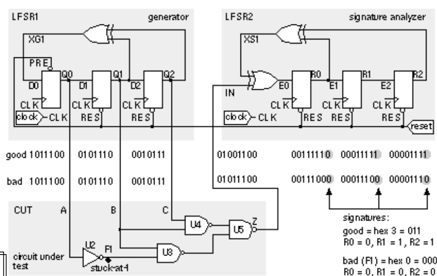
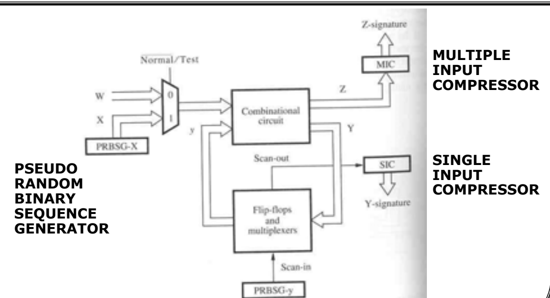


Fig. 14.25, Page 769
ASICs by M. Smith
© 1997 A-W-L, Inc.
Used by permission.

© 2003 -- Don Bouldin

BUILT-IN SELF-TEST (BIST)



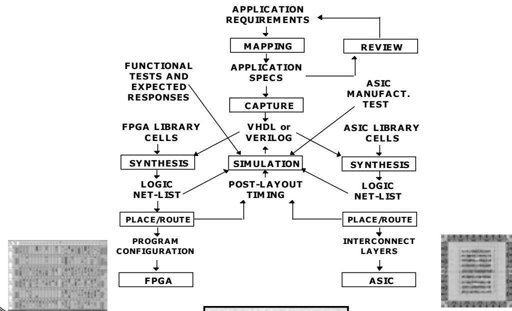
MULTIPLE INPUT COMPRESSOR

PSEUDO RANDOM BINARY SEQUENCE GENERATOR

SINGLE INPUT COMPRESSOR

© 2003 -- Don Bouldin

DESIGN FLOW FOR FPGAS AND ASICS



© 2003 -- Don Bouldin

COMPARISON OF PRODUCT DEVELOPMENT

Design Stage	FPGA (weeks)	ASIC (weeks)
Design Specification	1.0	1.0
Design Entry	1.6	1.6
Functional Simulation	2.4	4.0
Test Vector Generation	0.0	6.4
Vendor Interface	0.0	1.6
Prototype Test	1.6	1.6
Prototype Lead Time	0.0	2.0
Production Lead Time	0.0	6.0
Total Design Cycle	7.0	24.0

© 2003 -- Don Bouldin

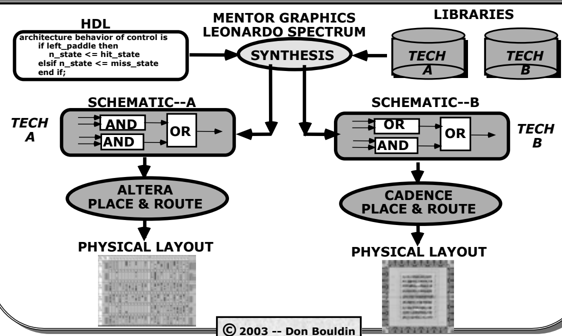
COMPARISON OF PRODUCT COSTS

EXPENSE	FPGA	ASIC
Raw unprogrammed part	8.00	4.00
Design/Simulation	3.15	7.92
Mfgr. Test Vectors	0	2.88
Place/Route/Masks	0	2.20
Final part	11.15	17.00

Costs in $/part assuming quantity < 200,000 copies

© 2003 -- Don Bouldin

HDL DESIGNS CAN BE TARGETED TO MULTIPLE LAYOUTS



© 2003 -- Don Bouldin