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Don Bouldin <dbouldin@gmail.com>

ElectricalandComputerEngr65148040FA2011: Calibre PEX

1 message

Zachary Michael Crane <zcrane@tennessee.edu> Fri, Sep 2, 2011 at 10:31 AM

I figured I'd save everybody the horror and suffering that it took for me to figure this out.

The first time you run calibre to generate your extracted parasitic schematic, you're going to have to define pins for your transistors and also your parasitics. I didn't see this mentioned anywhere in the tutorial, so if I missed it, shame on me and you can disregard this. Otherwise, check out page 4 of this PDF, and do note that they are using a different technology.

The transistors can be found in the default library that calibre first pulls up, so you can just press the "auto map pins" button and you're done with the nmos and pmos.

This isn't the case for the parasitic devices. To find them:

In the library box, you'll want to type analogLib (don't miss the capital L)
In the cell box, you'll want to type either res or cap, depending on which parasitic device you're mapping.
The view should default to symbol

Over to the right, in the box entitled "pin map," if you've found the library path correctly, all you should have to do is click, and the window will update with pins that are available to map, and then you can click auto map pins again and you should be good.

link: http://www.uio.no/studier/emner/matnat/ifi/INF4420/v10/PostLayoutTutorialTSMC90nm.pdf

Cadence Tips (not complete)

How to run Layout XL

In the schematic view go to: Tools – Design Synthesis – Layout XL (click “ok” on the two pop-up windows)

Now you should have the Virtuoso layout window popping up.

Go to: Design – Gen from source... (click ok)

Post layout simulation (tsmc90nm)

In order to be able to run post layout simulations, the following needs to be fulfilled.

1) ALL pin names have to be capital letters (schematic and layout)
2) GND and VDD need to be pins specified as “inputOutput” (schematic and layout)

In Virtuoso, when assigning pins to nets (wires) “Create Symbolic Pin – Display Pin Name Option...” (Shift-P), make sure that the pin layer (pn) is specified for the metal layer (“M1” in this case) your pin is supposed to be in. This is indicated with the red arrow in Figure 1. LVS requires this as well.

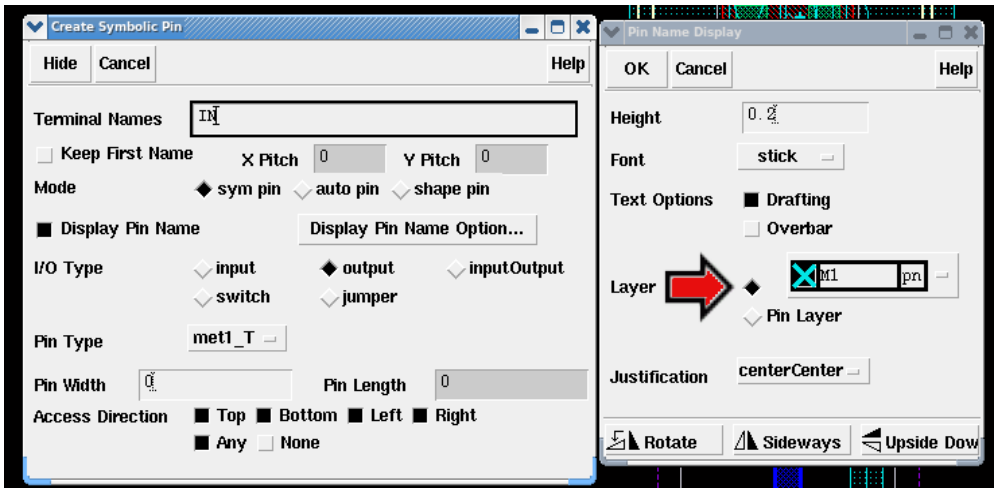

Figure 1: Create pin

After DRC and LVS are complete without errors, you can then do parasitic extraction.

In Virtuoso layout , go to Calibre – PEX.

In the Rules tab, specify the directory for the PEX rules file “calibre.rcx”. See Figure 2.

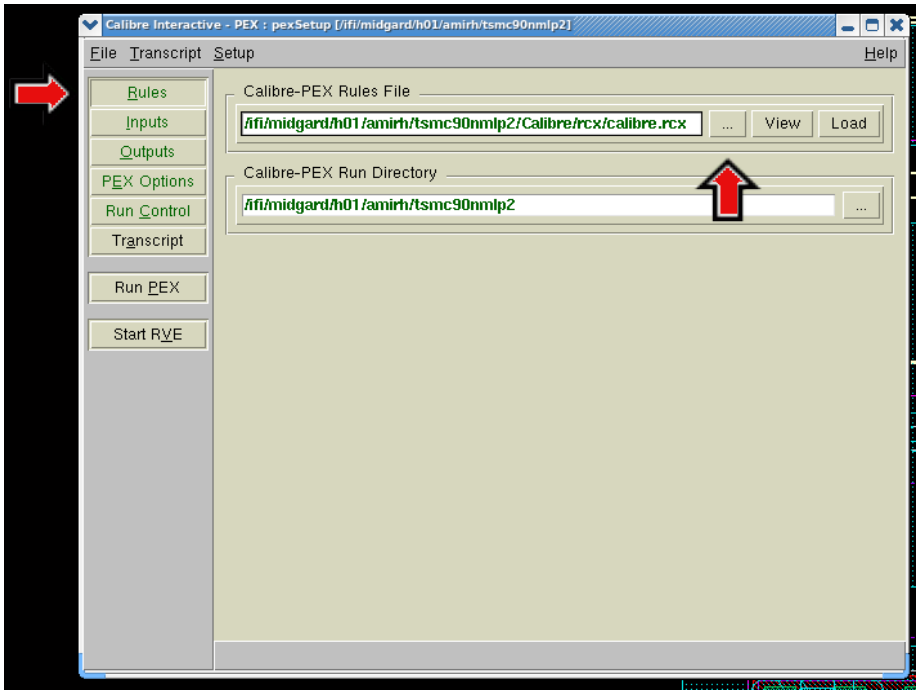

Figure 2: PEX setup - Rules

In the Inputs - Netlist tab, select “Export from schematic viewer”. See Figure 3.

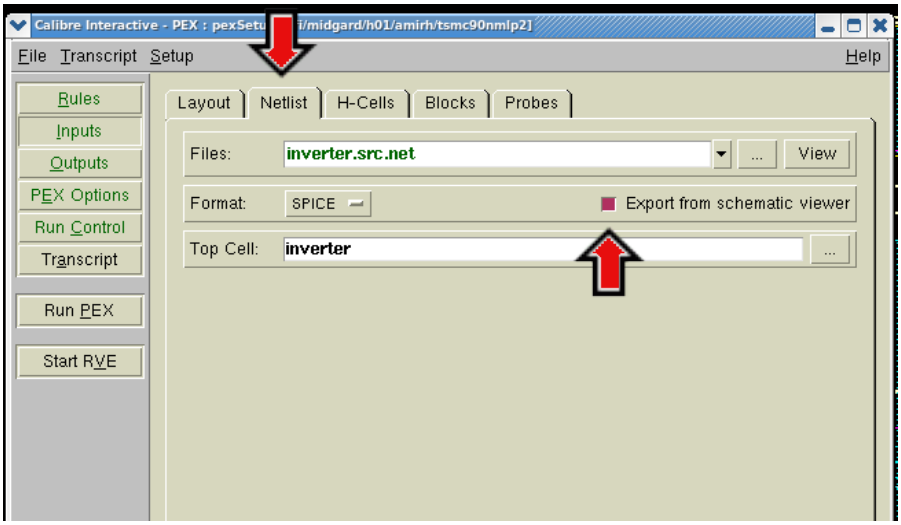

Figure 3: PEX setup - Inputs

In the Outputs – Netlist tab, make sure that the format is “CALIBREVIEW” and that “SCHEMATIC” names are used. See Figure 4.

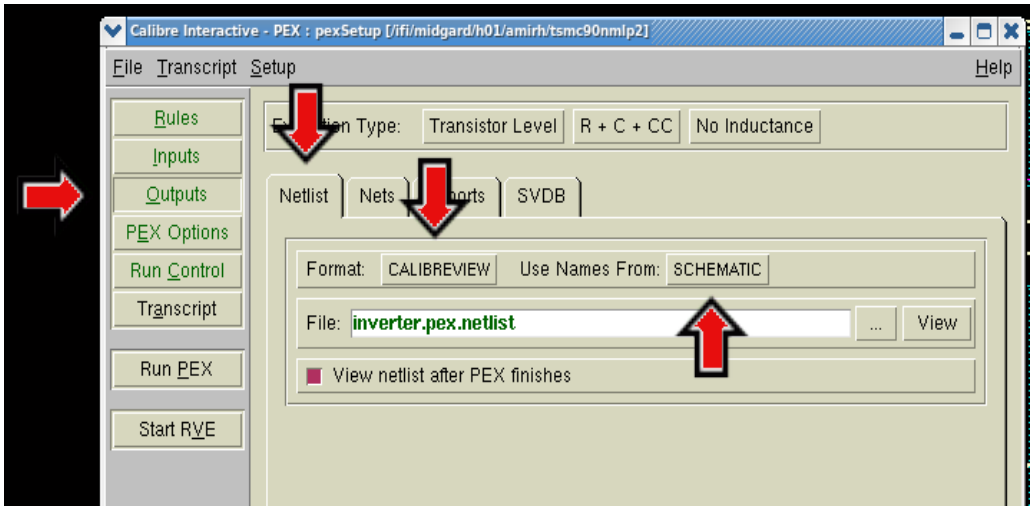

Figure 4: PEX setup - Outputs

Run PEX

If everything goes well, you should get the Calibre View Setup window popping up.

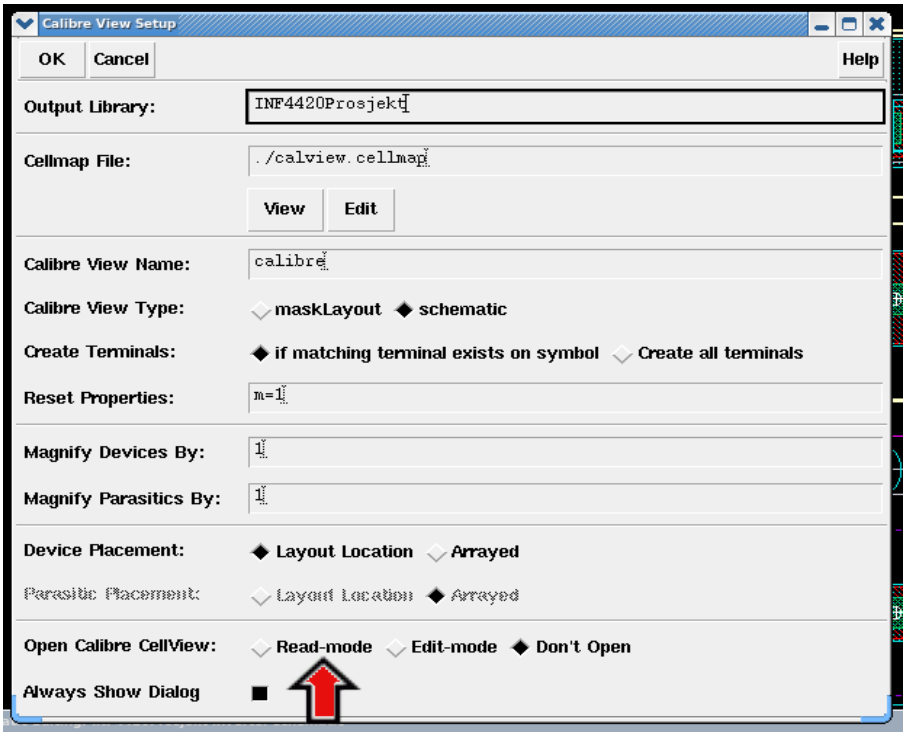

Figure 5: Calibre View Setup

You should click on the Open Calibre CellView “Read-mode” to verify that there are parasitic components in your extracted netlist.

Click OK

When running PEX for the first time (i.e. ./calview.cellmap file is empty): After clicking OK in Calibre View Setup, another window will pop up, Map Calibre Device, see Figure 6. This window wants you to map device pins from already existing cells in the library.

For example, if the specified device is “nch_mac”: Click “Browse”, find the “nch_mac” *symbol* in the tsmcN90rf library, and click on “Auto Map Pins”.

Click OK.

An identical window pops up and asks you to perform the same procedure again. Repeat the process for all the other devices you have used in your design.

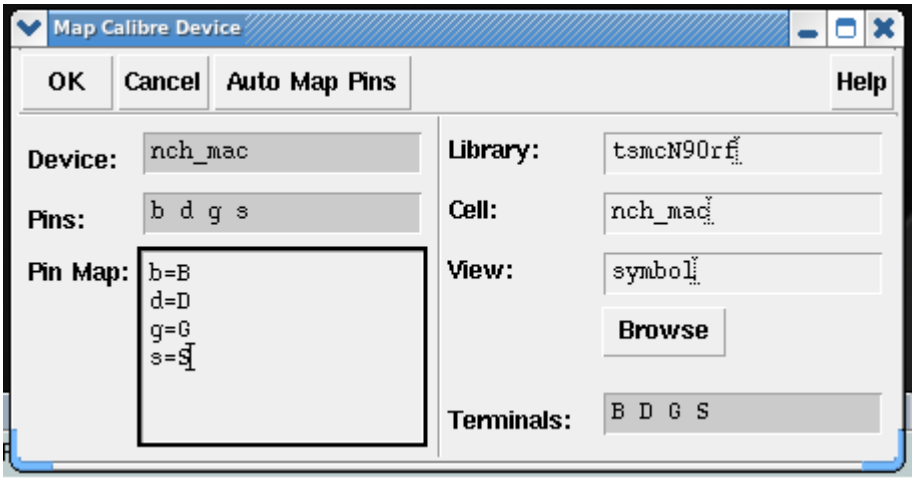

Figure 6: Device Mapping

If the extraction completed without errors/warnings, you should see your new netlist appear like the one shown in Figure 7.

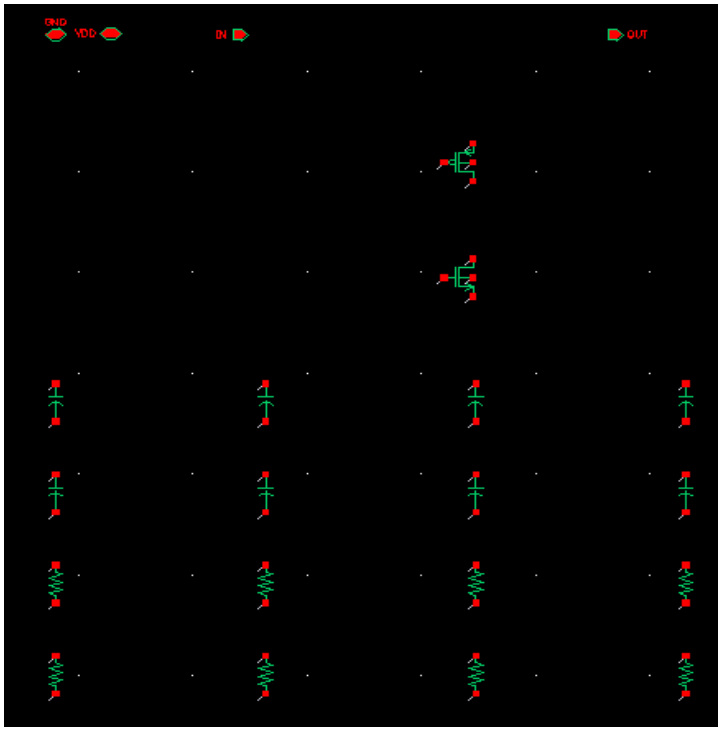

Figure 7: Extracted netlist

Figure 7 shows ports/pins, transistors, and parasitic components (R and C). Sometimes it is

necessary to open the new netlist in “Edit mode”, because the extraction fails and some ports are missing. Then you can add these port manually like you do in the schematic. Just make sure the names match. However, everything you modify in this schematic must also be modified in the netlist file (<cellname>.pex.netlist).

Now we have to specify that we want to run simulation based on the extracted netlist. In the Library Manager go to: File - New - Cell View . The Cell Name must be your testbench cell. The view is “config” and the tool used is the Hierarchy-Editor. Illustrated in Figure 8.

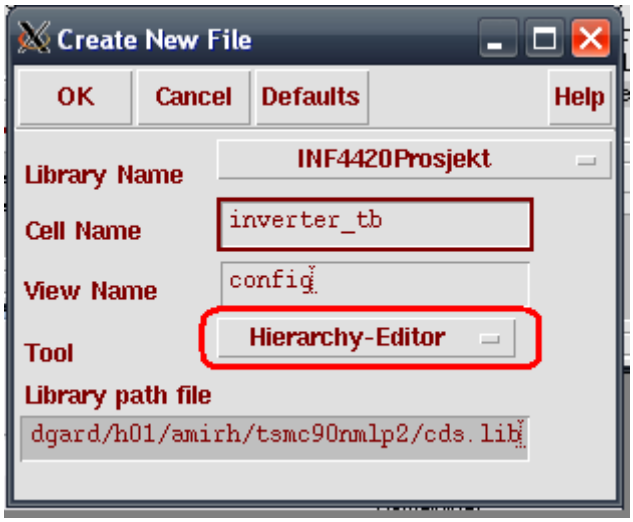

Figure 8: Create config view

Click Ok.

The Hierarchy editor pops up automatically. In the Top Cell View, type “schematic”. See Figure 9. Press “Use Template...”, choose the template name “spectre” and click OK. Click OK in the “New Configuration” window as well.

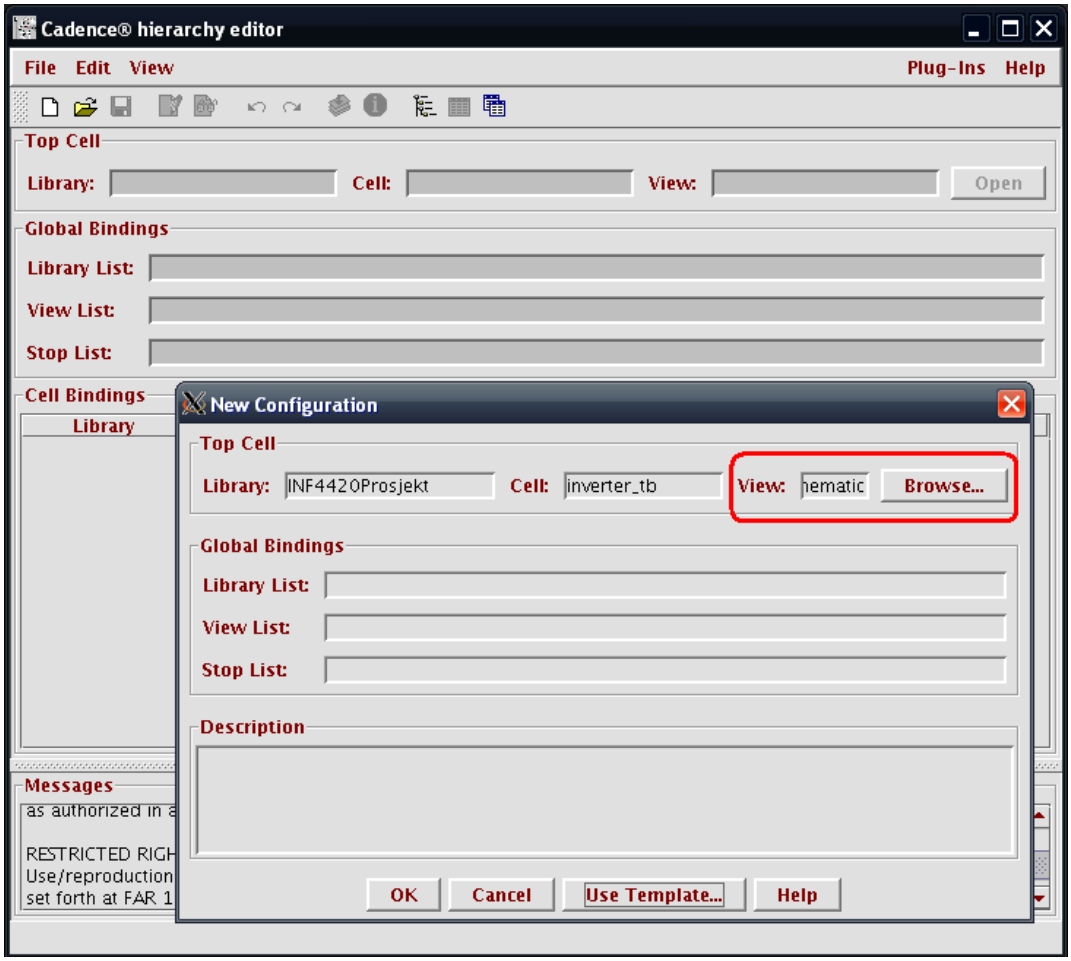

Figure 9: Hierarchy editor

Now you should get all cells listed in the hierarchy editor. In order to be able to run simulations based on the extracted netlist. You must right-click on “inverter” cell, go to “Set Cell View” and select “calibre”. See Figure 10.

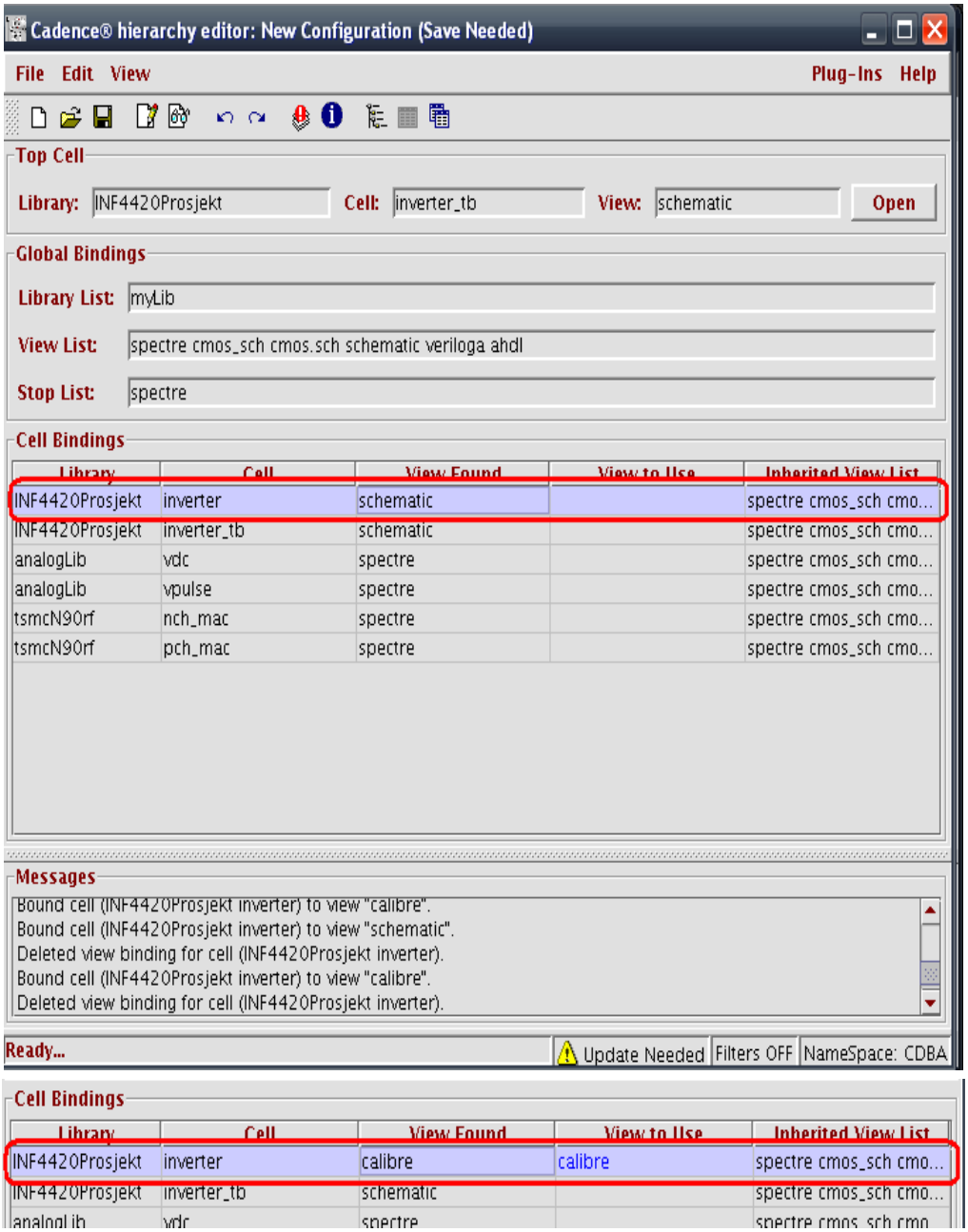

Figure 10: Change from schematic view to calibre view

Save and exit.

In the Library Manager, open your testbench using the “config” view (not schematic view). Click OK in the window that pops up.

Setup your simulation as your normally do. In the Analog Environment, go to Simulation – Netlist – Create.

Run the simulation.